Simple Solution to Overcome Fault Recovery Issues of Grid-Forming Inverter With Current Limiter

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***Abstract*—Grid-forming inverters with priority current limiter suffer the fault recovery issue, commonly manifested as the failure to exit from current limitation after fault clearance. To overcome this issue, this article proposes a virtual power P_{IVS}-feedback method. This method employs the virtual power of the internal voltage source P_{IVS} as power feedback, rather than relying on the actual output power P_{e}. The inherent fault recovery issue of priority current limiters can be well-solved in this simple yet efficient way. Furthermore, the proposed universal virtual power P_{IVS}-feedback framework can be expanded from a specific case of *d*-axis priority current limiter to other cases of circular current limiters. Besides, a comparative study of typical virtual power feedback methods shows the feasibility and superior applicability of the proposed method. Compared to existing methods, the proposed method eliminates the necessity for complex control design, additional line or grid information, and control structure reconfiguration. Comprehensive theorical analysis and hardware-in-loop experiments verify the effectiveness of the proposed method.**

***Index Terms*—Current limitation, current limiter, fault recovery, grid-forming (GFM) control.**

I. Introduction

GRID-FORMING (GFM) inverter is deemed to be one of the most promising solutions for future bulk power systems [1], [2]. The GFM inverter is controlled as a controlled voltage source, which can work in weak grids and provide necessary voltage support [3]. Power synchronization control [4], [5], [6] and virtual synchronous generator control [7], [8], [9] are the two typical GFM control methods. Although GFM inverters have similar output characteristics to synchronous generators (SGs), semiconductor-based devices are more fragile with overcurrent issues. Usually, the inverter can only handle 1.2–2 p.u. overcurrent [10], while SG can withstand 5–7 p.u. overcurrent. Current limitation methods are of vital importance.

To restrict the output currents of GFM inverters during large disturbances, existing current-limiting strategies can be classified into two categories [11]: 1) Indirect current limiting methods, which limit output current by introducing virtual impedance [12], [13], [14] or modifying the voltage reference vector or [15], [16], [17]; 2) direct current limiting methods, which rely on current limiters [18], [19], [20], [21], [22], [23], [24], [25], [26]. Both direct and indirect current-limiting strategies have advantages and disadvantages.

Indirect strategies can naturally limit the output current without causing inner-loop windup, meanwhile preserving the GFM characteristics during faults. In study [13], the design principle of virtual impedance is given for retaining optimal GFM characteristics during faults. By adaptively reducing the power set points and further modifying the voltage reference vector, the method in study [15] curtails the output current during fault conditions. In study [16], active power and reactive power control loops are reconfigured for controlling the power angle and limiting the voltage reference magnitude to achieve the fault current limitation. As these methods rely on the reference of the voltage controller, the control bandwidth is lower than that of the direct current limiter that uses a faster current inner loop. These methods may react too slowly to suppress the rapidly rising transient peak current at the beginning of a fault. In study [14], a two-stage adaptive virtual impedance is proposed, which can suppress the initial peak fault current. However, the adaptive virtual impedance requires fast real-time calculations. In study [17], the current limitation is achieved by dynamically rescaling the voltage reference vector, and power reference. However, the grid voltage information is still required to retain the GFM properties with successful symmetrical and asymmetrical fault ride-through.

Different from indirect methods, direct current limiting methods use circular or priority-based current limiters to directly restrict the current reference signals for the inner current loop [10], [18], [19]. Owing to the high bandwidth of the inner current loop, direct methods can quickly and accurately limit the fault current [11]. Different types of current limiters possess their respective advantages and disadvantages. Optimal phase-priority current limiter exhibits superior transient synchronization stability [20]. However, determining the optimal phase depends on grid voltage, grid impedance, and initial power setpoint. In

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contrast, d-axis priority current limiter and q-axis priority current limiter are more practical for implementation [21]. Considering that GFM inverters primarily output active power under normal operating conditions, the d-axis current component dominates, leading to a smoother transient response in d-axis priority current limiter after fault clearance. Nevertheless, all the priority current limiters encounter the issue where the GFM inverter may fail to exit the current-limitation mode even after fault clearance [10], [11]. Circular current limiters can avoid this phenomenon, as it retains the current-phasor angle generated by the inner voltage controller [22]. However, the circular current limiter inherently narrows the peak of the power angle characteristics, resulting in great degradation of transient synchronization stability [22], [23]. Also, the circular current limiter presents the equivalent resistive output impedance characteristic, which poses challenges for conventional relay protection schemes [24]. So far, no consensus has been reached on the most favorable current limiter [25]. This article mainly focuses on the analysis of GFM inverters equipped with d-axis priority current limiter.

Despite extensive efforts to study the stability mechanisms [21], [23], fault-ride-through performance [26], [27], [28], and stability enhancement methods [29], [30] of GFM inverters with the current limiters, the postfault behavior after fault clearance still needs to be further investigated. As noted in studies [10], [11], and [25], GFM inverters with priority current limiters face a fault recovery issue, commonly referred to as the "windup" problem. This issue means that the GFM inverter fails to return to its original stable equilibrium point after the fault is cleared, instead settling at a new stable equilibrium point introduced by the current limiter. In other words, the GFM inverter with a priority current limiter has difficulty in exiting the current limitation mode after fault clearance [31].

To deal with the fault recovery issue, the postfault recovery process and "windup" phenomenon are elucidated through theoretical analysis [31], [32]. In studies [25] and [33], the existence of the saturated stable equilibrium point is analyzed and the GFM inverter might be clamped in the current-saturation mode even after the fault is cleared. However, no control strategy is presented for exiting the current saturation mode. Furthermore, improved methods are studied in works [34], [35], and [36]. In study [34], the active power synchronization loop of the GFM inverter turns into the reactive power synchronization way while the current limiter is triggered. However, it needs extra control signals to realize mode-switching. An auxiliary mode-switch control loop with a dynamic control parameter related to the q-axis component of the output voltage is modified in study [35]. However, the accuracy line impedance information is required. Furthermore, a hybrid synchronization method with torque error feedforward is proposed to enhance transient stability and ensure fault recovery to GFM mode [36]. However, the modified control algorithm with the step-by-step coefficient design still requires the information of line impedance and grid voltage, which is complicated to implement. In summary, how to ensure successful recovery with a practical method continues to be an open issue that merits further attention.

The virtual power feedback control, also referred to as fictitious power feedback control, has attracted growing research interest for GFM inverters with current limiters [37], [38], [39], [40]. Virtual power exhibits adaptive behavior depending on whether the current limiter is activated. When the current limiter is not triggered, the virtual power coincides with the actual output power of the inverter, whereas once the current limiter is engaged, the virtual power changes adaptively. The virtual feedback method reshapes the virtual power-angle characteristics in current limitation mode and substantially embeds more control flexibility for the improvement of the fault-ride-through ability of GFM inverters.

However, the calculation of virtual power is not unique. The virtual power in studies [37] and [38] is obtained through the actual output voltage and unsaturated current reference (virtual current). These methods aim to improve the transient synchronization stability of GFM inverters with circular current limiter. In study [39], the virtual power is calculated using the voltage reference (virtual voltage) and the unsaturated current reference (virtual current). Although this method is effective on both priority current limiters and the circular current limiter, the inner voltage control loop must adopt virtual admittance control. The actual output power cannot be accurately controlled to be the same as power reference during normal operation. Also, it is not suitable when the inner voltage loop adopts the proportional-integral (PI)-based controller. In [40], virtual power is also calculated by the internal voltage (virtual voltage) and virtual current. Unlike [39], the virtual current is not the unsaturated current reference i_{ref}. Instead, the virtual current is calculated through a predesigned virtual impedance between the virtual voltage and the output voltage. These various virtual power feedback methods employed with different current limiters lead to different power feedback-angle characteristics, potentially resulting in undesirable instability if the virtual power is incompatible with the specific current limiter employed. To date, a unified and systematic study that comparing various virtual power feedback methods with different current limiters is still lacking.

To find a simple solution to address the fault recovery issue, this article proposes the universal virtual power P_{IVS}-feedback method, which greatly enhances the fault-ride-through ability of GFM inverters with current limiters. In addition, a comprehensive comparative study is carried out among three typical virtual power feedback methods with different current limiters. It provides practical guidelines for selecting the proper virtual power method that matches specific current limiters. The main contributions are as follows.

1) *A universal virtual power feedback GFM control method:* The core modification lies in utilizing the virtual power P_{IVS} of the equivalent internal voltage source, as the power feedback, instead of the actual output power. During normal operation, the P_{IVS}-feedback method is completely identical to the traditional GFM control. During current limitation operation, P_{IVS} changes autonomously to ensure successful recovery after fault clearance. Furthermore, the proposed universal virtual power P_{IVS}-feedback method can also be effectively applied to other types of current limiters, such as q-axis priority current limiter and circular current limiter.

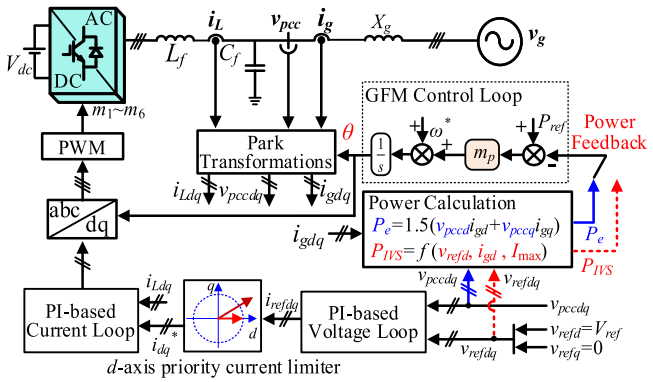

Fig. 1. Configuration of the Grid-connected GFM inverter.

2) *Autonomous fault recovery from current limitation mode to normal GFM operation mode without additional sensors:* As virtual power P_{IVS} changes autonomously according to different operation modes, the proposed method reshapes the virtual power angle characteristics to achieve fault recovery without additional grid operation information. Compared with existing methods [34], [35], [36], [37], [38], [39], [40], the proposed method provides a simple solution that eliminates the need for the accurate parameters design and additional information of grid voltage and line impedances.
3) *Comprehensive comparative study of three typical virtual power feedback ways with different current limiters:* By analyzing the derived power–angle characteristics, this study examines the differences in applicability of the three typical virtual power feedback methods when employed with d-axis priority current limiter and the circular current limiter. It reveals how different combinations significantly influence the transient stability and fault recovery capabilities of GFM inverters and can provide practical guidelines to select appropriate virtual power feedback schemes based on specific current limiters.
4) The mechanism for excellent fault recovery performance is revealed by comprehensive phasor diagram analysis. Taking the GFM inverter with d-axis priority current limiter as an example, the analysis results indicate that no matter how long the fault lasts, the fault recovery issue of the GFM inverters can always be well-solved by the proposed virtual power P_{IVS}-feedback GFM control after fault clearance. As a simple method, it can realize unified operation between the current limitation mode and normal operation mode.

II. Review of GFM Inverter With DPCL

A. System Configuration

Fig. 1 shows the GFM inverter grid-connected system configuration. A dc voltage source is applied to provide a stable dc link voltage V_{dc}. L_f and C_f represent the inductance and the capacitor of the LC filter. X_g represents the grid impedance. $\boldsymbol{v_g}$, $\boldsymbol{v_{\mathrm{pcc}}}$, $\boldsymbol{i_g}$, and $\boldsymbol{i_L}$ represent the grid voltage, the output PCC voltage, the output current, and the inductor current, respectively. m_1–m_6 are the pulsewidth modulation drive signals.

Both the traditional GFM control method and the proposed P_{IVS}-feedback method are involved in Fig. 1. The control signal of the traditional GFM control is expressed in a blue solid line, and the power feedback of the traditional GFM control is the real output power P_e. The control signal of the proposed modified power feedback control is expressed in a red dashed line, using P_{IVS} instead of P_e as the power feedback. More details of virtual power P_{IVS}-feedback control will be further introduced in Section III.

The traditional GFM control in this article adopts power synchronization control, which is expressed as follows:

$$\omega = \omega^* + m_p \left(P_{\mathrm{ref}} - P_e\right) \tag{1}$$

where m_p represents the P–ω droop coefficient, P_{ref} is the active power reference and P_e is the output active power at the PCC, and ω^* and ω are the frequency reference and output angular frequency.

The rotating angle θ of Park transformation is generated by (1). The voltage reference is designed as $v_{\mathrm{ref}\,d} = V_{\mathrm{ref}}$, $v_{\mathrm{ref}\,q} = 0$ in the rotating d–q reference frame, thus, the voltage reference vector $\boldsymbol{v_{\mathrm{ref}}}$ is aligned with the d-axis directly. The angle difference δ is viewed as the virtual power angle, $\delta = \theta$-θ_g, which represents the angle difference between the rotating angle θ of the d–q rotating axis and the grid voltage angle θ_g.

The voltage & current loop adopts dual-loop vector-voltage control (VVC) with the proportional-integral (PI) controller [41]. The dual-loop VVC loop is used for regulating the output voltage $\boldsymbol{v_{\mathrm{pcc}}}$ to track the voltage reference $\boldsymbol{v_{\mathrm{ref}}}$ during normal operation. The generated current reference $i_{\mathrm{ref}\,dq}$ is expressed as follows:

$$i_{\mathrm{ref}dq} = \left(k_{Vp} + k_{Vi}\int\right)\left(v_{\mathrm{ref}dq} - v_{\mathrm{pccdq}}\right) + j\omega_g C_f v_{\mathrm{pccdq}} \tag{2}$$

where k_{vp} and k_{vi} are the proportional coefficient and integral coefficient of the PI-based voltage loop, respectively. When current limiter is triggered, the integral item is disabled to avoid the integral wind-up phenomena. The voltage integral controller is clamped, and its output will remain at the nominal value of I_{ndq} in normal operation mode.

The d-axis priority current limiter is implemented for overcurrent protection during fault conditions, which can be expressed as follows [19]:

$$\begin{cases} i_d^* = \frac{i_{\mathrm{ref}d}}{|i_{\mathrm{ref}d}|} \cdot \min\left(|i_{\mathrm{ref}d}|, I_{\max}\right) \\ i_q^* = \frac{i_{\mathrm{ref}q}}{|i_{\mathrm{ref}q}|} \cdot \min\left(|i_{\mathrm{ref}q}|, \sqrt{I_{\max}^2 - (i_d^*)^2}\right) \end{cases} \tag{3}$$

where $i_{\mathrm{ref}\,dq}$ represents the generated current reference of the outer voltage control loop and $i_{dq}{}^*$ represents the input current reference for the inner current control loop after d-axis priority current limiter. For the sake of simplification, capacitor current and the dynamics of the inductor and capacitor are neglected in later analysis.

According to (3), GFM inverters with d-axis priority current limiter have the following three operation modes.

1) Normal operation mode (NOM).
2) Current limitation mode stage 1 (CLM S1).
3) Current limitation mode stage 2 (CLM S2).

Fig. 2 shows the diagrams of the different modes.

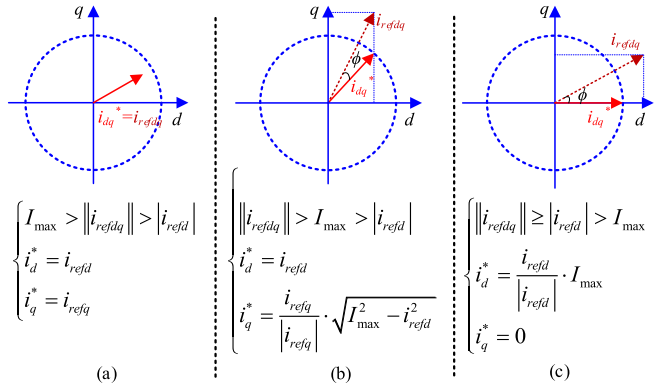

Fig. 2. Illustration of the d-axis priority current limiter. (a) Normal operation mode (NOM). (b) CLM S1. (c) CLM S2.

B. *Fault Recovery Issue Due to* D-*Axis Priority Current Limiter*

It is required that the GFM inverter restore normal operation mode from current limitation after fault clearance. Postfault phenomenon through theoretical analysis is reported in [31] and [32]. The two conditions for successful fault recovery can be summarized as follows:

1) *Condition 1:* After fault clearance, the power angle δ must satisfy the following:

$$\left\{\delta \left| \|i_{\text{ref}}^{\text{NOM}}(\delta)\| < I_{\max}\right.\right\} \cap \left\{\delta \left| \|i_{\text{ref}}^{\text{CLM}}(\delta)\| < I_{\max}\right.\right\} \neq \emptyset \tag{4}$$

where $i_{\text{ref}}{}^{\text{NOM}}$ denotes the generated current reference in normal operation mode and $i_{\text{ref}}{}^{\text{CLM}}$ represents the generated current reference in current limitation mode. Detailed derivations of these conditions can be found in Appendix A.

2) *Condition 2:* During the transient process, the power angle δ controlled by the GFM control (1) must pass through the stable equilibrium point under current limitation mode and ultimately converge to the stable equilibrium point of the system in normal operation mode.

Condition 1 can be fulfilled through the proper design of the power set point. However, different fault clearance angles influence the postfault transient behavior of GFM inverter, the validity of *Condition* 2 cannot be universally guaranteed. Fig. 3 shows the impacts of different fault clearance angles on postfault transient behavior. In Fig. 3(a), when the fault is cleared within a shorter time, the GFM inverter can exit the current limiting mode after fault clearance and eventually restores to the stable equilibrium point *a* of the system in the normal operation mode. In Fig. 3(b), when the fault is cleared after a longer time, the GFM inverter cannot exit the current limiting mode and eventually stabilizes at the stable equilibrium point *e* of the system in the current limiting mode.

Simulation results are given in Fig. 4 to directly reflect this fault recovery issue. Grid voltage drops to 0.2 p.u. at 2 s and the fault is cleared with different fault clearing time (FCT).

When $\text{FCT}_1 = 0.1$ s, the GFM inverter can successfully recover to normal operation mode and be stable in the previous stable equilibrium point (SEP), which is shown in Fig. 4(a).

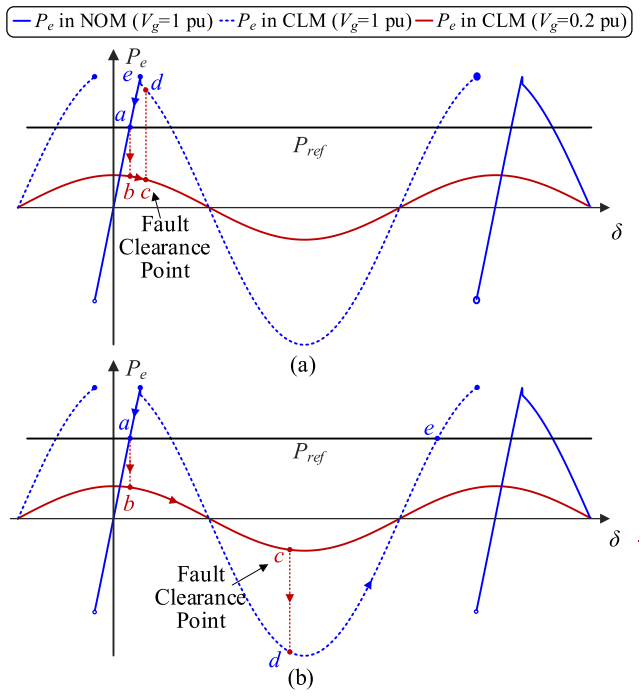

Fig. 3. Power angle Pe – δ curves of the GFM inverter with d-axis priority current limiter. (a) Successful fault recovery. (b) Failed fault recovery.

However, when the fault clearing time increases, the GFM inverter will be clamped in current limitation mode and be stable at another SEP introduced by the *d*-axis priority current limiter [seen in Fig. 4(b) with $\text{FCT}_2 = 1.03$ s and Fig. 4(c) with $\text{FCT}_3 = 1.5$ s]. With triggering current limitations, the traditional GFM control cannot guarantee *Condition* 2 for successful recovery to normal GFM operation after fault clearance.

III. Modified GFM Method for Fault Recovery

As is pointed in studies [21] and [26], *d*-axis current limiter can be modeled as a variable virtual impedance between the internal voltage $\boldsymbol{v}_{\mathbf{IVS}} = \boldsymbol{v}_{\mathbf{ref}}$ and the terminal voltage $\boldsymbol{v}_{\mathbf{pcc}}$, which is shown Fig. 5. Detail derivations for this equivalent model are shown in Appendix B. Inspired by the equivalent circuit, the P_{IVS}-feedback GFM control method is proposed to achieve successful fault recovery from current limitation mode to normal operation mode. P_{IVS} refers to the virtual power of the internal voltage source of the GFM inverter.

A. *Virtual Power* P_{IVS}*-Feedback GFM Control Method for d-Axis Priority Current Limiter*

As is depicted in Fig. 6, the P_{IVS}-feedback method can be expressed as follows:

$$\begin{cases} \omega = \omega^* + m_p\left(P_{\text{ref}} - P_{\text{IVS}}\right) \\ V_{\text{ref}d} = V_{\text{ref}} \\ V_{\text{ref}q} = 0 \end{cases} \tag{5}$$

where V_{ref} represents the amplitude of voltage reference, which is set as constant for sake of analysis. The voltage reference $\boldsymbol{v}_{\mathbf{ref}}$

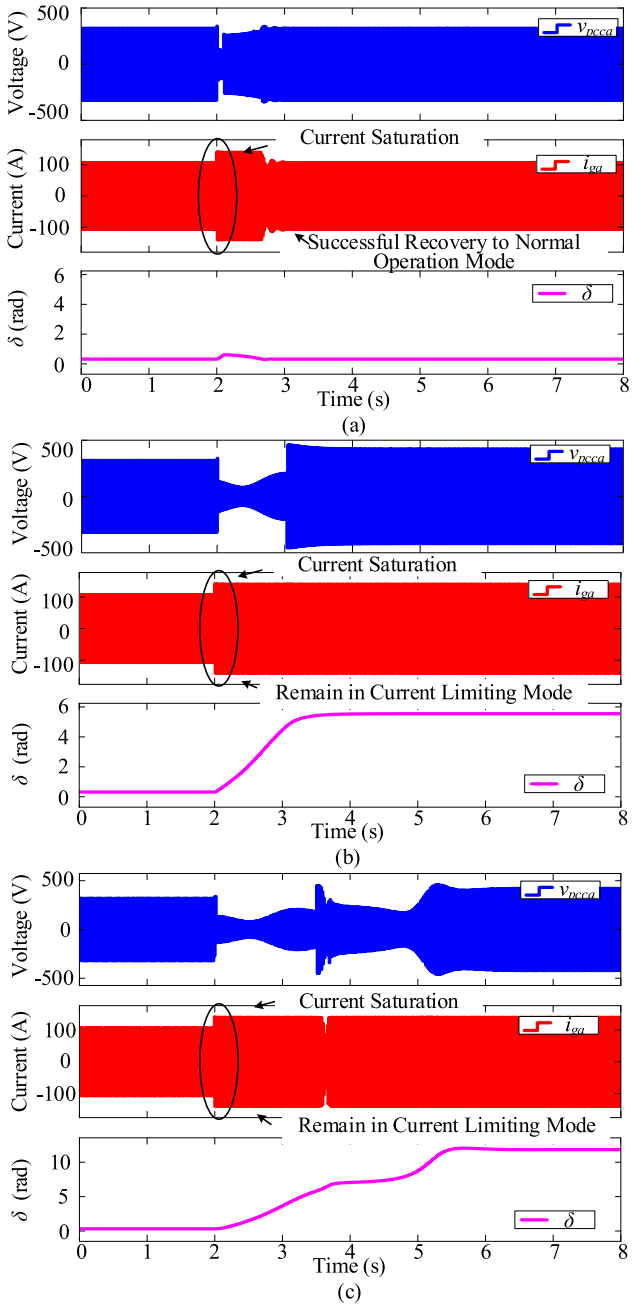

Fig. 4. Simulation results with different fault clearing time (FCT): (a) FCT1 = 0.1 s, (b) FCT2 = 1.03 s, and (c) FCT3 = 1.5 s.

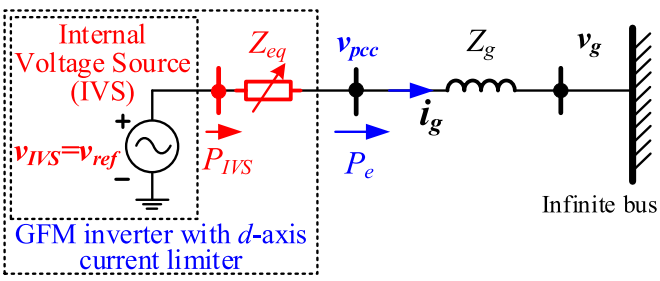

Fig. 5. Equivalent circuit of the GFM inverter with DPCL.

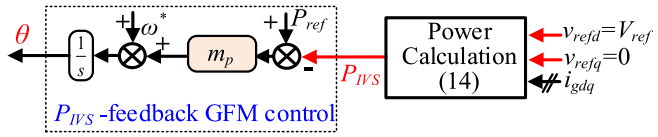

Fig. 6. PIVS-feedback GFM control method.

generated through (5) is viewed as the internal voltage $\boldsymbol{v}_{\mathbf{IVS}}$, $\boldsymbol{v}_{\mathbf{IVS}} = \boldsymbol{v}_{\mathbf{ref}}$.

Thus, P_{IVS} can be easily calculated through the voltage reference $\boldsymbol{v}_{\mathbf{ref}}$ (virtual voltage) and the actual output current $\boldsymbol{i}_{\boldsymbol{g}}$ in d–q frame

$$P_{\mathrm{IVS}} = \frac{3}{2}\left(v_{\mathrm{ref}d} i_{gd} + v_{\mathrm{ref}q} i_{gq}\right) = \frac{3}{2} V_{\mathrm{ref}} i_{gd} \tag{6}$$

Compared with traditional GFM control in Fig. 1, the only modification is that the power feedback uses P_{IVS}, the equivalent virtual power of the internal voltage source, instead of the actual output power P_e at the PCC.

B. Characteristics Analysis Under Different Operation Modes

P_{IVS} changes autonomously according to operation modes. In normal operation mode, the d-axis priority current limiter is not triggered. Due to the tracking function of the inner PI-based voltage loop, the output voltage $\boldsymbol{v}_{\mathbf{pcc}}$ is equal to the internal voltage $\boldsymbol{v}_{\boldsymbol{IVS}}$ and the equivalent variable virtual impedance Z_{eq} equals zero. The power transmission characteristics of P_{IVS} can be derived as follows:

$$P_{\mathrm{IVS}} = P_e = \frac{3 V_{\mathrm{ref}} V_g}{2 X_g} \sin\delta \tag{7}$$

where V_g and X_g represent the grid voltage amplitude and grid impedance, respectively. $\delta = \theta - \theta_g$ represents the power angle as well as the phase angle difference between $\boldsymbol{v}_{\mathbf{IVS}}$ and $\boldsymbol{v}_{\boldsymbol{g}}$.

Thus, when the GFM inverter operates in normal operation mode, $P_{\mathrm{IVS}} = P_e$, $\boldsymbol{v}_{\mathbf{IVS}} = \boldsymbol{v}_{\mathbf{pcc}}$. The P_{IVS}-feedback method is completely identical to traditional GFM control, providing the same voltage/frequency support and grid-forming service.

In current limitation mode, the d-axis priority current limiter is triggered. $\left\| i_{\mathrm{ref}dq} \right\|$ is larger than $I_{\max}$, $\left\| i_{gdq} \right\| = I_{\max}$. $\boldsymbol{v}_{\mathbf{pcc}}$ is no longer equal to $\boldsymbol{v}_{\boldsymbol{IVS}}$. Then, P_{IVS} can be derived as follows:

$$P_{IVS} = \begin{cases} \frac{3}{2} V_{ref} I_{\max} cos\varphi, \text{ CLM S1} \\ \frac{3}{2} V_{ref} I_{\max}, \text{ CLM S2} \end{cases} \tag{8}$$

where $\varphi = \theta - \theta_i$ represents virtual power factor angle between $\boldsymbol{v}_{\mathbf{IVS}}$ and $\boldsymbol{i}_{\boldsymbol{g}}$, which can be further calculated as follows:

$$\varphi = \arctan \left| \frac{\sqrt{I_{\max}^2 - (i_{\mathrm{ref}d})^2}}{i_{\mathrm{ref}d}} \right|. \tag{9}$$

According to (2) and (3), the phase angle condition for entering CLM S1 from CLM S2 can be derived as follows:

$$|\delta| < \cos^{-1}\left[\frac{k_{Vp} V_{\mathrm{ref}} - (I_{\max} - I_{nd})}{k_{Vp} V_{\mathrm{pcc}}} \right]. \tag{10}$$

Thus, the phase angle boundary can be further expressed as follows:

$$\begin{cases} \delta_{b1} = cos^{-1}\left[\frac{k_{Vp}V_{\rm ref}-(I_{\max}-I_{nd})}{k_{Vp}V_{\rm pcc}}\right] \\ \delta_{b2} = -cos^{-1}\left[\frac{k_{Vp}V_{\rm ref}-(I_{\max}-I_{nd})}{k_{Vp}V_{\rm pcc}}\right] \end{cases} \tag{11}$$

where δ_{b1} and δ_{b2} represent the critical angles between CLM S1 and CLM S2 and $V_{\rm pcc}$ represents the output voltage amplitude of PCC.

It is worth mentioning that CLM S1 is a transitional state [32], and when the d-axis priority current limiter is triggered, the GFM inverter will eventually operate at CLM S2, which will be elaborated in the following analysis. In CLM S2, $P_{\rm IVS} > P_{\rm ref}$, δ will first decrease and then increase in the opposite direction according to (5), which can ensure the GFM inverter successfully exit current limitation mode after fault clearance.

The postfault process and the mechanism of the proposed method to guarantee successful fault recovery to normal operation mode will be analyzed in Sections IV and V.

C. Effect of Reactive Power-Voltage Control Loop

Considering the reactive power -voltage (Q_e-$V_{\rm ref}$) control loop, the voltage reference amplitude $V_{\rm ref}$ will change when grid fault occurs. The Q_e-$V_{\rm ref}$ control loop can be expressed as follows:

$$V_{ref} = v^* + n_Q\left(Q_{ref} - Q_e\right) \tag{12}$$

where V^* represents the basis value of voltage amplitude, $Q_{\rm ref}$ and Q_e represents the reactive power reference and output reactive power, and n_Q is the reactive power-voltage coefficient.

Considering the transmission characteristics of reactive power Q_e, the $P_{\rm IVS}$–δ characteristic in current limitation mode can be derived as follows:

$$P_{\rm IVS}\left(\delta\right) = \frac{I_{\max}\left[1.5n_QV_g{\rm cos}\delta - X_g + f\left(\delta\right)\right]}{2n_Q} \tag{13}$$

where

$$f\left(\delta\right) = \sqrt{\left(X_g - 1.5n_QV_g{\rm cos}\delta\right)^2 + 6n_QX_g\left(V^* + n_QQ_{\rm ref}\right)}. \tag{14}$$

According to study [42], the coefficient n_Q is usually designed as follows:

$$0 \le n_Q \le \frac{\Delta V_{\max}}{\Delta Q_{\max}} \tag{15}$$

where $\Delta V_{\max}$ and $\Delta Q_{\max}$ are the maximum allowable variations of voltage and reactive power.

Fig. 7 shows the $P_{\rm IVS}$–δ curves with different grid voltage sags (V_{gf} = 0.1–0.5 p.u.). Even though the maximum value of n_Q is considered, the calculated $P_{\rm IVS}$ through (13) under current limitation mode is still larger than $P_{\rm ref}$. Thus, the fault recovery mechanism is the same as that with constant voltage reference control. In current limitation mode, $P_{\rm IVS} > P_{\rm ref}$, δ first decrease and then increase in the opposite direction, which can ensure the GFM inverter successfully exit current limitation mode after fault clearance. Thus, the proposed method can still guarantee successful fault recovery after fault clearance.

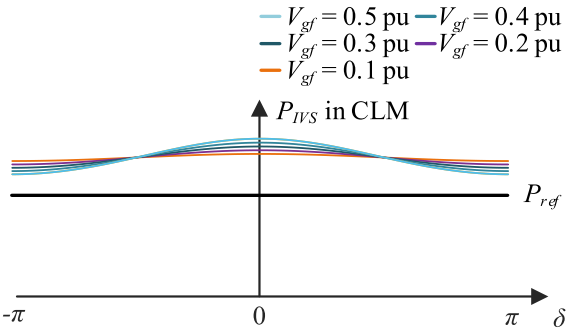

Fig. 7. Power-angle PIVS-δ curves with Qe-Vref control loop under different grid voltage sags in current limitation mode.

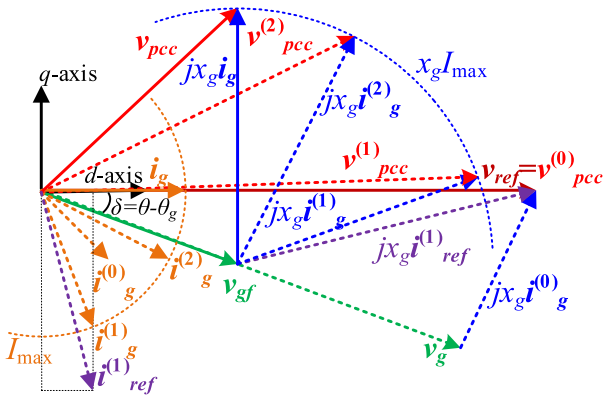

Fig. 8. Phasor diagram of GFM inverter from NOM to CLM S2.

IV. Fault Recovery Analysis Under Proposed Method

This section presents the fault recovery analysis under the $P_{\rm IVS}$-feedback method. Phasor diagram analysis combined with the trajectory of δ is implemented to elaborate the postfault process. The capacitor current and the dynamics of the inductor and capacitor are neglected, $\boldsymbol{i_g} \approx \boldsymbol{i_L}$.

To simplify the analysis, an important assumption is stated here: The dynamics of δ are slower than the dynamics of voltage loop. As the timescales of power control loop and voltage/current inner loop are about 10 times, these loops are fully decoupled [43]. This assumption is valid since the bandwidth of voltage/current inner loop control is usually much higher than those of power-angle loop controls. Thus, we first analyze the change in output current $\boldsymbol{i_g}$ based on the voltage-current phasor diagram. Then, the dynamics of δ for the next steps are considered.

A. Fault Process Analysis Before Fault Clearance

When grid voltage sag occurs, $\boldsymbol{v_g}$ turns into $\boldsymbol{v_{gf}}$. There will be two possible ways for the GFM inverter to change from NOM to CLM. The first scenario occurs when the fault current reference $i_{\rm ref}$ satisfies $|i_{{\rm ref}\,d}| > I_{\max}$, causing the inverter to directly switch from normal operation mode to CLM S2. The second scenario involves that the inverter initially transits from normal operation mode to CLM S1 and ultimately reaches CLM S2. Fig. 8 shows the phasor diagram. The process of NOM → CLM S1 → CLM S2 can be divided into the following steps:

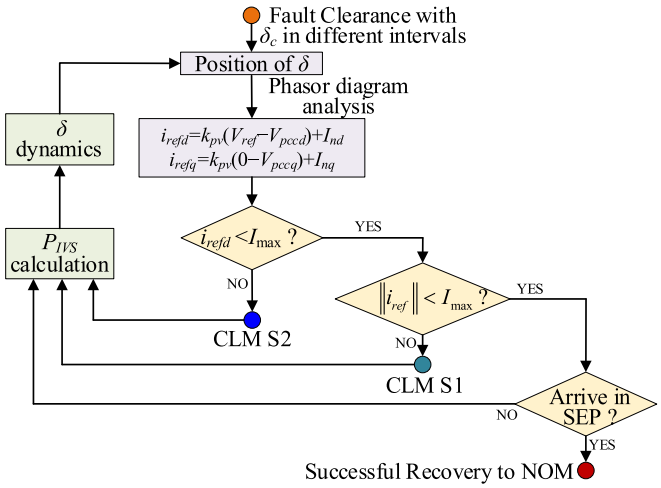

Fig. 9. Fault recovery process of PIVS-feedback GFM control.

Step 0: $\boldsymbol{v}_g$ turns into $\boldsymbol{v}_{gf}$, and $\boldsymbol{v}_{\mathbf{pcc}}=\boldsymbol{v}_{\mathbf{ref}}$ remains unchanged. The current reference $\boldsymbol{i}^{(1)}_{\mathbf{ref}}$ is generated. The inverter enters CLM S1, $\boldsymbol{i}^{(0)}_g$ turns to $\boldsymbol{i}^{(1)}_g$, and $i^{(1)}{}_{gd}$ decreases, $i^{(1)}{}_{gd} < i^{(0)}{}_{gd} = I_{nd}$.

Step 1: The output voltage $\boldsymbol{v}^{(0)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$, which is re-established according to $\boldsymbol{v}_{gf}$ and $jx_g\boldsymbol{i}^{(1)}_g$. Thus, $v^{(1)}{}_{\mathrm{pcc}\,d}$ decreases, $v^{(1)}{}_{\mathrm{pcc}\,d} < v^{(0)}{}_{\mathrm{pcc}\,d} = v_{\mathrm{ref}\,d}$.

Step 2: Due to $k_{Vi} = 0$, the current reference $i^{(2)}{}_{\mathrm{ref}\,d} = k_{Vp}(v_{\mathrm{ref}\,d}-v^{(1)}{}_{\mathrm{pcc}\,d})+I_{nd}$ further increases, $i^{(2)}{}_{\mathrm{ref}\,d} > i^{(1)}{}_{gd}$. Thus, the output current can come from $\boldsymbol{i}^{(1)}_g$ to $\boldsymbol{i}^{(2)}_g$. Repeat the above steps, the output voltage and current reach $\boldsymbol{v}_{\mathbf{pcc}}$ and $\boldsymbol{i}_g$ finally.

In summary, when grid fault occurs and the current limitation is triggered, the variation process of output voltage and current is: $\boldsymbol{v}^{(0)}_{\mathbf{pcc}} \rightarrow \boldsymbol{v}^{(1)}_{\mathbf{pcc}} \rightarrow \boldsymbol{v}^{(2)}_{\mathbf{pcc}} \rightarrow \boldsymbol{v}_{\mathbf{pcc}}$, $\boldsymbol{i}^{(0)}_g \rightarrow \boldsymbol{i}^{(1)}_g \rightarrow \boldsymbol{i}^{(2)}_g \rightarrow \boldsymbol{i}_g$. The mode of operation changes firstly from NOM to CLM S1 and finally arrives at CLM S2.

According to above analysis, regardless of the way taken after the grid fault, the operation mode of the GFM inverter finally arrives in CLM S2. Then, the motion of δ is considered. In CLM S2, $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$, δ decreases according to (5). Different fault clearing time determines different δ_c at different intervals. Therefore, the postfault recovery analysis under the P_{IVS}-feedback method should be comprehensively discussed in six scenarios ($0^0 < \delta_c < \delta_{b1}$, $\delta_{b2} < \delta_c < 0^0$, $-90^0 < \delta_c < \delta_{b2}$, $-180^0 < \delta_c < -90^0$, $-270^0 < \delta_c < -180^0$, $\delta_{b1}-360^0 < \delta_c < -270^0$). The flowchart of postfault recovery analysis is shown in Fig. 9.

B. Postfault Analysis With Fault Clearance At $0^0 < \delta_c < \delta_{b1}$

Fig. 10 shows the phasor diagram when the fault is cleared with $0^0 < \delta_c < \delta_{b1}$. The process after fault clearance can be divided into the following steps:

Step 0: When the fault is cleared, $\boldsymbol{v}_{gf}$ turns to $\boldsymbol{v}^{(1)}_g$. The output current cannot be suddenly changed, $\boldsymbol{i}^{(0)}_g = \boldsymbol{i}^{(1)}_g$. Thus, the output voltage $\boldsymbol{v}^{(0)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$, and the d-axis voltage component $v^{(1)}{}_{\mathrm{pcc}\,d}$ increases, $v^{(1)}{}_{\mathrm{pcc}\,d} > v^{(0)}{}_{\mathrm{pcc}\,d}$. According to

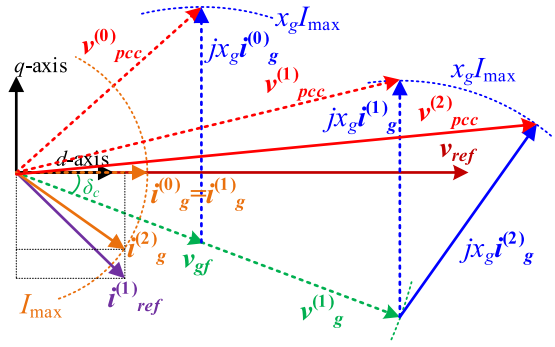

Fig. 10. Phasor diagram of GFM inverter with $0^0 < \delta c < \delta b1$.

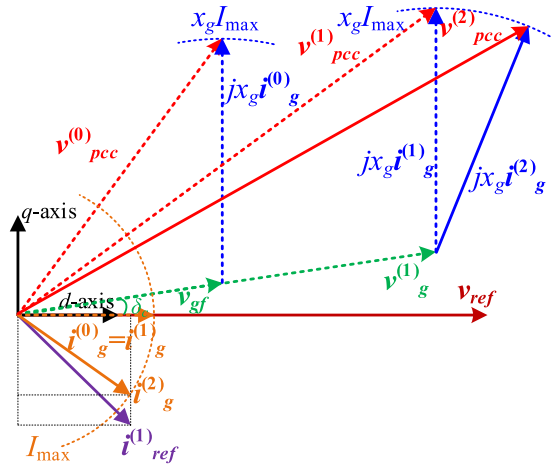

Fig. 11. Phasor diagram of GFM inverter with $\delta b2 < \delta c < 0^0$.

(10), $i^{(1)}{}_{\mathrm{ref}\,d} = k_{Vp}(v_{\mathrm{ref}\,d}-v^{(1)}{}_{\mathrm{pcc}\,d})+I_{nd} < I_{\max}$ due to $0^0 < \delta_c < \delta_{b1}$. The operation mode comes from CLM S2 into CLM S1.

Step 1: Considering that $i^{(1)}{}_{\mathrm{ref}\,q} = k_{Vp}(0-v^{(1)}{}_{\mathrm{pcc}\,q}) + I_{nq} < I_{nq} < 0$, $\boldsymbol{i}^{(1)}_{\mathbf{ref}}$ can be determined, and $\boldsymbol{i}^{(1)}_g$ turns to $\boldsymbol{i}^{(2)}_g$ according to $\boldsymbol{i}^{(1)}_{\mathbf{ref}}$.

Step 2: Effected by $\boldsymbol{i}^{(2)}_g$, $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(2)}_{\mathbf{pcc}}$, $v^{(2)}{}_{\mathrm{pcc}\,d}$ increases, $v^{(2)}{}_{\mathrm{pcc}\,q}$ decreases. Then, both $i_{\mathrm{ref}\,d}$ and $i_{\mathrm{ref}\,q}$ decrease, the phasor $\boldsymbol{i}_g$ rotates counterclockwise. Furthermore, $v_{\mathrm{pcc}\,d}$ increases while $v_{\mathrm{pcc}\,q}$ decreases. Then, $i_{\mathrm{ref}\,d}$ and $i_{\mathrm{ref}\,q}$ continue to decrease.

The above process will be repeated until $\| i_{\mathrm{ref}} \| < I_{\max}$, the inverter can finally recover to NOM, $P_{\mathrm{IVS}} = P_e$.

C. Fault Clearance At $\delta_{b2} < \delta_c < 0^0$

As δ decreases continuously with longer fault clearing time, the fault may be cleared with $\delta_{b2} < \delta_c < 0^0$. Fig. 11 shows the phasor diagram.

Step 0: $\boldsymbol{v}_{gf}$ turns to $\boldsymbol{v}^{(1)}_g$, $\boldsymbol{i}^{(0)}_g = \boldsymbol{i}^{(1)}_g$. $\boldsymbol{v}^{(0)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$, $v^{(1)}{}_{\mathrm{pcc}\,d}$ increases, $v^{(1)}{}_{\mathrm{pcc}\,d} > v^{(0)}{}_{\mathrm{pcc}\,d}$. $i^{(1)}{}_{\mathrm{ref}\,d} = k_{Vp}(v_{\mathrm{ref}\,d} - v^{(1)}{}_{\mathrm{pcc}\,d}) + I_{nd} < I_{\max}$ due to $\delta_{b2} < \delta_c < 0^0$. The operation mode comes into CLM S1.

Step 1: Considering that $i^{(1)}{}_{\mathrm{ref}\,q} = k_{Vp}(0 - v^{(1)}{}_{\mathrm{pcc}\,q}) + I_{nq} < I_{nq} < 0$, $\boldsymbol{i}^{(1)}_{\mathbf{ref}}$ can be determined, and $\boldsymbol{i}^{(1)}_g$ turns to $\boldsymbol{i}^{(2)}_g$ according to $\boldsymbol{i}^{(1)}_{ref}$.

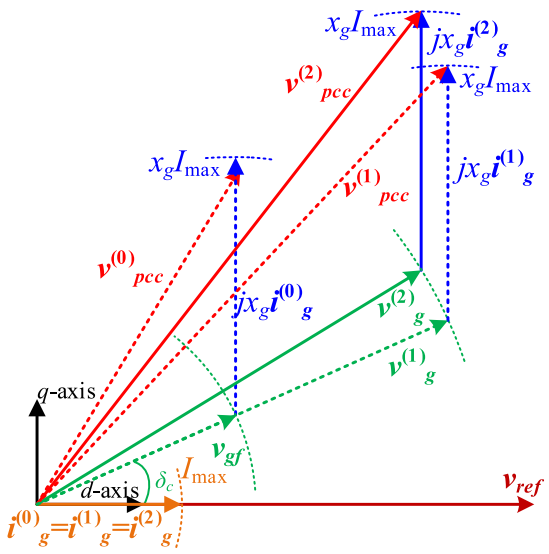

Fig. 12. Phasor diagram of GFM inverter with -90^0 < δc < δb2.

Step 2: $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(2)}_{\mathbf{pcc}}$, $v^{(2)}{}_{\mathrm{pcc}\,d}$ increases, while $v^{(2)}{}_{\mathrm{pcc}\,q}$ decreases. Then, both $i_{\mathrm{ref}\,d}$ and $i_{\mathrm{ref}\,q}$ decrease and the phasor $\boldsymbol{i}_g$ rotates counterclockwise. Furthermore, $v_{\mathrm{pcc}\,d}$ increases, v_{pccq} decreases. The above process will be repeated until $\| i_{\mathrm{ref}} \| < I_{\max}$, the inverter can finally recover to normal operation mode and be stable at the stable equilibrium point of normal operation mode.

D. Fault Clearance At $-90^0 < \delta_c < \delta_{b2}$

Fig. 12 shows the phasor diagram with $-90^0 < \delta_c < 0^0$.

Step 0: $\boldsymbol{v}_{gf}$ turns to $\boldsymbol{v}^{(1)}_g$, $\boldsymbol{v}^{(0)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$, $v^{(1)}{}_{\mathrm{pcc}\,d}$ increases, $v^{(1)}{}_{\mathrm{pcc}\,d} > v^{(0)}{}_{\mathrm{pcc}\,d}$. According to (18), $i^{(1)}{}_{\mathrm{ref}\,d} > I_{\max}$. The inverter remains in CLM S2, $\boldsymbol{i}^{(0)}_g = \boldsymbol{i}^{(1)}_g = \boldsymbol{i}^{(2)}_g$.

Step 1: As $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$, δ continues to decrease. The grid voltage $\boldsymbol{v}^{(1)}_g$ turns to $\boldsymbol{v}^{(2)}_g$. And$\boldsymbol{v}^{(1)}_{\boldsymbol{pcc}}$ turns to $\boldsymbol{v}^{(2)}_{\boldsymbol{pcc}}$, $v^{(2)}{}_{pccd}$ decreases, $i^{(2)}{}_{d\mathrm{ref}}$ increases, $i^{(2)}{}_{\mathrm{ref}\,d} > i^{(1)}{}_{\mathrm{ref}\,d} > i^{(0)}{}_{\mathrm{ref}\,d} > I_{\max}$. Thus, the inverter remains in CLM S2.

Step 2: δ decreases and enters the next interval $(-180^0, -90^0)$.

When fault clearance angle locates at the interval $(-180^0 < \delta_c < -90^0)$, $(-270^0 < \delta_c < -180^0)$, and $(\delta_{b1}-360^0 < \delta_c < -270^0)$, the phasor diagram analysis is similar with that at the interval $(-90^0 < \delta_c < \delta_{b2})$, detailed analysis can be found at Appendix C.

E. Discussion

From the above analysis, several insights can be drawn:

1) When the *d*-axis priority current limiter is triggered, the GFM inverter changes from normal operation mode to CLM S1 first and finally enters CLM S2. During current limitation mode, δ continues to decrease due to $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$. Different fault clearance time leads to different intervals of δ_c.
2) When δ_c lies in the interval $(\delta_{b2}+n\times360°, \delta_{b1}+n\times360°)$, where $n = 0, 1, 2, \ldots$, the inverter can exit current limitation mode and recover to normal operation mode.
3) When δ_c is out of the interval $(\delta_{b2}+n\times360°, \delta_{b1}+n\times360°)$, the inverter cannot exit current limitation mode immediately. Due to $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$, δ decreases and enters the next interval $(\delta_{b2}+n\times360°, \delta_{b1}+n\times360°)$ and finally recovers to normal operation mode.

In summary, the proposed method ensures that the GFM inverter with the *d*-axis priority current limiter can exit current limitation and restore to the GFM operation mode after fault clearance, regardless of how long the fault persists.

V. Proposed Universal Virtual Power P_{IVS}-Feedback Method and Comparative Study With Different Current Limiters

The above analysis proves that the proposed P_{IVS}-feedback method in (5) and (6) can well address the fault recovery issue caused by *d*-axis priority current limiter. To explore and extend the applicability of the proposed method to other current limiters, a universal P_{IVS}-feedback method is proposed in this section, which exhibits identical power angle characteristics across priority current limiter and circular current limiter. Then, a comparative study through theorical analysis is provided to summarize the advantages and disadvantages of the main typical virtual power feedback methods equipped with different current limiters.

A. Universal Virtual Power P_{IVS}-Feedback Method

Compared with (5) and (6), only a modification of calculation of P_{IVS} is made. The universal P_{IVS}-feedback control with the modified calculation of P_{IVS} is as follows:

$$\begin{cases} \omega = \omega^* + m_p\,(P_{\mathrm{ref}} - P_{\mathrm{IVS}}) \\ V_{\mathrm{ref}\,d} = V_{\mathrm{ref}} \\ V_{\mathrm{ref}\,q} = 0 \end{cases}, P_{\mathrm{IVS}}$$
$$= \begin{cases} \frac{3V_{\mathrm{ref}}\,i_{gd}}{2}, \|i_{\mathrm{ref}\,dq}\| < I_{\max} \\ \frac{3V_{\mathrm{ref}}\,I_{\max}}{2}, \|i_{\mathrm{ref}\,dq}\| \geq I_{\max} \end{cases}. \tag{16}$$

Equation (16) shows that the calculation of P_{IVS} changes when current limiter is triggered. P_{IVS} equals the apparent power (capacity) of the internal voltage source in the current limitation mode. When the proposed universal method works with *d*-axis priority current limiter, P_{IVS} after modification is the same as that in the previously proposed method in CLM S2, due to $i_{\mathrm{gd}} = I_{\max}$ when *d*-axis priority current limiter is triggered under severe grid faults.

Under this modification, no matter whether priority current limiter or circular current limiter that the proposed method works with, it has the identical power angle characteristics.

1) In normal operation mode ($\|i_{\mathrm{ref}\,dq}\| < I_{\max}$), $P_{\mathrm{IVS}} = P_e$, the proposed method does not influence the grid-forming ability

$$P_{\mathrm{IVS}} = P_e = \frac{3V_{\mathrm{ref}}V_g}{2X_g}\sin\delta \tag{17}$$

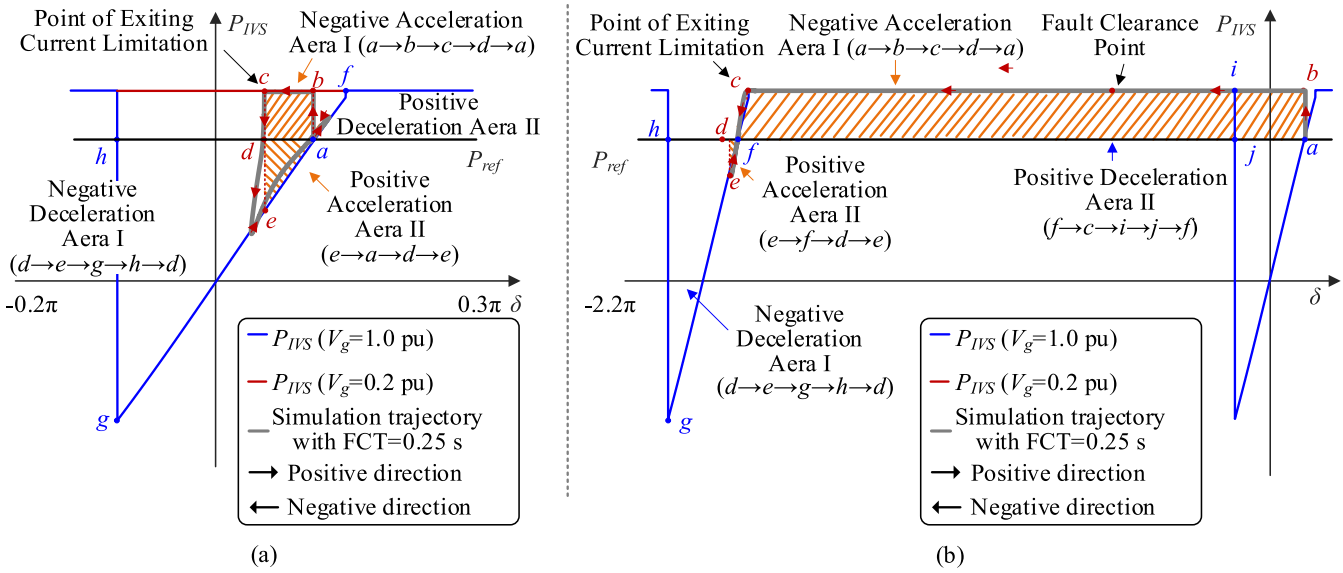

Fig. 13. Power-angle PIVS-δ curves of the proposed universal method with different fault clearance angle. (a) When fault clearance angle lies in the interval (δb2, δb1), FCT = 0.25 s. (b) When fault clearance angle lies out of the interval (δb2, δb1), FCT = 0.625 s.

2) In current limitation mode ($\|i_{\mathrm{ref}\,dq}\| \geq I_{\max}$), P_{IVS} is larger than P_{ref}

$$P_{\mathrm{IVS}} = \frac{3}{2} V_{\mathrm{ref}} I_{\max} > P_{\mathrm{ref}}. \tag{18}$$

Fig. 13 shows the power-angle curves of the proposed method with two typical scenarios. The first scenario shown in Fig. 13(a) corresponds the previous analysis in Section IV with the fault clearance angle lies in the interval (δ_{b2}, δ_{b1}). The second scenario shown in Fig. 13(b) corresponds the previous analysis in Section IV with the fault clearance angles lies out of the interval (δ_{b2}, δ_{b1}).

When fault occurs, $\|i_{\mathrm{ref}\,dq}\| \geq I_{\max}$, then, $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$. The P_{IVS}-δ curve changes to the green line. As long as the GFM inverter operates in current limitation mode, no equilibrium point exists due to $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$, thus preventing the GFM inverter from stabilizing in current limitation mode. Define the increasing direction of δ as the positive direction, whereas the decreasing direction is defined as the negative direction. $P_{\mathrm{IVS}} > P_{\mathrm{ref}}$ drives δ moves towards negative direction. with the operating point following the trajectory: $a \rightarrow b$.

In Fig. 13(a), the fault clearance angle lies in the interval (δ_{b2}, δ_{b1}). According to the fault recovery analysis in Section IV, the GFM inverter can exit current limitation mode at Point c, thus, P_{IVS} equals P_e and the operation point moves from c to e. During this process, the negative acceleration area I is the region bounded by a closed curve ($a \rightarrow b \rightarrow c \rightarrow d \rightarrow a$). The negative deacceleration area I ($d \rightarrow e \rightarrow g \rightarrow h \rightarrow d$) prevents δ from keeping increased in negative direction. Then, the operation point will follow the route: $e \rightarrow a$. In this subsequent process, the region enclosed by the closed curve ($d \rightarrow e \rightarrow a \rightarrow d$) serves as the positive acceleration area II, while the positive deceleration area II can prevents δ from continuing to increase in positive direction. Once the acceleration area is less than that of the deceleration area, the GFM inverter can stabilize at point a, ultimately.

In Fig. 13(b), the fault clearance angle lies out of the interval (δ_{b2}, δ_{b1}). The GFM inverter cannot directly exit current limitation mode, instead δ continues to move towards the negative direction and finally exits the current limitation mode at Point c. Then, P_{IVS} changes and equals P_e, and the operation point moves from c to e. During this process, the negative acceleration area I is the region bounded by a closed curve ($a \rightarrow b \rightarrow c \rightarrow f \rightarrow a$). The negative deacceleration area I ($d \rightarrow e \rightarrow g \rightarrow h \rightarrow d$) prevents δ from keeping increased in negative direction. Then, the operation point will follow the route: $e \rightarrow a$. In this subsequent process, the region enclosed by the closed curve ($e \rightarrow f \rightarrow d \rightarrow e$) serves as the positive acceleration area II, while the positive deceleration area II ($f \rightarrow c \rightarrow i \rightarrow j \rightarrow f$) can prevents δ from continuing to increase in positive direction. Once the acceleration area is less than that of the deceleration area, the GFM inverter can stabilize at point f, which is the stable equilibrium point from the previous period at point a, ultimately.

Across both two typical scenarios, the proposed method expands the deceleration area, thereby significantly enhancing the transient synchronization stability, and guarantees the successful fault recovery from current limitation mode to normal operation mode of the GFM inverter with the current limiter.

B. Equivalent Models of Various Virtual Power Feedback Methods With Various Current Limiters

To better reflect the relationship between internal voltage (virtual voltage), unsaturated current reference (virtual current), output voltage (actual voltage) and output current (actual current), Fig. 14 shows the further developed equivalent circuit, which can clearly display the relationship among $\boldsymbol{v}_{\mathbf{IVS}}$, $\boldsymbol{v}_{\mathbf{pcc}}$, $\boldsymbol{i}_{\mathbf{ref}}$, and $\boldsymbol{i}_g$. $\boldsymbol{i}_n$ denotes the nominal output current at the setpoint in normal operation mode. Z_{VVC} denotes the equivalent impedance of

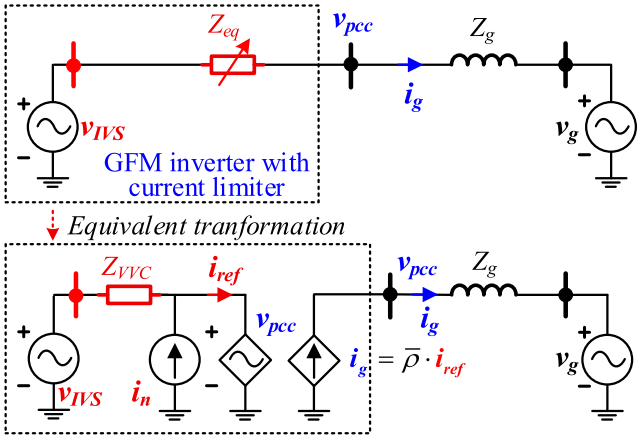

Fig. 14. Equivalent circuit model of the GFM inverter with current limiter.

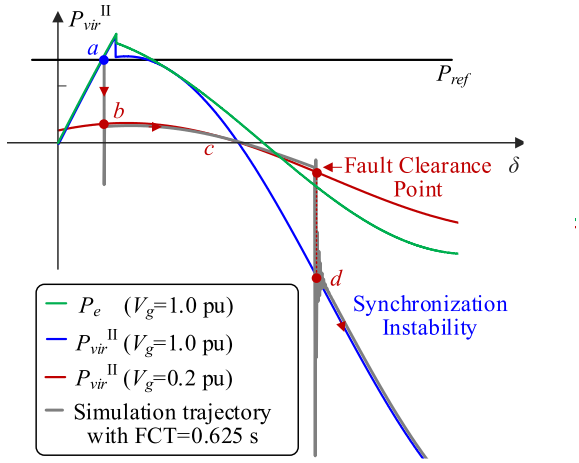

Fig. 15. Power-angle PvirII–δ curves of virtual power way II [37] with d-axis priority current limiter.

the inner voltage vector control loop. When current limiter is triggered, the integral item of PI-based VVC is disabled and Z_{VVC} can be expressed as follows:

$$Z_{\mathrm{VCC}} = \frac{1}{k_{Vp}} \tag{19}$$

where k_{Vp} represents the proportional coefficient of PI controller.

$\bar{\rho}$ represents the current saturation vector between unsaturated current reference $\boldsymbol{i}_{\mathbf{ref}}$ and the actual output current $\boldsymbol{i}_g$, which can be expressed as follows [44]:

$$\bar{\rho} = \begin{cases} \rho e^{j(\delta - \theta_{i\mathrm{ref}} - \gamma)}, & \text{priority current limiter} \\ \rho, & \text{circular current limiter} \end{cases}, \rho = \frac{I_{\max}}{\|i_{\mathrm{ref}dq}\|} \tag{20}$$

where $\theta_{i\mathrm{ref}}$ donates the phase angle of the unsaturated current reference, γ donates the phase angle of the priority current limiter, and $\gamma = 0$ with d-axis priority current limiter.

According to Fig. 14, the different implementations of virtual power can be divided into the following three main categories:

1) The proposed method, which combines internal voltage $\boldsymbol{v}_{\mathbf{IVS}}$ (virtual voltage) and actual output current $\boldsymbol{i}_g$;
2) Virtual power way II [37], [38], which combines actual output voltage $\boldsymbol{v}_{\mathbf{pcc}}$ and unsaturated current reference $\boldsymbol{i}_{\mathbf{ref}}$ (virtual current);
3) Virtual power way III [39], [40], which combines internal voltage $\boldsymbol{v}_{\mathbf{IVS}}$ (virtual voltage) and current reference $\boldsymbol{i}_{\mathbf{ref}}$ (virtual current).

Apparently, different current limiters yield varying $\boldsymbol{i}_g$, $\boldsymbol{v}_{\mathbf{pcc}}$, and $\boldsymbol{i}_g$, and further determine the different virtual power-angle characteristics of virtual power implementations. Consequently, the impacts of two typical current limiters (d-axis priority current limiter and circular current limiter) across the prementioned three typical virtual power implementations will be discussed.

C. Different Virtual Power Feedback Methods With d-Axis Priority Current Limiter

1) Proposed Method: According to the previous analysis, the proposed method can well address the fault recovery issue and enhance the transient synchronization stability of GFM inverter with d-axis priority current limiter.

2) Virtual Power Way II in [37], [38]: When $\|i_{\mathrm{ref}dq}\| \geq I_{\max}$, the virtual power $P_{\mathrm{vir}}{}^{\mathrm{II}}$ under virtual power way II with d-axis priority current limiter in [37] can be derived as follows:

$$P_{\mathrm{vir}}^{\mathrm{II}} = \frac{3}{2}\left(a_{\mathrm{II}}\cos\delta + b_{\mathrm{II}}\sin\delta + c_{\mathrm{II}}\right) \tag{21}$$

where

$$\begin{cases} a_{\mathrm{II}} = V_g\left(k_{Vp}V_{\mathrm{ref}} - 2k_{Vp}I_{\max}X_g + I_{nd}\right) \\ b_{\mathrm{II}} = -V_g I_{nq} \\ c_{\mathrm{II}} = I_{\max}X_g\left(I_{nd} + k_{Vp}V_{\mathrm{ref}}\right) - k_{Vp}\left(V_g^2 + I_{\max}^2 X_g^2\right). \end{cases} \tag{22}$$

Detailed derivations can be seen in Appendix D. Fig. 15 shows the virtual power-angle $P_{\mathrm{vir}}{}^{\mathrm{II}}$–$\delta$ curves under different operation modes. The corresponding parameters are consistent with those in the hardware-in-loop (HIL) tests. As depicted in Fig. 15, $P_{\mathrm{vir}}{}^{\mathrm{II}}$ in CLM after fault clearance is almost below P_e, resulting in a greatly large acceleration aera and a very small deceleration area for maintaining synchronization. The simulation trajectory shows the consistency with the derived virtual power-angle curves. Thus, the transient synchronization stability of the GFM inverter with d-axis priority current limiter is significantly degraded under virtual power way II [37].

Literature [38] adopts the virtual power way II with a modification in synchronization loop, which is expressed as follows:

$$\omega = \omega^* + m_p\left[P_{\mathrm{ref}} - P_e - k\left(P_{\mathrm{vir}}^{\mathrm{II}} - P_{\mathrm{Lim}}\right)\right] \tag{23}$$

where P_{Lim} denotes also a virtual power but is close to P_e.

When $\|i_{\mathrm{ref}dq}\| \geq I_{\max}$, the control law in (23) can be further expressed in the form of virtual power $P_{\mathrm{vireq}}{}^{\mathrm{II}}$ feedback as follows:

$$\omega = \omega^* + m_p[P_{ref} - \underbrace{kP_{vir}^{\mathrm{II}} + (k-1)P_e}_{P_{\mathrm{vireq}}^{\mathrm{II}}}] \tag{24}$$

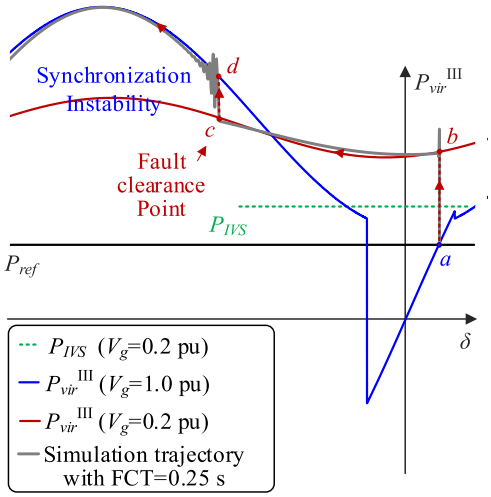

Fig. 16. Power-angle PvirIII–δ curves of virtual power way III [39] with d-axis priority current limiter.

where $P_{\text{vireq}}{}^{\text{II}}$ represents the equivalent virtual power as the feedback, and can be approximately derived as follows:

$$P_{\text{vireq}}^{\text{II}} = \frac{3}{2}\left[k\left(a_{\text{II}}\cos\delta + b_{\text{II}}\sin\delta + c_{\text{II}}\right) - (k-1)\, I_{\max} V_g \cos\delta\right]. \tag{25}$$

Apparently, coefficient k provides an additional control freedom to adjust the $P_{\text{vireq}}{}^{\text{II}}$-$\delta$ curves then may help the GFM inverter improve transient synchronization stability and exit current limitation mode. However, the quantitative design of k relies on additional information such as the grid voltage and grid impedance. Improper design also leads to transient instability.

3) Virtual Power III Way in [39], [40]: When $\left\|i_{\text{ref}\,dq}\right\| \geq I_{\max}$, the virtual power $P_{\text{vir}}{}^{\text{III}}$ under virtual power III way with d-axis priority current limiter is derived as follows:

$$P_{\text{vir}}^{\text{III}} = \frac{3}{2} V_{\text{ref}}\left[I_{nd} + k_{Vp}\left(V_{\text{ref}} - V_g\cos\delta\right)\right. . \tag{26}$$

Detailed derivations can be seen in Appendix D. Fig. 16 shows the power-angle $P_{\text{vir}}{}^{\text{III}}$–$\delta$ curves under different operation modes. The corresponding parameters are consistent with those in the HIL tests. As depicted in Fig. 16, $P_{\text{vir}}{}^{\text{III}}$ in CLM is larger than P_{ref}. During fault, the motion trajectory of δ is similar with that under the proposed P_{IVS}-feedback method shown in Fig. 13. However, under the same fault conditions, $P_{\text{vir}}{}^{\text{III}}$ is also great larger than P_{IVS}, which can lead to a greater angle excursion of δ, such that δ may overshoot the point of exiting current limitation mode. Besides, $P_{\text{vir}}{}^{\text{III}}$ – δ curves in current limitation mode sustains a larger accelerating area after fault clearing, causing δ to continue to move toward the negative direction and making loss of synchronism more likely. Therefore, in terms of the transient synchronization stability of the GFM with d-axis priority current limiter, virtual power way III in [39] exhibits weaker than the proposed method.

Literature [40] also adopts virtual power way III. Different from [39], the virtual current is not the unsaturated current reference i_{ref}, instead, the virtual current is calculated through a predesigned virtual impedance $Z_x\angle\theta_x$ between internal voltage $\boldsymbol{v}_{\mathbf{IVS}}$ and actual output voltage $\boldsymbol{v}_{\mathbf{pcc}}$. It is worth noting that this virtual impedance Z_x is not applied in the voltage control loop, it is only applied in virtual current calculation. The virtual current $\boldsymbol{i}_{\mathbf{vir}}$ is calculated as follows:

$$\boldsymbol{i}_{\text{vir}} = \frac{\boldsymbol{v}_{\text{IVS}} - \boldsymbol{v}_{\text{pcc}}}{Z_x\angle\theta_x}. \tag{27}$$

Thus, when $\left\|i_{\text{ref}\,dq}\right\| \geq I_{\max}$, the virtual power $P_{\text{vireq}}{}^{\text{III}}$ with d-axis priority current limiter in [40] can be derived as follows:

$$P_{\text{vireq}}^{\text{III}} = \frac{3}{2} V_{\text{ref}}\left[V_g\sin\delta\sin\theta_x + \left(V_{\text{ref}} - V_g\cos\delta - X_g I_{\max}\right)\cos\theta_x\right]. \tag{28}$$

Similar with method in study [38], the predesigned $Z_x\angle\theta_x$ also provides two additional control freedom Z_x and θ_x to reshape the $P_{\text{vireq}}{}^{\text{III}}$–$\delta$ curves, then make it possible to help the inverter improve transient synchronization stability and exit current limitation mode. However, the proper design for Z_x and θ_x also relies on additional grid information, causing complexity in parameters design.

D. Different Virtual Power Feedback Methods With Circular Current Limiter

1) Proposed Method: Although $\boldsymbol{i}_{\boldsymbol{g}}$ and $\boldsymbol{v}_{\mathbf{pcc}}$ are different from those with d-axis priority current limiter, the P_{IVS} – δ curves remains the same under the universal P_{IVS}-feedback method (16). Thus, the proposed method can enhance the transient synchronization stability of GFM inverter with circular current limiter.

2) Virtual Power Way II in [37], [38]: The actual output power with circular current limiter $P_e{}^{\text{CCL}}$ can be expressed as follows [22]:

$$P_e^{\text{CCL}} = \frac{3}{2}\left[\frac{R_e\left(V_{\text{ref}}^2 - V_{\text{ref}}V_g\cos\delta\right) + X_g V_{\text{ref}} V_g\sin\delta}{R_e^2 + X_g^2} - R_e I_{\max}^2\right] \tag{29}$$

where R_e represents the equivalent virtual resistance of circular current limiter, which can be expressed as follows:

$$R_e = \max\left\{0, \operatorname{Re}\left(\sqrt{\frac{V_{\text{ref}}^2 - 2V_{\text{ref}}V_g\cos\delta + V_g^2}{I_{\max}^2} - X_g^2}\right)\right\} \tag{30}$$

Thus, the virtual power $P_{\text{vir}}{}^{\text{II}}$ with circular current limiter in [37] can be derived as follows:

$$P_{\text{vir}}^{\text{II}} = \frac{1}{\rho} P_e^{\text{CCL}} \tag{31}$$

where

$$\frac{1}{\rho} = \max \left\{1, k_{Vp}\sqrt{\frac{\left(V_{\text{ref}} + \frac{I_{nd}}{k_{Vp}} - V_g\cos\delta\right)^2 + \left(\frac{I_{nq}}{k_{Vp}} V_g\sin\delta\right)^2}{I_{\max}^2} - X_g^2}\right\}. \tag{32}$$

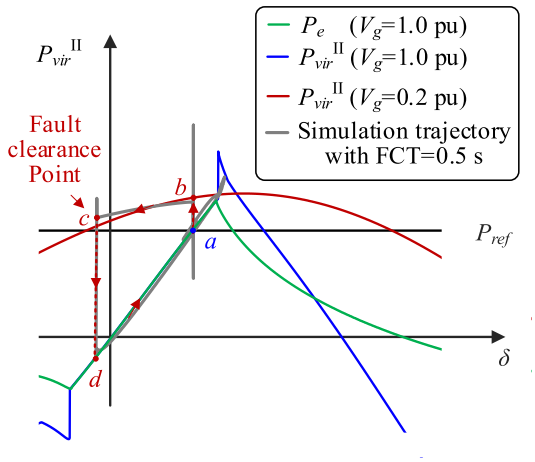

Fig. 17. Power-angle PvirII-δ curves of virtual power way II [37] with circular current limiter.

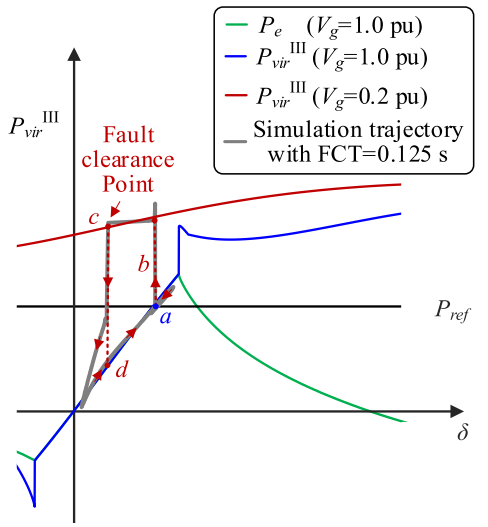

Fig. 18. Power-angle PvirIII-δ curves of virtual power way III [39] with circular priority current limiter.

Detailed derivations can be seen in Appendix D. Fig. 17 shows the power-angle $P_{\rm vir}^{\rm II}$–δ curves with circular current limiter. During fault, $P_{\rm vir}^{\rm II}$ is also larger than $P_{\rm ref}$, δ moves towards the negative direction with the operating point following the trajectory: $a \rightarrow b \rightarrow c$. After fault clearance, $P_{\rm vir}^{\rm II}$–δ enlarges the power-angle curves compared with P_e–δ curve, and thus, the transient synchronization stability of GFM inverter with circular current limiter can be enhanced.

As for method in [38], the equivalent virtual power $P_{\rm vireq}^{\rm II}$ with circular current limiter can be expressed as follows:

$$P_{\rm vireq}^{\rm II} = \left(\frac{k-\rho\,(k-1)}{\rho}\right) P_e^{\rm CCL} \tag{33}$$

when $k \geq 1$, the method in [38] also can enhance the transient synchronization stability of GFM inverter with circular current limiter.

3) Virtual Power Way III in [39], [40]: The virtual power $P_{\rm vir}^{\rm III}$ with circular current limiter in [39] can be derived as follows:

$$P_{\rm vir}^{\rm III} = \frac{1}{\rho}\left(P_e^{\rm CCL} + R_e I_{\rm max}^2\right). \tag{34}$$

Detailed derivations can be seen in Appendix D. Fig. 18 shows the power-angle $P_{vir}^{\rm III}$–δ curves with circular current limiter. The trajectory of δ is similar with that under the virtual power way II as $P_{\rm vir}^{\rm III}$ is larger than $P_{\rm ref}$ during fault. However, it has a much larger acceleration area and leads to a greater angle excursion of δ. It means that under the same fault clearance time, the system may stabilize at the previous period of the stable equilibrium point a, compared with the proposed method and the method in [37].

Similar with method in [38], method in [40] can adjust the predesigned virtual impedance $Z_x\angle\theta_x$ to enhance the transient synchronization stability of GFM inverter with circular current limiter. Notably, there is no explicit relationship between the calculated virtual current $\boldsymbol{i}_{\rm vir}$ and the output current $\boldsymbol{i}_g$ under the circular current limiter, hereby granting greater degrees of freedom in control design. Nevertheless, proper parameter design for Z_x and θ_x remains a complex task in practical engineering applications.

E. Simulation Demonstration and Discussion

To further provide a more intuitive demonstration and validate the effectiveness of the theoretical analysis on the applicability of the three virtual power methods, simulation results under d-axis priority limiting and circular limiting are presented in Figs. 19 and 20.

When d-axis priority current limiter is employed with FCT = 0.25 s, Fig. 19 shows that under traditional GFM method (actual output power feedback), the inverter stabilizes at the stable equilibrium point $\delta_s^{\rm CLM}$ in the current limitation mode. Only the proposed $P_{\rm IVS}$-feedback method can realize the successful fault recovery, while the GFM inverter under virtual power way II [37] and virtual power way III [39] lose synchronization. The trajectories of δ under different virtual power methods are consistent with the theoretical analysis in Section V-C.

When circular current limiter is employed with FCT = 0.25 s, Fig. 20 shows that the traditional GFM loses synchronization stability after fault clearance. All the virtual power methods can maintain synchronization, which shows the effectiveness on transient synchronization stability enhancement. It is also noting that the GFM inverter under the proposed method and virtual power way II [37] can recover to the previous stable equilibrium point $\delta_s^{\rm NOM}$ while the GFM inverter under the virtual power way III [39] stabilizes at the previous period of the previous stable equilibrium point ($\delta_s^{\rm NOM}$-2π). The trajectories of δ under different virtual power methods are consistent with the theoretical analysis in Section V-D.

Comparative studies are further summarized in Table I. All the virtual power feedback methods can be applied with circular current limiter but only the methods in [38], [40] and the proposed method can improve the performance of the GFM inverter with d-axis priority current limiter. On one hand, methods in [38]

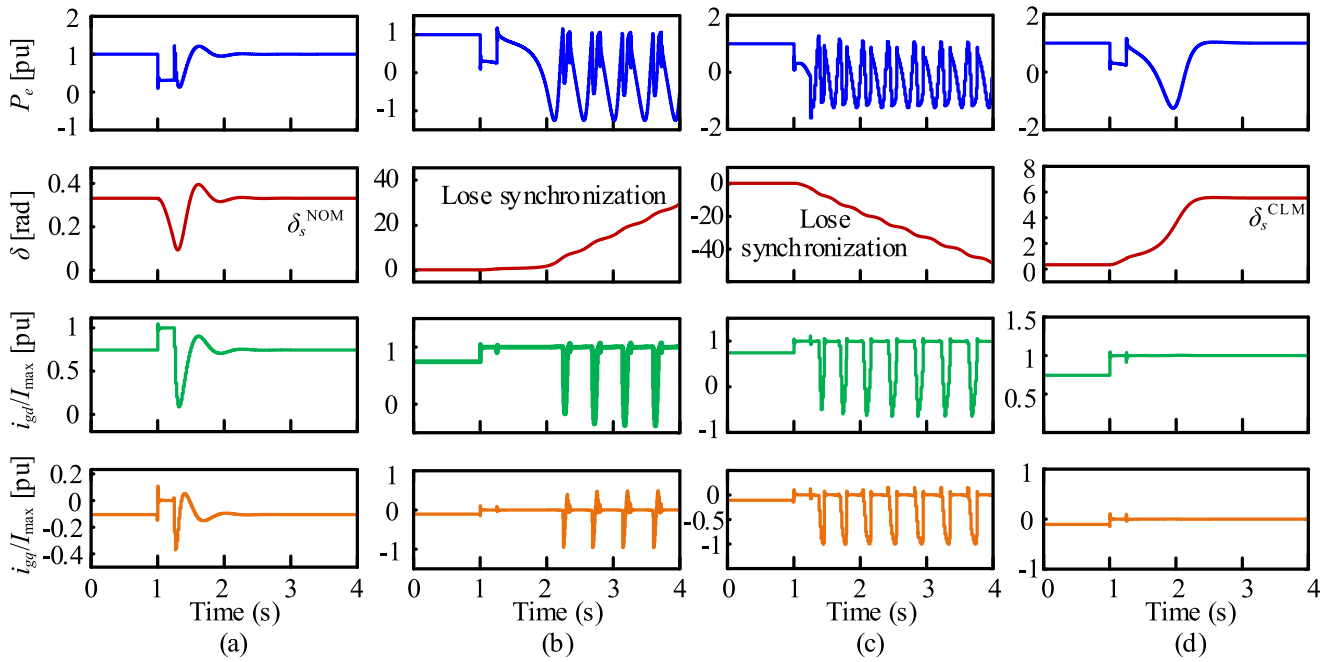

Fig. 19. Comparative simulation results for the GFM inverter with d-axis priority current limiter with FCT = 0.25 s. (a) Proposed method. (b) Virtual power way II [37]. (c) Virtual power way III [39]. (d) Traditional GFM method.

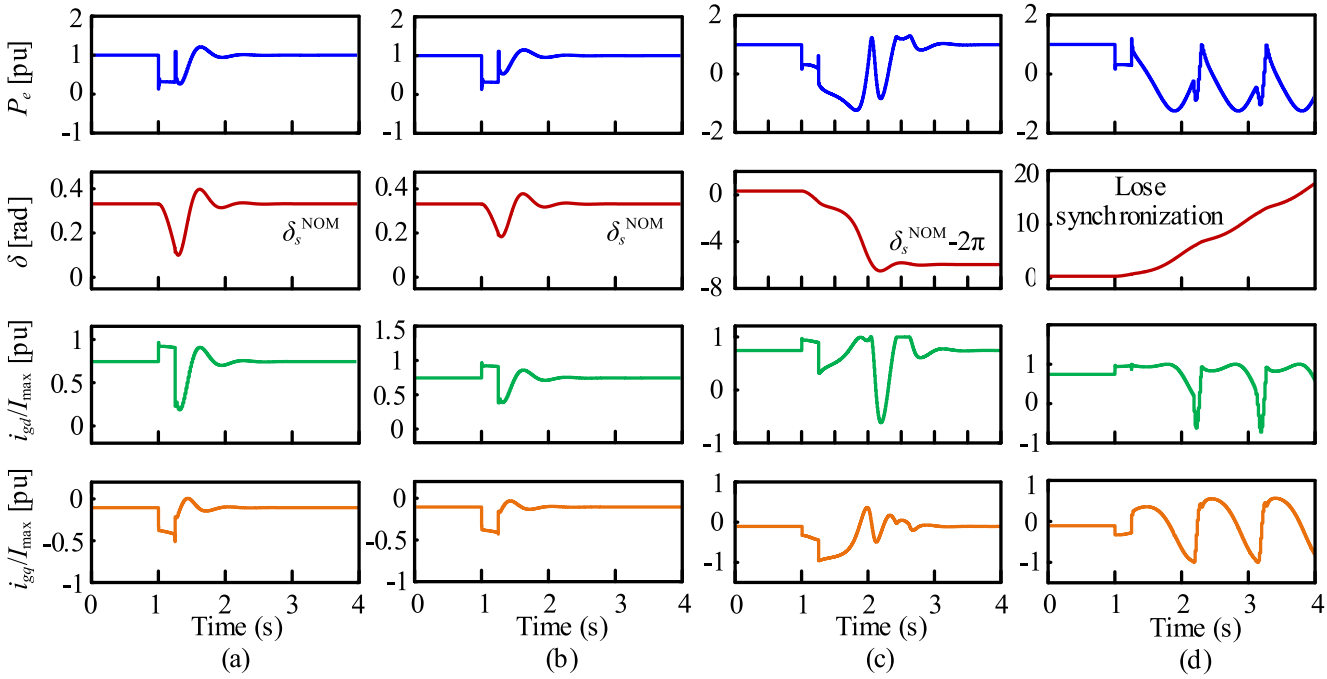

Fig. 20. Comparative simulation results for the GFM inverter with circular current limiter with FCT = 0.25 s. (a) Proposed method. (b) Virtual power way II [37]. (c) Virtual power way III [39]. (d) Traditional GFM method.

and [40] introduce additional control freedom degrees to provide more control flexibility. On the other hand, more information on parameter design is required. Different from all the virtual power methods, the proposed method uses the internal voltage (virtual voltage) and output current (actual current) to obtain the internal power P_{IVS}. According to (16), the virtual power angle characteristics of the proposed universal virtual power P_{IVS}-feedback method remain unaffected by the types of current limiters and external grid faults.

The proposed method can provide a simple way for ensuring successful fault recovery and enhancing transient synchronization stability for the GFM inverter with the *d*-axis priority current

TABLE I
COMPARISONS AMONG OTHER VIRTUAL POWER FEEDBACK METHODS [37], [38], [39], [40]

Categories	Obtained way for virtual power	Applicability in d-axis priority current limiter	Applicability in circular current limiter
Proposed method	Voltage reference (**virtual voltage**) and output current (**actual current**)	✓Successful fault recovery in exiting current limitation and transient stability enhancement	✓Transient stability enhancement
Virtual power way II [37]	Output voltage (**actual voltage**) and unsaturated current reference (**virtual current**)	× Failure to guarantee the exit from current limitation, and degradation of transient stability	✓Transient stability enhancement
Virtual power way II [38]	Output voltage (**actual voltage**) and unsaturated/saturated current reference (**virtual current**)	Possibility of guaranteeing the exit from current limitation and enhancing transient stability depends on the proper design of parameter k	Possibility of enhancing transient stability depends on the proper design of parameter k
Virtual power way III [39]	Voltage reference (**virtual voltage**) and unsaturated current reference (**virtual current**)	× Possibility of exiting current limitation mode, but with degradation in transient stability	✓Transient stability enhancement
Virtual power way III [40]	Voltage reference (**virtual voltage**) and calculated current reference by predesigned virtual impedance (**virtual current**)	Possibility of guaranteeing the exit from current limitation and enhancing transient stability depends on the proper design of virtual impedance $Z_x\angle\theta_x$ for virtual current calculation	Possibility of enhancing transient stability depends on the proper design of virtual impedance $Z_x\angle\theta_x$ for virtual current calculation

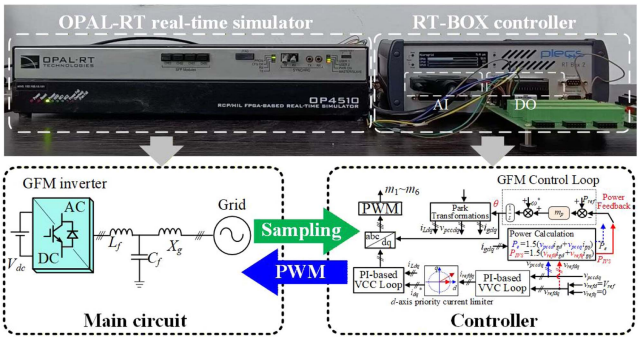

Fig. 21. Configuration of the HIL system.

TABLE II
PARAMETERS OF THE HIL SYSTEM

Parameters	Value	Parameters	Value
DC voltage V_{dc}	600 V	Rated active power P_{ref}	50 kW
Grid voltage V_g	311 V	Rated voltage V_{ref}	320 V
Grid frequency f_g	50 Hz	P-ω droop coefficient m_p	8e-5 (rad/s)/W
Rated frequency f^*	50 Hz	Nominal current I_n	107 A
Line impedance X_g	1 Ω	Maximum current $I_{\max}$	140 A
L_f of LC filter	1.2 mH	Proportional coefficient k_{Vp}	0.5 A/V
C_f of LC filter	50 μF	Integral coefficient k_{Vi}	50 A/(V·s)

limiter and circular current limiter. Comparative HIL results verify this in Section VI.

VI. EXPERIMENTAL VERIFICATIONS

Both HIL tests and experimental tests are carried out to verify the effectiveness of the above analysis. In Section VI-A–F, the test cases are based on the HIL platform shown in Fig. 21. Experiment test based on RTU-BOX and RTI-INV8020IR inverter are in Section VI-G.

The main circuit is emulated in OPAL-RT4510, and the controller is implemented in RT-BOX. The sampling frequency and switching frequency are 10 kHz. The value of the output current is restricted to 140 A by current limiter. The experimental parameters are listed in Table II.

A. Comparisons Among Existing Methods

Comparison results among the proposed P_{IVS}-feedback method, traditional GFM method, and virtual power feedback methods in studies [37], [38], and [39] are presented in Fig. 22. The traditional GFM method employs power synchronization control [4]. In this case, the three phase grid voltage amplitude drops to 0.2 p.u., and persists for 0.625 s.

After fault clearance, it can be seen in Fig. 22(a) that the inverter under the proposed P_{IVS}-feedback method initially undergoes a transient process, then successfully exits from current limitation and resynchronizes with the grid. In contrast, although the inverter under traditional method can resynchronize with the grid after fault clearance, the inverter remains clamped in the current limitation mode, as is depicted in Fig. 22(b). Furthermore, the results under the virtual power II way [37] are shown in Fig. 22(c). The results under virtual power II way [38] with $k = 1.5$ are shown in Fig. 22(d). The results under virtual power way III [39] are shown in Fig. 22(e).

Under these methods, the inverter fails to exit the current limitation mode and eventually loses synchronization after the fault is cleared, demonstrating that such methods [37] and [39] are not suitable for GFM inverters with the d-axis priority current limiter. As for the method in study [38], the improper parameter k also causes synchronization instability.

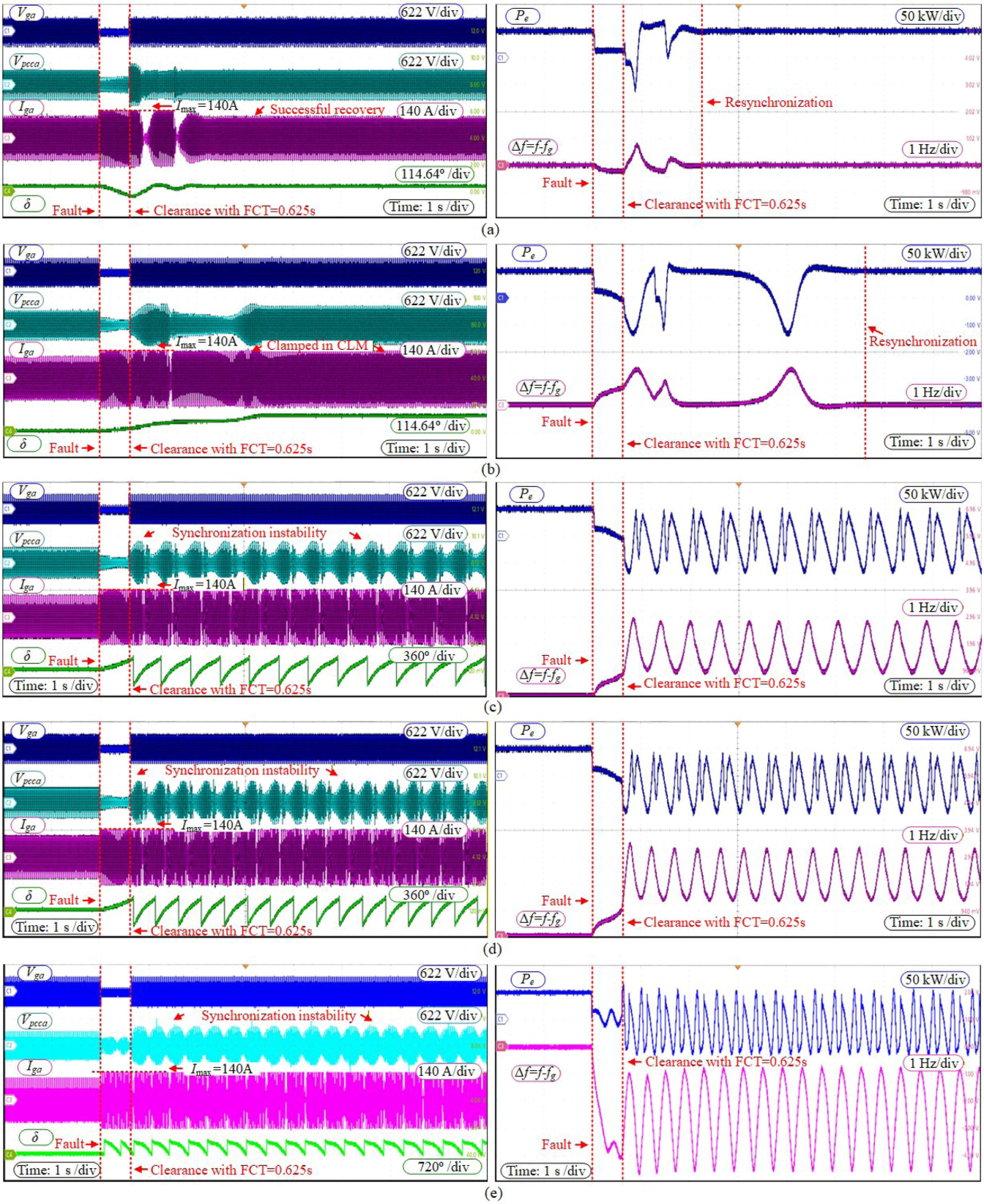

Fig. 22. HIL experimental results with FCT = 0.625 s. (a) Under P_{IVS}-feedback GFM control. (b) Under traditional GFM control. (c) Under virtual power way II [37]. (d) Under virtual power way II [38]. (e) Under virtual power way III [39].

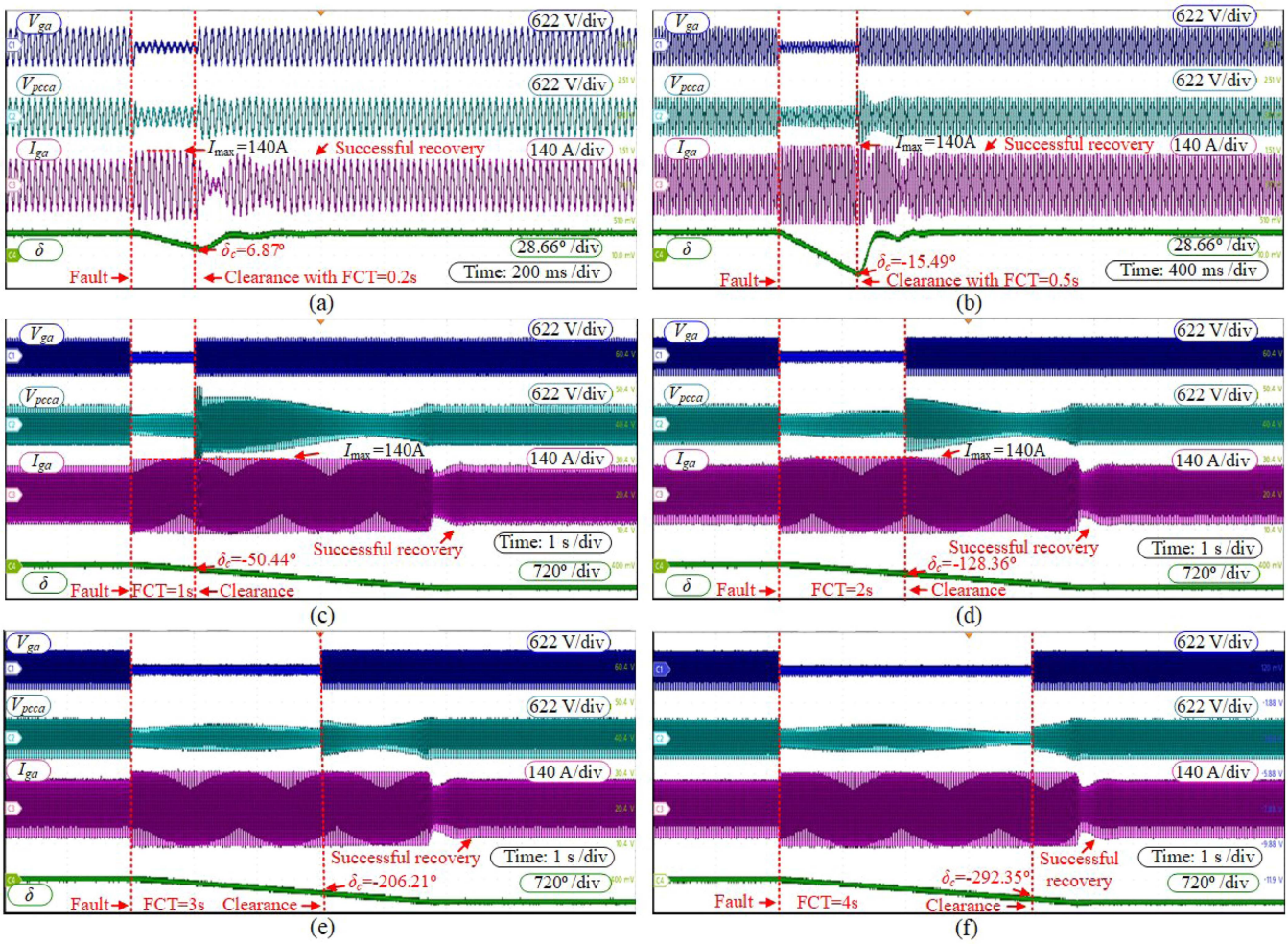

Fig. 23. HIL experimental results with different FCT. (a) $FCT_1 = 0.2$ s. (b) $FCT_2 = 0.5$ s. (c) $FCT_3 = 1$ s. (d) $FCT_4 = 2$ s. (e) $FCT_5 = 3$ s. (f) $FCT_6 = 4$ s.

B. Fault Clearance With Different FCT

According to (11), the angle boundary between CLM S1 and CLM S2 can be calculated: $\delta_{b1} = 38.49^0$, $\delta_{b2} = -38.49^0$. Fig. 23 shows the experiment results with different fault clearing time (FCT).

When $FCT_1 = 0.2$ s and $FCT_2 = 0.5$ s, $\delta_{c1} = 6.87^0 \in (0, \delta_{b1})$ and $\delta_{c2} = -15.49^0 \in (\delta_{b2}, 0)$. After fault clearance, the GFM inverter undergoes a resynchronization process, then finally exits current limitation mode and recovers to normal operation mode. The power angle can recover to the initial steady-state equilibrium. These two cases in Fig. 23(a) and (b) correspond to the analysis in Section IV-B and C.

When $FCT_3 = 1$ s, $FCT_4 = 2$ s, $FCT_5 = 3$ s, and $FCT_6 = 4$ s, $\delta_{c3} = -50.44^0 \in (-90^0, \delta_{b2})$, $\delta_{c4} = -128.36^0 \in (-180^0, -90^0)$, $\delta_{c5} = -206.21^0 \in (-270^0, -180^0)$, and $\delta_{c6} = -292.35^0 \in (\delta_{b1} - 360^0, -270^0)$. After fault clearance, the inverter first remains in CLM S2. It takes longer time for δ to decrease and enter the interval $(-360^0, \delta_{b1}\text{-}360^0)$. Thus, the GFM inverter can finally exit CLM and be stable at the steady-state equilibrium point of the next power angle period. These four cases in Fig. 23(c)–(f) correspond to Section IV-D and Appendix C.

The above experiments are consistent with the postfault behavior analysis. The P_{IVS}-feedback GFM inverter with the DPCL can always exit the current limitation mode and resynchronize with the grid after fault clearance.

C. Comparisons With Frequency Freezing Method

Comparisons between the proposed P_{IVS}-feedback GFM control and frequency freezing method in study [45] are carried out. In this test, grid faults are characterized by grid frequency drop and grid voltage phase jump.

The control structure of the frequency freezing method is depicted in Fig. 24. When $\left\|I_{\mathrm{ref}\,dq}\right\| < I_{\max}$, EN = 0. When $\left\|I_{\mathrm{ref}\,dq}\right\| > I_{\max}$, EN = 1, thus the active power-frequency synchronization loop is frozen.

1) *0.5 Hz Grid frequency drop:* The grid frequency drops to 49.5 Hz and persists for 1 s. Fig. 25 shows the EN signal curve of the frequency freezing method. Fig. 26(a) and (b) shows the results under the proposed method and the frequency freezing method.

When the drop of the grid frequency occurs, the GFM inverter shall participate in frequency regulation and output more active

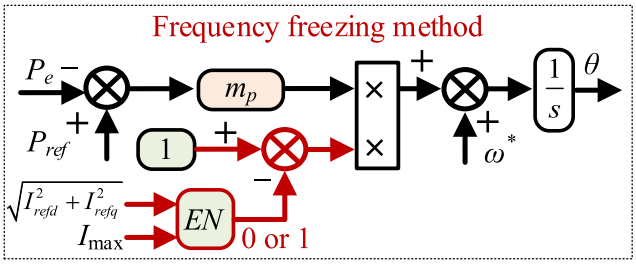

Fig. 24. Control structure of the frequency freezing method for GFM inverter.

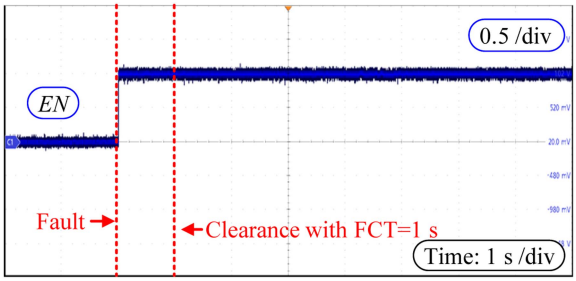

Fig. 25. Curve of EN signal of the frequency freezing method under 0.5 Hz grid frequency drop.

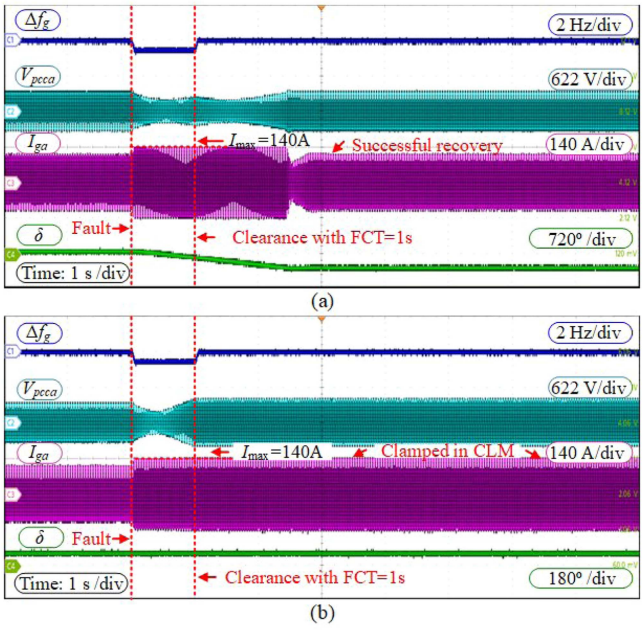

Fig. 26. HIL experimental results under 0.5 Hz grid frequency drop. (a) Under proposed method. (b) Under frequency freezing method.

power according to the droop coefficient m_p. However, when severe grid frequency drop occurs, the GFM inverter also faces the risk of overcurrent. When the magnitude of the output current increases and reaches the maximum, the current limiter is triggered, and the GFM inverter works in current limitation mode. Fig. 26(a) shows that the GFM inverter under the proposed method can exit from current limitation after the grid frequency disturbance is cleared. However, the GFM inverter under the frequency freezing method fails to exit the current limitation

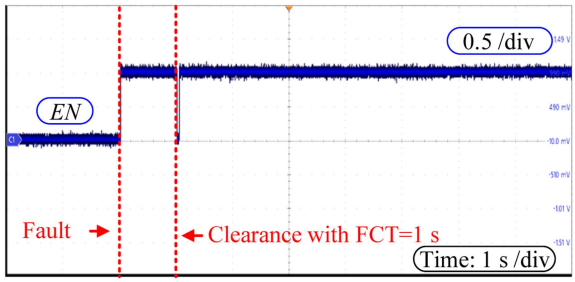

Fig. 27. Curve of EN signal of the frequency freezing method under 50° grid voltage phase jump.

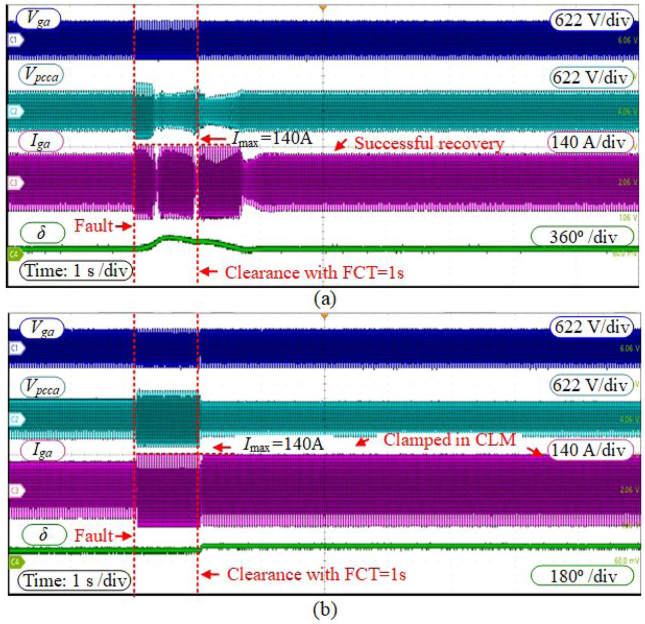

Fig. 28. HIL experimental results under 50° grid voltage phase jump. (a) Under proposed method. (b) Under frequency freezing method.

mode, which is shown in Fig. 26(b). The EN signal in Fig. 25 is also clamped to be high level.

2) *50° Grid voltage phase jump:* The 50° grid voltage phase jump occurs as the fault and persists for 1 s. Fig. 27 shows the EN signal curve of the frequency freezing method. Fig. 28(a) and (b) shows the results under the proposed method and the frequency freezing method.

When the voltage phase jump occurs, the magnitude of the output current increases and reaches the maximum. The current limiter is triggered and the GFM inverter works in current limitation mode. Fig. 28(a) shows that the GFM inverter under the proposed method can exit from current limitation after the grid phase disturbance is cleared. However, the GFM inverter under the frequency freezing method fails to exit the current limitation mode, which is shown in Fig. 28(b). The EN signal in Fig. 27 is also clamped to be high level.

The comparison results indicate that, when d-axis priority current limiter is triggered by grid faults, like frequency drops and voltage phase jumps, the proposed P_{IVS}-feedback method demonstrates significant advantages in exiting from current limitation and maintaining synchronization stability.

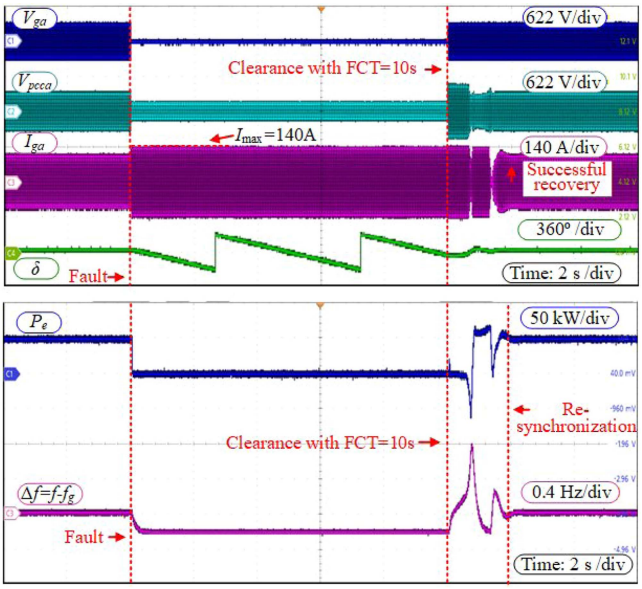

Fig. 29. HIL experimental results with FCT = 10s under 100% grid voltage sag.

D. Under 100% Voltage Sag

In this case, 100% voltage sag symmetrical fault occurs and persists for 10 s. Fig. 29 shows the HIL results. During fault, the output active power P_e reduce to zero. The d-axis priority current limiter is triggered to limit the amplitude of the current to the maximum. δ decreases under the proposed method. After fault clearance, the GFM inverter with d-axis priority current limiter can finally exit the current limitation mode and resynchronize with the grid. The virtual power angle δ is finally stable at δ_e-720°, where δ_e is the initial equilibrium angle before the fault. This test under 100% grid voltage sag is still consistent with the postfault behavior analysis.

E. Under the Asymmetrical Grid Fault

As the asymmetrical fault is more frequent [46], [47], a single line-to-ground (SLG) fault is considered in this case. A negative sequence control loop is added to control the negative sequence current to zero while the previous control loop remains unchanged as the positive sequence loop. In this case, a SLG-fault occurs in phase A. Fig. 30 shows the control structure of the sequence-based inner loop considering the asymmetrical fault.

Fig. 31(a) displays the waveforms of the three-phase grid voltage, where the grid voltage amplitude (V_{ga}) of phase A drops to 0 p.u. and this fault persists for 1 s. Fig. 31(b) shows the waveforms of the three-phase output current. By controlling the negative sequence current to zero, the output current of the three-phase becomes symmetrical, and the amplitude is limited within $I_{\max}$ during the fault. Fig. 31(c) shows the waveforms of the output active power P_e, the frequency difference Δf and the virtual power angle δ. After the asymmetrical fault is cleared, Fig. 31(b) and Fig. 31(c) demonstrate that under the proposed P_{IVS}-feedback method, the GFM inverter with d-axis priority current limiter can still exit the current limitation mode and recover to normal GFM operation.

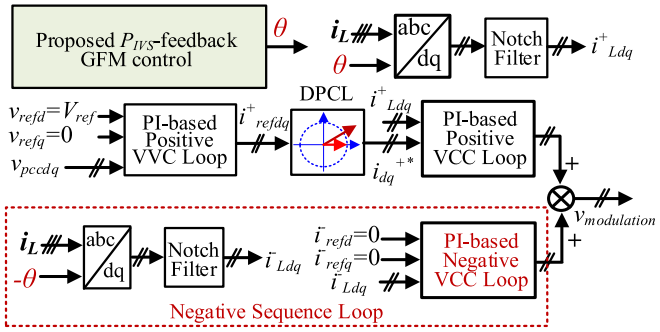

Fig. 30. Control structure of the sequence-based inner loop considering the asymmetrical fault.

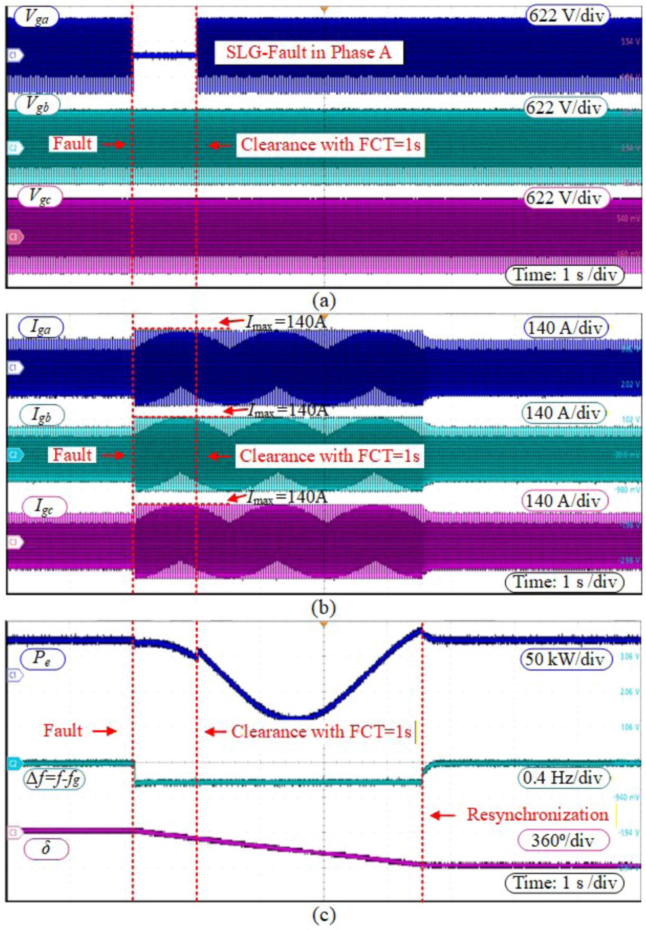

Fig. 31. HIL experimental results with FCT = 1s under SLG-Fault in phase A. (a) Voltage waveforms of grid voltage. (b) Output current waveforms of the GFM inverter. (c) Waveforms of the output active power, frequency difference and virtual power angle.

F. Influence of Reactive Power-Voltage Control Loop

In this case, the influence of reactive power-voltage control loop (12) is investigated. According to (15), the reactive power -voltage coefficient n_Q is selected as $n_Q = 0.002$ V/Var. The grid voltage drops to 0.2 p.u. and lasts for 0.625 s. Fig. 32 shows the

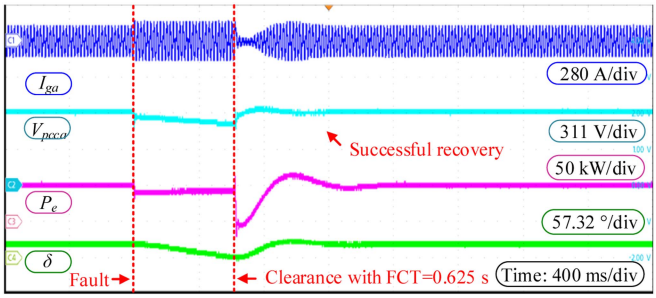

Fig. 32. HIL results with d-axis current limiter and reactive power-voltage loop.

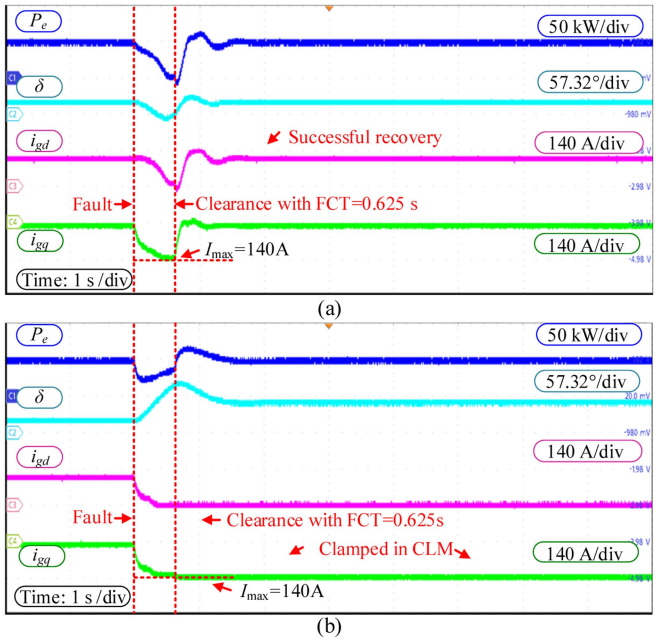

Fig. 33. HIL results with q-axis priority current limiter: (a) under the proposed universal method; (b) under the traditional GFM method.

HIL test results. When the fault occurs, the voltage amplitude V_{ga} decreases due to reactive power-voltage control loop. It also can be seen that δ decreases. This occurs because P_{IVS} is still larger than P_{ref}, which is consistent to the previous analysis in Section III-C. After fault clearance, the GFM inverter can also successfully exit the current limitation mode and recover to normal GFM operation.

G. Application With Other Current Limiters

To evaluate the feasibility of the proposed method with other current limiters, the performance of the universal P_{IVS}-feedback control method with q-axis priority current limiter and circular current limiter is tested in this case. The grid voltage also drops to 0.2 p.u. and persists for 0.625 s. The control parameters are the same as that in the previous cases.

1) *q-axis priority current limiter:* Fig. 33 shows comparative HIL test results with q-axis priority current limiter. The q-axis priority current limiter in the d–q frame is expressed as follows [24]:

$$\begin{cases} i_q^* = \frac{i_{\mathrm{ref}q}}{|i_{\mathrm{ref}q}|} \cdot \min\left(|i_{\mathrm{ref}q}|, I_{\max}\right) \\ i_d^* = \frac{i_{\mathrm{ref}d}}{|i_{\mathrm{ref}d}|} \cdot \min\left(|i_{\mathrm{ref}d}|, \sqrt{I_{\max}^2 - \left(i_q^*\right)^2}\right) \end{cases}. \tag{35}$$

Similar as d-axis priority current limiter, q-axis priority current limiter also causes the fault recovery issue.

In Fig. 33(b), the GFM inverter with q-axis priority current limiter under the traditional GFM method is clamped in current limitation mode, with its output fully allocated to the q-axis current component. Fig. 33(a) shows that the GFM inverter under the proposed method can successfully exit the current limitation mode and recover the normal GFM operation.

2) *Circular current limiter:* Fig. 34 shows comparative HIL test results with circular current limiter. The circular current limiter in the d–q frame is expressed as follows [22]:

$$\begin{cases} i_d^* = \frac{i_{\max}}{\|i_{\mathrm{ref}dq}\|} \cdot i_{\mathrm{ref}d} \\ i_q^* = \frac{i_{\max}}{\|i_{\mathrm{ref}dq}\|} \cdot i_{\mathrm{ref}q} \end{cases} \tag{36}$$

As circular current limiter degrades the transient synchronization stability, the GFM inverter under the circular limiter loses the synchronization stability after fault clearance, which is shown in Fig. 34(b). Fig. 34(a) shows that the GFM inverter under the proposed method can remain synchronized after fault clearance. The GFM inverter first operates in current limitation mode, δ continues to decrease due to P_{IVS} feedback. After fault clearance, the GFM inverter gradually exits the current limitation mode, and δ finally stabilizes at the stable equilibrium point of previous period.

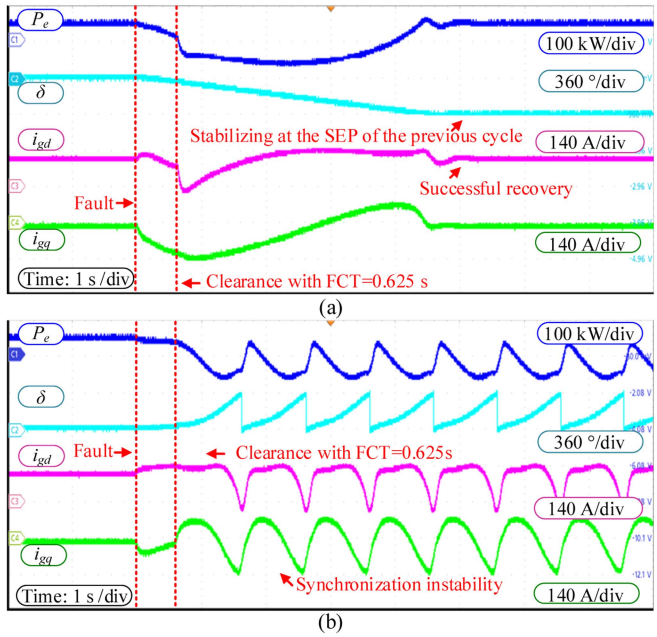

Fig. 34. HIL results with circular current limiter: (a) under the proposed universal method; (b) under the traditional GFM method.

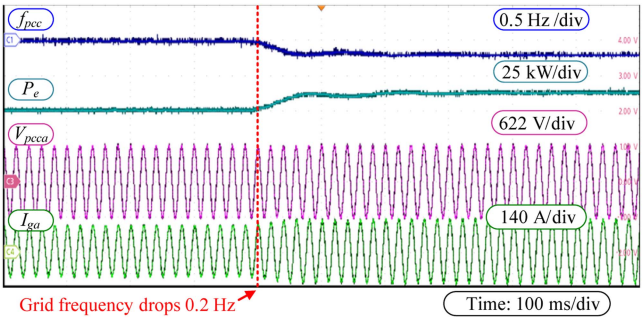

Fig. 35. HIL results for primary frequency regulation ability verification.

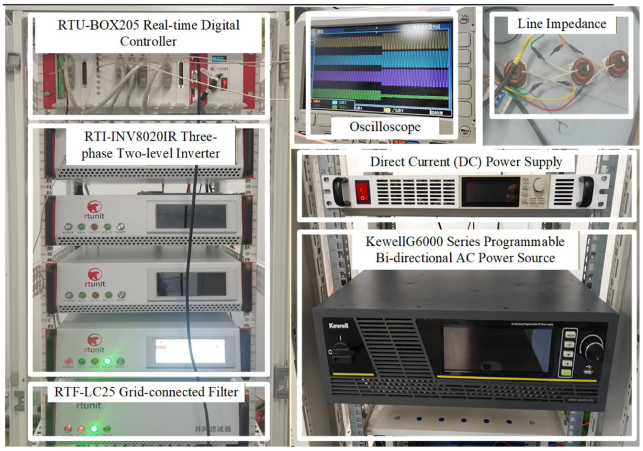

Fig. 36. Configuration of the experimental setup based on RTU-BOX 205 platform.

H. Verification for Primary Frequency Regulation Ability

In this case, the grid frequency drops 0.2 Hz and the GFM inverter can operate in normal mode, where the current limiter is not triggered. Fig. 35 shows that during normal operation, the proposed method also can participate in the primary frequency regulation according to the droop coefficient m_p. The proposed P_{IVS}-feedback method is identical to power synchronization control in normal operation mode.

I. Experimental Verification

Experiments are carried out to verify the feasibility of the proposed method. The experimental setup is shown in Fig. 36, which is based on the RTU-BOX 205 with RTI-INV8020IR three phase two-level inverter. The DSP-based RTU-BOX 205 controller compiles programs and runs as the controller with a 10 kHz inverter switching frequency. Corresponding parameters are listed in Table III.

In this case, the three phase grid voltage amplitude drops to 0.25 p.u. and persists for 2 s. Fig. 37 shows the experiment results under the proposed method and the traditional GFM method.

After fault clearance, it can be seen in Fig. 37(a) that the inverter under the traditional GFM control fails to exit the current limitation mode. On the contrary, Fig. 37(b) shows that the inverter under the proposed P_{IVS}-feedback method successfully exits from current limitation and resynchronizes with the grid,

TABLE III
PARAMETERS OF THE EXPERIMENTAL TEST

Parameters	Value	Parameters	Value
DC voltage V_{dc}	300 V	Rated active power P_{ref}	600 W
Grid voltage V_g	110 V	P-ω droop coefficient m_p	0.001 (rad/s)/W
Rated voltage V_{ref}	115 V	Nominal current I_n	3.6 A
Grid frequency f_g	50 Hz	Maximum current $I_{\max}$	5 A
Rated frequency f^*	50 Hz	Proportional coefficient k_{Vp}	0.2 A/V
Line impedance X_g	0.5 Ω	Integral coefficient k_{Vi}	10 A/(V·s)
L_f of LC filter	1.5 mH	Proportional coefficient k_{Ip}	9 V/A
C_f of LC filter	22 μF	Integral coefficient k_{Ii}	2000 V/(A·s)

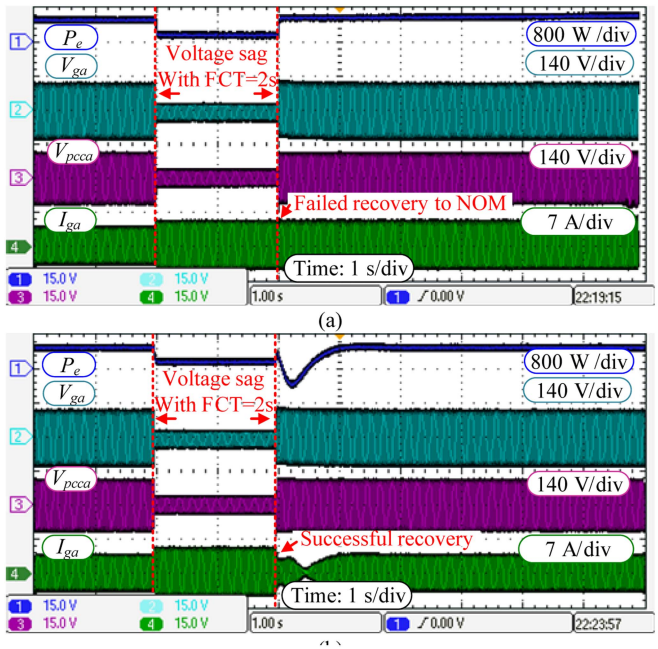

Fig. 37. Experimental results with FCT = 2 s. (a) Under traditional GFM control. (b) Under P_{IVS}-feedback GFM control.

demonstrating the priority of the proposed method in fault recovery.

VII. CONCLUSION

This article proposes a virtual power P_{IVS}-feedback control method for GFM inverters to overcome the fault recovery issues of priority current limiter. The proposed method utilizes the virtual power of the internal voltage source P_{IVS}, instead of the real output power, as the power feedback. It is revealed that under the P_{IVS}-feedback GFM control, the GFM inverter with d-axis priority current limiter can always exit the current limitation mode and restore to normal GFM mode after the fault clearance. Successful fault recovery is guaranteed, meanwhile, the advantages of traditional GFM control are maintained during normal operation. Furthermore, a universal virtual P_{IVS}-feedback method is proposed, which can be extended to both priority current limiters and the circular current limiter. Besides, a comparative study among various virtual power feedback

methods with different current limiters shows the feasibility of the proposed method and provides practical guidelines for selecting appropriate virtual power feedback methods based on different application scenarios and requirements. As a simple and practical method, the proposed method does not need any complex control process design, extra line/bus information and control structure reconfiguration, which can be easily extended for engineering applications.

Appendix A
Condition 1 for Fault Recovery With *d*-Axis Priority Current Limiter

When the *d*-axis priority current limiter is not triggered, the GFM inverter operates as a controlled voltage source, thus, the power angle condition $\{\delta \| \|i_{\text{ref}}^{\text{NOM}}(\delta)\| < I_{\max}\}$ for not triggering current limiter can be derived as follows:

$$\sqrt{\frac{V_{\text{ref}}^2 + V_g^2 - 2V_{\text{ref}}V_g\cos\delta}{X_g^2}} < I_{\max}. \tag{37}$$

When the *d*-axis priority current limiter is triggered, the GFM inverter operates as a controlled current source. The integral coefficient k_{Vi} of the voltage control loop is set as 0. Based on the assumption neglecting the capacitor current and the dynamics of the inductor and capacitor, $i_g \approx i_L = i_{\text{ref}}$. Thus, the generated current reference $i_{\text{ref}\,dq}$ is changed as follows:

$$i_{\text{ref}\,dq} \approx k_{Vp}\left(v_{\text{ref}\,dq} - v_{pccdq}\right) + I_{ndq}. \tag{38}$$

The power angle condition $\{\delta \| \|i_{\text{ref}}^{\text{CLM}}(\delta)\| < I_{\max}\}$ for exiting from the current limitation mode can be derived as follows:

$$\sqrt{\begin{array}{l}\left[I_{nd} + k_{Vp}\left(V_{\text{ref}} + -V_g\cos\delta\right)\right]^2 \\ +\left[I_{nq} + k_{Vp}\left(V_g\sin\delta - X_g I_{\max}\right)\right]^2\end{array}} < I_{\max}. \tag{39}$$

Appendix B
Equivalent Circuit of the GFM Inverter With *d*-Axis Priority Current Limiter

When the GFM inverter is equipped with *d*-axis priority current limiter, the mathematical relationship between $i_{dq}{}^*$ and $i_{\text{ref}\,dq}$ can be further derived as follows:

$$\begin{aligned} i_{dq}^* &= \bar{\alpha}\cdot i_{\text{ref}\,dq} \\ \bar{\alpha} &= \left|\min\left(1, \frac{I_{\max}}{\|i_{\text{ref}\,dq}\|}\right)\right| e^{-j\phi} \end{aligned} \tag{40}$$

where $\bar{\alpha}$ represents the mathematical expression of *d*-axis priority current limiter, which indicates the relationship between the unsaturated current reference $i_{\text{ref}\,dq}$ before the current limiter and the saturated current reference $i_{dq}{}^*$ after the current limiter. ϕ represents the phase difference between $i_{dq}{}^*$ and $i_{\text{ref}\,dq}$

$$\phi = \begin{cases} 0, \text{NOM} \\ arctan\left(\left|\frac{i_{\text{ref}\,q}}{i_{\text{ref}\,d}}\right|\right) - arctan\left(\left|\frac{\sqrt{I_{\max}^2 - (i_{\text{ref}\,d})^2}}{i_{\text{ref}\,d}}\right|\right), \text{CLM S1} \\ arctan\left(\left|\frac{i_{\text{ref}\,q}}{i_{\text{ref}\,d}}\right|\right), \text{CLM S2} \end{cases}. \tag{41}$$

In normal operation mode, $v_{\text{pcc}\,dq} = v_{\text{ref}\,dq}$, we have

$$i_{\text{ref}\,dq} = k_{Vi}\int\left(v_{\text{ref}\,dq} v_{\text{pcc}\,dq}\right) = I_{ndq}. \tag{42}$$

Considering (40), it can be derived as follows:

$$i_{gdq} = I_{\max dq} = \bar{\alpha}\cdot k_{Vp}\left(v_{\text{ref}\,dq} - v_{\text{pcc}\,dq}\right) + \bar{\alpha}\cdot I_{ndq} \tag{43}$$

where $I_{\max\,dq}$ is expressed as the output current during CLM.

The mathematical expression between $I_{\max\,dq}$ and I_{ndq} is as follows:

$$\begin{aligned} I_{ndq} &= \bar{\beta}\cdot I_{\max\,dq} \\ \bar{\beta} &= \frac{\left\|I_{ndq}\right\|}{I_{\max}} e^{-j\sigma} \end{aligned} \tag{44}$$

where $\bar{\beta}$ is the phasor to express the relationship between the nominal current I_{ndq} in normal operation mode and the output maximum current $I_{\max\,dq}$. σ represents the phase difference between the output current I_{ndq} in normal operation mode and the output maximum current $I_{\max\,dq}$ in current limitation mode

$$\sigma = \arctan\left(\left|\frac{I_{\max\,q}}{I_{\max\,d}}\right|\right) - \arctan\left(\left|\frac{I_{nq}}{I_{nd}}\right|\right) \tag{45}$$

Combining (43) and (44), we have

$$Z_{\text{eq}}\cdot i_{gdq} = \left(v_{\text{ref}\,dq} - v_{pccdq}\right) \tag{46}$$

where Z_{eq} takes up a complex value

$$Z_{\text{eq}} = \frac{\left(1\bar{\alpha}/\bar{\beta}\right)}{\bar{\alpha}\cdot k_{Vp}}. \tag{47}$$

Equations (46) and (47) show that the *d*-axis priority current limiter can be modeled as a variable virtual impedance between the internal voltage $\boldsymbol{v}_{\mathbf{IVS}} = \boldsymbol{v}_{\mathbf{ref}}$ and the terminal voltage $\boldsymbol{v}_{\mathbf{pcc}}$ of the GFM inverter. During normal operation, the *d*-axis priority current limiter will not be triggered, $i_{gdq} = I_{ndq}$. The value of Z_{eq} equals 0 and $\boldsymbol{v}_{\mathbf{IVS}} = \boldsymbol{v}_{\mathbf{pcc}}$. When *d*-axis priority current limiter is triggered, Z_{eq} adaptively changes to restrict the output current within the maximum value.

Appendix C
Phasor Diagram Analysis After Fault Clearance at Other Intervals

1) *Fault Clearance at* $-180^0 < \delta_c < -90^0$ Fig. 38 shows the phasor diagram with $-180^0 < \delta_c < -90^0$.

Step 0: $\boldsymbol{v}_{gf}$ turns to $\boldsymbol{v}^{(1)}{}_g$, then, $\boldsymbol{v}^{(0)}{}_{\mathbf{pcc}}$ turns into $\boldsymbol{v}^{(1)}{}_{\mathbf{pcc}}$. Notice that $v^{(1)}{}_{\text{pcc}\,d}$ is negative and its absolute value increases, $v^{(1)}{}_{\text{pcc}\,d} < v^{(0)}{}_{\text{pcc}\,d} < 0$. $i^{(1)}{}_{\text{ref}\,d} = k_{Vp}(v_{\text{ref}\,d} - v^{(1)}{}_{\text{pcc}\,d}) + I_{nd}$, $i^{(1)}{}_{\text{ref}\,d} > i^{(0)}{}_{\text{ref}\,d} > I_{\max}$. The inverter remains in CLM S2.

Step 1: With δ decreases, $\boldsymbol{v}^{(1)}{}_g$ turns to $\boldsymbol{v}^{(2)}{}_g$, $\boldsymbol{i}^{(0)}{}_g = \boldsymbol{i}^{(1)}{}_g = \boldsymbol{i}^{(2)}{}_g$, $\boldsymbol{v}^{(1)}{}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(2)}{}_{\mathbf{pcc}}$, $v^{(2)}{}_{\text{pcc}\,d}$ decreases and $i^{(2)}{}_{\text{ref}\,d}$ increases, $i^{(2)}{}_{\text{ref}\,d} > i^{(1)}{}_{\text{ref}\,d} > i^{(0)}{}_{\text{ref}\,d} > I_{\max}$. Thus, the inverter remains in CLM S2.

Step 2: δ decreases and enters the interval $(-270^0, -180^0)$.

2) *Fault Clearance at* $-270^0 < \delta_c < -180^0$

Fig. 39 shows the phasor diagram with $-270^0 < \delta_c < -180^0$.

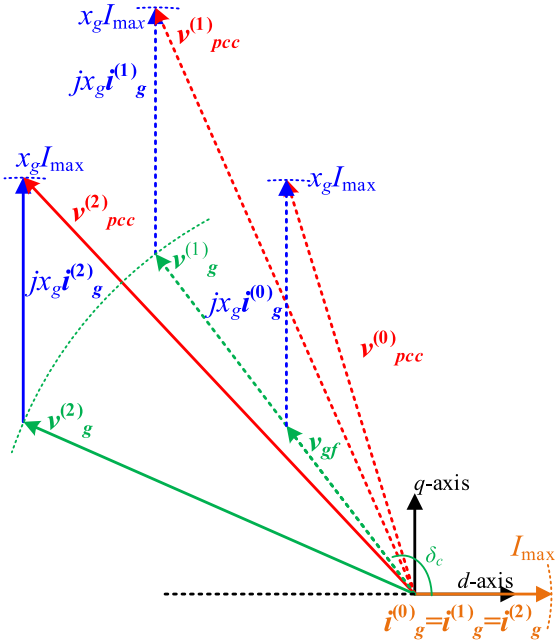

Fig. 38. Phasor diagram of GFM inverter with $-180^0 < \delta_c < -90^0$.

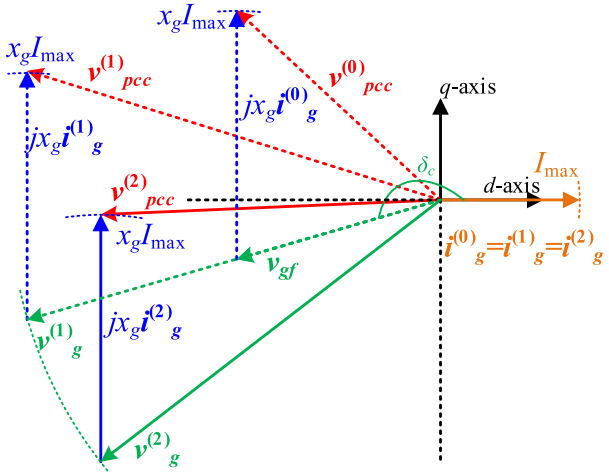

Fig. 39. Phasor diagram of GFM inverter with $-270^0 < \delta_c < -180^0$.

Step 0: $\boldsymbol{v}_{gf}$ turns into $\boldsymbol{v}^{(1)}_g$,$\boldsymbol{v}^{(0)}_{\mathbf{pcc}}$ turns into $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$, ${v^{(1)}}_{\mathrm{pcc}\,d} < {v^{(0)}}_{\mathrm{pcc}\,d} < 0$. ${i^{(1)}}_{\mathrm{ref}\,d} = k_{Vp}({v_{\mathrm{ref}\,d}}\text{-}{v^{(1)}}_{\mathrm{pcc}\,d}) + I_{nd}$, ${i^{(1)}}_{\mathrm{ref}\,d} > {i^{(0)}}_{\mathrm{ref}\,d} > I_{\max}$. The inverter remains in CLM S2.

Step 1: With δ decreases, $\boldsymbol{v}^{(1)}_g$ turns to $\boldsymbol{v}^{(2)}_g$, $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(2)}_{\mathbf{pcc}}$, ${v^{(2)}}_{\mathrm{pcc}\,d}$ decreases. Although ${i^{(2)}}_{\mathrm{ref}\,d}$ decreases, ${i^{(2)}}_{\mathrm{ref}\,d}$ is still larger than $I_{\max}$ because δ is out of ($\delta_{b2}+n\times360°$, $\delta_{b1}+n\times360°$) (n = 01,2,…). Thus, the inverter still remains in CLM S2.

Step 2: δ decreases and enters the interval (δ_{b1}-360^0, -270^0).

3) *Fault Clearance at* δ_{b1}-$360^0 < \delta_c < -270^0$

Fig. 40 shows the phasor diagram with δ_{b1}-$360^0 < \delta_c < -270^0$.

Step 0: $\boldsymbol{v}_{gf}$ turns to $\boldsymbol{v}^{(1)}_g$,$\boldsymbol{v}^{(0)}_{pcc}$ turns to $\boldsymbol{v}^{(1)}_{pcc}$. ${v^{(1)}}_{pccd}$ is positive and its value increases, ${v^{(1)}}_{\mathrm{pcc}\,d} > {v^{(0)}}_{\mathrm{pcc}\,d} > 0$. ${i^{(1)}}_{\mathrm{ref}\,d} = k_{Vp}({v_{\mathrm{ref}\,d}}\text{-}{v^{(1)}}_{\mathrm{pcc}\,d}) + I_{nd}$, ${i^{(1)}}_{\mathrm{ref}\,d} < {i^{(0)}}_{\mathrm{ref}\,d}$. Although ${i^{(1)}}_{\mathrm{ref}\,d}$

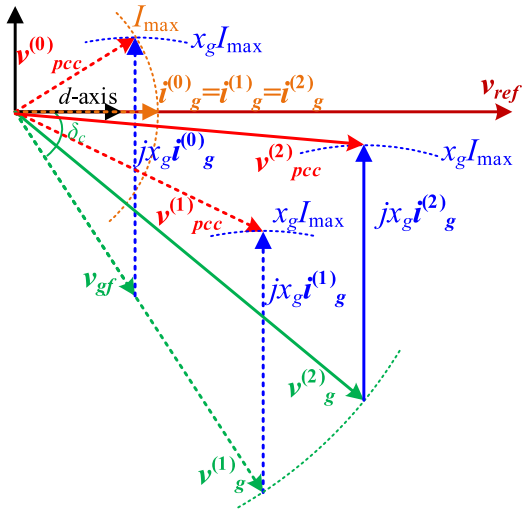

Fig. 40. Phasor diagram of GFM inverter with δ_{b1}-$360^0 < \delta_c < -270^0$.

decreases, it is still larger than $I_{\max}$ because δ_c is out of ($\delta_{b2}+n\times360°$, $\delta_{b1}+n\times360°$), where n = 01,2,…. The inverter stays in CLM S2.

Step 1: With δ decreases, $\boldsymbol{v}^{(1)}_g$ turns to $\boldsymbol{v}^{(2)}_g$ and $\boldsymbol{v}^{(1)}_{\mathbf{pcc}}$ turns to $\boldsymbol{v}^{(2)}_{\mathbf{pcc}}$, ${v^{(2)}}_{\mathrm{pcc}\,d}$ increases. ${i^{(2)}}_{\mathrm{ref}\,d} = k_{Vp}({v_{\mathrm{ref}\,d}}\text{-}{v^{(2)}}_{\mathrm{pcc}\,d}) + I_{nd} < {i^{(1)}}_{\mathrm{ref}\,d} < {i^{(0)}}_{\mathrm{ref}\,d}$. Although ${i^{(2)}}_{\mathrm{ref}\,d}$ decreases, ${i^{(2)}}_{\mathrm{ref}\,d}$ is still larger than $I_{\max}$ because δ is out of ($\delta_{b2}+n\times360°$, $\delta_{b1}+n\times360°$) (n = 01,2,…). Thus, the inverter remains in CLM S2.

Step 2: δ further decreases and enters the interval (-360^0, $\delta_{b1}-360^0$). The next process is consistent with that in Section IV-B. ${i_{\mathrm{ref}\,d}} < I_{\max}$, the operation mode comes into CLM S1. And the inverter will exit the current limitation mode and recover to normal operation mode.

APPENDIX D
DIFFERENT VIRTUAL POWER-ANGLE CHARACTERISTICS WITH DIFFERENT CURRENT LIMITERS

1) ${P_{\mathrm{vir}}}^{\mathrm{II}}$ in [37] with *d*-axis current priority current limiter

When *d*-axis priority current limiter is triggered and the integral item of the PI-based voltage controller is disable, the output voltage $\boldsymbol{v}_{pcc}$ can be expressed in *d*–*q* form as follows:

$$\begin{cases} v_{\mathrm{pcc}d} = V_g cos\delta \\ v_{\mathrm{pcc}q} = X_g I_{\max} - V_g sin\delta \end{cases}. \tag{48}$$

Then, according to (38), the unsaturated current reference i_{ref} can be expressed in *d*–*q* form as follows:

$$\begin{cases} i_{\mathrm{ref}d} = k_{Vp}\left(V_{\mathrm{ref}} - V_g cos\delta\right) + I_{nd} \\ i_{\mathrm{ref}q} = k_{Vp}\left(V_g sin\delta - X_g I_{\max}\right) + I_{nq} \end{cases}. \tag{49}$$

As the virtual power ${P_{\mathrm{vir}}}^{\mathrm{II}}$ under virtual power way II [37] is calculated through

$$P_{\mathrm{vir}}^{\mathrm{II}} = \frac{3}{2}\left(v_{\mathrm{pcc}d} i_{\mathrm{ref}d} + v_{\mathrm{pcc}q} i_{\mathrm{ref}q}\right). \tag{50}$$

Thus, when $\left\| i_{\mathrm{ref}dq} \right\| \geq I_{\max}$, ${P_{\mathrm{vir}}}^{\mathrm{II}}$ with *d*-axis priority current limiter can be derived as follows:

$$P_{\mathrm{vir}}^{\mathrm{II}} = \frac{3}{2}\left(a_{\mathrm{II}} \cos\delta + b_{\mathrm{II}} \sin\delta + c_{\mathrm{II}}\right) \tag{51}$$

where

$$\begin{cases} a_{\mathrm{II}} = V_g\left(k_{Vp}V_{\mathrm{ref}} - 2k_{Vp}I_{\max}X_g + I_{nd}\right) \\ b_{\mathrm{II}} = -V_g I_{nq} \\ c_{\mathrm{II}} = I_{\max}X_g\left(I_{nd} + k_{Vp}V_{\mathrm{ref}}\right) - k_{Vp}\left(V_g^2 + I_{\max}^2X_g^2\right) \end{cases}. \tag{52}$$

2) $P_{\mathrm{vir}}{}^{\mathrm{III}}$ in [39] with d-axis current priority current limiter

As the virtual power $P_{\mathrm{vir}}{}^{\mathrm{III}}$ under virtual power way III [39] is calculated through

$$P_{\mathrm{vir}}^{\mathrm{III}} = \frac{3}{2}(\underbrace{V_{ref}}_{V_{\mathrm{refd}}} i_{\mathrm{refd}} + \underbrace{0}_{V_{\mathrm{refq}}} \cdot i_{\mathrm{refd}}). \tag{53}$$

According to (49), when $\left\| i_{\mathrm{ref}dq} \right\| \geq I_{\max}$, $P_{\mathrm{vir}}{}^{\mathrm{III}}$ with d-axis priority current limiter can be derived as follows:

$$P_{\mathrm{vir}}^{\mathrm{III}} = \frac{3}{2}V_{\mathrm{ref}}[I_{nd} + k_{Vp}\left(V_{\mathrm{ref}} - V_g\cos\delta\right). \tag{54}$$

3) $P_{\mathrm{vir}}{}^{\mathrm{II}}$ in [37] with circular current limiter

When circular current limiter is triggered and the integral item of the PI-based voltage controller is disable, the output voltage $\boldsymbol{v_{\mathrm{pcc}}}$ can be expressed in d–q form as follows:

$$\begin{cases} v_{\mathrm{pccd}} = V_g cos\delta - X_g i_{gq} \\ v_{\mathrm{pccq}} = X_g i_{gd} - V_g sin\delta \end{cases}. \tag{55}$$

The relationship between unsaturated current reference $\boldsymbol{i_{\mathrm{ref}}}$ and output current $\boldsymbol{i_g}$ can be expressed as in d–q form:

$$\begin{cases} i_{\mathrm{ref}d} = \frac{1}{\rho} i_{gd} \\ i_{\mathrm{ref}q} = \frac{1}{\rho} i_{gq}. \end{cases} \tag{56}$$

Combine (49), (55) and (56), we have

$$\begin{cases} i_{refd} = k_{Vp}(V_{ref} - V_g\cos\delta + X_g\rho i_{refq}) + I_{nd} \\ i_{refq} = k_{Vp}(V_g\sin\delta + V_g\sin\delta - X_g\rho i_{refd}) + I_{nq} \end{cases} \tag{57}$$

Then, we have

$$\frac{1}{\rho} = \max \left\{ 1, k_{Vp}\sqrt{\frac{\left(V_{\mathrm{ref}} + \frac{I_{nd}}{k_{Vp}} - V_g\cos\delta\right)^2 + \left(\frac{I_{nq}}{k_{Vp}}V_g\sin\delta\right)^2}{I_{\max}^2} - X_g^2} \right\}. \tag{58}$$

According to (50), when $\left\| i_{\mathrm{ref}dq} \right\| \geq I_{\max}$, $P_{\mathrm{vir}}{}^{\mathrm{II}}$ with circular current limiter can be derived as follows:

$$\begin{aligned} P_{\mathrm{vir}}^{\mathrm{II}} &= \frac{3}{2}(v_{\mathrm{pccd}} i_{\mathrm{refd}} + v_{\mathrm{pccq}} i_{\mathrm{refq}}) \\ &= \frac{3}{2}(v_{\mathrm{pccd}}\frac{1}{\rho} i_{\mathrm{gd}} + v_{\mathrm{pccq}}\frac{1}{\rho} i_{\mathrm{gq}}) \\ &= \frac{1}{\rho} \cdot \underbrace{\frac{3}{2}(v_{\mathrm{pccd}} i_{\mathrm{gd}} + v_{\mathrm{pccq}} i_{\mathrm{gq}})}_{P_e^{\mathrm{CCL}}} \end{aligned} \tag{59}$$

where $P_e{}^{\mathrm{CCL}}$ is expressed in (29).

4) $P_{\mathrm{vir}}{}^{\mathrm{III}}$ in [39] with circular current limiter

According to (53), when $\left\| i_{\mathrm{ref}dq} \right\| \geq I_{\max}$, $P_{\mathrm{vir}}{}^{\mathrm{III}}$ with circular current limiter can be derived as follows:

$$\begin{aligned} P_{\mathrm{vir}}^{\mathrm{III}} &= \frac{3}{2}(\underbrace{V_{\mathrm{ref}}}_{V_{\mathrm{refd}}} i_{\mathrm{refd}} + \underbrace{0}_{V_{\mathrm{refq}}} \cdot i_{\mathrm{refd}}) \\ &= \frac{3}{2}(V_{\mathrm{ref}}\frac{1}{\rho} i_{\mathrm{gd}}) \\ &= \frac{3V_{\mathrm{ref}} i_{\mathrm{gd}}}{2\rho} \end{aligned} \tag{60}$$

According to [22], we have

$$\left.\frac{3}{2}V_{\mathrm{ref}} i_{gd} = \underbrace{\frac{3}{2}\left(v_{\mathrm{pccd}} i_{gd} + v_{\mathrm{pccq}} i_{gq}\right)}_{P_e^{\mathrm{CCL}}} + \frac{3}{2}R_e I_{\max}^2 \right). \tag{61}$$

Thus, when $\left\| i_{\mathrm{ref}dq} \right\| \geq I_{\max}$, $P_{\mathrm{vir}}{}^{\mathrm{II}}$ with circular current limiter can be derived as follows:

$$P_{\mathrm{vir}}^{\mathrm{III}} = \frac{3}{2\rho}\left[P_e^{\mathrm{CCL}} + R_e I_{\max}^2\right]. \tag{62}$$

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