Real-Time Parameter Estimation in SS Compensated Wireless Power Transfer Systems Considering Nonlinearity of the Diode Rectifier

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***Abstract*—A real-time parameter estimation method is proposed for series–series compensated wireless power transfer systems in this article. Unlike conventional approaches that model the input impedance as purely resistive, a more accurate inductive model is established with the consideration of the nonlinearity of diode rectifiers. Based on the derived model, the key system parameters can be accurately estimated in real time, by simply sampling the primary compensation capacitor voltage and the input voltage. This method eliminates the need for bilateral communication and causes zero interference on normal system operation as no prior or special actions are required. The estimation procedures are presented in detail and verified on a prototype. Experimental results demonstrate the feasibility of the proposed method, which achieves a high-accuracy estimation of the coupling coefficients and output voltage in 131 μs.**

***Index Terms*—Coupling coefficient, real-time estimation, wireless power transfer (WPT).**

I. INTRODUCTION

WIRELESS power transfer (WPT) has experienced a rapid development over the past two decades, widening the scope of applications in many fields including portable electronics [1], medical implants [2], [3], automation [4], and electric vehicles [5], [6]. With the success in commercialization, Hui et al. [7] advocates a paradigm shift from “compatibility” to “optimal performance” for the next generation of WPT. One of the key suggestions proposed in [7] is to divert the majority of control functions to the primary side, leaving only protective functions (such as overcurrent, overvoltage, and overtemperature protections) on the secondary side.

To fully leverage the primary-side control in WPT, it is essential to develop a fast and accurate parameter estimation method that relies solely on primary-side measurements. This requirement stems from the fact that the coupling coefficient and the load condition critically affect efficiency optimization and output regulation. Moreover, without a physical link, the spatial alignment between the transmitting and receiving coils is subject to environmental variations, resulting in time-varying coupling conditions. This poses a strong demand for the real-time estimation on primary-side control of WPT.

The solutions adopted in previous literature typically employ one or more of the following approaches.

1) Using wireless communication.
2) Adding auxiliary circuits or components.
3) Taking special actions, such as frequency sweeping, shorting the rectifier, or skipping pulses.

Wireless communication is frequently employed in the estimation methods [8], [9], [10] for dual-side data transmission and reception. Although straightforward and effective, this approach is vulnerable to electromagnetic interference, which can result in data loss, errors, or even complete communication failure. Moreover, for real-time estimation, low-latency communication devices are required.

Additional circuits or components are used for detection or to introduce a new state in the WPT system [11], [12], [13]. In [11], an additional magnetic ring is connected in series with transmitting coil to detect voltage transients for estimation. In [12], a voltage clipper is added on the output side, providing a special state for calibration before estimation. A special parallel *LC* branch is added on the receiver side with a designated resonant frequency in [13], which virtually forms a short-circuit in the rectifier specifically for the seventh-order harmonic component. While effective, these methods increase system cost and complexity.

Special action methods are approaches that momentarily disrupt the normal operation of WPT systems to induce identifiable system states for performing parameter estimation [14], [15], [16]. In [14], a searching algorithm is employed to identify parameters by sweeping frequency while shorting the rectifier. The coupling coefficient is estimated in [15] by first introducing two special states, i.e., short-circuit and open-circuit states on the receiver-side, and subsequently detecting the zero-phase-angle by frequency sweeping. In [16], the damped frequency of the

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Received 3 September 2025; revised 24 November 2025 and 22 December 2025; accepted 3 January 2026. Date of publication 12 January 2026; date of current version 20 March 2026. This work was supported by the Hong Kong Research Grants Council under the General Research Fund under Grant 17204724. Recommended for publication by Associate Editor B. Shao. *(Corresponding author: Jiayang Wu.)*

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This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/TPEL.2026.3653046.

Digital Object Identifier 10.1109/TPEL.2026.3653046

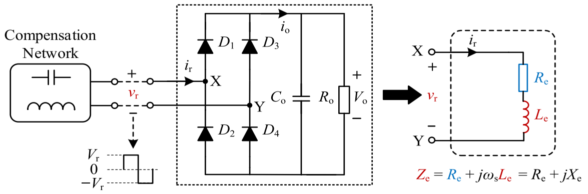


Fig. 1. Conceptual circuit of a diode rectifier in WPT systems.

system is identified for estimation by perturbing the system through pulse skipping. As the normal operation of the system is either halted or interfered with the special action methods, their application scope is typically limited.

Harmonic analysis-based estimation methods are those that extract harmonic components for parameter identification [17], [18], [19], [20]. For example, the estimation method in [17] is based on the second harmonic component in an equivalent virtual short-circuit state. However, the method requires the use of high-bandwidth analog-to-digital converters (ADC). In [18], the third harmonic components of the primary current and voltage are extracted with Kalman filter for analysis. While effective, the analog harmonic extractor is subject to working frequency variations. In [19], the method analyzes the total harmonic distortion of the input current using fast Fourier transform (FFT) to perform estimation. This method is computationally intensive, which limits real-time estimation speed and demands high-bandwidth ADCs for the necessary FFT processing.

Moreover, existing estimation methods [21], [22], [23] are based on the assumption that the diode rectifier behaves as a purely resistive load. In reality, the nonlinearity of the diode rectifier introduces an inductive impedance component at kHz frequencies [24], [25], which renders the simple resistive model inaccurate and compromises estimation accuracy.

To address the abovementioned issues, this article proposes a real-time estimation method for the coupling coefficient and output voltage of series–series (SS) compensated WPT systems with consideration of the diode rectifier nonlinearity. The proposed method offers the following features.

1) Fast estimation with the response time of submillisecond.
2) Zero Interference on the Normal Operation of the System: No prior or special actions are required, such as calibration, frequency sweeping, output shorting, or pulse skipping.
3) Bilateral communication is not needed.
4) Low sampling rate of two samples per switching period.

II. SIMPLIFIED MODEL OF THE DIODE RECTIFIER

The input impedance of the diode rectifier is commonly modeled as a purely resistive load, named the resistive model. In practice, the input impedance exhibits inductive at kHz frequencies due to diode nonlinearity and varies with working conditions. Therefore, the input impedance of the diode rectifier Z_e can be modeled as an effective resistance R_e and an effective inductance L_e in series, as shown in Fig. 1.

The typical waveforms of diode rectifiers in a WPT system are shown in Fig. 2. Assuming the system operates in steady state, the output voltage V_o remains constant. Therefore, the input voltage of the rectifier v_r is a square wave with the amplitude V_r. Its edges align with the zero-crossing points of the rectifier input current i_r due to the diode conduction characteristic. The rectifier angle γ is defined as the phase difference between the fundamental components $v_{r,1}$ and $i_{r,1}$ of v_r and i_r, respectively. The phase of $v_{r,1}$ is taken as reference. As v_r is a periodical signal in steady state, it is given by

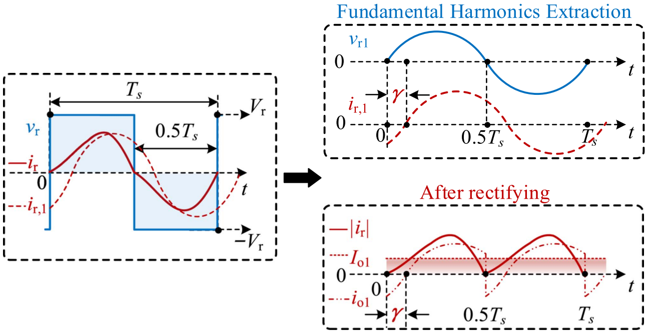


Fig. 2. Typical steady waveforms of a diode rectifier in WPT systems.

$$v_r(t) = \begin{cases} V_r, 0 \leq t \leq 0.5T_s \\ -V_r, 0.5T_s \leq t \leq T_s \end{cases}, V_r = V_o + 2V_D \tag{1}$$

where T_s is the switching period and V_d denotes the forward voltage drop of each diode in the rectifier.

By conducting Fourier decomposition on v_r, $v_{r,1}$ is derived as

$$v_{r,1} = V_{r1}\sin(\omega_s t) = \frac{4}{\pi}(V_o + 2V_D)\sin(\omega_s t) \tag{2}$$

where ω_s is the working angular frequency and V_{r1} is the amplitude of $v_{r,1}$.

As shown in Fig. 2, i_{o1} represents the rectified current $i_{r,1}$. Hence, the equivalent average output current I_{o1} is given by

$$\begin{aligned} I_{o1} &= \frac{1}{T_s/2}\int_0^{\frac{T_s}{2}} i_{o1}dt \\ &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} I_{r1}\sin(\omega_s t - \gamma)dt = \frac{2}{\pi}I_{r1}\cos\gamma \end{aligned} \tag{3}$$

where I_{r1} stands for the amplitude of $i_{r,1}$.

Considering the rectifier angle, the phasors of Z_e, i.e., $\mathbf{Z_e}$ is expressed as

$$\mathbf{Z}_e = \frac{\mathbf{V_{r1}}}{\mathbf{I_{r1}}} = \frac{V_{r1}}{I_{r1}}\angle\gamma \tag{4}$$

where $\mathbf{V_{r1}}$ and $\mathbf{I_{r1}}$ are the phasors of $v_{r,1}$, and $i_{r,1}$, respectively.

By substituting (2) and (3) into (4), we have

$$\mathbf{Z}_e = R_r\cos\gamma\angle\gamma, where R_r = \frac{8}{\pi^2}\frac{(V_o + 2V_D)}{I_{o1}}. \tag{5}$$

Note that $\mathbf{Z_e}$ is reduced to R_r when assuming γ is zero. Hence, the physical meaning of R_r is the diode rectifier's equivalent impedance of resistive model, which considers the input voltage and current of the rectifier are in phase. According to (5), Z_e can be expressed as

$$Z_e = R_e + jX_e where \begin{cases} R_e = R_r\cos^2\gamma \\ X_e = 0.5R_r\sin 2\gamma \end{cases}. \tag{6}$$

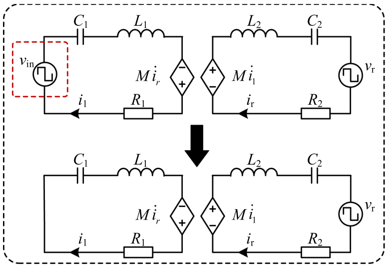


Fig. 3. Equivalent circuit of the SS compensated topology for high-order harmonics of i_r.

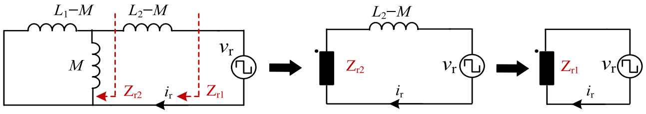


Fig. 4. Simplified equivalent circuits for high-order harmonics in SS compensated topology.

It is noted that the sum of the harmonics of i_r equals zero at the moments that v_r toggles. Utilizing this characteristic, the angle γ can be analyzed in the time domain. In this article, we are focused on the SS compensated topology. In steady state, there are equivalently two voltage sources, i.e., the primary input voltage v_{in} and v_r, as shown in Fig. 3.

Here, L_1 and L_2 stand for the primary and secondary self-inductances, i_1 represents the primary current, and M denotes the mutual inductance. As WPT systems exhibit strong filtering feature for the input source v_{in}, hence, the input source's influence on higher-order harmonics of i_r, is negligible [24], [25]. Consequently, only v_r is considered for deriving higher-order harmonics of i_r. As v_r is a periodically symmetric square wave in steady state, it only contains odd-order harmonics, given as

$$v_r = \sum_{n=1}^{\infty} \frac{4V_r}{(2n-1)\pi} \sin\left((2n-1)\omega_s t\right). \tag{7}$$

Correspondingly, i_r also contains only odd-order harmonics. Assuming the resonant frequencies of primary and secondary sides are the same or close to each other, the inductive reactance is dominant over the capacitive reactance for both sides at harmonic frequencies, which are much higher than the resonant frequency. Therefore, the T-model for high order harmonics of i_r can be simplified by only considering the inductive reactance, as depicted in Fig. 4.

For $i_{r,m}$, (the mth harmonic of i_r, where m is an odd integer), the effective impedances are expressed as

$$Z_{r2} = j[m\omega_s(L_1 - M)]//(jm\omega_s M) = jm\omega_s M(1 - M/L_1) \tag{8}$$

$$Z_{r1} = Z_{r2} + jm\omega_s(L_2 - M) = jm\omega_s L_2(1 - k^2) \tag{9}$$

where the coupling coefficient $k = M/\sqrt{L_1 L_2}$.

By combining (7) and (9), $i_{r,m}$ is derived as

$$i_{r,m}(t) = \frac{v_{r,m}}{Z_{r1}} = \frac{1}{m^2} \frac{4V_r \cos(m\omega_s t)}{(1-k^2)\pi\omega_s L_2}. \tag{10}$$

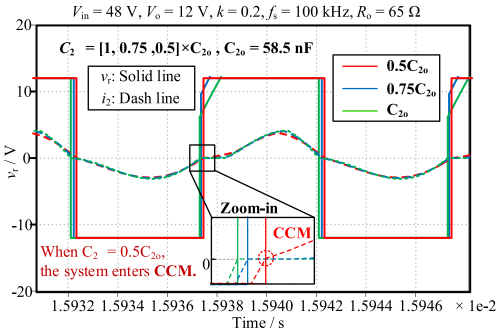


Fig. 5. Key waveforms of the diode rectifier under various secondary capacitances.

According to (10), the sum of the higher-order harmonics of i_r at time $t = 0$ is

$$\begin{aligned}\sum_{m=3}^{\infty} i_{r,m}(0) &= \frac{4V_r}{(1-k^2)\pi\omega_s L_2} \sum_{n=1}^{\infty} \frac{1}{(2n+1)^2} \\ &= \left(\frac{\pi^2}{8} - 1\right) \frac{4V_r}{(1-k^2)\pi\omega_s L_2}.\end{aligned} \tag{11}$$

The fundamental component of i_r (i.e., $i_{r,1}$) at time $t = 0$ can be derived from (2) and (5), given as

$$i_{r,1}(0) = \frac{\mathbf{V_{r1}}}{\mathbf{Z}_e} = \frac{4}{\pi} \frac{V_r}{R_r} \tan(-\gamma). \tag{12}$$

Due to the conduction characteristics of diodes, the sum of fundamental and higher order harmonics of rectifier current is zero at $t = 0$, as shown in Fig. 2. Mathematically, this given by

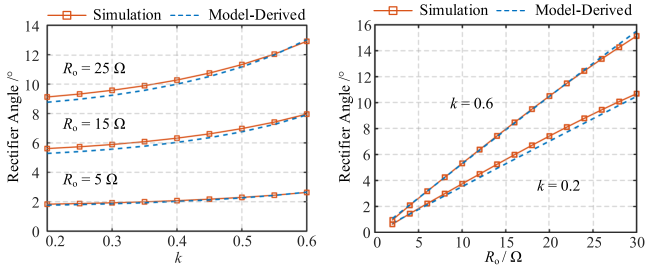
$$\begin{aligned}i_{r,1}(0) + \sum_{m=3}^{\infty} i_{r,m}(0) = 0 \Rightarrow \tan(\gamma) \\ = \left(\frac{\pi^2}{8} - 1\right) \frac{R_r}{(1-k^2)\omega_s L_2}.\end{aligned} \tag{13}$$

It is noted that (13) is valid only for the continuous conduction mode (CCM) of diode rectifiers. Under discontinuous conduction mode (DCM), v_r is not a standard square wave and contains rich and complex even-order harmonics, invalidating the previous assumptions. Employing the proposed model in DCM may decrease estimation accuracy to below 90%. However, DCM of diode rectifiers occurs only under extremely light load conditions [26]. Therefore, the proposed model remains applicable across most operational scenarios. In practice, DCM can be readily avoided by design, thereby securing the model robustness across intended operating conditions. For example, the critical load resistance $R_{o \cdot c}$ is determined by f_s and C_2. Therefore, the value of C_2 can be adjusted to maintain CCM operation according to the practical need. As shown in Fig. 5, the system gradually exits DCM by reducing the capacitance of C_2 while the resonant frequency is held constant.

Simulation works are conducted to verify the derived model under the parameters listed in Table I. For simplicity, the diodes are modeled as ideal in the simulation, neglecting nonideal effects such as the forward voltage drop and junction capacitance. As shown in Fig. 6, the model-derived results show a

TABLE I
PARAMETERS IN SIMULATION

Parameters	Symbol	Values
Primary/Secondary capacitor	C_1 / C_2	58.6 nF
Primary/Secondary self-inductance	L_1 / L_2	59.9 μH
Working frequency	f_s	85 kHz

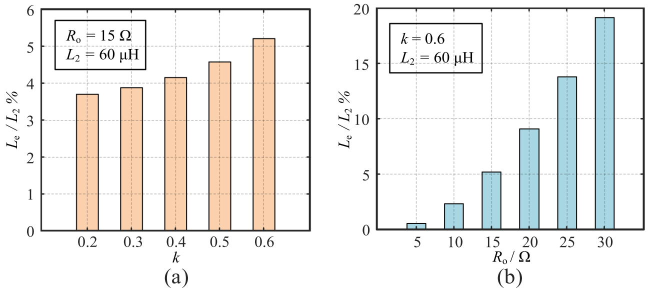


(a) (b)

Fig. 6. Comparison of the rectifier angles γ between simulation and model-derived results. (a) γ versus k. (b) γ versus R_o.

TABLE II
RESISTIVE MODEL AND INDUCTIVE MODEL FOR THE DIODE RECTIFIER UNDER VARIOUS LOAD RESISTANCES

Load Resistance	Resistive Model	Inductive Model	
R_o / Ω	R_e / Ω	R_e / Ω	L_e / μH
5	4.06	4.05	0.35
10	8.11	8.04	1.40
15	12.16	11.93	3.12
20	16.22	15.68	5.44



(a) (b)

Fig. 7. Ratio of the effective inductance to the secondary self-inductance under (a) Various k. (b) Various R_o.

good agreement with the simulation results, which verifies the correctness of the theoretical analysis. The results indicate that the rectifier angle γ increases monotonically with load resistance and decreases with coupling coefficient.

The comparison between the resistive and inductive models across various load resistances when k is 0.6 is summarized in Table II. The comparison indicates that the effect of the rectifier angle is non-negligible, especially under large load resistances. As shown in Fig. 7, the effective inductance L_e reaches 20% of the secondary self-inductance. Besides, the effective resistance also slightly differs between the two models.

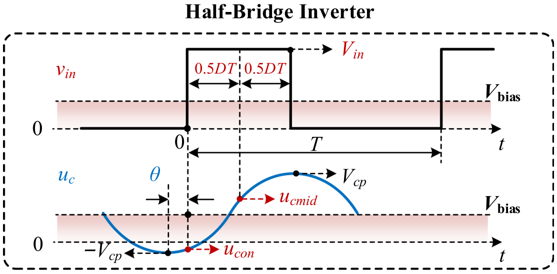


Fig. 8. Conceptual waveforms illustrating the adopted sample method for a half-bridge inverter.

III. PROPOSED REAL-TIME ESTIMATION METHOD

In this section, the principles of the proposed estimation method are elaborated. There are three unknown parameters: 1) mutual inductance M, 2) load resistance R_o, and 3) rectifier angle γ. According to the derived diode rectifier model in Section II, γ is dependent on M and R_o. Consequently, only M and R_o remain as independent variables determined by two equations. These equations are derived from the equivalent circuit analysis and power balance principles, as detailed in the following.

A. *Operating Parameters Derivation From Signal Sampling*

Prior to estimation, three quantities should be acquired: 1) primary current i_1; 2) input impedance Z_{in}; and 3) primary input voltage v_{in}. This article adopts a straightforward sampling method to derive these quantities in a SS compensated topology. The rationale is to reconstruct the fundamental component of the compensated capacitor voltage u_c by sampling u_c at special instants, i.e., at the turn-ON point and the midpoint of duty cycle of the inverter upper switch, as shown in Fig. 8. Once u_c is obtained, i_1 can then be derived via the reconstruction process described below.

The two sampled values u_{con} and u_{cmid} are expressed as

$$\begin{cases} u_{con} = V_{cp}\cos(\pi+\theta) + V_{\text{bias}} \\ u_{cmid} = V_{cp}\cos(\pi+\theta+\pi D) + V_{\text{bias}} \end{cases} \tag{14}$$

where V_{bias} is the dc bias voltage of u_c, which equals to DV_{in}; V_{cp} denotes the amplitude of u_c, and θ is the phase difference between the rising edge of v_{in} and the negative peak of u_c. A positive θ indicates that the rising edge of v_{in} lags the negative peak of u_c.

From (14), V_{cp} and θ can be derived as

$$\begin{cases} V_{cp} = (V_{\text{bias}} - u_{con})\sec(\theta) \\ \theta = \tan^{-1}[\cot(\pi D) - \frac{u_{cmid}-V_{\text{bias}}}{u_{con}-V_{\text{bias}}}\csc(\pi D)]. \end{cases} \tag{15}$$

With the deduced V_{cp} and θ, u_c is reconstructed as

$$u_c = V_{cp}\cos(\pi+\theta+\omega_s t) \tag{16}$$

where ω_s is the working angular frequency.

As C_1 is in series with the primary coil in SS compensated systems, we have

$$i_1 = C_1\frac{du_c}{dt} \Rightarrow i_1 = C_1\omega_s V_{cp}\sin(\theta+\omega_s t). \tag{17}$$

Note that duty cycle D and working frequency f_s are known in the analysis as they are controller-set parameters. After deriving i_1, the input impedance Z_{in} can then be obtained. The primary input voltage v_{in} is a square wave, as shown in Fig. 8. Through Fourier decomposition, its fundamental component v_{s} can be derived as

$$v_s = \frac{2}{\pi}\sin(\pi D)V_{\text{in}}\cos(\omega_s t - \pi D). \tag{18}$$

By combining (17) and (18), Z_{in} is given by

$$\mathbf{Z}_{\text{in}} = \frac{\mathbf{V}_{\text{s}}}{\mathbf{i}_1} = \frac{2}{\pi}\frac{V_{\text{in}}\sin(\pi D)}{C_1\omega_s V_{cp}}\angle(0.5 - D)\pi - \theta \Rightarrow$$

$$Z_{\text{in}} = \frac{2}{\pi}\frac{V_{\text{in}}\sin(\pi D)}{C_1\omega_s V_{cp}}[\sin(D\pi + \theta) - j\cos(D\pi + \theta)] \tag{19}$$

where $\mathbf{Z}_{\text{in}}$, $\mathbf{V}_{\text{s}}$, and $\mathbf{i}_1$ are the phasors of Z_{in}, v_{s}, and i_1, respectively.

Moreover, the input power can be simultaneously derived from the dc input voltage V_{in} and i_1, by using

$$P_{\text{in}} = V_{\text{in}} f_s \int_0^{DT_s} i_1 dt. \tag{20}$$

Besides, switching loss and conduction loss of the inverter are missing for input power calculation in previous modeling, that means the actual input power is less than the calculated value, expressed as

$$P_{\text{in\_actual}} = P_{in\_cal} - P_{\text{loss\_on\_inverter}}. \tag{21}$$

To achieve a high estimation accuracy, the missing losses should be compensated. In previous analysis, primary current i_1 including its amplitude and phase referring to rising edge of v_{in} is acquired, which enables the calculation of inverter losses. By substituting $t = 0$ and $t = DT_{\text{s}}$ into (17), the turn-OFF current for the upper switch and lower switch are derived as

$$\begin{cases} i_{1\text{\_low\_off}} = C_1\omega_s V_{cp}\sin(\theta) \\ i_{1\text{\_up\_off}} = C_1\omega_s V_{cp}\sin(\theta + 2\pi D). \end{cases} \tag{22}$$

Normally, the switch turn-OFF energy E_{OFF} is provided in the datasheet for a specified drain-source voltage V_{ds} and current I_{ds}. As E_{OFF} is approximately proportional to the product of turn-OFF voltage and current, the turn-OFF loss can be derived as

$$P_{\text{off}} = f_s E_{\text{off}}\frac{V_{\text{in}}(|i_{1\text{\_up\_off}}| + |i_{1\text{\_low\_off}}|)}{V_{ds}I_{\text{dc}}}. \tag{23}$$

As the ZVS is achieved in the whole working range, the switching loss is equal to the turn-OFF loss. For the conduction loss P_{con}, it can also be derived by (17), given as

$$P_{con} = 0.5{I_{1\text{p}}}^2 R_{\text{on}} = 0.5R_{\text{on}}(C_1\omega_s V_{cp})^2 \tag{24}$$

where R_{ON} is the switch ON-state resistance and $I_{1\text{p}}$ is the amplitude of i_1.

By combining (23) and (24), the compensation for input power is given as

$$P_{\text{in\_actual}} = P_{\text{in\_}cal} - (P_{\text{off}} + P_{con}). \tag{25}$$

TABLE III
PARAMETERS FOR DERIVATION OF PREREQUISITES

Parameters	Symbol	Acquisition Method
Dc Input Voltage	V_{in}	Sample circuit
Capacitor Voltages	u_{con}, u_{cmid}	Sample circuit
Resonant Frequency	f_s	MCU Register
Duty Ratio	D	MCU Register
Primary Capacitance	C_1	LCR Meter
Switch On-state Resistance	R_{on}	Device Datasheet
Switch Turn-off energy	E_{off}	Device Datasheet

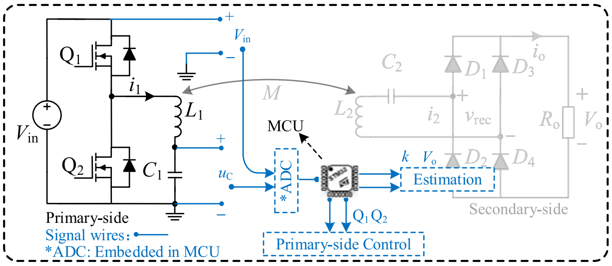


Fig. 9. Conceptual control diagram for the proposed estimation method.

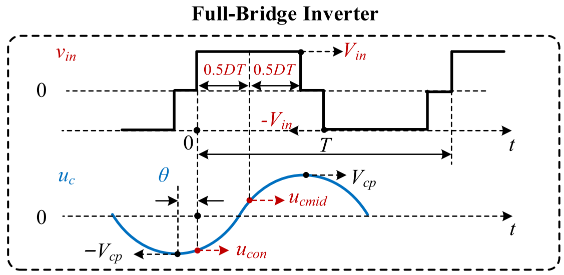


Fig. 10. Conceptual waveforms for the adopted sample method based on full-bridge inverter.

The parameters required for the preceding derivation are tabulated in Table III. With prior knowledge of the primary capacitance, switch ON-resistance, and switch turn-OFF energy, all computations can be conducted in real time within the digital controller. The corresponding simplified control diagram is depicted in Fig. 9.

In this work, the half-bridge inverter is chosen as a case study. The rationales of the proposed method for half-bridge and full-bridge inverters are identical. The subtle differences lie in (14), (15), and (18). The differences arise from the presence of a dc bias voltage, which the full-bridge inverter output does not have, as shown in Fig. 10. Therefore, (14), (15), and (18) should be revised as

$$\begin{cases} u_{con\_\text{full}} = V_{cp}\cos(\pi + \theta) \\ u_{cmid\_\text{full}} = V_{cp}\cos(\pi + \theta + \pi D) \end{cases} \tag{26}$$

$$\begin{cases} V_{cp\_\text{full}} = -u_{con}\sec(\theta) \\ \theta_{\text{full}} = \tan^{-1}[\cot(\pi D) - \frac{u_{cmid}}{u_{con}}\csc(\pi D)] \end{cases} \tag{27}$$

$$v_{s\_\text{full}} = \frac{4}{\pi}\sin(\pi D)V_{\text{in}}\cos(\omega_s t - \pi D). \tag{28}$$

Apart from these alterations, the remaining derivations are unchanged for full-bridge inverter systems.

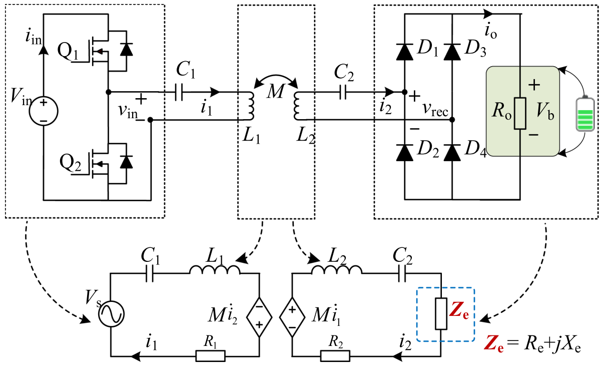


Fig. 11. Equivalent circuit of the SS compensated topology.

B. Principles of the Proposed Estimation Method

The equivalent circuit of the SS compensated topology is presented in Fig. 11. Its describing circuit equations are given as

$$(R_1 + jX_1)\mathbf{I_1} - j\omega_s M\mathbf{I_2} = \mathbf{V_s} \tag{29}$$

$$j\omega_s M\mathbf{I_1} + [(R_\mathrm{e} + R_2) + j(X_2 + X_\mathrm{e})]\mathbf{I_2} = 0 \tag{30}$$

where $\mathbf{I}_1$ is the primary current phasor, $\mathbf{I}_2$ is the secondary current phasor, and $\mathbf{V_s}$ is the input voltage phasor; $|\mathbf{V_s}| = 2V_{\mathrm{in}}/\pi$, and $X_i = \omega L_i - 1/(\omega C_i)$, $i = 1$ or 2.

According to (30), the term $j\omega_s M\mathbf{I}_2$ can be derived as

$$j\omega_s M\mathbf{I_2} = \frac{{\omega_s}^2 M^2 \mathbf{I_1}}{(R_\mathrm{e} + R_2) + j(X_2 + X_\mathrm{e})}. \tag{31}$$

By substituting (29) into (31), we have

$$\begin{aligned}&(R_1 + jX_1)\mathbf{I_1} - \frac{{\omega_s}^2 M^2 \mathbf{I_1}}{(R_\mathrm{e} + R_2) + j(X_2 + X_\mathrm{e})} = \mathbf{V_s}\\ &\Rightarrow (R_\mathrm{e} + R_2) + j(X_2 + X_\mathrm{e}) = \frac{{\omega_s}^2 M^2}{(R_1 + jX_1) - \mathbf{V_s}/\mathbf{I_1}}.\end{aligned} \tag{32}$$

Given that the phases of the two complex terms on both sides of (32) are equal, the relation is given by

$$\frac{R_\mathrm{e} + R_2}{X_2 + X_\mathrm{e}} = -\frac{\mathrm{Re}(Z_{\mathrm{in}}) - R_1}{\mathrm{Im}(Z_{\mathrm{in}}) - X_1} \tag{33}$$

where the input impedance Z_{in} is defined as $\mathbf{V_s} / \mathbf{I}_1$. Re(.) and Im(.) denote the real and imaginary parts of a complex number, respectively.

It is worth noting that (33) is valid only when $X_2 + X_\mathrm{e}$ is NOT zero. Otherwise, the denominator becomes zero, rendering the expression undefined. Hence, new formulations are required when $X_2 + X_\mathrm{e} = 0$. We designate the condition $X_2 + X_\mathrm{e} \neq 0$ as Case I, and the condition $X_2 + X_\mathrm{e} = 0$ as Case II. The corresponding equations for Case II are derived from (32) as

$$\begin{cases} X_2 + X_\mathrm{e} = 0 \\ R_\mathrm{e} + R_2 = \frac{-{\omega_s}^2 M^2}{\mathrm{Re}(Z_{\mathrm{in}}) - R_1} = \frac{L_1 L_2 {\omega_s}^2 k^2}{R_1 - \mathrm{Re}(Z_{\mathrm{in}})}. \end{cases} \tag{34}$$

Since (33) and (34) apply to different cases, the criterion for case judgement is given as

$$\begin{cases} \mathrm{Im}(Z_{\mathrm{in}}) - X_1 \neq 0, \mathrm{Case I} \\ \mathrm{Im}(Z_{\mathrm{in}}) - X_1 = 0, \mathrm{Case II} \end{cases}. \tag{35}$$

The second equation for Case I is derived from the perspective of power balance. Ignoring the switching loss on the inverter, the input power is expressed as

$$P_{\mathrm{in}} = 0.5{I_1}^2 R_1 + 0.5 I_2^2 (R_e + R_2) \tag{36}$$

where I_1 and I_2 stand for the amplitudes of $\mathbf{I}_1$ and $\mathbf{I}_2$, respectively.

From (29), I_2 is derived as

$$I_2 = \frac{|\mathbf{V_s} - (R_1 + jX_1)\mathbf{I_1}|}{\omega_s M} \Rightarrow I_2^2 = \frac{|\mathbf{V_s} - (R_1 + jX_1)\mathbf{I_1}|^2}{{\omega_s}^2 M^2}. \tag{37}$$

By combining (36) and (37), the second equation is derived as

$$R_\mathrm{e} + R_2 = \frac{2{\omega_s}^2 (P_{\mathrm{in}} - 0.5{I_1}^2 R_1)}{|\mathbf{V_s} - (R_1 + jX_1)\mathbf{I_1}|^2} M^2. \tag{38}$$

According to the criterion in (35), the solutions will be derived on a case-by-case basis as follows.

Case I: $\mathrm{Im}(Z_{\mathrm{in}}) - X_1 \neq 0$

Since there are distinct equations for different cases, relevant equations and conditions are collected together for the Case I solution, specifically (5), (13), (33), and (38), given as follows:

$$\begin{cases} X_\mathrm{e} = 0.5R_\mathrm{r} \sin 2\gamma, R_\mathrm{e} = R_\mathrm{r} \cos^2\gamma \\ \tan\gamma = (\frac{\pi^2}{8} - 1)\frac{R_\mathrm{r}}{(1-k^2)\omega_s L_2} \\ \frac{R_\mathrm{e} + R_2}{X_2 + X_\mathrm{e}} = -\frac{\mathrm{Re}(Z_{\mathrm{in}}) - R_1}{\mathrm{Im}(Z_{\mathrm{in}}) - X_1} \\ R_\mathrm{e} + R_2 = \frac{2{\omega_s}^2 L_1 L_2 (P_{\mathrm{in}} - 0.5{I_1}^2 R_1)}{|\mathbf{V_s} - (R_1 + jX_1)\mathbf{I_1}|^2} k^2. \end{cases} \tag{39}$$

By rearranging (39), a quadratic equation with respect to tan γ is obtained as

$$A_1 (\tan\gamma)^2 + B_1 \tan\gamma + C_1 = 0 \tag{40}$$

where

$$\begin{cases} A_1 = K_2 K_3 (K_1 X_2 - R_2) - K_1 R_2 + K_1 K_2 \\ B_1 = K_1 X_2 - K_2 \\ C_1 = K_2 K_3 (K_1 X_2 - R_2) \\ K_1 = -\frac{\mathrm{Re}(Z_{\mathrm{in}}) - R_1}{\mathrm{Im}(Z_{\mathrm{in}}) - X_1} \\ K_2 = \frac{2{\omega_s}^2 L_1 L_2 (P_{\mathrm{in}} - 0.5{I_1}^2 R_1)}{|\mathbf{V_s} - (R_1 + jX_1)\mathbf{I_1}|^2} \\ K_3 = (\frac{\pi^2}{8} - 1)\frac{1}{\omega_s L_2}. \end{cases}$$

As analyzed in previous section, all the symbolic coefficients in (40) are known. Thus, the solution for tan γ can be easily obtained by solving the quadratic formula without any complex operation or searching algorithm.

Case II: $\mathrm{Im}(Z_{\mathrm{in}}) - X_1 = 0$

$$\begin{cases} X_\mathrm{e} = 0.5R_\mathrm{r} \sin 2\gamma, R_\mathrm{e} = R_\mathrm{r} \cos^2\gamma \\ \tan\gamma = (\frac{\pi^2}{8} - 1)\frac{R_\mathrm{r}}{(1-k^2)\omega_s L_2} \\ X_2 + X_\mathrm{e} = 0 \\ R_\mathrm{e} + R_2 = \frac{L_1 L_2 {\omega_s}^2 k^2}{R_1 - \mathrm{Re}(Z_{\mathrm{in}})}. \end{cases} \tag{41}$$

Similarly, a quadratic equation with respect to $\tan\gamma$ is obtained by rearranging (41), and is given by

$$A_2(\tan\gamma)^2 + B_2\tan\gamma + C_2 = 0 \tag{42}$$

where

$$\begin{cases} A_2 = K_4(1 + K_3X_2) - R_2 \\ B_2 = X_2 \\ C_2 = K_3K_4X_2 \\ K_4 = \frac{L_1L_2{\omega_s}^2}{R_1 - \mathrm{Re}(Z_{\mathrm{in}})}. \end{cases}$$

By applying the quadratic formula, the explicit solutions for $\tan\gamma$ is derived from (40) and (42) in both cases, given as

$$\tan\gamma_i = \frac{-B_i \pm \sqrt{{B_i}^2 - 4A_iC_i}}{2A_i} \tag{43}$$

where the subscript i denotes the Case i.

With the obtained $\tan\gamma$, R_{r} is derived from (13) and (38) as

$$R_{\mathrm{r}} = (K_2 - R_2) \Bigg/ \left[\frac{1}{1 + (\tan\gamma)^2} + \frac{K_2K_3}{\tan\gamma}\right]. \tag{44}$$

Subsequently, k is derived from (13) with the solved $\tan\gamma$ and R_{r}, given as

$$k = \sqrt{1 - \left(\frac{\pi^2}{8} - 1\right)\frac{R_{\mathrm{r}}}{\tan\gamma}\frac{1}{\omega_s L_2}}. \tag{45}$$

By combining (3), (5), and (36), V_o is derived as

$$V_{\mathrm{o}} = \frac{\pi}{4}I_2R_{\mathrm{r}}\sqrt{\frac{1}{1 + (\tan\gamma)^2}} - 2V_D \tag{46}$$

where

$$I_2 = \sqrt{\frac{2P_{\mathrm{in}} - {I_1}^2R_1}{R_{\mathrm{r}}\frac{1}{1+(\tan\gamma)^2} + R_2}}.$$

Although there are two mathematical solutions for $\tan\gamma$ as indicated in (43), only one solution is practically valid, while the other results in an unrealistically high output voltage and output power that exceeds the input power.

The flow chart of the whole estimation process is summarized in Fig. 12. Following these procedures, a closed-loop simulation comparison is conducted on a SS compensated WPT system under the condition that of 48 V-in and 12 V-out, utilizing the variable frequency and phase shifted control method. For a fair comparison, the estimation result that does not consider γ is derived from the same pattern and information of the proposed method but simplified by assuming γ is zero. As shown in Fig. 13, the consideration of the rectifier angle in the method improves the overall estimation accuracy, particularly under light load conditions. For instance, the estimated V_{o} and k both show approximately 4% improvement in accuracy under a light load condition where R_{o} is 15 Ω. The simulation results indicate that the proposed estimation method considering the rectifier nonlinearity exhibits higher accuracy than those that ignore it.

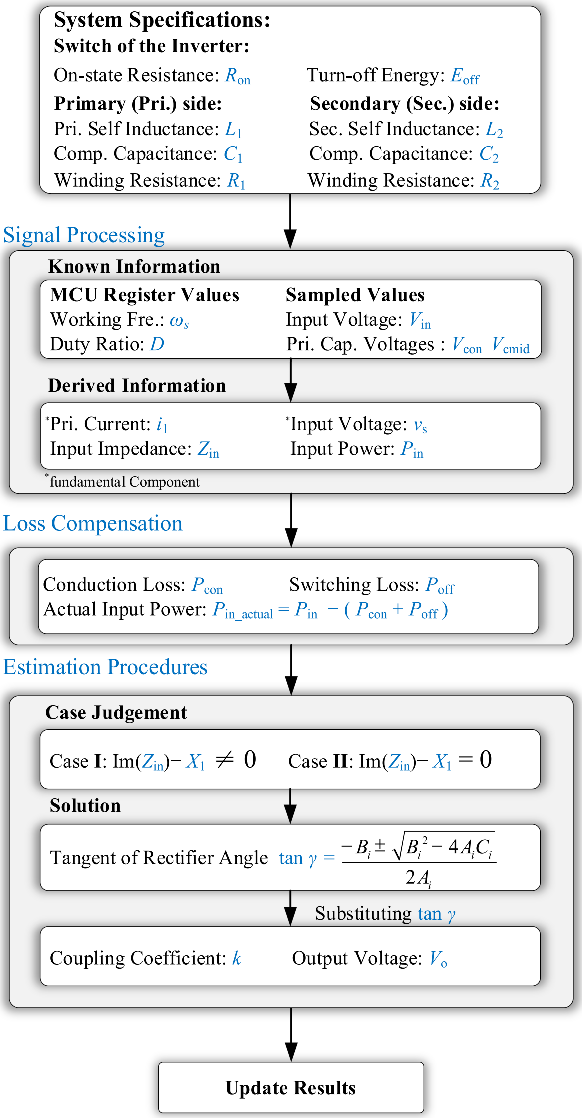
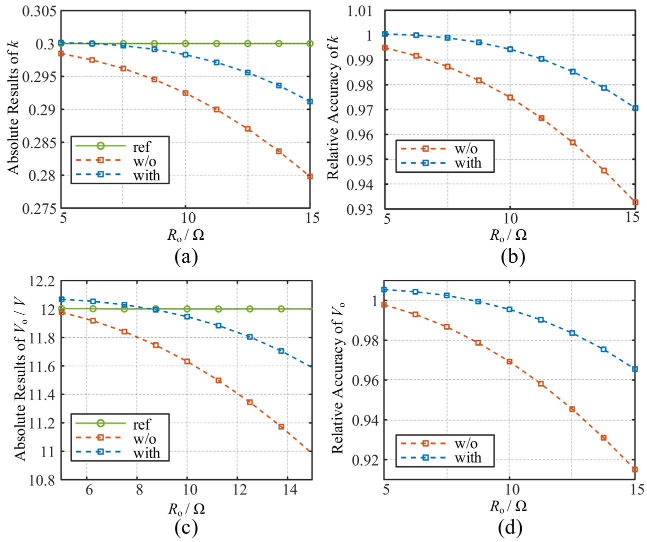


Fig. 12. Flowchart of the estimation process.

C. Consideration on Nonideal Effects

In practical systems, parasitic parameters of devices have influence on previous analysis, which are conducted in an ideal situation. Therefore, the effects of parasitic parameters are investigated to enhance the feasibility of this method.

1) On the primary side, the inverter output voltage v_{in} is slightly distorted by switches' parasitic capacitance, which is not a square wave but a trapezoidal one. Nonetheless, the nonideal square wave has little impact on the method since the rising and falling time caused by switches' parasitic capacitance are typically of tens of nanoseconds, which is negligible compared to the switching period in kilohertz applications. Additionally, for the deadtime, it can be absorbed into the effective duty ratio as the deadtime value is already stored in the microcontroller unit (MCU). In experiment, a digital comparator embedded in MCU is employed to trigger sample events.



(a) (b) (c) (d)

Fig. 13. Comparison of estimation results with and without rectifier angle. (a) Measured and estimated k. (b) Relative error of the estimated k. (c) Measured and estimated V_{o}. (d) Relative error of the estimated V_{o}.

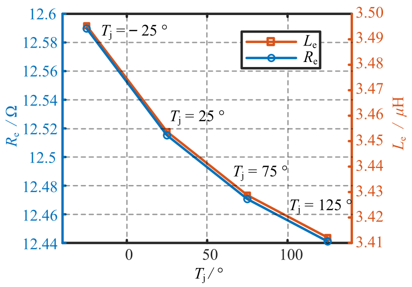


Fig. 14. Model-derived rectifier impedance versus diode junction temperature.

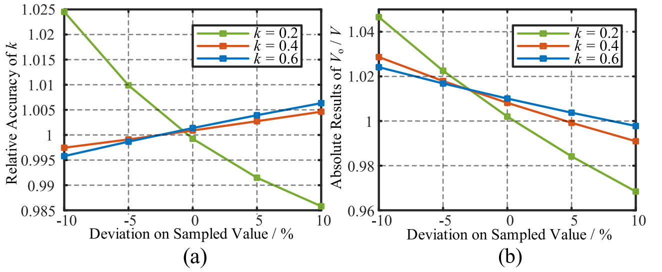
Therefore, the sampling points can be adjusted flexibly according to the deadtime, which can eliminate the effect of deadtime.

2) On the secondary side, the forward voltage drop of diodes V_{D} is dependent on junction temperature T_{j} and forward current I_{F}, which can be expressed as

$$V_D = f(I_F, T_j). \tag{47}$$

In WPTs, the operating temperature is usually in the range from -25° to 125° where V_{D} shows a positively monotonical relationship with I_{F}, and a negatively monotonical relationship with T_{j}. As a case study, the relationship among V_{D}, I_{F}, and T_{j} is obtained from the diode datasheet (Model: YQ3RSM10SD). The conditions under simulation are that input voltage is 48 V, coupling coefficient is 0.6, load resistance is 15 Ω, and working frequency is 85 kHz. As shown in Fig. 14, the model derived results R_{e} and L_{e} exhibit a monotonically decreasing trend with the diode junction temperature; however, the observed variations are negligible. The same conclusion is also for I_{F}, which induces variations on V_{D} of a similar scale. Therefore, the model demonstrates only marginal dependence on both diode temperature and forward current.

Although variations in V_{D} minimally affect the model's accuracy, they are a direct source of error in the output voltage estimation, as indicated in (46). The estimation accuracy can be further improved by obtaining a more accurate V_{D} from a datasheet-based I_{F}-T_{j} look-up table, if the implementation of temperature sensors is feasible.



(a) (b)

Fig. 15. Sensitivity analysis of estimation to deviations on sampling deviations. (a) k. (b) V_{o}.

For nonlinear capacitance effects, it causes slight deviation between the zero-crossing points of rectifier input current i_{r} and rectifier input voltage v_{r} [25]. Nonetheless, its impact is significantly less pronounced at kHz frequencies than at MHz frequencies [27], [28], [29]. The model of nonlinear capacitance effects on time shift has been derived in [28] and [29], given as

$$t_{\text{shift}} = \frac{T}{2\pi}\sqrt{\frac{4R_oQ_j}{4R_oQ_j + V_oT}} \tag{48}$$

where Q_{j} denotes the output junction charge of diode.

According to the datasheet of diode (Model: YQ3RSM10SD), the parasitic capacitance is around 70 pF under reverse voltage of 12 V. Substituting the working conditions that R_{o} is 15 Ω and f_{s} is 85 kHz into (48) gives a the time shift of 40.8 ns. Compared to the switching period (11.76 μs corresponding to 85 kHz), the deviation caused by nonlinear capacitance effects is negligible. An iterative correction can be applied to compensate for the parasitic capacitance in high frequency applications (e.g., MHz). The baseline estimation results (without compensation) are considered the first iteration. Subsequently, the calculated time shift is fed into (43) to derive an updated γ, which in turn is used to compute more precise results.

D. *Sensitivity Analysis*

The practical implementation faces inherent challenges from sampling noise and parasitic parameters. Sampling noise introduces errors into the measured values, while parasitic parameters cause deviations in the model. To evaluate their effect on estimation accuracy, the sensitivity analysis is conducted as follows.

The sample error's effects are presented in Fig. 15(a) and (b). Intentional errors ranging from −10% to +10% were introduced to the sampled values to assess estimation robustness. For coupling coefficient estimation, the results show a negligible impact under strong coupling conditions (e.g., $k = 0.4$ and 0.6,). Under weak coupling conditions, a 10% sampling error induces approximately a 2.5% deviation in the estimated k. For output voltage estimation, a 10% sampling error leads to a deviation of about 2.5% under strong coupling, which increases slightly to around 4% under weak coupling but still considered acceptable.

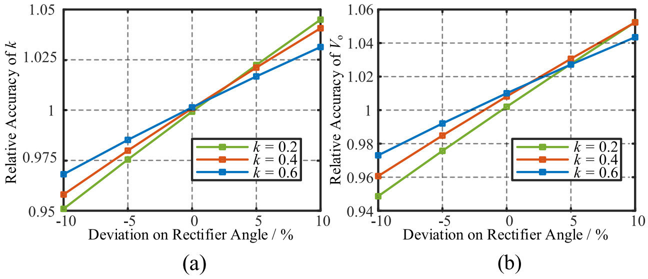


Fig. 16. Sensitivity analysis of modeling deviation on estimation accuracy. (a) k. (b) V_{O}.

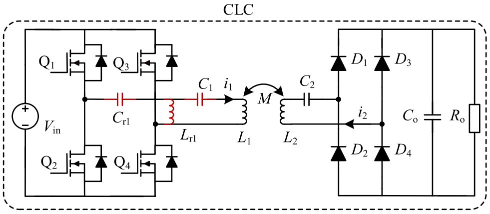


Fig. 17. Typical configuration of the CLC compensation topology.

The impact of model error is illustrated in Fig. 16(a) and (b). For both the coupling coefficient and output voltage estimation, the deviation varies quasi-linearly with the introduced error in the rectifier angle. The system becomes more sensitive to these errors under weaker coupling. Specifically, a 10% model error results in an estimation deviation of approximately 3% (k) and 4% (V_{O}) at $k = 0.6$, which increases to about 5% for both parameters at $k = 0.2$. The results demonstrate strong robustness against model errors. Although higher accuracy is attainable through a more detailed model with parasitic parameters, this would entail a corresponding increase in estimation time. Given that parasitic parameters (e.g., junction capacitance) are not as critical in kHz applications as in the MHz range, a balance between accuracy and real-time capability was struck in this work, supported by a detailed analysis on the impact of parasitic parameters.

E. Applicability

The proposed estimation method has the potential to be applied in other compensation networks such as SP and CLC.

Primary capacitor voltage sampling is the foundation of this method. Since both SS and SP compensation topologies share an identical primary-side structure (series compensation), the derivation for operating parameters like input power and primary current is directly applicable to SP topologies.

Due to parallel compensated capacitor in *LCC* compensation topologies, the operating parameters derivation based on capacitor voltage sampling cannot be directly applied. Nevertheless, it becomes available after modification on the primary compensation configuration by swapping the primary inductor and capacitors, which make it a CLC-type compensation [30], [31], [32]. The configuration is depicted in Fig. 17. While the proposed method cannot be applied into *LCC* topologies, the derived diode rectifier model is available for *LCC* systems working in the vicinity of the resonant frequency. The reason is that the high-order harmonics equivalent circuits are same for these compensation topologies.

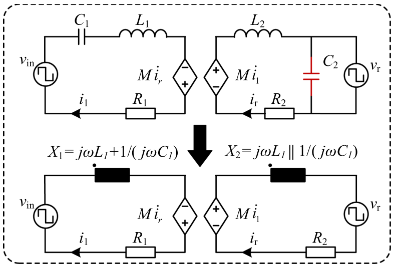


Fig. 18. Unified equivalent circuit of the SP compensated topology.

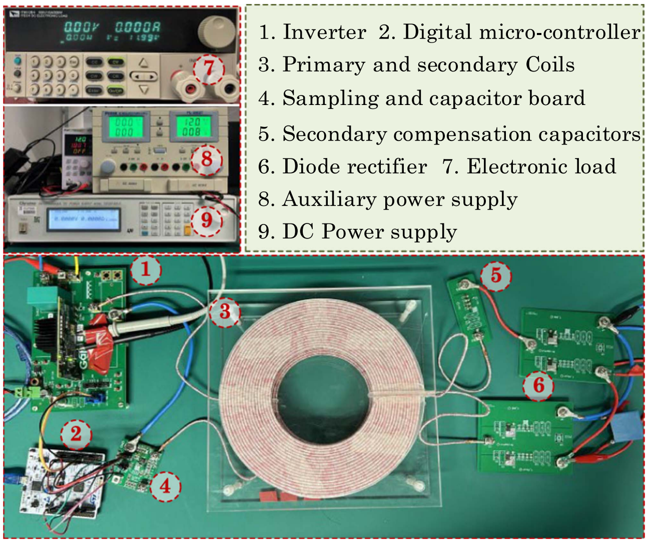


Fig. 19. Experiment setup.

Although differing in configuration, these compensation topologies can be modeled in a unified manner, making them compatible with the proposed method. The SP compensation topology is exemplified as following. While its secondary compensated capacitor is in parallel with the output rectifier, it can be transformed into an equivalent component, named as X_2, which is in series with the output, as shown in Fig. 18. In this transformed state, the SP topology shares identical circuit equations with the SS topology. Therefore, the proposed method is applicable to the SP compensated topology. This conclusion can be generalized to other compensation topologies, provided their equivalent circuits can be transformed into the same canonical form. In this form, the specific topology only determines the values of the equivalent reactance X_1 and X_2.

IV. EXPERIMENTAL VERIFICATION

To verify the feasibility of the proposed estimation method, experimental validation is conducted through a SS compensated WPT prototype with a full-bridge diode rectifier, as shown in Fig. 19. The system specifications are tabulated in Table IV where L_1, L_2, C_1, and C_2 are tested by the LCR meter. The digital platform is the STM32G474RET6, which includes embedded ADC modules. The diode rectifier consists of four Schottky

TABLE IV
SYSTEM SPECIFICATION

Parameters	Symbol	Values
Dc Input voltage	V_{in}	48 V
Output voltage	V_o	12 V
Equivalent Load resistance	R_o	5–15 Ω
Primary capacitor	C_1	58.64 nF
Primary self-inductance	L_1	59.93 μH
Secondary capacitor	C_2	58.50 nF
Secondary self-inductance	L_2	59.91 μH
Coupling coefficient	k	0.188–0.598

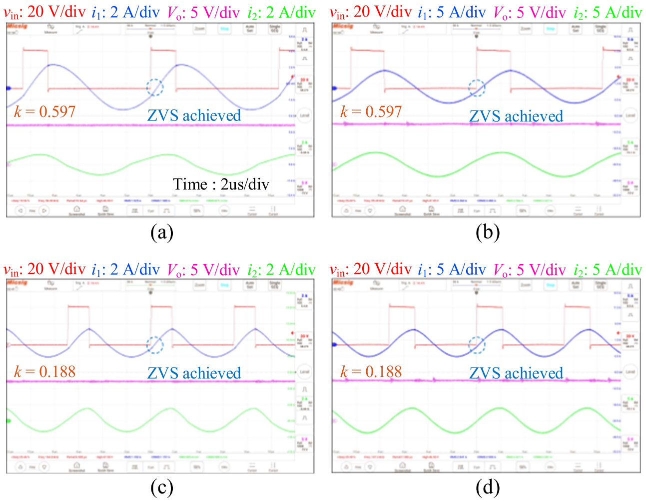


Fig. 20. Steady state waveforms under different coupling and load conditions. The equivalent load resistance 15 Ω. (a) k is 0.598. (c) k is 0.188. The equivalent load resistance 5 Ω. (b) k is 0.598. (d) k is 0.188.

diodes (Model: YQ3RSM10SD). The voltage load is emulated by constant voltage mode of the electronic load.

To better demonstrate the performance in a wide operation range, a variable frequency and phase shifted control is adopted with ZVS and power regulation [33]. As ZVS is achieved throughout the entire operating range, voltage spikes are effectively suppressed at switching instants, preventing interference with the voltage sampling circuit. The steady waveforms under light and heavy load conditions are presented in Fig. 20. The results indicate that ZVS is achieved in the whole operating range.

For each experimental case, 1500 data points were collected through real time estimation conducted in the microcontroller. Corresponding statistical metrics, including the mean error and standard deviation, were calculated to enhance the credibility of the results. As shown in Figs. 21, 22, and 23, the estimated results demonstrate high accuracy with a maximal error of ∼3% for k and ∼5% error for V_o. The minimal standard deviations observed across all cases (each comprising 1500 data points) confirm the high credibility of the obtained results.

The signal-to-noise ratio (SNR) of sampled capacitor voltages decreases under light-load conditions because the sampled capacitor voltage amplitude is typically low when the primary current is small. As a result, the effect of sampling error becomes more pronounced under light-load conditions. Additionally, under weak coupling conditions, the higher turn-OFF current induces larger voltage spikes across stray inductances. This degrades the (SNR), thereby contributing to increased estimation errors. This mechanism is consistent with the trend that estimation accuracy monotonically decreases with the coupling coefficients. To mitigate this effect, good PCB layout design and ADC noise filter are effective approaches.

In practice, Case II occurs less frequently than Case I owing to two main factors: the effective inductive nature of the input impedance of rectifier and the zero-voltage-switching (ZVS) design requirement. The inductive input impedance of diode rectifiers intrinsically lowers the secondary-side resonant frequency.

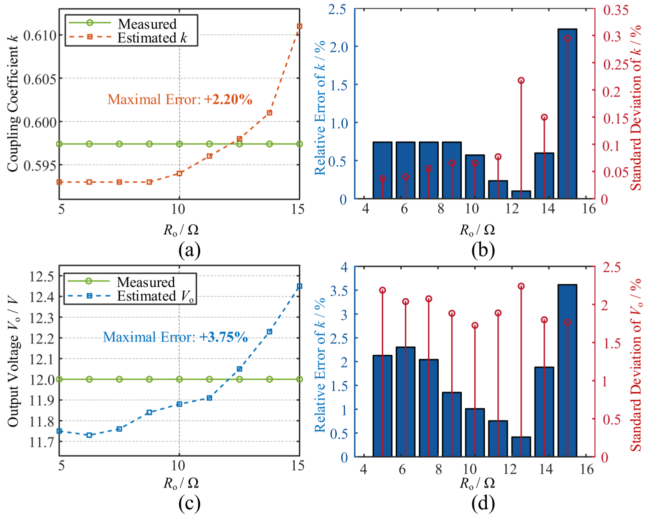


Fig. 21. Estimation results for coupling coefficient and output voltage ($k = 0.598$). (a) Measured versus estimated k. (b) Relative error and standard deviation of k. (c) Measured versus estimated V_o. (d) Relative error and standard deviation of V_o.

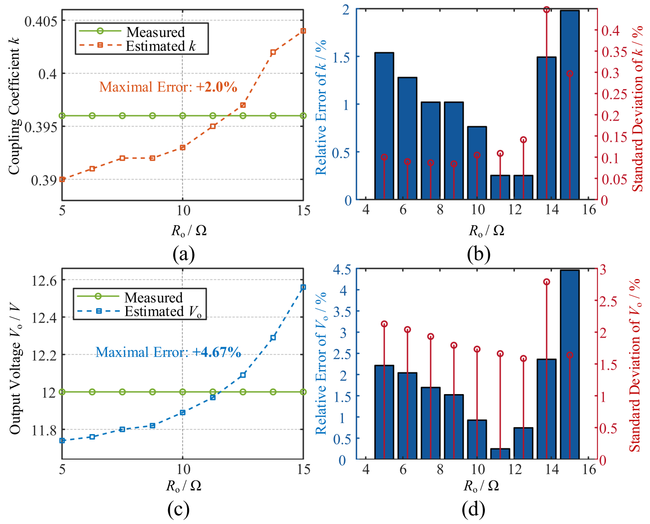
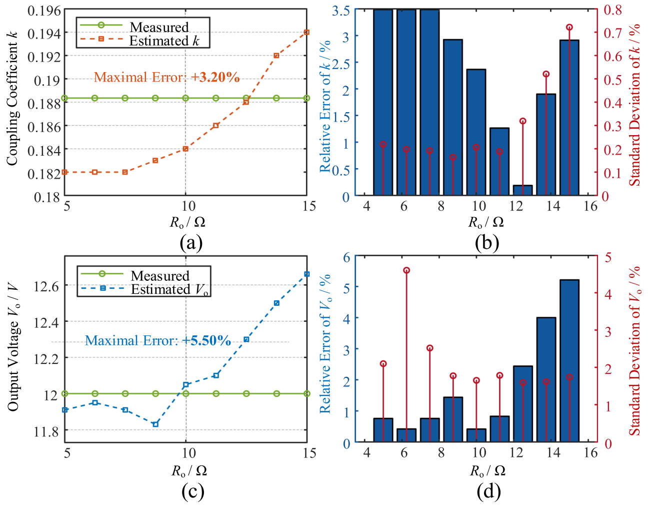
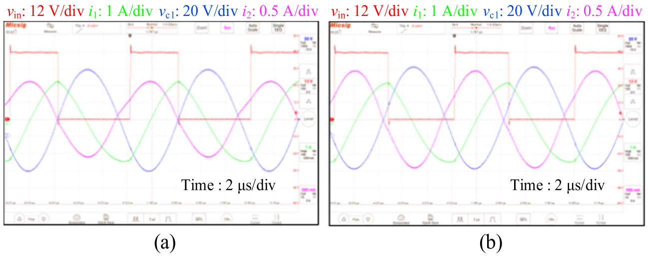


Fig. 22. Estimation results for coupling coefficient and output voltage ($k = 0.396$). (a) Measured versus estimated k. (b) Relative error and standard deviation of k. (c) Measured versus estimated V_o. (d) Relative error and standard deviation of V_o.



(a) (b) (c) (d)

Fig. 23. Estimation results for coupling coefficient and output voltage ($k = 0.188$). (a) Measured versus estimated k. (b) Relative error and standard deviation of k. (c) Measured versus estimated V_o. (d) Relative error and standard deviation of V_o.



(a) (b)

Fig. 24. Key waveforms of the SS compensated topology in Case II. (a) Duty cycle is 0.35. (b) Duty cycle is 0.45.

Moreover, to achieve ZVS, systems are typically designed to operate above the resonant frequency, which fails to satisfy the criterion for Case II. To establish the required operating condition, C_2 was adjusted from 58.5 nF to 39.62 nF. Without this adjustment, operation in Case II would not be attainable across the entire operating range.

In Case II, the secondary side is reflected as a purely resistive impedance on the primary side. Consequently, the secondary current is in phase with the derivative of the primary current, being therefore in antiphase with the primary capacitor voltage. A frequency sweep was conducted to identify the operating points for Case II, after which the proposed method was verified at these points, as shown in Fig. 24. The validation results, shown in Fig. 25, indicate a maximum estimation error of approximately 3%.

The online parameter estimation is evaluated in two cases including dynamic coupling coefficient and dynamic output voltage. The experimental waveforms and the corresponding real time estimation results are presented in Fig. 26. The software STM32CubeMonitor is adopted for logging the estimation results from the registers of microcontroller. When changing the output voltage setting from 12 V to 10 V and to 14 V, the estimated output voltage rapidly tracks these changes while the estimated coupling coefficient remains stable. When changing the coupling coefficient from 0.58 to 0.18, the estimated coupling coefficient follows the variation of k immediately while the estimated voltage maintains close agreement with the actual output voltage throughout the transient period.

Videos are also attached in the supplementary material to demonstrate the effectiveness of the proposed method. The graphic user interface designed in STM32CubeMonitor display the estimation results and other control variables including duty cycle, working frequency, and power reference in real-time. Video 1 demonstrates the dynamic response under a varying k. While the receiver coil is manually displaced, the estimated V_o maintains stability, and the estimated k promptly tracks the changes in coupling. Video 2 demonstrates the dynamic response to changes in output voltage. While adjusting the electric load

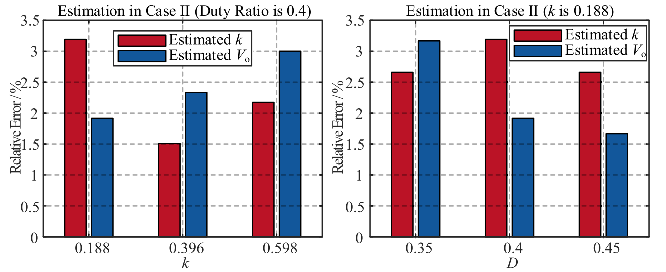
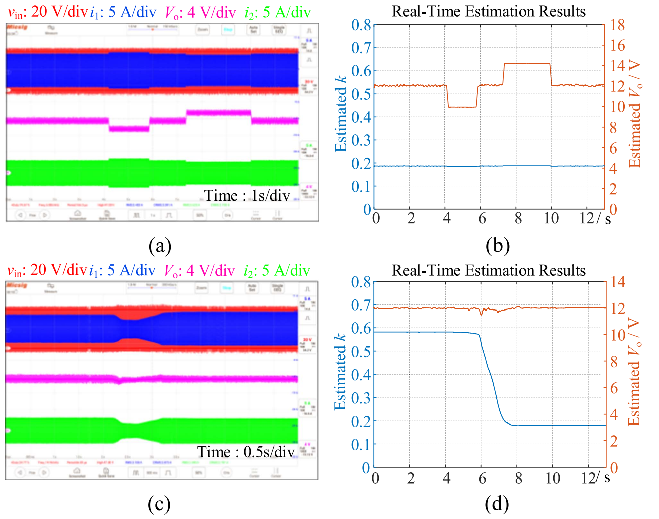


Fig. 25. Estimation results for coupling coefficient and output voltage in Case II.



(a) (b) (c) (d)

Fig. 26. Online estimation results and experimental waveforms. Changing V_o: (a) experimental waveforms and (b) estimation results. Changing k: (c) experimental waveforms and (d) estimation results.

TABLE V
COMPUTATIONAL RESOURCE UTILIZATION OF PROPOSED METHOD

Item	Utilization	Measurement Method
Estimation Time	~131 μs	SysTick timer-based Calculation
RAM Consumption	2.9 KB	Memory map analysis in IDE (STM32CubeIDE)
Flash Consumption	45.33 KB	Memory map analysis in IDE (STM32CubeIDE)

TABLE VI
COMPARISON WITH OTHER ESTIMATION METHODS

Ref.	Range of k	Range of V_o and R_o	Maximal Errors: k	Maximal Errors: V_o	Online	Execution Time	Computational Complexity	Additional Hardware	Communication Free	Sampling Rate	No Impact on System
[8]	0.24	600 V 36 Ω–360 Ω	7 %	6.7 %[1]	☑	~7 ms	Simple	No	☒	Low	☒
[9]	0.18–0.26	60 V 12 Ω–25 Ω	3.38 %	4.82 %[1]	☑	2-5 s	Complex	No	☑	High	☑
[11]	0.15–0.31	25 V–30 V /	3.5 %	7 % (2.1 V)*	☑	/	Medium	Magnetic Ring	☑	High	☑
[12]	0.10–0.19	3.6 V–4.2 V 2.2 Ω–2.5 Ω	3 %	NA	☑	16 ms	Medium	Voltage Clipper	☑	Low	☒
[14]	0.22–0.35	200 V 50 Ω–200 Ω	3 %	NA	☒	3.6 s	Simple	No	☒	Low	☒
[15]	0.2–0.6	/	1.75 %	NA	☒	<11 ms	Simple	No	☑	Low	☒
[17]	0.3–0.62	100 V /	5 %	NA	☑	150 µs	Medium	No	☑	High	☑
[19]	0.2–0.34	66 V 1.6 Ω–3.5 Ω	5.1 %	3.6 %[1]	☑	37.3 ms	Medium	No	☑	High	☑
This article	0.19–0.59	12 V 5 Ω–15 Ω	3.2 %	5.5 % (0.66 V)*	☑	~131 µs	Simple	No	☑	Low	☑

1: The error is for the load resistance. 2: The symbol "*" denotes the absolute error value. 3: The symbol '/' denotes that the specific data is not provided in the reference. 4: NA represents output voltage estimation is not available in this reference.

to different voltage levels, the estimated k remains stable, and the estimated V_o accurately tracks the set variations.

The estimation time and resources utilized for the proposed method are tabulated in Table V. The single estimation process is completed in approximately 131 μs as measured by reading the SysTick register. This result verifies the real-time and feasibility of the proposed method.

To highlight the advantages of the proposed method, the comparison with prior works including computational complexity and estimation time is conducted in Table VI. Compared to other approaches, the proposed method ensures fast real-time estimation within submilliseconds. Moreover, only low sampling rate is required in the proposed method, which significantly relief storage needs as well as cost of high performance ADC module. Since the estimation results are obtained by solving a quadratic equation, the computational overhead is low compared to other complex operations such as FFT. Critically, this method has no impact on system operation, allowing seamless integration into existing systems. For applications with stricter dynamic response requirements, a more advanced controller platform can be employed. For instance, the STM32H7 series microcontroller whose core frequency is up to 480 MHz, could reduce the calculation time by a factor of 2.8.

V. CONCLUSION

A real-time parameter estimation method for the SS compensated topology is presented in this article. Unlike traditional methods that model the input impedance of diode rectifier as a purely resistive load, a more accurate inductive rectifier. Based on the derived model, the real-time estimation method is presented in detail with a simple primary side voltage sampling. The feasibility of the proposed method is verified experimentally in a wide coupling range from 0.188 to 0.598. Experimental results demonstrate that the proposed method achieves high-accuracy estimation of both the coupling coefficient and output voltage, with a very short response time of 131 μs. Critically, it requires no prior calibration or bilateral communication, and its zero interference with normal system operation ensures seamless integration into existing WPT systems.

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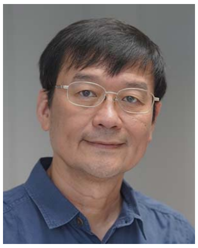

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