Output Capacitance Extraction of *p*-GaN HEMTs Under Multi Pulse Switching Across Variable Frequencies and Drain-Bias Stress

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***Abstract*—This article proposes a method to extract the output capacitance (C_{OSS}) of 200 V Schottky *p*-GaN high-electron-mobility transistor under multipulse switching conditions. By employing a gate-source shorted configuration, both C_{GD} and C_{DS} are captured during switching transients. To minimize ringing oscillations, a four-layer printed circuit board with low parasitic inductance was designed, along with a top-cooled heat sink to enhance thermal management. The results under various switching frequencies and OFF-state V_{DS} biases reveal that C_{OSS} variations arise from the combined effects of V_{DS}-induced electron trapping during the OFF-state and hole injection during reverse conduction. The extraction method and findings contribute to the accurate evaluation of C_{OSS} in multipulse switching applications and aid in the design of power converters and the switching performance prediction of gallium nitride power devices.**

***Index Terms*—Hole injection, multipulse test, OFF-state V_{DS} bias stress, output capacitance (C_{OSS}), Schottky-type p-gallium nitride (GaN) gate high-electron mobility transistor (HEMT).**

I. Introduction

GALLIUM nitride (GaN) high-electron-mobility transistors (HEMTs) have attracted considerable interest due to their superior performance [1], [2], [3]. The *p*-GaN HEMTs, which feature a *p*-GaN gate structure to achieve enhancement-mode operation, are particularly noteworthy [4], [5]. The *p*-GaN HEMTs have been commercialized across a wide voltage rating from 100 to 650 V and show great potential in power supplies for consumer electronics, data centers, electrical vehicles, and renewable energy systems, etc. However, further investigations are still needed to fully leverage the advantages of *p*-GaN HEMTs in power applications, particularly under switching conditions.

One of the crucial challenges is accurately extracting the output capacitance (C_{OSS}). C_{OSS} directly influences switching losses by discharging stored charges during the transition from OFF-state to ON-state, especially at high switching frequencies [6], [7]. In addition, the drain-bias-induced trapping processes in buffer or barrier layers further complicates the behavior of C_{OSS}, making precise extraction more challenging. Therefore, a dynamic evaluation of C_{OSS} is essential for accurate switching performance prediction and power circuits design.

Various methods have been employed to characterize the C_{OSS} of GaN HEMTs, including small-signal measurements [8], the Sawyer–Tower method [9], nonlinear resonance in unclamped inductive switching (UIS) $*$circuits [10], and the half-bridge no-load circuit method [11], [12], [13], [14]. However, these approaches have significant limitations: either the testing conditions stem from nonswitching scenarios, or the gate to drain capacitance (C_{GD}) and gate charge (Q_G) are not considered. These limitations lead to inaccurate C_{OSS} extraction derived from switching energy losses. A recent study [15] introduced a test platform with an auxiliary switch to extract dynamic E_{OSS} losses under hard-switching conditions. However, this method still neglects the C_{GD} component and voltage-current (*V–I*) overlap losses, leading to inaccurate estimation of C_{OSS}. Therefore, testing methods for C_{OSS} under switching conditions still require further research and improvement.

In this article, we propose a method for extracting the C_{OSS} of GaN HEMTs in multi pulse tests under different switching frequencies and OFF-state V_{DS} stress conditions. The gate and source of the high-side GaN device are shorted to simultaneously charge the C_{GD} and drain-source capacitance (C_{DS}), ensuring that both C_{GD} and C_{DS} are captured. Additionally, SPICE simulations are employed to subtract the *V–I* overlap losses from Q_G versus gate-source voltage (V_{GS}) curve. This test enables accurate evaluation of the C_{OSS} of the high-side GaN device during the turn-ON switching transient of the low-side device

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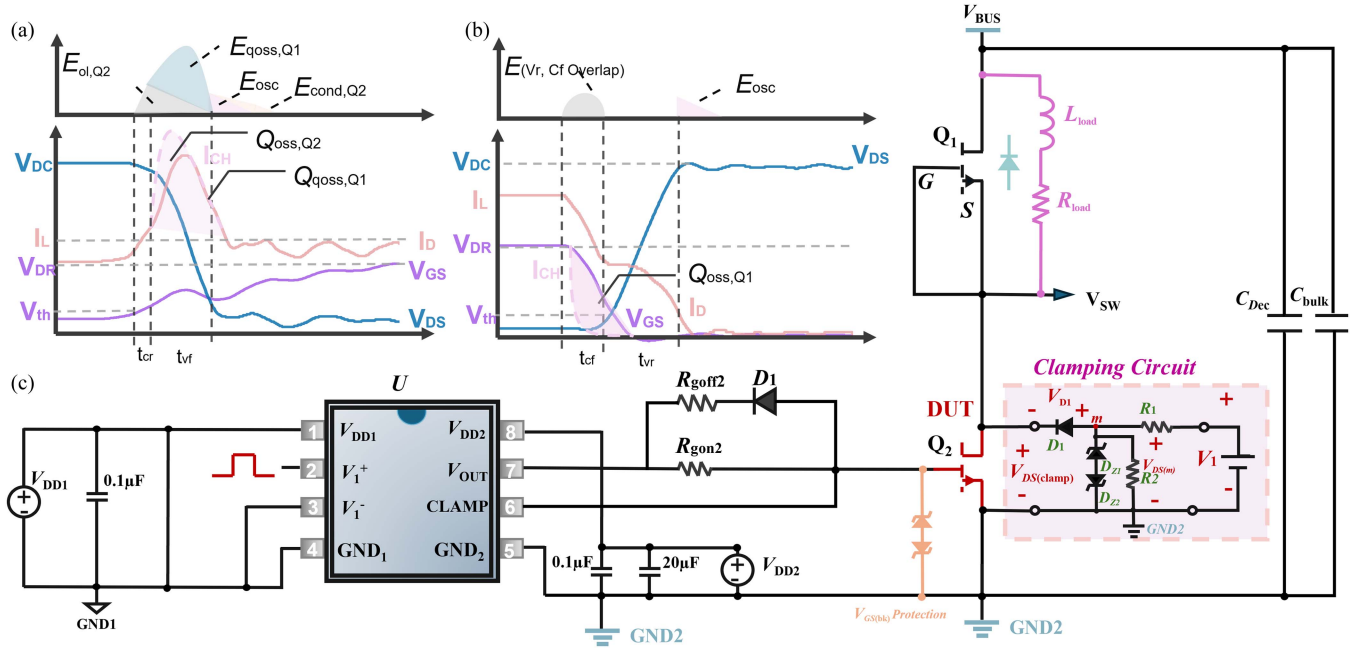

Fig. 1. (a) Switching-ON. (b) Switching-OFF transient waveforms illustrating C_{OSS} energy losses. (c) Multipulse test circuit topology with gate and source of Q_1 shorted for hard-switching C_{OSS} extraction, including a clamping circuit for $R_{DS(ON)}$ characterization.

under multipulse test conditions. This method is demonstrated on commercial 200 V Schottky *p*-GaN HEMTs [16], which features a *p*-GaN gate to achieve enhancement mode normally-OFF operation. The dynamic behavior of C_{OSS} is investigated by comparing the C_{OSS} extracted from distinct pulses (1st, 8th, and 15th) under various switching frequencies (100, 150, 250, and 400 kHz) and V_{DS} biases. Based on experimental results, this article analyzes the mechanisms influencing C_{OSS} variations under pulsed switching conditions, including OFF-state V_{DS} induced charge trapping and hole injections during reverse conduction. Given the significant impacts of C_{OSS} on switching-transient characteristics, this article assists in accurately evaluating and predicting GaN power-device switching performance and outlines design considerations—using dynamic $C_{OSS}(V_{DS}, f_{SW})$ in place of static values for loss estimation and soft-switching margin assessment—to guide GaN power-circuit design.

The rest of this article is organized as follows: Section II describes the extraction techniques for C_{OSS}, the design of the switching circuit, PCB layout, and experimental settings. Section III extracts and analyzes the dynamic C_{OSS} of GaN HEMTs under different switching frequencies and OFF-state V_{DS} stress conditions. Section IV summarizes the findings and contributions of this article. Finally, Section V concludes this article.

II. Multipulse Switching C_{OSS} Extraction Design

A. Proposed Testing Circuit Design and Methodology

Traditional half-bridge circuits can capture capacitive energies during the turn-ON transition [17]. However, this approach presents inherent limitations. During the turn-ON transition, the potential difference between the gate and source makes it difficult to measure C_{RSS} (reverse transfer capacitance) in multipulse switching circuits, leading to inaccuracies in the extraction of C_{OSS}. Conventional half-bridge double pulse test setups typically utilize either a diode-based top device or an actively switched configuration. The diode-based method cannot directly measure active-switch C_{OSS} and therefore requires an auxiliary commutation loop to route the discharge through the active switch [15], [18]. Active-switch configurations add complexity through precise dead-time control requirements and gate-driver-induced oscillations, significantly obscuring accurate measurement of capacitive losses [19].

In this article, we use the modified half-bridge topology to address these issues shown in Fig. 1(c). Shorting the gate and source of the upper switch (Q_1) turns it into a reverse-conducting GaN Schottky-barrier diode. The lower switch (Q_2) is actively switched, enabling output capacitance extraction of Q_1 ($C_{OSS,Q1}$) through Q_2's turn-ON transient. This configuration enables the accurate extraction of dynamic C_{OSS} by accounting for both C_{GD} and C_{DS}. The simplified layout makes minimizing parasitic inductances easier, thereby reducing deviations in switching-loss measurements. The lower switch Q_2 is actively controlled, whereas Q_1 operates with its gate connected to the source to provide a reverse-conduction path. An isolated gate driver (ADUM4121A) is utilized to isolate signal and power grounds, further improving measurement reliability. Decoupling capacitors are implemented to mitigate parasitic effects, and back-to-back configured Zener diodes are connected across the gate-source terminals of Q_2 to protect against gate voltage overshoot. A clamping circuit is incorporated to assist precise measurement of the ON-state resistance of the lower switch [20], [21], [22].

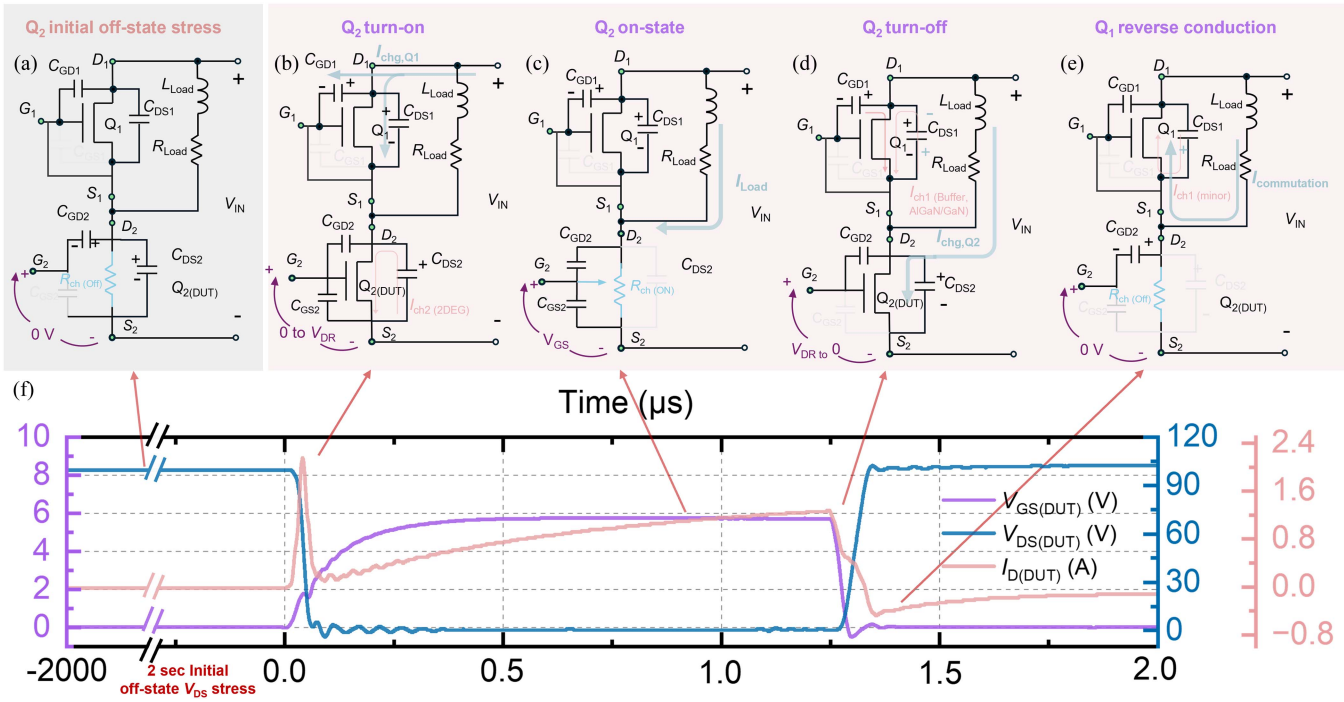

Fig. 2. Operation states of the proposed half-bridge circuit. (a) Initial OFF-stress period. (b) Q_2 turn-ON transient. (c) Q_2 ON-state. (d) Q_2 turn-OFF transient. (e) Q_2 OFF-state with Q_1 reverse conduction. (f) Corresponding measured switching waveforms of $V_{\mathrm{GS(DUT)}}$, $V_{\mathrm{DS(DUT)}}$, and $I_{\mathrm{D(DUT)}}$ showing the dynamic evolution across phases (a)–(e).

The detailed operating stages of the proposed testing circuit are illustrated in Fig. 2. As shown, five fundamental transient phases are involved.

1) Before the pulsewidth modulation (PWM) operation starts, an initial OFF-state stress (∼2 s) is applied to Q_2 to precondition traps in the buffer and barrier layers.
2) When Q_2 is turned ON, C_{DS2} discharges through its 2DEG channel, and simultaneously C_{DS1} and C_{GD1} of Q_1 charge through the commutation path, enabling dynamic extraction of $C_{\mathrm{OSS},\,Q1}$.
3) In the conduction phase, the capacitances remain constant and the load current flows steadily through Q_2.
4) During turn-OFF, the load current begins charging C_{DS2} of Q_2, while C_{DS1} and C_{GD1} of Q_1 discharge, including a small forward leakage in Q_1.
5) Once C_{DS2} is fully charged, $V_{\mathrm{DS},\,Q1}$ becomes slightly negative, and the inductor current commutates to Q_1 through its 2DEG conduction path.

This reverse-conduction interval continues until the full load current is transferred from Q_2 to Q_1. Because the inductor current does not decay to zero within one switching cycle, a small negative current remains at the beginning of the subsequent Q_2 turn-ON, resulting in the nonzero initial $I_{D,Q2}$ observed in later pulses. Fig. 2(f) shows the measured $V_{\mathrm{GS}(\,Q2)}$, $V_{\mathrm{DS}(\,Q2)}$, and $I_{\mathrm{D}(\,Q2)}$ waveforms at 100 V and 400 kHz, encompassing all stages (a–e). The clean switching transitions demonstrate optimized PCB layout and minimized parasitic inductance.

In the proposed method, the upper-switch capacitive energy is extracted during the lower-switch switching-ON transient. Over this interval, the total switching energy comprises voltage–current overlap losses ($E_{ol,\,Q2}$), upper-switch capacitive charging energy ($E_{q\mathrm{OSS},\,Q1}$), oscillation-related losses (E_{OSC}), and self-discharge losses of lower switch ($E_{\mathrm{OSS},\,Q2}$). The self-discharge component cannot be captured by the oscilloscope because the lower-switch C_{OSS} energy dissipates through the device channel. As depicted in Fig. 1(a), switching-ON energy loss of Q_2 is obtained by integrating $V_{\mathrm{DS},\,Q2}(\mathrm{t})$ and $I_{D,\,Q2}(t)$ under multipulse switching conditions.

In accordance with JEDEC JEP200 and IEC 60747, the integration interval spans the 10% –90% portion of the transition, thereby excluding posttransition ringing. These standards specify that the $V_{\mathrm{DS},\,Q2}(t)$ $I_{D,\,Q2}(t)$ integral begins when the drain current of Q_2 first reaches 10 % of its peak value (t_1) and ends when the drain-source voltage falls to 90 % of its initial value (t_2) [23]. The $I^2R_{\mathrm{DS(ON)}}$ conduction tail occurring after t_2, which is typically $< 3\%$ due to the intrinsic device V_{DS} fall during turn-ON. Parasitic oscillation losses are limited to ≤ 5 % by the optimized four-layer PCB design (see Section II-B). Therefore, the capacitive energy of the upper switch, $E_{q\mathrm{OSS},\,Q1}$, is obtained from the Q_2 turn-ON measurement, as given in

$$E_{\mathrm{on},Q_2} = \int_{t_1}^{t_2} V_{DS,Q_2}\,(t)\; I_{D,Q_2}\,(t)\; dt \;= E_{ol,Q_2} \;+ E_{q\mathrm{OSS},Q_1}. \tag{1}$$

Within this interval, only two measurable terms remain: $E_{ol,\,Q2}$, and the displacement-current energy required to charge C_{OSS} of Q_1. Section II-C quantifies $E_{ol,\,Q2}$ using LTSpice, after which (1) is used to obtain $E_{q\mathrm{OSS},\,Q1}$ and estimate $C_{\mathrm{OSS},\,Q1}$ [24], [25], [26]. Notably, to bias the energy balance toward the capacitive term during measurement, the R–L load is set

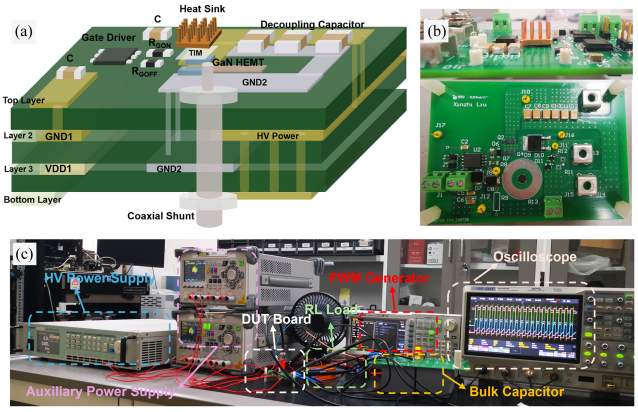

Fig. 3. (a) Schematic of the proposed copper heat sink design for enhanced thermal management. (b) Cross-sectional and top view of the four-layer PCB with heat sink. (c) Experimental setup for C_{OSS} extraction.

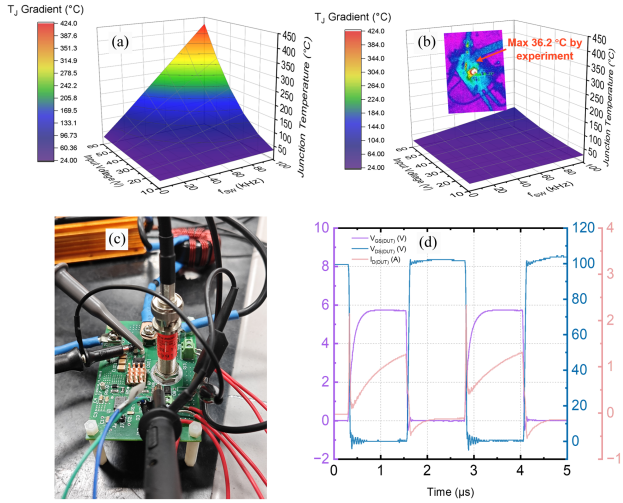

Fig. 4. Simulated junction temperature of DUT (a) without and (b) with the customized top-mounted heat sink. Inset of (b): infrared thermography showing a maximum surface temperature of 36.2°C during tests. (c) Experimental setup with four-layer PCB, SSDN-10 coaxial shunt, high-voltage differential probe for $V_{\mathrm{DS},\,Q2}$, and passive probe for $V_{\mathrm{GS},\,Q2}$. (d) Measured $V_{\mathrm{GS},\,Q2}$, $V_{\mathrm{DS},\,Q2}$, and $I_{D,\,Q2}$ waveforms at 100 V and 400 kHz, demonstrating stable switching with reduced parasitic effects enabled by the optimized PCB layout.

to 30 Ω/26 μH, limiting $I_{D,\,Q2} < 2$ A; since $E_{ol,\,Q2}$ scales with load current, this suppression ensures that $E_{q\mathrm{OSS},\,Q1}$ contributes ≈70% –80% of $E_{\mathrm{on},\,Q2}$.

B. Optimized Four-Layer PCB Design and Experimental Hardware Setup

To practically implement the proposed measurement methodology, the hardware setup based on an optimized PCB layout was developed. A four-layer PCB configuration with vertically interconnected copper layers was employed ([see Fig. 3(a) and (b)]) to minimize parasitic inductances. Reduced parasitic inductance mitigates ringing oscillations, resulting in more precise switching waveforms and improved accuracy in dynamic C_{OSS} extraction under high-frequency switching conditions [27], [28]. Given the DUT is a 200 V top-cooled GaN HEMT with a land-grid-array package (1.6-mm width), thermal management was also prioritized [29]. A compact customized heat sink (1.5 cm × 1.5 cm), attached directly to the DUT through a thermal interface material, ensures effective heat dissipation despite limited PCB space due to the coaxial current-shunt layout.

Fig. 3(c) illustrates the multipulse experimental setup for dynamic C_{OSS} extraction. While load conditions affect transient behavior, the selected load limits the Q_2 current and reduces current-overlap energy, yielding controlled, repeatable transitions on the optimized four-layer PCB. Experimental testing employs a programmable high-voltage dc supply (Faith FTP032-1500-3.5) to provide the input V_{IN}, a linear dc supply (RIGOL DP832A) for the gate driver bias, and a PWM signal generator (RIGOL DG5072) to control the pulse timing. Switching waveforms were captured using a 500 MHz, 5 GSa/s digital oscilloscope (SIGLENT SDS5054X) operated at full bandwidth to accurately resolve high-speed transients. $V_{\mathrm{DS},\,Q2}(t)$ was measured by a high-voltage differential probe (SIGLENT DPB-HVP-7030A) connected in a Kelvin configuration directly to the drain and source pads of Q_2. $I_{D,\,Q2}(t)$ was sensed through a coaxial shunt (SSDN-10, 10 mΩ, >200 MHz bandwidth) inserted in the source return of Q_2 with four-terminal sensing; the measured source current was inverted in sign to obtain I_D. For low-voltage V_{GS} nodes, passive probes (RIGOL PVP2350) with ground-spring terminations were employed to minimize loop inductance and ringing. All voltage and current channels were subjected to precise time alignment to ensure accurate *V–I* correlation during energy evaluation.

Fig. 4 summarizes the validation of measurement accuracy and thermal stability of the proposed setup. Fig. 4(a) shows the SPICE-assisted thermal simulation of EPC2215 junction temperature without a heat sink under varying switching frequency and input voltage. Fig. 4(b) presents the corresponding simulation with the customized heat sink together with the infrared thermography measured during the experiment, confirming a maximum surface temperature of 36.2°C. Fig. 4(c) illustrates the experimental arrangement using a four-layer PCB with coaxial shunt and differential probing. Representative waveforms in Fig. 4(d) demonstrate stable operation at 100 V and 400 kHz with minimized parasitic effects, verifying that the setup provides reliable switching data for subsequent C_{OSS} extraction.

C. SPICE-Based V–I *Overlap Loss Subtraction and Final C_{OSS} Extraction*

As described in Section II-A, accurate extraction of $C_{\mathrm{OSS},\,Q1}$ requires subtracting the *V–I* overlap loss of the lower switch, $E_{ol,\,Q2}$, from the measured energy given by (1). The overall extraction framework is summarized in Fig. 5, which outlines a four-step process for dynamic C_{OSS} evaluation under switching conditions. Step 1 and step 2 were detailed in Sections II-A and II-B, covering waveform acquisition and ON-switching energy calculation. Step 3 and step 4 focus on *V–I* overlap loss subtraction and final C_{OSS} derivation. To quantify and remove these overlap losses, device-specific gate-charge characteristics

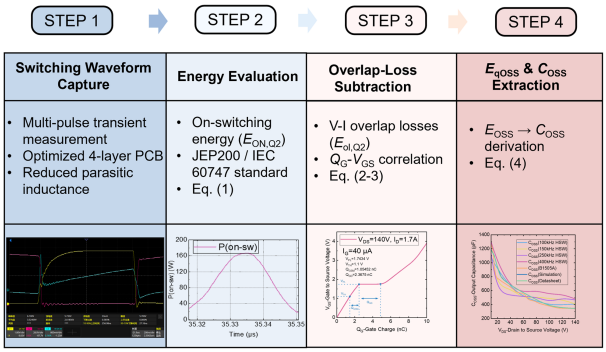

Fig. 5. Flowchart of the proposed dynamic C_{OSS} extraction under hard-switching. The process includes waveform acquisition, ON-switching energy evaluation per JEP200/IEC 60747, *V–I* overlap loss subtraction via Q_G–V_{GS} correlation, and final C_{OSS} derivation from the measured switching energy.

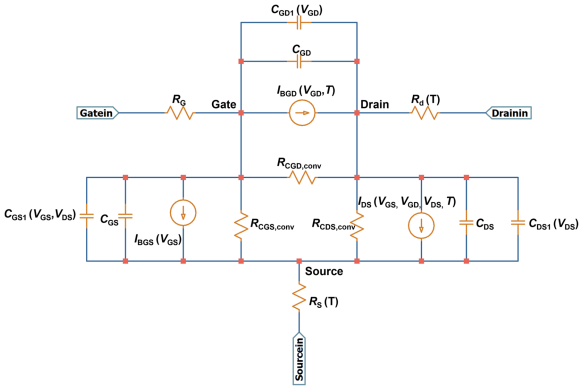

Fig. 6. Semi-empirical SPICE model of the EPC2215 schottky p-GaN HEMT for Q_G–V_{GS} and dynamic C_{OSS} evaluation, combining fitted and physics-inspired parameters: nonlinear charge-controlled capacitances (C_{GS1}, C_{GD1}, C_{DS1}), temperature-dependent resistors [$R_D(T)$, $R_S(T)$], convergence resistors, Schottky leakage diodes (I_{BGS}, I_{BGD}), and voltage -coupled current source (I_{DS} (V_{GS}, V_{GD}, V_{DS}, T)) [16].

(Q_G–V_{GS}) were simulated using the EPC2215 Level-3 SPICE model [16], as illustrated in Fig. 6.

In Schottky p-GaN HEMTs, overlap losses arise from concurrent *dv/dt* and *di/dt* transitions during the Miller plateau. The magnitude of these losses depends on the gate-charge distribution and the effective gate resistance. Two equivalent formulations are used for their quantification: in the time-domain approach, the overlap interval is modeled as two energy trapezoids—one during the drain-current rise ($E_{cr,Q2}$) and the other during the drain-voltage fall ($E_{vf,Q2}$)—expressed in (2) and in the charge-domain approach, substituting $t = \Delta Q/I_G$ with gate currents determined by plateau voltages yields (3)

$$E_{ol,Q_2} = E_{cr,Q_2} + E_{vf,Q_2} = \frac{1}{2} V_{DS,Q_2} I_{D,Q_2} \left(t_{cr,ON,Q_2} + t_{vf,ON,Q_2}\right) \quad (2)$$

$$E_{ol,Q_2} = \frac{1}{2} V_{DS,Q_2} I_{D,Q_2} \left(\frac{Q_{GSM}}{\frac{V_{DR}-\left(\frac{V_{PL}+V_{TH}}{2}\right)}{R_{gon2}}} + \frac{Q_{GD}}{\frac{V_{DR}-V_{PL}}{R_{gon2}}} \right). \quad (3)$$

TABLE I
TEST PARAMETERS FOR THE PROPOSED C_{OSS} EXTRACTION

Parameters	Values	Comments
DC Input Voltage V_{IN}	10 V, 20 V, 40 V, 60 V, 80 V, 100 V, 120 V, and 140 V	Eight step-up points per condition; 20 min rest between voltage steps for thermal/trap recovery.
Load resistance R_{load}	30 Ω	Limits I_D < 2 A at V_{DS}=140 V (≈1.7 A), supressing $E_{ol,Q2}$ and biasing toward $E_{qOSS,Q1}$
Load Inductance L_{load}	26 µH	Sets *di/dt* and stabilizes current; with 30 Ω yields controlled, repeatable transients on the 4-layer PCB.
Switching frequency f_{SW}	100, 150, 250, 400 kHz	Each voltage tests 4 frequencies, 20 min recovery time
PWM input	3.5 V, 50% DC	Logic-level drive to the gate driver (input). Duty cycle=50%
Gate Voltage V_{GS}	6 V	Driver output to Q_2 (active device).
Initial off-state V_{DS} stress	2 s	Apply once per (V_{IN}, *fsw*) condition before acquisition to establish trap occupancy (affects pulse #1).
Recorded pulses per test	20	$C_{OSS,Q1}$ extracted at pulse 1, 8, 15
Integration interval	JEDEC JEP200 / IEC 60747 10–90%	Excludes post-transition ringing and $I^2R_{DS(ON)}$ tail; residual ringing ⩽ 5% with the optimized 4-layer layout (see Section II-B).

Here, Q_{GSM} and Q_{GD} represent the gate-source Miller charge and gate-drain charge; V_{PL} is the Miller plateau voltage, V_{TH} is the threshold voltage, V_{DR} is the drain reference voltage at the onset of the Miller plateau, and R_{gon2} denotes the effective ON-state gate resistance of active switch Q_2 [7]. The required Q_G–V_{GS} data were obtained from SPICE simulations utilizing an empirically fitted level-3 model for the EPC2215 device [16]. The simulation parameters for $I_{D,Q2}$ and $V_{DS,Q2}$ were aligned with experimental conditions. Eight sets of Q_G–V_{GS} curves were simulated corresponding to the experimental testing conditions given in Table I. Substituting these values into the charge-domain expression gives $E_{ol,Q2}$, which is then subtracted from the integral in (1) to obtain the final dynamic $E_{qQSS,Q1}$. Therefore, the remaining capacitive energy component corresponds to the charge-discharge transition of $C_{OSS,Q1}$ is obtained from the extracted switching energy using

$$C_{OSS,Q1} = \frac{2E_{qOSS,Q1}}{(V_{DS,Q2})^2} = \frac{2\left(E_{on,Q2} - E_{ol,Q2}\right)}{(V_{DS,Q2})^2}. \quad (4)$$

However, discrepancies exist between the simulated curves and real-world dynamic conditions, particularly under multipulse test scenarios. OFF-state V_{DS} stress widens the depletion region, altering C_{GD} and the associated Q_G–V_{GS} curve.

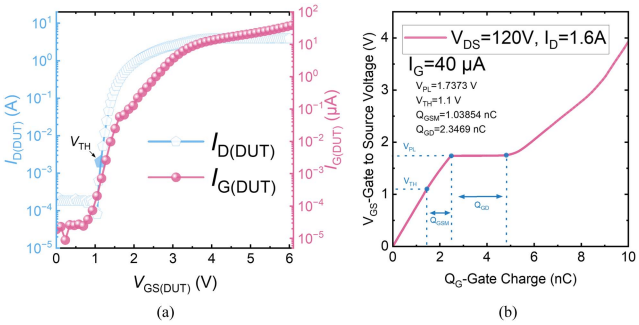

Fig. 7. (a) Transfer characteristics of the 200 V p-GaN HEMT, measured using the B1506 HC module with a test current compliance to 4 A under $V_{\mathrm{DS}} = 5$ V. (b) Simulated Q_G-V_{GS} curves generated with $I_G = 40$ μA under $V_{\mathrm{DS}} = 120$ V, $I_D = 1.6$ A.

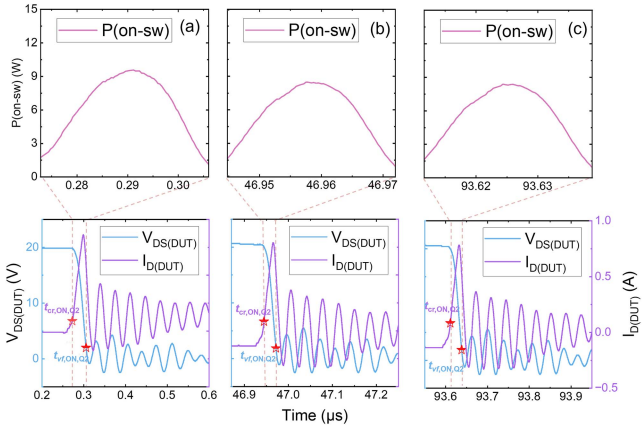

Fig. 8. Extraction of $E_{q\mathrm{OSS},Q1}$ losses at $f_{\mathrm{sw}} = 150$ kHz and $V_{\mathrm{IN}} = 20$ V for the (a) 1st pulse, (b) 8th pulse, and (c) 15th pulse.

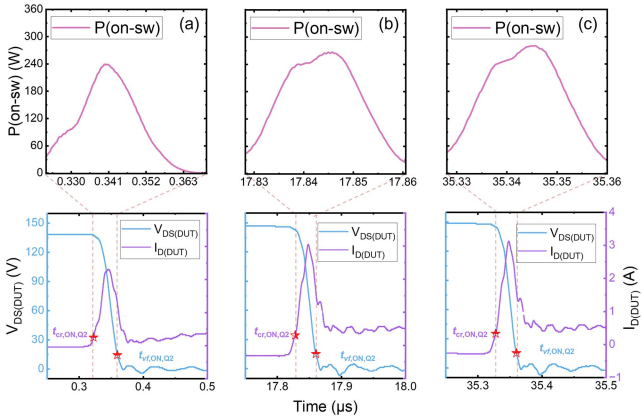

Fig. 9. Extraction of $E_{q\mathrm{OSS},Q1}$ losses at $f_{\mathrm{sw}} = 400$ kHz and $V_{\mathrm{IN}} = 140$ V for the (a) 1st pulse, (b) 8th pulse, and (c) 15th pulse.

Dynamic variations in V_{TH} also impact the Q_G–V_{GS} characteristics [30]. Xu et al. [31] further indicates that a diminished reverse-transfer capacitance (C_{RSS}) can significantly reduce the observable Miller plateau, contributing additional discrepancies. To minimize these SPICE-simulation-related uncertainties, a higher value 30 Ω load resistor was chosen to inherently reduce *V–I* overlap losses. The simulation method explicitly considered three key variables: V_{DS}, I_D (as a dependent load), and gate current (I_G). The simulated I_G was set consistent with measured gate currents during actual switching, while the selections of I_D and V_{DS} were matched to the corresponding multipulse switching test values. To measure the I_G and V_{TH} of the DUT under actual operating conditions, a B1506 device analyzer was used to test the high-current (HC) transfer characteristics of GaN devices. The V_{TH} was defined as the V_{GS} when I_D reached 10 mA. As shown in Fig. 7(a), measured V_{TH} under high-voltage conditions was 1.1 V, and typical I_G was around 40 μA. These experimentally derived parameters were incorporated into the SPICE simulation for precise characterization.

Fig. 7(b) presents an example simulated Q_G–V_{GS} curve obtained at $V_{\mathrm{DS},Q2} = 120$ V and $I_{D,Q2} = 1.6$ A, representing one of the eight simulated operating points. The current level was aligned with the experimentally measured RMS current and showed negligible variation across switching frequencies, indicating stable loading. Data were evaluated using the integration interval defined in Section II-A [23].

III. Results and Discussion

Section III presents experimental evaluation of the proposed dynamic $C_{\mathrm{OSS},Q1}$ extraction technique. This section analyzes the extracted C_{OSS} under dynamic switching conditions across various input voltages (V_{IN}) and frequencies, together with the associated physical mechanisms. By combining the modified half-bridge topology, the optimized four-layer PCB layout, and SPICE-based *V–I* overlap subtraction presented in Section II, dynamic $C_{\mathrm{OSS},Q1}$ can be experimentally extracted from the measured switching energy. The experimental parameters, including switching frequencies, are summarized in Table I. Before each test condition, a 20-minzero-bias recovery was performed with $V_{\mathrm{DS},Q2} = 0$ V and $V_{\mathrm{GS},Q2} = 0$ V to neutralize gate-stack and buffer traps, allowing the 2DEG channel to stabilize for repeatable measurements. After stabilization, 20 pulses were recorded at drain voltages of 10–140 V. Tests were also conducted at various frequencies from 100 to 400 kHz to examine the impacts of switching frequency on C_{OSS}. This range aligns with those used in current GaN-based converters [32], [33], and the 400 kHz upper limit was set to ensure accurate and stable transient capture using the optimized PCB test board. No nonrecoverable device degradation was observed throughout the entire experiment.

A. Hard-Switching C_{OSS} Characterization With Capacitive Losses Analysis

As given in Table I, the experiments were conducted at four switching frequencies and eight different input voltage levels. For each condition, multiple pulse tests were performed, extracting the first, eighth, and fifteenth pulses for $C_{\mathrm{OSS,Q1}}$ comparison. Figs. 8 and 9 present typical waveforms under various operating situations. As shown in Figs. 8 and 9, the eighth and fifteenth pulses exhibit a small negative initial $I_{D,Q2}$ due to the prior reverse-conduction interval of Q_1. This residual current does not influence the calculation of ON-switching energy, since the integration starts at t_1 when $I_{D,Q2}$ crosses zero. Once $I_{D,Q2}$

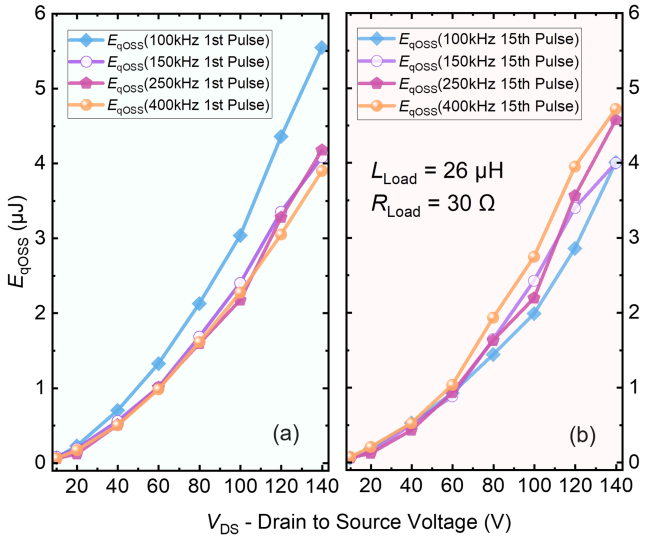

Fig. 10. Energy stored in $C_{OSS,Q1}$ during switching-on transient ($E_{qOSS,Q1}$) under OFF-state V_{DS} bias stress and various frequencies for the (a) 1st pulse and (b) 15th pulse.

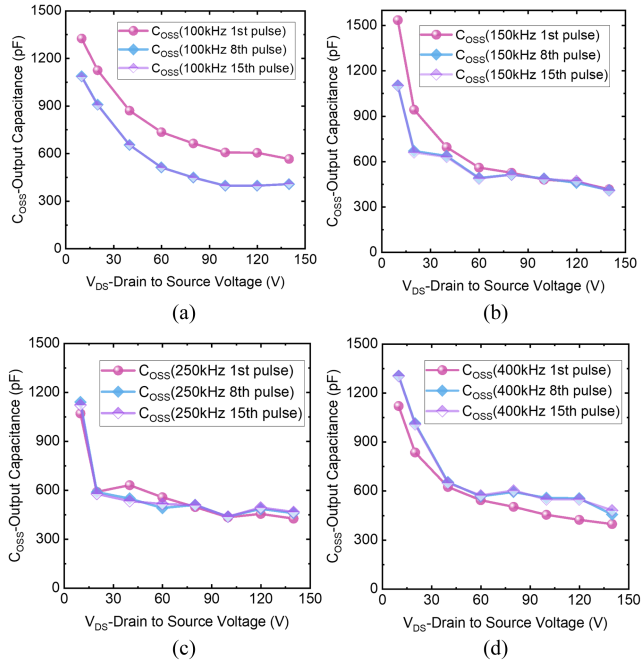

Fig. 11. $C_{OSS,Q1}$ extraction results for the 1st, 8th, and 15th pulses under varying PWM frequencies. (a) 100 kHz. (b) 150 kHz. (c) 250 kHz. (d) 400 kHz.

becomes positive and $V_{DS,Q2}$ starts to fall, the *di/dt* and *dv/dt* slopes are nearly identical to those of the first pulse, indicating that the intrinsic switching behavior is not significantly altered by the preceding reverse-conduction current. The freewheeling interval with constant $V_{DS,Q2}$ does not contribute to the ON-switching energy calculation. The $V_{DS,Q2}$–$I_{D,Q2}$ transients for the first, eighth, and fifteenth pulses [see Fig. 8(a)–(c)] exhibited significant peak overshoot and oscillations, attributed to a larger intrinsic $C_{OSS,Q1}$ at lower $V_{DS,Q2}$. This overshoot had a considerable impact on switching losses. To ensure compliance with IEC 60747 and JEDEC's JEP200 standards, the $V_{DS,Q2}$ measurements were limited to the first cycle's 10% falling point, thereby eliminating the effects of subsequent oscillation cycles and removing oscillation losses.

Fig. 9 depicts switching-on losses at a higher frequency of 400 kHz and an input voltage of 140 V. The $V_{DS,Q2}$–$I_{D,Q2}$ transients [see Fig. 9(a)–(c)] showed less oscillation, attributed to lower instantaneous $C_{OSS,Q1}$, indicating improved waveform stability under these conditions. However, the power loss curves displayed slight peak distortions during the eighth and fifteenth pulses due to incomplete $C_{OSS,Q1}$ charging and discharging caused by the higher switching frequency. Similar to Fig. 8, parasitic oscillation losses were reduced by focusing on the switching interval between 10% $I_{D,Q2,ON}$ and 10% $V_{DS,Q2,OFF}$.

Fig. 10 compares the distribution of energy stored in the output capacitance of Q_1 ($E_{qOSS,Q1}$) during the switching-on transient at different V_{IN} and switching frequencies (f_{SW}) for the first pulse [see Fig. 10(a)] and the fifteenth pulse [see Fig. 10(b)]. Under the initial switching condition at 100 kHz, $E_{qOSS,Q1}$ for the first pulse is significantly higher than that for the fifteenth pulse. However, in subsequent tests at 150 to 400 kHz, $E_{qOSS,Q1}$ for the fifteenth pulse converges with that of the first pulse. Additionally, $E_{qOSS,Q1}$ varies significantly with different f_{SW} under the same pulse. For the fifteenth pulse, E_{qOSS} increases considerably at higher f_{SW}, particularly at 400 kHz. In contrast, for the first pulse, the 100 kHz test shows the highest $E_{qOSS,Q1}$, while the 400 kHz test shows the lowest. The relatively stable $E_{qOSS,Q1}$ at lower frequencies and $V_{DS,Q2}$ levels implies that energy losses are mostly determined by the device's inherent capacitance. However, as $V_{DS,Q2}$ increases, *V–I* overlap losses account for a greater portion of the total energy losses, which may introduce variances in $E_{qOSS,Q1}$ extraction.

Fig. 11 presents the extracted $C_{OSS,Q1}$ results for the 1st, 8th, and 15th pulses under different f_{SW}. At 100 kHz [see Fig. 11(a)], the $C_{OSS,Q1}$ value of the first pulse is significantly higher than those of the eighth and fifteenth pulses. At 150 kHz [see Fig. 11(b)], the $C_{OSS,Q1}$ value of the first pulse remains higher than the subsequent pulses until $V_{DS,Q2}$ reaches 60 V, at which point the $C_{OSS,Q1}$ values become approximately equal across different pulses. This equalization is reported under a fixed duty ratio $D = 50\%$. For a given f_{sw}, the per-cycle off-interval $\Delta t_{off} = (1 - D)/f_{sw}$ is constant across pulses; adopting a different D would change Δt_{off} and could shift the point at which the equalization occurs. In Fig. 11(c), under 250 kHz, the $C_{OSS,Q1}$ values of the first pulse are close to those of the eighth and fifteenth pulses, showing only minor differences. At 400 kHz [see Fig. 11(d)], the first pulse depicts a similar trend to the eighth and fifteenth pulses. Additionally, when the input stress exceeds 60 V, the $C_{OSS,Q1}$ value at 400 kHz slightly increases compared to lower frequencies.

By comparing the $C_{OSS,Q1}$ values in Fig. 11 with the static datasheet values, it is observed that at initial $V_{DS,Q2}$, the measured switching-based $C_{OSS,Q1}$ is slightly lower (~3% –8%) than the datasheet values [16]. As $V_{DS,Q2}$ increases, larger deviations up to ~28% –37% emerge. In addition, unlike the datasheet trend of continuous decrease in $C_{OSS,Q1}$ with rising $V_{DS,Q2}$, the measured $C_{OSS,Q1}$ stabilizes beyond 100 V.

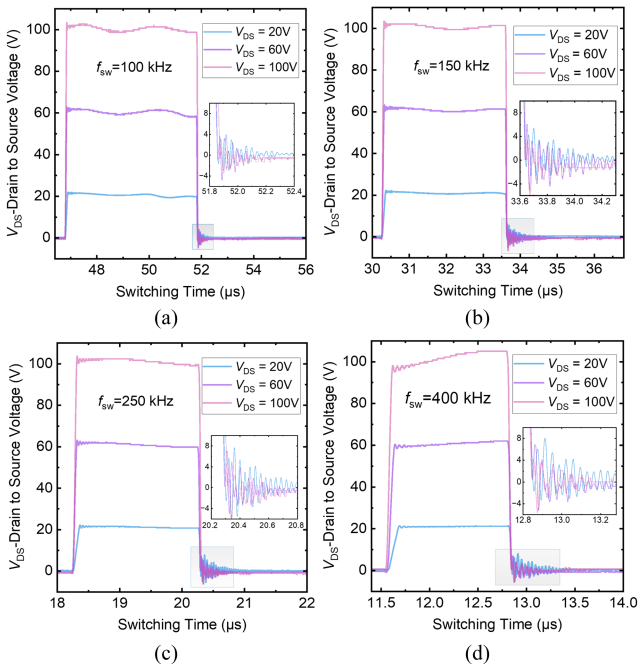

Fig. 12. Comparison of $V_{\mathrm{DS},Q2}$ ringing oscillation effects at input voltages of 20 V, 60 V, and 100 V for pulse switching frequencies of (a) 100 kHz, (b) 150 kHz, (c) 250 kHz, and (d) 400 kHz.

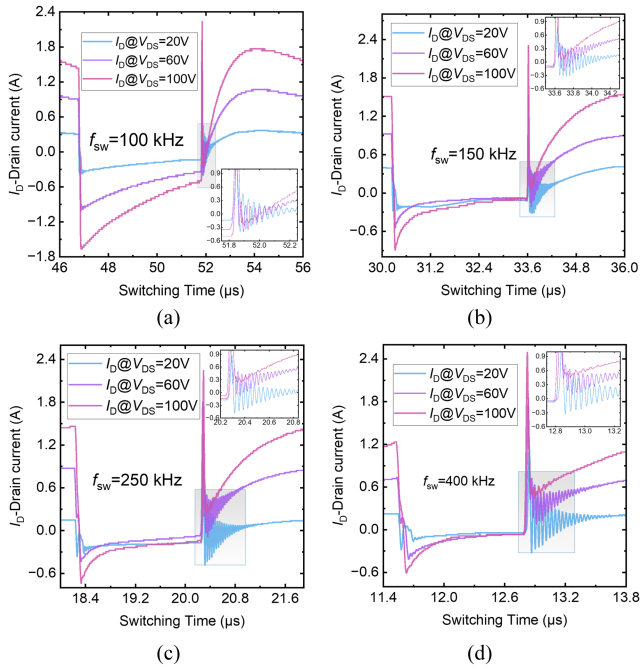

Fig. 13. Comparison of $I_{D,Q2}$ ringing oscillation effects at input voltages of 20 V, 60 V, and 100 V for pulse switching frequencies of (a) 100 kHz, (b) 150 kHz, (c) 250 kHz, and (d) 400 kHz.

These differences indicate that relying solely on static datasheet $C_{\mathrm{OSS},Q1}$ can misestimate device behavior under switching. In the studied conditions, employing dynamic C_{OSS} (V_{DS}, f_{SW}) in place of static values provides a more representative basis for estimating capacitive turn-ON energy and switching-loss contributions. Beyond loss estimation, these dynamic capacitance characteristics support soft-switching margin assessment and general switching-transition design across topologies. The observed sensitivity to OFF-state stress and frequency identifies conditions where capacitance departs from its first-pulse value. Incorporating the extracted C_{OSS} (V_{DS}, f_{SW}) thus links the measurement protocol of Section II to design-level decisions.

Figs. 12 and 13 present the switching transients used for extracting dynamic $C_{\mathrm{OSS,Q1}}$ and illustrate how $V_{\mathrm{DS},Q2}$ and f_{SW} influence the overshoot and ringing that bound the integration interval. In Fig. 12, distinct overshoot and damped ringing are observable across all tested frequencies. For a given f_{SW}, increasing $V_{\mathrm{DS},Q2}$ results in smaller ringing amplitude, reflecting the voltage-dependent reduction of C_{OSS} at higher drain bias. The effect of switching frequency (100–400 kHz) is comparatively minor, though the ringing envelope becomes slightly more pronounced at higher frequencies. Fig. 13 shows the corresponding $I_{D,Q2}$ waveforms. The current exhibits stronger variation with bias than the voltage, consistent with the displacement-current component associated with $C_{\mathrm{OSS},Q1}$ charging and discharging. Transient reverse conduction is evident from the negative current segments at all frequencies (≈ -1.8 A at 100 kHz and ≈ -0.6 A at 400 kHz). The $I_{D,Q2}$ oscillation exhibits a weak and nonmonotonic dependence on switching frequency, consistent with the trends summarized in Fig. 12.

B. *Off-State* V_{DS} *Stress and Frequency Dependent Switching Stress Influence on* $C_{OSS,Q1}$

This section comprehensively analyzes the electron trapping and hole injection process in GaN HEMTs to reveal the possible mechanisms for the observed $C_{\mathrm{OSS},Q1}$ variations. In the experimental setup, the $C_{\mathrm{OSS},Q1}$ values were extracted from Q_1 with its gate and source terminals shorted. During operation, Q_1 initially remains OFF, then undergoes negative V_{SD} reverse conduction during commutation, and finally returns to the OFF-state. During the first 2-s OFF-state V_{DS} bias period, Q_2 (the DUT) is subjected to a high drain voltage stress, whereas Q_1 experiences nearly zero potential difference. Thus, $C_{\mathrm{OSS},Q1}$ values obtained from Q_1 during the first pulse are unaffected by OFF-state V_{DS} bias stress. As Q_2 is subsequently turned ON, Q_1 begins to experience OFF-state V_{DS} stress, followed by reverse conduction during Q_2's turn-OFF, and finally recovers from both phases. As illustrated in Fig. 11(a), the discrepancies in $C_{\mathrm{OSS},Q1}$ values between the first and later pulses (e.g., 8th and 15th) arise from the cumulative effects of both OFF-state V_{DS} stress and reverse conduction.

At OFF-state, V_{DS} bias stress induces electron trapping in both the buffer and surface layers of Q_1, as shown in Fig. 14(a). The trapped charges extend the depletion region before the next ON-switching event, reducing C_{GD} and C_{DS} [34], [35]. Electron trapping accumulates with stress time. This behavior is consistent with TCAD simulations on *p*-GaN HEMTs showing OFF-state electrostatic-potential accumulation and progressive electron capture in the buffer; moreover, shorter off-intervals limit trap filling [36]. Therefore, as the number of pulses

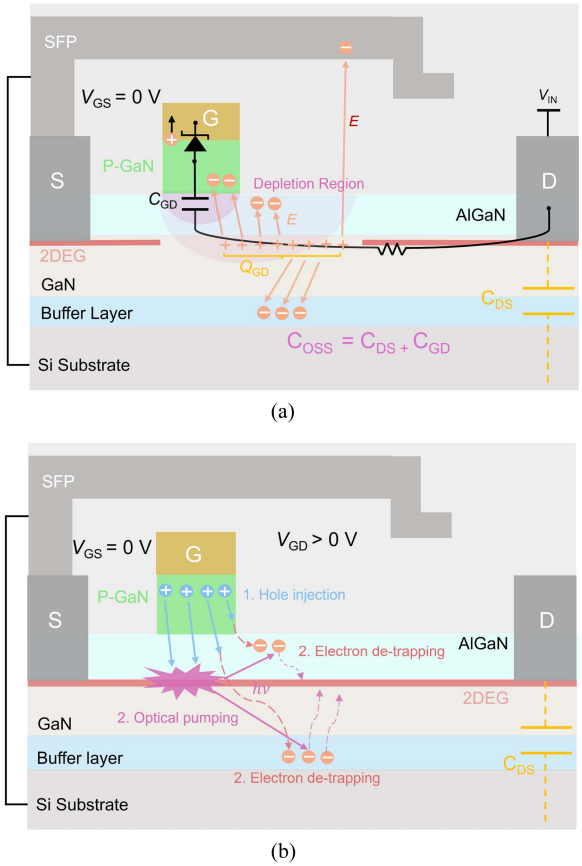

Fig. 14. Cross-sectional schematic of a Schottky *p*-GaN HEMT device structure illustrating C_{OSS} components under (a) OFF-state drain voltage stress (Q_1) and (b) frequency-dependent V_{SD} bias induced during reverse conduction.

increases, a decrease in $C_{OSS,Q1}$ is observed at a frequency of 100 kHz, as shown in Fig. 11(a). While at higher switching frequencies, the per-cycle OFF-state interval is shorter for the same pulse number, which reduces the time available for electron trapping and thereby lessens the deviation observed between different pulses, as shown in Fig. 11(b) and (c).

During the switching period after OFF-state stress, Q_1 experiences a near soft-switching condition and is then reversely turned ON. The positive V_{GD} bias facilitates hole injection from the *p*-GaN layer into the barrier and buffer layers [37], [38], [39], as depicted in Fig. 14(b). The injected holes could be recombined with 2DEG to generate photons. These photons may subsequently reach deep-level traps in the buffer layer or at the AlGaN/passivation interfaces to release the trapped electrons [40], [41]. A portion of holes could also assist the emission of trapped electrons [42], [43]. This hole-injection pathway is supported by carrier-density simulations under reverse drain bias, which show that a transient positive V_{GD} bias injects holes across the *p*-GaN/AlGaN barrier and reopens the 2DEG channel [44]. During reverse conduction, this process compensates for the negative charges accumulated during the previous OFF-state V_{DS} stress. These interactions between electron trapping and compensation processes result in a stable C_{DS} after multiple pulse cycles for all the measured frequencies (see Fig. 11).

The frequency directly influences the hole injection and subsequent electron trapping compensation. The reverse conduction occurs more frequently with higher operation frequency, allowing both the direct hole-assisted electron detrapping and the photon pumping to occur more often and effectively. At a high frequency of 400 kHz, $C_{OSS,Q1}$ increases after multipulse stress due to the enhanced hole-injection process, as illustrated in Fig. 11(d).

The mechanisms could also provide several insights into the C_{OSS} behaviors of power GaN HEMTs subjected to hard-switching conditions, similar to Q_2. One of the differences is the higher V_{GS} at ON-state compared to the reverse conduction experienced by Q_1, which promotes more hole injections to provide stronger compensation for electron trapping. Another difference is the harsher switching transients. More hot electrons could be trapped into the buffer and barrier layer, worsening ON-resistance and reducing C_{OSS}. Meanwhile, impact ionization becomes significant during such harsh switching, the generated holes could also assist in the electron detrapping as that occurs at ON-state [20]. Overall, the power HEMTs are expected to exhibit a stronger trapping-detrapping equilibrium under hard-switching conditions.

The trends in Section III-B on the dependence of $C_{OSS,Q1}$ on OFF-state V_{DS} stress and frequency-related trapping and recovery during reverse conduction provide direct design guidance. For a given operating range defined by V_{DS} and f_{SW}, the measured dynamic C_{OSS} should replace static datasheet values when estimating capacitive turn-ON energy and switching losses. Using the extracted C_{OSS} as a function of V_{DS} and f_{SW} connects the measurement protocol in Section II to design-level decisions.

C. Comparison With Reported Methods

Table II compares this article extraction framework with reported C_{OSS} characterization techniques [9], [10], [11], [12], [13], [14], [15]. The proposed multipulse switching approach exhibits high representativeness to real converter operation while maintaining moderate hardware complexity, unlike resonance-based or auxiliary-switch platforms that require additional circuitry. By integrating both C_{GD} coupling and *V–I* overlap correction, the proposed method achieves accurate dynamic C_{OSS} (V_{DS}, f_{SW}) extraction under practical switching conditions. The SPICE-assisted subtraction isolates conduction and displacement components, relating measured switching energy with intrinsic device behavior. This approach shows that the switching based $C_{OSS,Q1}$ deviates notably from datasheet values, with 3% –8% error at low $V_{DS,Q2}$ and up to 28% –37% at higher drain bias. Unlike the datasheet trend of monotonic decrease observed in static datasheets, the measured $C_{OSS,Q1}$ reveals frequency-dependent behavior influenced by OFF-state stress and charge trapping. These results indicate that static parameters significantly underestimate or overestimate capacitive energy during practical switching operations.

Overall, this article distinctive feature lies in providing a converter-representative, hardware-practical method that captures the dynamic influence of V_{DS} stress and f_{SW} on C_{OSS}. The extracted capacitance data enable more precise design of

TABLE II
COMPARISON OF REPORTED C_{OSS} EXTRACTION METHODS AND THIS ARTICLE

Ref.	Load	Switching frequency	Hardware complexity	Test Mode	Switching realism	C_{OSS} Accuracy
[9] Sawyer–Tower (JESTPE 2021)	No	1 kHz–1 MHz	Low	Steady-state	Low	Low
[11] No-load half-bridge (TPEL 2022)	No	100–500 kHz	Medium	Multipulse	Low	Medium
[14] EPE 2023 (Review)	/	/	Low	Single-pulse and steady-state	Low	Low
[10] UIS-based characterization (ECCE 2022)	Yes	500 kHz	Medium	Single-pulse and steady-state	Medium	Medium
[12] Nonlinear resonance (TPEL 2020)	Yes	1 kHz–1 MHz	Medium	Single-pulse	Medium	Medium
[13] High-dv/dt resonance (IPEMC 2020)	Yes	/	Medium	Single-pulse	Medium	Medium
[15] Modified hard-switching (ISPSD 2024)	Yes	5–40 kHz	High	Multipulse	High	High
This article (multipulse soft-switching)	Yes	100–400 kHz	Medium	Multipulse	High	High

soft-switching conditions, resonant-tank tuning, and converter-level loss prediction in high-frequency GaN applications. This framework bridges device-level characterization with circuit-level optimization, enhancing both efficiency and reliability assessment.

IV. CONCLUSION

This article introduces an extraction method for the C_{OSS} of p-GaN HEMTs under multipulse test conditions, applying a gate-source shorted configuration to accurately capture both C_{GD} and C_{DS} during switching transients. The results reveal the influences of OFF-state V_{DS} bias and frequency on C_{OSS}, where C_{OSS} decreases with increasing pulse numbers at lower switching frequencies, while higher frequencies exhibit minimal variations or slight increases. These changes are primarily driven by the interplay between electron trapping induced by OFF-state V_{DS} bias and hole injection during reverse conduction. At lower frequencies, increased pulse cycles exacerbate V_{DS}-induced electron trapping during the OFF-state, extending the depletion region and leading to a reduction in C_{OSS}. In contrast, higher frequencies result in fewer trapped electrons due to shorter OFF-state durations per pulse. Additionally, hole injections from the p-GaN layer compensates trapped electrons through photon generation and direct recombination, stabilizing C_{OSS} across multiple cycles. The extracted dynamic C_{OSS} (V_{DS}, f_{SW}) provides a representative basis for estimating capacitive turn-ON energy and switching-loss contributions in the studied conditions, supports assessment of soft-switching margins and switching-transition optimization across topologies, and can support more accurate prediction of GaN device switching performance, thereby informing GaN power-circuit design.

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