Multilayer Device-Level Electro-Thermal Real-Time Simulation and Multipurpose HIL Testing of Power Electronics Converters

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***Abstract*—Real-time simulation (RTS) of power electronic converters (PECs) has become increasingly crucial throughout their lifecycle in modern electrified transportation systems, yet remains constrained by computational limitations. This article presents a multilayer device-level electrothermal RTS methodology that simultaneously addresses electrical-thermal coupling effects and semiconductor switching characteristics while maintaining computational efficiency. A novel multipurpose hardware-in-the-loop (HIL) testing framework is subsequently developed by systematically integrating the proposed electrothermal RTS, enhancing both functional verification capabilities and testing efficiency. Experimental validation is conducted through an field programmable gate array (FPGA)-based implementation for an interleaved bidirectional DC–DC converter. The real-time simulation results demonstrate high consistency compared to offline LTspice simulations. Successful integration with the HIL testing confirms the methodology's effectiveness in enabling concurrent electro-thermal analysis and control strategy verification, significantly advancing the development of reliable PECs for electrified transportation.**

***Index Terms*—Hardware-in-the-loop (HIL) testing, high frequency converter, real-time simulation (RTS), silicon carbide (SiC) devices.**

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I. Introduction

THE progressive electrification of transportation, such as electric vehicles and more electric aircraft, has driven the extensive adoption of power electronic converters (PECs) across various segments, including motor/generator driving, electrical power distribution, and electro-mechanical actuation [1]. As a core enabling technology in the digitalized R&D of power electronics, real-time simulation (RTS) plays a vital role throughout the entire development cycle of PECs [3]. From the design to the validation stages, RTS-based hardware-in-the-loop (HIL) testing offers a cost-effective, time-efficient, flexible, and safe approach to conducting converter tests, integration tests, and system tests before deployment, significantly enhancing testing efficiency [4]. In the commission stage, RTS, combined with techniques such as virtual-physical interaction and data fusion, enables the creation of digital twins for remote monitoring, fault prediction, and diagnostics of power electronic equipment [5]. Consequently, the accuracy of RTS directly determines the fidelity of HIL testing and the reliability of digital twins, thereby influencing the development efficiency of PECs.

The accuracy of RTS is tightly related to the modeling complexity [6]. In general, the more complex model leads to a more accurate simulation. However, the modeling complexity is constrained by the simulation speed. As for the RTS, the time for the model computing in each time-step is very limited to the nanosecond-level, and very limited numerical operations can be done, especially with the employment of the wide bandgap devices [7], [8]. The possible model is thus very limited. In the commercial RTS solver, the static model is usually used, where the steady turn-ON and turn-OFF states are considered, and the switching transient is neglected. The representative model is the switching function model [9], the binary resistor model [10], and the associated discrete circuit model [11]. Efforts in recent years have been made to integrate the switching transient behaviors and implement the device-level RTS. The behavioral model of the switches is usually used with reasonable simplifications and assumptions. Lin and Dinavahi [12] proposed an IGBT fourth-order nonlinear equivalent model, enabling the application of the IGBT device-level behavior in the RTS of high-voltage DC circuit breakers. Shen and Dinavahi [13] proposed a variable time-step approach to apply the nonlinear Lauritzen's diode

model in the device-level RTS of a single-phase full-wave rectifier circuit. All these models require an iterative numerical solver and need a microsecond-level simulation time step. To reduce the solving complexity, Bai et al. [14] proposed a piecewise linear transient model for the IGBT/diode, and reduced the time-step to 50 ns. However, the linearization cannot account for the high-frequency oscillations. The authors [15], [16], [17] have implemented the device-level RTS based on a curve fitting model, which scales offline-measured transient waveforms proportionally according to the operating voltage and current, and enables shorter transient simulation time-steps. However, the curve fitting model is intrinsically weak in generalization. Bai et al. [18] has thus proposed an adaptive curve-fitting method and implemented the device-level RTS with a 25 ns time-step. The authors [19], [20], [21] proposed a two-level quasi-transient RTS strategy, which uses system-level simulation results to back-calculate the device-level transient waveforms. The simplified transient model is used to generate high-resolution transient switching waveforms (highest 5 ns). Li et al. [22] proposed a data-driven device-level RTS where the transient waveforms can be generated by the neural networks with a comparative accuracy to the physics-based model.

The increasing demand for higher efficiency, power density, overload capability, and environmental adaptability in electrified transportation has driven the evolution of power electronic devices, represented by those based on silicon carbide (SiC) [23]. SiC devices, compared to their silicon (Si) counterparts, offer significantly higher switching frequencies and faster switching transients, enabling improved performance in high-power applications [24]. Despite advancements in device-level RTS, current technologies still struggle to accurately simulate the behavior of SiC devices during fast switching events, characterized by transients on the order of several nanoseconds and with high-frequency oscillations. As a result, the computing power required to simulate SiC-based power electronics in RTS environments remains insufficient.

Moreover, with the increasing power demand in electric vehicles and more electric aircraft, energy-optimization-driven control strategies have garnered considerable attention, particularly those focused on managing the electro-thermal behavior of PECs to enhance power density and dynamic response [25], [26]. Accurate simulations of the electro-thermal behaviors are therefore critical. To address these challenges, electro-thermal RTS platforms are indispensable, as they enable HIL testing for various innovative technologies. These include temperature-based and efficiency-based optimization controls, electro-thermal integrated management, fault prediction, health monitoring, and fault-tolerant control—areas that cannot be effectively explored or tested through traditional HIL methodologies.

To overcome the current limitations in the computational capacity of RTS, this article introduces a multilayer device-level electro-thermal RTS method for PECs. By coordinating mixed execution rates, the complex device-level solvers are efficiently integrated into the RTS framework. Furthermore, a SiC MOSFET model based on a multiple piecewise linearization approach is developed for field programmable gate array (FPGA)-based simulation, achieving high accuracy on par with that of LTspice simulations. In addition, a multipurpose HIL testing methodology, enhanced by the proposed RTS, is presented, significantly extending the capabilities of traditional HIL systems. To demonstrate its effectiveness, an interleaved bidirectional converter (IBC) in the more electric aircraft power system is utilized as a case study to implement the multipurpose HIL testing. Various tests are conducted, thereby validating the robustness and efficiency of the proposed electro-thermal RTS and multipurpose HIL testing of PECs.

The remainder of this article is organized as follows. Section II details the multilayer device-level electro-thermal modeling method. Section III presents a SiC MOSFET model based on a multiple piecewise linearization method. Section IV takes an interleaved bidirectional converter as the case study, detailing FPGA implementation of the multilayer device-level electro-thermal RTS. Section V introduces a multipurpose HIL testing method based on the proposed RTS and demonstrates its application in various tests. Section VI concludes this article and gives directions for future research.

II. Multilayer Device-Level Electro-Thermal RTS of Power Electronics

A. Device-Level Electro-Thermal Model

The structure of the device-level electro-thermal model of PECs for RTS is shown in Fig. 1, consisting of four components: the electrical model, thermal model, power loss module, and electrical parameters update module. The electrical model provides the voltage, current, and switch status for the power loss module to find the exact power losses at the moment. The loss of the power semiconductor (PS) is fed to the thermal model, where the junction temperature is computed. The temperature-sensitive electrical parameters (TSEPs) in the electrical model are thus updated, and the electrical and thermal behaviors are coupled in RTS.

1) Electrical Model: The electrical model is developed based on the circuit topology, and primarily involves two steps: component modeling and network modeling. The main components of converters include the PS, the resistor, the capacitor, the inductor, and the source. Modeling the PS can be the most cumbersome. To balance the modeling accuracy and solving efficiency, the switches are modeled at two levels in this article. The static model is used in the RTS of the converter, which focuses on the system-level behaviors, while the transient model is used for generating the device-level characteristics and implemented in a slower-than-real-time manner to relieve the intensive computing efforts. The system-level model provides the steady-state turn-ON and turn-OFF voltage and current for the device-level model, and the device-level results reproduce the transient waveforms that can be used to analyze the device stress and update the switching losses table in the power loss module. By coordinating the execution rates, both the system-level and device-level behaviors can be presented with sufficient accuracy.

2) Thermal Model: Due to the inherent susceptibility of PS to failure and its tightly coupled electro-thermal behavior, this article focuses on the electro-thermal model for PS. The

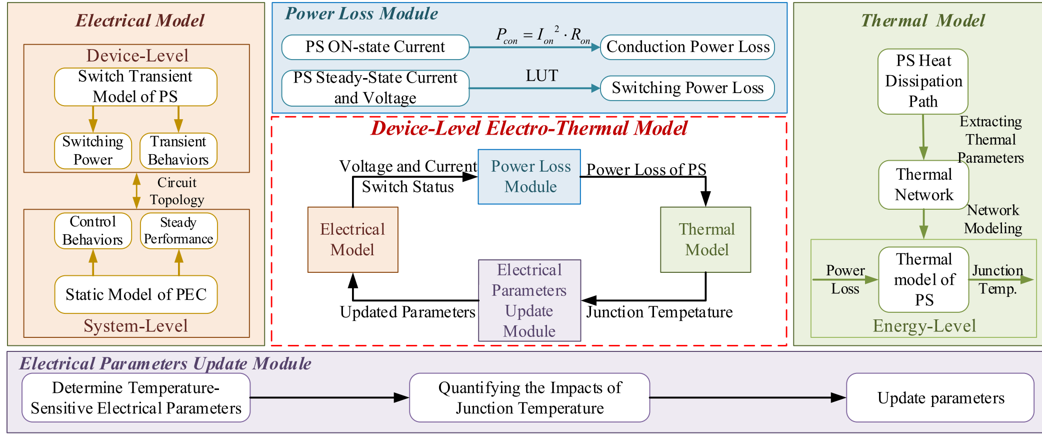

Fig. 1. Structure of the device-level electro-thermal model, showing the integration of the electrical model, thermal model, power loss module, and electrical parameters updating module.

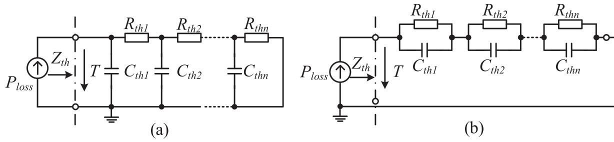

Fig. 2. Thermal network model. (a) Cauer model. (b) Foster model.

one-dimensional thermal network is adopted for its simplicity and ease of parameter extraction, making it suitable for RTS, as shown in Fig. 2. Either the Cauer network or the Foster model can be used. The thermal resistance R_{th} and thermal capacitance C_{th} in the Cauer model correspond to the thermal behaviors of each internal layer of the module, and the components in the Foster model are fitted to match thermal response rather than physical structure. After formulating the thermal network, the thermal model can be solved in the same manner as the electrical model.

3) Power Loss Module: The power loss module computes the power dissipation of the PS, serving as the input for the thermal model. The power loss includes the conduction loss, switching loss, and static power loss (neglected in this article). The conduction power loss P_{con} is calculated by the following:

$$P_{\text{con}} = {I_{\text{on}}}^2 \cdot R_{\text{on}} \tag{1}$$

where I_{on} is the ON-state current, and R_{on} is the ON-state resistance of the device.

Calculating switching losses uses the datasheet-based method, the mathematical model, and the physical model. However, when facing the RTS, the datasheet information lacks generality, the mathematical model needs extensive data obtained from the experiments, and the physical model is complex for the solver. Therefore, to obtain the power losses in a fast and accurate way, this article proposes a lookup table (LUT) method to compute the switch losses. The LUT stores the switching energy loss in different steady-state voltages and currents. The energy losses are then converted to power losses based on energy conservation. The typical turn-ON duration T_{on} and turn-OFF duration T_{off} are selected, and the energy losses are assumed to be produced evenly in each time-step within that time, as indicated in the following:

$$P_{\text{sw}} = \frac{\text{LUT}_E(V, I)}{T_{\text{on}} \text{ or } T_{\text{off}}} \tag{2}$$

where V and I represent the switch voltage and current in the steady states.

The conduction losses P_{on} and switching losses P_{sw} will be fed to the thermal model together with the switch status. As junction temperature variations alter the electrical parameters, the loss LUT will be continuously updated from the switching transient newly produced by the device-level model.

4) Electrical Parameters Update Module: In the electrical parameters update module, the impacts of junction temperature on TSEPs are quantified, mathematically reflecting the influence of thermal effects on electrical behaviors. The TSEPs of a PS usually include the on-state resistance, threshold voltage, turn-OFF delay time, and Miller plateau voltage. The thermal effects are modeled by fitting the relationship provided by the datasheet. By modifying the TSEPs in the electrical model and providing the losses to the thermal model, the electrical and thermal behaviors of the PS are thus coupled and modeled in the RTS.

B. Multilayer Simulation Framework

Device-level RTS for high-frequency devices like SiC MOSFETS remains challenging, as the ultrafast switching process demands extremely small time-steps that exceed the computing capacity of RTS. To overcome this challenge, this article proposes a multilayer simulation approach for accommodating the device-level model in RTS.

1) Structure: The multilayer simulation structure is illustrated in Fig. 3.

In layer 1, the system-level electro-thermal model runs in real-time, in which the switch static model is used in the simulation to ensure the real-time capability. In layer 2, the switch transient model operates in a slower-than-real-time manner and is capable

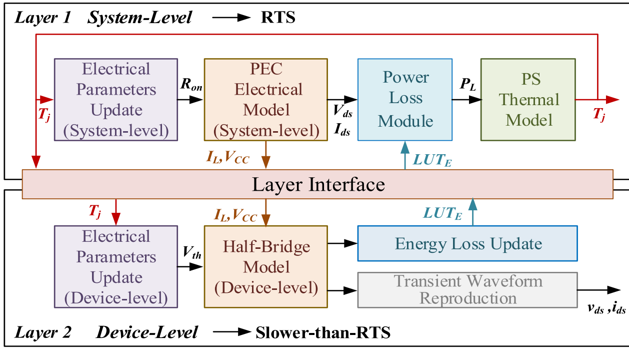

Fig. 3. Structure of the proposed multilayer device-level electro-thermal real-time simulation framework.

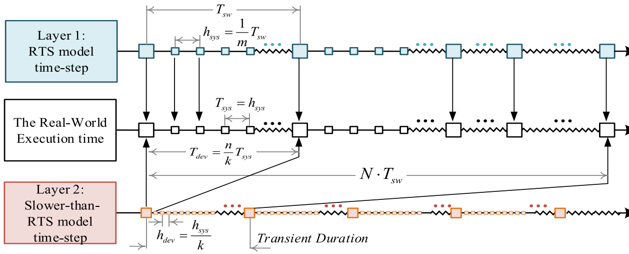

Fig. 4. Timing sequence of the multilayer real-time simulation.

of generating the detailed switching transients. Slower-than-real-time-simulation refers to a simulation where the execution speed is a fixed multiple slower than real time, as proposed in [27]. The transient model may not be necessary to be simulated in real time if the important information, such as switching losses and electrical stresses, is computed with sufficient accuracy. The two layers exchange data through the layer interface at a predefined frequency to ensure simulation accuracy.

2) Timing Relationship: The timing sequence of the multilayer simulation is shown in Fig. 4. Assuming the converter switching period is T_{sw}, the RTS time-step in Layer 1 h_{sys} is computed by (3), where m is a scaling factor to ensure sufficient simulation accuracy, which is generally greater than 100. The execution time T_{sys} equals the simulation time-step h_{sys} in RTS

$$T_{\text{sys}} = h_{\text{sys}} = \frac{1}{m} T_{\text{sw}}. \tag{3}$$

In Layer 2, to capture short switching transients of the PS, a much smaller simulation time-step h_{dev} is required, as given in (4), where k is related to the switching time and the switching dynamics. The shorter switching time and higher order of the switching dynamic are, the larger value of k and thus a smaller device-level time-step h_{dev} will be. Due to the high complexity of the transient model, the actual execution time per step is T_{dev} is larger than h_{dev}, as shown in (4), making the simulation n times slower than RTS. n is determined by the computing capacity of the solver

$$\begin{cases} h_{\text{dev}} = \frac{1}{k} h_{\text{sys}} \\ T_{\text{dev}} = n \cdot h_{\text{dev}} \end{cases}. \tag{4}$$

Consequently, the relationship between the execution time of the transient model and the switching period is shown in the following:

$$T_{\text{dev}} = \frac{n}{mk} T_{\text{sw}}. \tag{5}$$

Furthermore, if a switching transient needs p device-level time-steps to describe, the total time that needs to reproduce the switching waveforms is given in the following:

$$T_{\text{tot}} = pT_{\text{dev}} = \frac{np}{mk} T_{\text{sw}} = N \cdot T_{\text{sw}}. \tag{6}$$

For example, to simulate a converter of 100 kHz ($T_{\text{sw}} = 10$ μs), a 50 ns system-level simulation time-step is used ($m = 200$), a 1 ns device-level simulation time-step is needed to reproduce a 100 ns switching transient ($k = 50$, $p = 100$) which needs 5 μs execution time for each computing step ($n = 5000$), and the total computing time for the transient will be $T_{\text{tot}} = 50T_{\text{sw}}$, which means the switching waveforms can be updated every 50 switching cycles.

Although the device-level simulation in Layer 2 operates in slower-than-real time, its asynchronous execution remains reasonable. The Layer 2 is designed for monitoring the transient behaviors when it's needed. The monitoring can be periodic or just called up by some events at specific time points. Typically, a meaningful operating-point shifting requires several switching cycles to reflect. By choosing a proper time interval, the transient waveforms can be monitored in a slower-than-real-time manner. To reserve some margin, the exact period between each data exchange between the two layers, T_{exc}, is a little larger than T_{tot}. The monitoring interval T_{mon} has to be bigger than T_{tot} for meaningful observations. T_{mon} is also suggested to be as small as possible to capture every transient behavior change. In addition, as the operating point shifting or junction temperature variations alter the electrical parameters, the switching loss LUT will be continuously updated from the newly produced transient results, and then be fed back to the power loss module in Layer 1 to revise the temperature computation.

Benefiting from the multilayer structure, the device-level model can be simulated with sufficient resolution to accurately represent the transient behavior. The constraint on model computing time is loosened to some extent, and a more complex model can be used to significantly improve the accuracy. This is very suitable for the wide bandgap devices, such as SiC MOSFET, where the model is relatively complex to describe the high-frequency oscillations, while the switching transient is very short to capture.

III. Multiple Piecewise Linearized SiC MOSFET Model

A. SiC MOSFET Equivalent Circuit

The multilayer simulation framework relieves the computing time of the switch transient, but the model still needs a dedicated design to speed up the solution and ensure convergence in the FPGA-based simulation. A typical equivalent circuit model of the SiC MOSFET is illustrated in Fig. 5(a), consisting of an equivalent stray inductor L_s, a variable parasitic capacitor C_{ds}, a variable parasitic capacitor C_{dg}, a constant parasitic capacitor

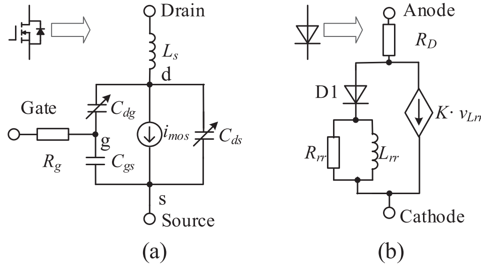

Fig. 5. Equivalent circuits of the SiC MOSFET behavioral model. (a) Switching channel model and (b) diode model.

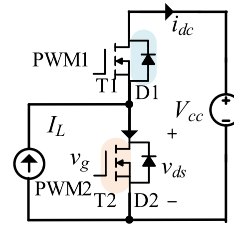

Fig. 6. Half-bridge commutation unit.

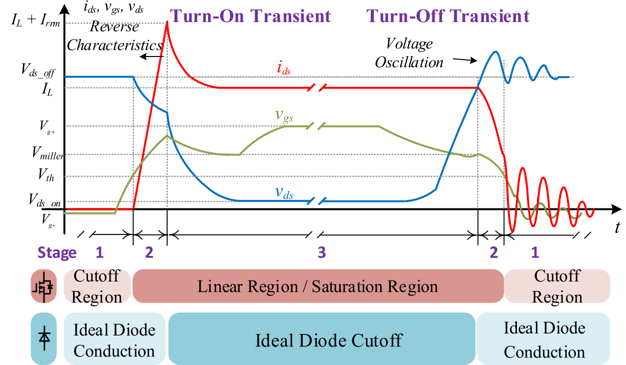

Fig. 7. Switching transient waveforms and operating states of the SiC MOSFET and ideal diode in the body diode model across different stages.

C_{gs}, and a controlled current source i_{mos} that emulates the dynamic characteristics of the conduction path. The equivalent circuit of the body diode or the anti-paralleled diode is shown in Fig. 5(b), including an ideal diode D1 to represent unidirectional conduction, a resistor R_D to emulate forward voltage drop, and a combination of inductor L_{rr}, resistor R_{rr}, and controlled current source Kv_{Lrr} to simulate reverse recovery characteristics.

Compared to the offline simulation, the model in Fig. 5 is already simplified. However, due to the nonlinearities, the model needs an iterative solver to find the numerical results, which can be time-consuming and weak in convergence. The nonlinearities primarily arise from the following three aspects:

1) inconsistency in the equations between different operating regions of the MOSFET and diode;
2) nonlinear output characteristics of the MOSFET in each operating region;
3) time-varying parameters Cdg and Cds in the equivalent circuit model.

A multiple piecewise linearization strategy is proposed in this article to mitigate the issues caused by nonlinearities in the transient model. It divides the switching transient into three stages based on the boundaries between operating regions, linearizes the nonlinear characteristics of i_{mos} in each phase, and treats time-varying parameters as piecewise constant. This strategy transforms a complex time-domain nonlinear problem into multiple linearized subproblems driven by segmented boundary conditions, significantly reducing computational complexity while maintaining accuracy. The resulting highly parallel structure is also well-suited for FPGA-based RTS.

B. Multiple Piecewise Linear Device-Level Solver

1) Piecewise Description of the Transient Process: A half-bridge commutation unit, including two MOSFETs and functioning as a three-port circuit, is shown in Fig. 6.

Since the time scale of the transient switching process is significantly smaller than that of the steady switching process, V_{cc} and I_L are considered constant during the transient.

Taking the commutation of T2 and D1 as an example, the switching transient is divided into three stages corresponding to the MOSFET operating regions and the ideal diode status in the diode model, as shown in Fig. 7. In Stage 1, the diode conducts the load current while the MOSFET remains in the cutoff region. In Stage 2, the MOSFET transitions to the linear regions, while the ideal diode in the diode model is conducting. In Stage 3, the ideal diode is reversely biased and the MOSFET operates in the linear region and the saturation region. Since the linear region and saturation region can share the same expressions, there is no need to further divide Stage 3 [28].

The equivalent circuit can be established for each stage, as shown in Fig. 8. Four state variables are selected to formulate the circuit equations: diode reverse recovery inductor current i_{Lrr}, drain–source current i_{ds}, gate–source voltage v_{gs}, and drain–source voltage v_{ds}. State-space equations are established for all three stages, providing a segmented model of the MOSFET, as given in (7). However, the presence of nonlinear terms still prevents direct solutions

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{7}$$

where $x = [v_{gs} \quad v_{ds} \quad i_{ds} \quad i_{Lrr}]^T, u = [v_g \quad V_{ds_\text{off}} \quad I_L \quad 1]^T$, $V_{ds_\text{off}} = V_{d_\text{on}} + I_L \cdot R_{d_\text{on}} + V_{cc}$ and the coefficients $\mathbf{A}$ and $\mathbf{B}$ corresponding to different stages are given in the Appendix.

To determine which specific stage the unit is in, the division criteria are illustrated in Fig. 9. During the turn-ON process, if $v_{gs} \leq V_{\text{th}}$, the MOSFET is cut off, and the unit is in stage 1. When $v_{gs} > V_{\text{th}}$, the MOSFET enters the linear region and starts to conduct. The unit is now in stage 2. With the increase of the drain current i_{ds}, the diode current i_d decreases, and the reverse recovery phenomenon occurs. When the reverse recovery current reaches its maximum value, the ideal diode in the diode model shown in Fig. 5(b) is cut off, meaning that $i_d \leq K{\cdot}v_{Lrr}$. The unit is now entering stage 3 until the switching pair reaches the steady state. In the turn-off stages, a negative v_g leads to a decrease in v_{gs}, and the v_{ds} starts to increase. After the v_{ds} is higher than

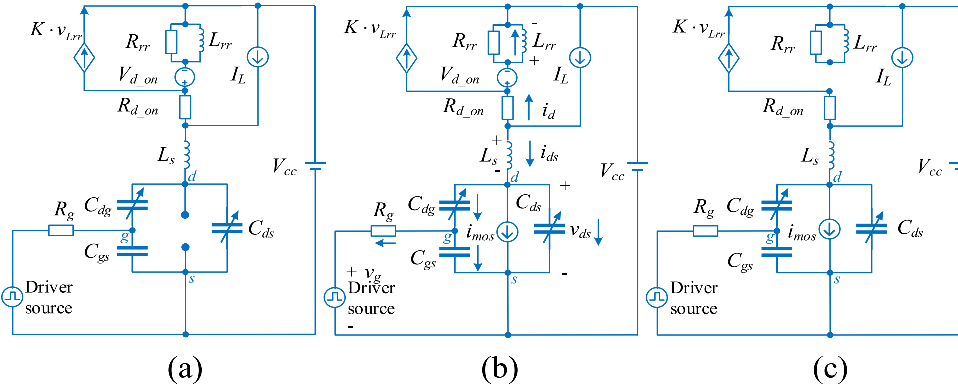

Fig. 8. Piecewise equivalent circuits for the switching process. (a) Stage 1. (b) Stage 2. (c) Stage 3.

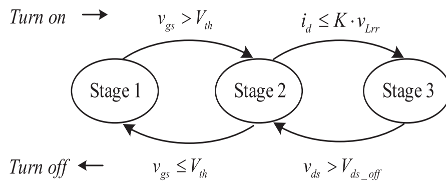

Fig. 9. Stage division criteria for the half-bridge commutation unit.

its steady-state turn-off value V_{ds_off}, the diode starts to conduct and the unit transitions from stage 3 to stage 2. When v_{gs} falls below the threshold voltage V_{th}, the MOSFET enters the cut-off region, and the unit transitions to stage 1.

2) Piecewise Linearization of Nonlinear Characteristics: The controlled current source i_{mos} is a function of the drain–source voltage v_{ds}, gate–source voltage v_{gs}, and junction temperature T_j, which can be expressed as $i_{\mathrm{mos}} = f(v_{ds}, v_{gs}, T_j)$. Since T_j can be considered constant during the transient process, i_{mos} is simplified to a bivariate function of v_{ds} and v_{gs}. To reduce the computing complexity, a bilinear interpolation-based LUT is used for the linearization of i_{mos}, which can be expressed by the following:

$$i_{\mathrm{mos}} = \begin{cases} 0, & v_{gs} \leq V_{\mathrm{th}} \\ \mathrm{LUT}\left(v_{ds}, v_{gs}\right), & v_{gs} > V_{\mathrm{th}} \end{cases} \quad (8)$$

where V_{th} denotes the threshold voltage.

Appropriate segmentation points for v_{ds} and v_{gs} are selected to divide the i_{mos} surface into multiple planes, as shown in Fig. 10. Next, for each plane, a first-order Taylor expansion of i_{mos} is performed at a reference operating point (v_{ds0}, v_{gs0}), yielding: $i_{\mathrm{mos}} = k_1 + k_2 \cdot v_{gs} + k_3 \cdot v_{ds}$, where k_1, k_2, and k_3 are given by the following:

$$\begin{aligned} k_1 &= f\left(v_{ds0}, v_{gs0}\right) - k_2 \cdot v_{ds0} - k_3 \cdot v_{gs0} \\ k_2 &= \left.\frac{\partial f(v_{ds}, v_{gs})}{\partial v_{gs}}\right|_{(v_{ds0}, v_{gs0})} \\ k_3 &= \left.\frac{\partial f(v_{ds}, v_{gs})}{\partial v_{ds}}\right|_{(v_{ds0}, v_{gs0})}. \end{aligned} \quad (9)$$

The linearized results are stored in a two-dimensional i_{mos} LUT, and those points not explicitly listed in the table are computed by the bilinear interpolation method. This approach enables an accurate linear representation of i_{mos} and reduces computational resource requirements.

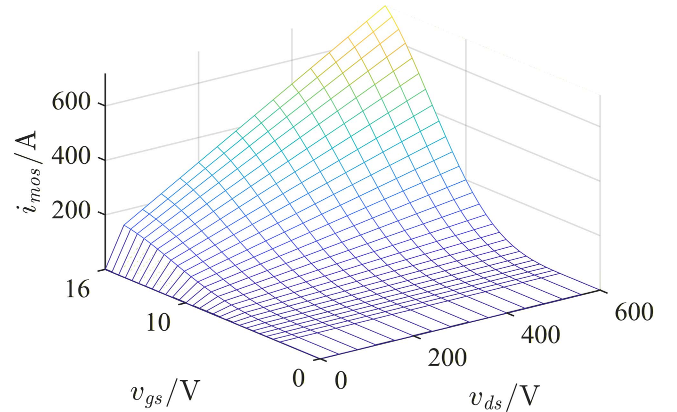

Fig. 10. Piecewise linearization of the i_{mos} surface based on v_{ds} and v_{gs}.

3) Piecewise Constant of Time-Varying Parameters: During the switching process, the capacitance of C_{gs} is treated as a constant, while the capacitances of C_{ds} and C_{dg} exhibit a nonlinear time-varying relationship with their corresponding voltages, as shown in the following:

$$\begin{cases} C_{ds} = f\left(v_{ds}\right) \\ C_{dg} = g\left(v_{dg}\right) \end{cases}. \quad (10)$$

The capacitance curves can be extracted from the datasheet or the manufacturer-provided model, and can be segmented into multiple regions based on voltage intervals, as shown in Fig. 11. Within each segment, the capacitance is assumed to be constant, and a capacitance LUT is used to store the value, effectively reducing the computational burden while still capturing the key nonlinear characteristics.

It needs to be mentioned that the multiple piecewise linear device-level solver is developed based on the half-bridge commutation unit shown in Fig. 6, which can be seen as the primary unit for the Boost/Buck-type topology, the single-phase full-bridge topology, the three-phase bridge-type topology, the multiphase bridge-type topology, etc. Therefore,

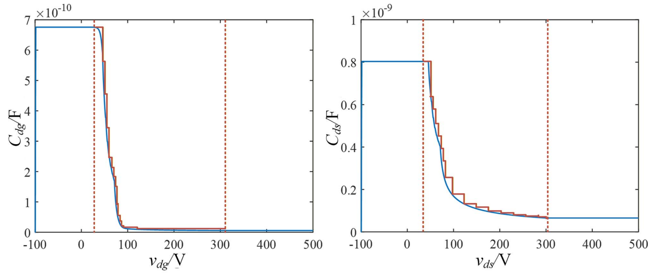

Fig. 11. Segmented *C–V* characteristics and LUT-based approximation.

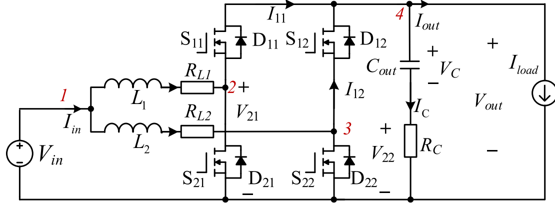

Fig. 12. Circuit topology of the IBC.

the proposed method can be used for those topologies. However, it may have limitations in the topologies that cannot be decomposed by half-bridge commutation units, for example, the switched-capacitor converter and the current source inverter.

IV. Case Study on FPGA

A. Introduction to the IBC

To validate the effectiveness and performance of the proposed device-level electro-thermal RTS, an interleaved bidirectional converter (IBC) is used as a case study, of which the low current ripple, compact size, high efficiency, and fault tolerance make it ideal for bidirectional power conversion in the more electric aircraft. The circuit of the IBC is shown in Fig. 12. The selected power device is the Wolfspeed SiC MOSFET C3M0060065J.

The real-time simulation unit used in our article is an FPGA evaluation board embedding a Xilinx XC7Z100-2FG900 FPGA chip, which includes 54 650 total slices, 55 4800 slice registers, 277 400 slice LUTs, 755 Block RAMs, and 2020 DSP48s.

The software platform adopted for FPGA coding and implementation is the NI LabVIEW, which utilizes graphical programming. When the model is programmed in the LabVIEW FPGA module, the module can automatically generate VHDL code and invoke the Xilinx Vivado compiler to create a bitstream file, which is then downloaded to the FPGA hardware to execute.

B. FPGA Implementation of Layer 1

The real-time implementation of Layer 1 is illustrated in Fig. 13. Layer 1 focuses on the system-level electro-thermal model of IBC. The variables from the previous step are first read from the shift register. The TSEPs, such as ON-state resistances, are updated based on the junction temperature. The switch statuses are identified based on the combination of the PWM signals and the inductor currents. The two half bridges can be decoupled from the topologies by inserting delays in the inductor currents. Therefore, the HBs can be solved, of which the results can be used for the integration of the inductor current and capacitor voltages. The current and voltage of switches are then sent to the power loss LUT, and the power loss is sent to the thermal model for computing the junction temperature. Finally, the overall variables are updated and prepared for the next step. All computations are completed within a 10 MHz single-cycle timed loop, and the RTS time-step of Layer 1 is 100 ns.

C. FPGA Implementation of Layer 2

The switch transient model solving process and parameter transfer flow of Layer 2 are shown in Fig. 14. The overall procedure is similar to that of Layer 1, but before each iteration, it requires identifying the operating status and retrieving the coefficients of i_{mos}, and the values of C_{ds}, and C_{gs}. The backward Euler method is employed to perform the integration of the state variables (referring to the Appendix). It can be seen that the largest state matrix is of four dimensions. To reduce computational complexity, an improved parallel matrix inversion method based on Gaussian elimination is used [29].

The simulation time-step of Layer 2 is 0.25 ns. One time-step needs an exact execution time of 5 μs. For a switching transient of 100 ns, 400 steps are included, whose total computing time will be 2000 μs. When a 50 kHz switching frequency is targeted, the switching waveforms can be updated every 100 switching cycles.

The total FPGA resource utilization of the two layers is summarized in Table I.

TABLE I
Device Resource Utilization on XC7Z100-2FFG900 FPGA

Device	Total	Used	Percentage of Total Resources
Total Slices	54 650	32 452	59.4
Slice Registers	554 800	48 029	8.7
Slice LUTs	277 400	95 082	34.3
Block RAMs	755	690	91.4
DSP48s	2020	1012	50.1

D. FPGA Simulation Results

To validate the accuracy and effectiveness of the proposed models, the FPGA-based simulation results are compared with the reference model provided by the manufacturer in LTspice.

1) System-Level Simulation Results: The basic parameters of the IBC are shown in Table II.

TABLE II
Basic Parameters of the IBC

Parameters	Value	Parameters	Value
$V_{in}(V)$	128	$I_{\mathrm{load}}\ (A)$	6
$C_{out}(\mu\mathrm{F})$	440	$R_C(m\Omega)$	0.5
$L_1(\mu H)$	800	$L_2(\mu H)$	800
$f_{sw}(kHz)$	50	Open-Loop Duty Cycle	0.6
Gate resistance(Ω)	10	Gate control voltage (V)	–5/16

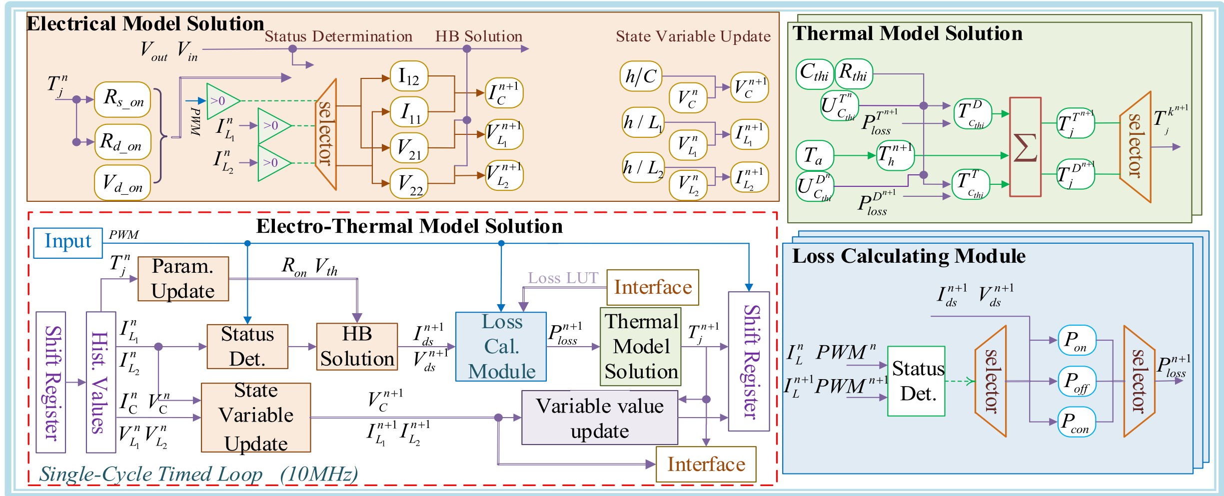

Fig. 13. Layer 1 electro-thermal model implementation in FPGA.

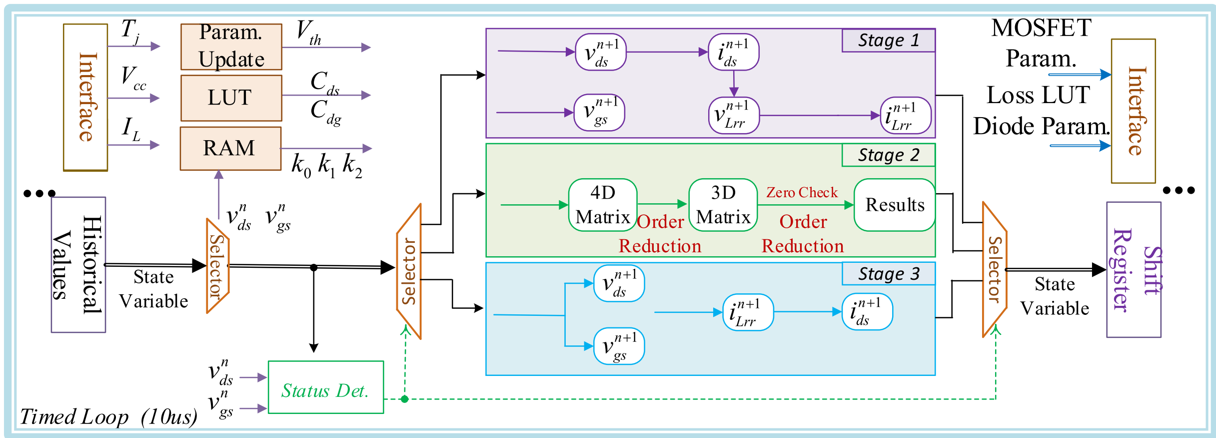

Fig. 14. Layer 2 SiC switching transient model implementation in FPGA.

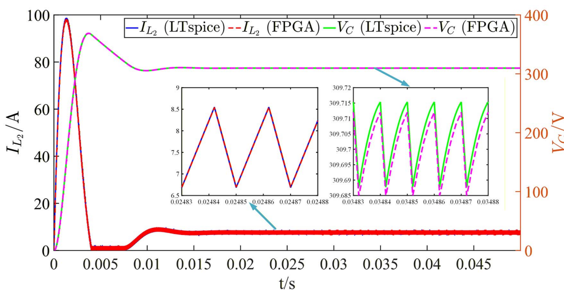

Fig. 15. Waveforms of inductor current and capacitor voltage during startup in open-loop boost mode of the IBC.

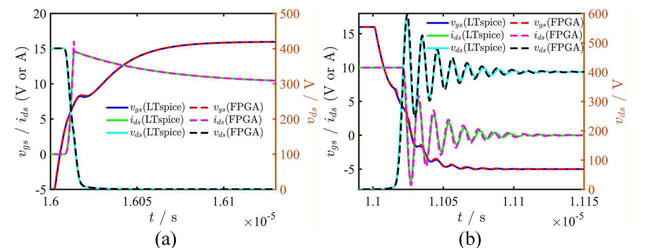

Fig. 16. Switching transient waveforms. (a) Turn-ON process. (b) turn-OFF process.

As an example of the IBC operating in open-loop boost mode, Fig. 15 shows the startup waveforms of the inductor L_2 current and the capacitor voltage under an input voltage of 128 V and a load current of 6 A. Additional tests at different voltage levels were conducted and showed that the average steady-state error in both voltage and current is less than 1%, indicating the high accuracy of the proposed model at system level.

2) Device-level Simulation Results: Device-level simulation results are depicted under V_{cc} = 400 V and I_L = 10 A. The turn-on and turn-off transient waveforms of v_{gs}, i_{ds}, and v_{ds} are presented in Fig. 16. The FPGA simulation results closely match those in LTspice, with discrepancies primarily observed in

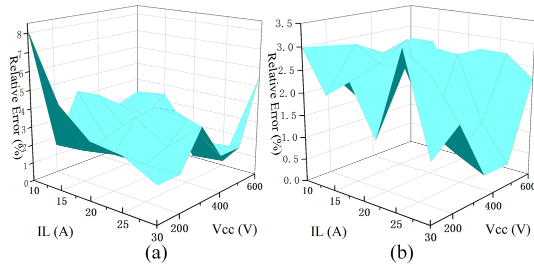

Fig. 17. Relative errors of switching loss energy of the proposed SiC transient model: (a) turn-ON process, (b) turn-OFF process.

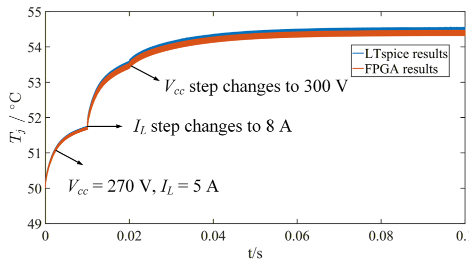

Fig. 18. Junction temperature responses to changing operating conditions.

regions of rapid waveform transitions due to the fixed-step nature of FPGA simulation. The SiC device model effectively captures key switching phenomena, including drain current overshoot, the Miller plateau in gate–source voltage, and oscillations in both drain current and drain–source voltage during turn-OFF.

With the values of V_{cc} ranging from 100 to 600 V and I_{L} from 10 to 30 A, thirty uniformly distributed operating conditions were simulated. Compared with LTspice results, the proposed model achieves average relative errors of 9.48% (turn-ON delay time), 6.55% (rise time), 2.08% (turn-OFF delay), 0.02% (fall time), and 0.28% (diode reverse recovery time). The relative errors of switching energy, as shown in Fig. 17, remain below 3% during turn-ON and below 8% during turn-OFF across all cases, validating the accuracy of the proposed SiC switching transient model.

3) Thermal Simulation Results: The thermal simulation was performed at 50 °C ambient, with ideal case cooling assumed to speed up steady-state convergence. Junction temperature responses were tested by alternating the operating conditions. As shown in Fig. 18, the proposed model can respond promptly to each condition change, with a steady-state temperature deviation of approximately 0.1 °C. The close agreement between the FPGA and LTspice simulation results validates the accuracy of the proposed thermal model and the LUT-based method in calculating the thermal behaviors.

V. Multipurpose HIL Testing

A. Introduction to Multipurpose HIL Testing

As shown in Fig. 19, due to limitations in the modeling accuracy of the RTS, conventional HIL testing in power electronics only considers electrical behaviors and is restricted to evaluating

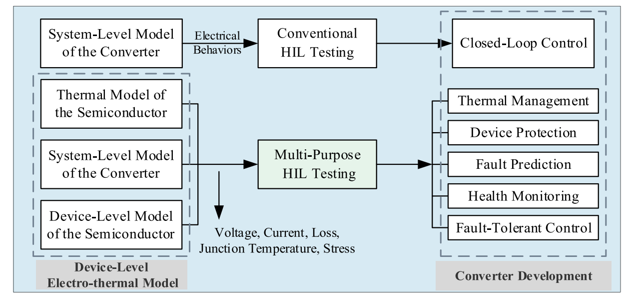

Fig. 19. Comparison of the conventional HIL testing and the proposed multipurpose HIL testing.

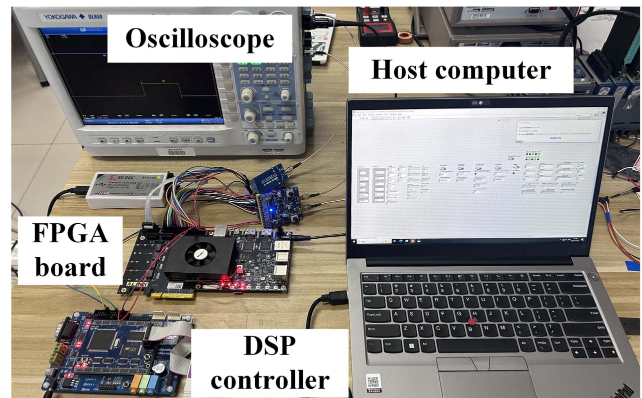

Fig. 20. Multipurpose HIL testing platform.

the closed-loop control performance of converters. By leveraging the proposed device-level electro-thermal RTS, which provides multidimensional information including the junction temperature, power loss, device stress, etc., the converter's behaviors can be more comprehensively characterized. This enables multipurpose HIL testing, which extends the capabilities of traditional HIL testing, supporting tasks such as design and validation of thermal management, device protection, fault prediction, health monitoring, and fault-tolerant control strategies in the converter's development cycle.

To give a case study, three groups of HIL testing were conducted, including a closed-loop control testing, a fault injection testing, and an active thermal control testing of an IBC converter. The HIL platform is shown in Fig. 20. It includes a host computer, a real-time simulator, a real-signal interface module, a DSP controller, and an oscilloscope. In addition, to further validate the behavior of the HIL system, a physical experimental platform with the same design parameters as the HIL simulation was constructed, as shown in Fig. 21. Due to laboratory constraints, the physical experiment can only be conducted under relatively low voltage. Therefore, the closed-loop testing and fault injection testing are conducted with a 48–72 V output in both the IBC prototype and HIL environment to validate the accuracy of the RTS. The 270 V high-voltage test is performed only on the HIL platform to test the active thermal control strategy, which further highlights the important role of multi-purpose HIL testing in the converter development cycle.

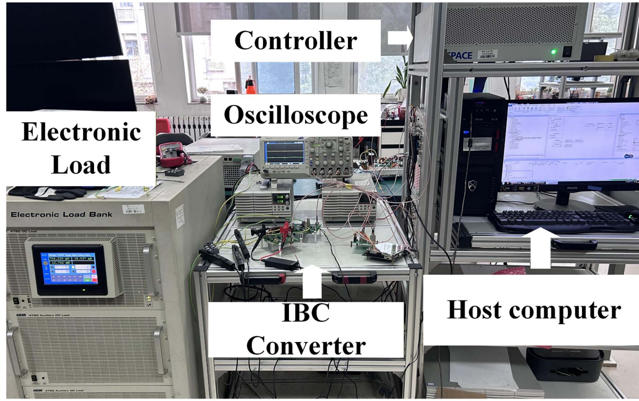

Fig. 21. Physical experimental platform of IBC.

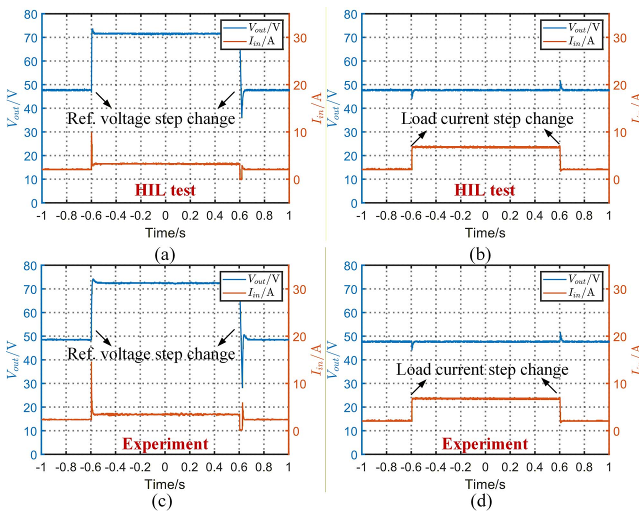

Fig. 22. Closed-loop testing results. (a) Responses of output voltage step change in HIL testing. (b) Responses of load current step change in HIL testing. (c) Responses of output voltage step change in physical experiment. (d) Responses of load current step change in physical experiment.

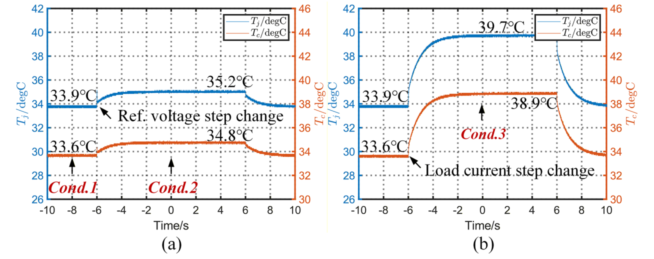

Fig. 23. Closed-loop testing thermal results. (a) Responses of output voltage step change. (b) Responses of load current step change.

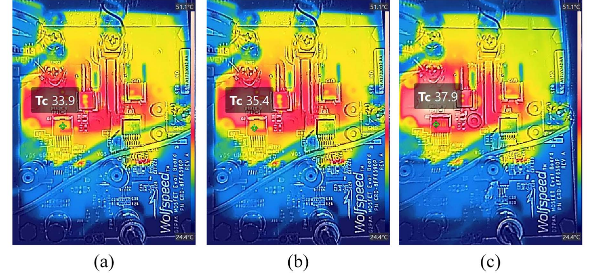

Fig. 24. Static temperature of real device under: (a) operating condition 1; (b) operating condition 2; (c) operating condition 3.

TABLE III
STATIC ERRORS OF CASE TEMPERATURE UNDER DIFFERENT OPERATING CONDITIONS

Number	Operating condition	HIL testing	Real device	Relative error
1	48 V, 1 A	33.6 °C	33.9 °C	0.9%
2	72 V, 1 A	34.8 °C	35.4 °C	1.7%
3	48 V, 3 A	38.9 °C	37.9 °C	2.6%
4	Fault injection	35.4 °C	37.1 °C	4.6%

B. Closed-loop Testing

The operating condition for the testing includes an input voltage of 24 V, a reference voltage of 48 V, a load current of 1 A, and a switching frequency of 50 kHz. The ambient temperature is 25 °C.

A dual-loop PI controller is implemented for the IBC. To evaluate the control performance, the reference voltage stepped from 48 to 72 V and then back to 48 V. The system responses, including the output voltage V_{out} and the input current I_{in} were observed. Subsequently, the load current I_{load} was stepped from 1 to 3 A and then returned to 1 A after a period of time.

The HIL testing results are shown in Fig. 22(a) and (b). When the reference voltage steps up, the output voltage rapidly tracks the change. To meet the increased output power demand, the input current rises accordingly. When the reference voltage drops back, an inverse response is observed. Similarly, when the load current steps up and down, the input current rapidly tracks the changes, with small fluctuations observed in the output voltage. The corresponding physical experimental results are shown in Fig. 22(c) and (d). It can be seen that the HIL testing results show a high degree of consistency with the experimental results.

One significant advantage of multipurpose HIL testing over conventional HIL testing is its ability to provide thermal information. As shown in Fig. 23, it provides the junction and case temperature responses of MOSFET S_{21}. To validate the thermal behaviors, static case temperature was measured using an infrared thermal camera for each operating condition, as shown in Fig. 24. The errors between HIL testing and real device are listed in Table III. It can be observed that the two sets of results show good agreement in terms of both absolute values and variation trend with changes in operating conditions.

The closed-loop HIL testing demonstrates that the proposed electro-thermal RTS can not only simulate the converter's electrical behaviors but also exhibit the temperature responses, providing valuable information in two domains for more comprehensive tuning and adjustment of the control strategies. It is also supposed to evaluate whether specific operating conditions may cause thermal overload, thereby defining safe operating boundaries for output voltage and load current.

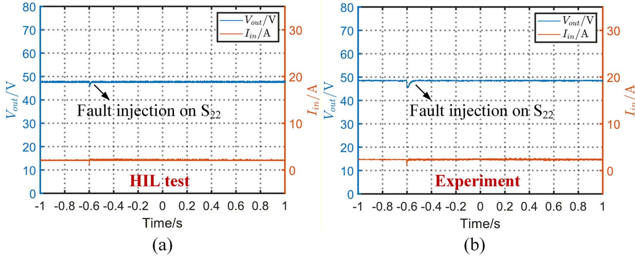

Fig. 25. Fault injection testing results. (a) Responses to the fault in HIL testing. (b) Response to the fault in physical experiment.

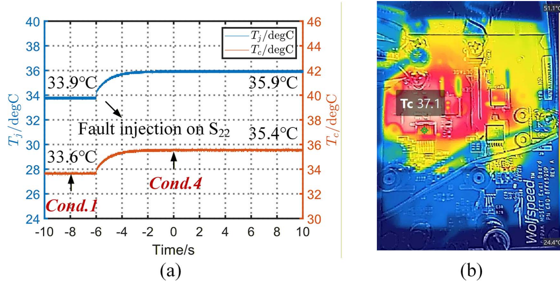

Fig. 26. Fault injection testing thermal results. (a) Response given by HIL testing. (b) Static case temperature of real device.

C. Fault Injection Testing

A fault is injected by disabling a failed switch S_{22} in the converter. Thus, only one phase can be used. As shown in Fig. 25(a) and Fig. 25(b), fault injection causes small transient fluctuations in both input current and output voltage. Although the system quickly recovers under the controller's regulation, the system ripple becomes larger. The responses of the HIL test and experiment also demonstrate excellent alignment.

Similarly, the HIL testing can provide thermal information. The junction temperature and case temperature of S_{21} in the healthy phase are shown in Fig. 26(a). At this operating point, the static case temperature given by HIL testing is 35.4 °C, while the real-device case temperature is 37.1 °C, as shown in Fig. 26(b). The static relative error is about 4.6%.

The fault injection HIL testing shows that the proposed electro-thermal RTS is capable of simulating the converter's behaviors under fault conditions. Both the electrical and thermal results show great agreement with the real device. It helps to observe the circuit's states during faults and then develop appropriate handling strategies to ensure safe operation. This enables further tasks such as device protection, health monitoring, and fault prediction in the converter's development.

D. Active Thermal Control Testing

The HIL platform validated under low-voltage conditions can be utilized to test strategies in high-voltage scenarios. The operating condition for this test includes an input voltage of 128 V, an output voltage of 270 V, a load current of 5 A, and a switching frequency of 50 kHz. The ambient temperature is assumed as 50 °C.

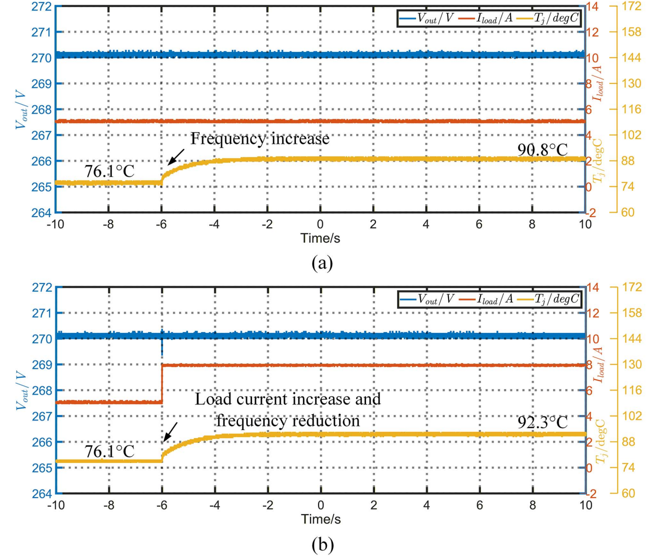

Fig. 27. Active thermal control testing results. (a) Increasing frequency to enhance control performance under thermal margin. (b) Reducing frequency. to mitigate temperature rise.

A commonly used active thermal control method is adjusting the switching frequency. It can be seen from Fig. 27(a) that the junction temperature remains relatively low under the baseline operating condition. This thermal margin allows for increasing switching frequency to 100 kHz to achieve better control performance and faster dynamic response, while maintaining the junction temperature within an acceptable range, as shown in Fig. 27(a). Similarly, when a higher load is required but excessive temperature rise is undesirable, the switching frequency can be reduced to alleviate thermal stress, trading off some control performance to ensure safety. When the load current increases from 5 to 8 A, the junction temperature increases from 76.1 to 106.7 °C. With active thermal control by reducing the switching frequency to 25 kHz, as shown in Fig. 27(b), the temperature rise caused by increasing the load current is reduced by 14.4 °C.

This test validates that the proposed electro-thermal RTS supports the design and validation of active thermal control strategies. It helps to explore a relatively optimal switching frequency, balancing the control performance and thermal behaviors, and enabling thermal management in the early design stage.

VI. Conclusion

Embracing the high-switching-frequency devices in RTS, such as SiC MOSFET, faces sharp conflicts between the modeling accuracy and simulation speeds. To provide a high-accuracy RTS of high-frequency PECs, a multilayer device-level electro-thermal RTS is proposed in this article. By implementing the system-level model and device-level model in two layers running at different rates collaboratively, the converter's electro-thermal behavior can be simulated in real time in conjunction with the accurate device-level transient characteristics. A multiple piecewise linear SiC MOSFET model is dedicated to the multilayer

electro-thermal RTS, which exhibits high accuracy against the LTspice model. Based on the electro-thermal RTS, a multipurpose HIL testing framework is further proposed. The power semiconductor's electro-thermal performance can be evaluated in real time, which provides a new validation merit in the HIL testing and speeds up the development cycles of power electronics.

The proposed RTS method provides an opportunity to directly integrate the device-level model of power semiconductors, especially the wide bandgap devices, into the existing RTS, which is initially impossible in the traditional way so far. The HIL platform can thus be updated to a multidomain testing environment, which will significantly promote the development efficiency of PECs in electrified transportation.

APPENDIX

This Appendix presents the detailed device-level model established in the case study discussed in this article.

The SiC MOSFET selected in the case study is the Wolfspeed C3M0060065J.

Predefine the coefficients as follows:

$$\alpha_{v_{ds}} = \frac{C_{dg} \cdot C_{gs} + C_{dg} \cdot C_{ds} + C_{ds} \cdot C_{gs}}{C_{dg} + C_{gs}} \tag{A1}$$

$$\alpha_{v_{gs}} = \frac{C_{dg} \cdot C_{gs} + C_{dg} \cdot C_{ds} + C_{ds} \cdot C_{gs}}{C_{dg} + C_{ds}} \tag{A2}$$

$$\beta = \frac{C_{dg}}{R_g \cdot (C_{dg} + C_{gs})} \tag{A3}$$

$$\gamma = \frac{C_{dg}}{C_{dg} + C_{ds}} \tag{A4}$$

$$\alpha_{rr} = \frac{R_{rr}}{L_s \cdot (1 + K \cdot R_{rr})} \tag{A5}$$

$$\delta = \frac{-R_{rr}}{L_{rr} \cdot (1 + K \cdot R_{rr})}. \tag{A6}$$

In stage 1, the state-space matrix can be derived as follows:

$$\begin{bmatrix} \dot{v}_{gs} \\ \dot{v}_{ds} \\ \dot{i}_{ds} \\ \dot{i}_{Lrr} \end{bmatrix} = \boldsymbol{A}_1 \begin{bmatrix} v_{gs} \\ v_{ds} \\ i_{ds} \\ i_{Lrr} \end{bmatrix} + \boldsymbol{B}_1 \begin{bmatrix} v_g \\ V_{ds_off} \\ I_L \\ 1 \end{bmatrix} \tag{A7}$$

where $V_{ds_off} = V_{d_on} + I_L \cdot R_{d_on} + V_{cc}$, $\boldsymbol{A_1}$ and $\boldsymbol{B_1}$ are given by the following:

$$\boldsymbol{A}_1 = \begin{bmatrix} \frac{-1}{\alpha_{v_{gs}} \cdot R_g} & 0 & \frac{\gamma}{\alpha_{v_{gs}}} & 0 \\ \frac{-\beta}{\alpha_{v_{ds}}} & 0 & \frac{1}{\alpha_{v_{ds}}} & 0 \\ 0 & \frac{-1}{L_s} & -\left(\frac{R_{d_on}}{L_s} + \alpha_{rr}\right) & -\alpha_{rr} \\ 0 & 0 & \delta & \delta \end{bmatrix} \tag{A8}$$

$$B_1 = \begin{bmatrix} \frac{1}{\alpha_{v_{gs}} \cdot R_g} & 0 & 0 & 0 \\ \frac{\beta}{\alpha_{v_{ds}}} & 0 & 0 & 0 \\ 0 & \frac{1}{L_s} & \alpha_{rr} & 0 \\ 0 & 0 & \frac{\alpha_{rr} \cdot L_s}{L_{rr}} & 0 \end{bmatrix}. \tag{A9}$$

In stage 2, the state-space matrix is the same as (A7), but $\boldsymbol{A_2}$ and $\boldsymbol{B_2}$are given by the following:

$$\boldsymbol{A}_2 = -\begin{bmatrix} \frac{1/R_g + \gamma \cdot k_2}{\alpha_{v_{gs}}} & \frac{\gamma \cdot k_3}{\alpha_{v_{gs}}} & \frac{-\gamma}{\alpha_{v_{gs}}} & 0 \\ \frac{\beta + k_2}{\alpha_{v_{ds}}} & \frac{k_3}{\alpha_{v_{ds}}} & \frac{-1}{\alpha_{v_{ds}}} & 0 \\ 0 & \frac{1}{L_s} & \frac{R_{d_on}}{L_s} + \alpha_{rr} & \alpha_{rr} \\ 0 & 0 & -\delta & -\delta \end{bmatrix} \tag{A10}$$

$$\boldsymbol{B}_2 = \begin{bmatrix} \frac{1}{\alpha_{v_{gs}} \cdot R_g} & 0 & 0 & -\frac{\gamma \cdot k_1}{\alpha_{v_{gs}}} \\ \frac{\beta}{\alpha_{v_{ds}}} & 0 & 0 & -\frac{k_1}{\alpha_{v_{ds}}} \\ 0 & \frac{1}{L_s} & \frac{-L_{rr} \cdot \delta}{L_s} & 0 \\ 0 & 0 & \delta & 0 \end{bmatrix} \tag{A11}$$

where k_1, k_2, and k_3 are given in (9).

In stage 3, i_{Lrr} is calculated by (A12), and i_{ds} is calculated by (A13)

$$\dot{i}_{L_{rr}} = -\frac{R_{rr} \cdot i_{L_{rr}}}{L_{rr}} \tag{A12}$$

$$i_{ds} = I_L + K \cdot R_{rr} \cdot i_{L_{rr}}. \tag{A13}$$

The state-space matrix of the other two variables can be derived as follows:

$$\begin{bmatrix} \dot{v}_{gs} \\ \dot{v}_{ds} \end{bmatrix} = \boldsymbol{A}_3 \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix} + \boldsymbol{B}_3 \begin{bmatrix} v_g \\ k_1 \\ i_{ds} \end{bmatrix} \tag{A14}$$

where $\boldsymbol{A_3}$ and $\boldsymbol{B_3}$ are given by the following:

$$\boldsymbol{A}_3 = \begin{bmatrix} -\frac{1/R_g + \gamma \cdot k_2}{\alpha_{v_{gs}}} & -\frac{\gamma \cdot k_3}{\alpha_{v_{gs}}} \\ \frac{-\beta - k_2}{\alpha_{v_{ds}}} & \frac{-k_3}{\alpha_{v_{ds}}} \end{bmatrix} \tag{A15}$$

$$\boldsymbol{B}_3 = \begin{bmatrix} \frac{1}{R_g \cdot \alpha_{v_{gs}}} & -\frac{\gamma}{\alpha_{v_{gs}}} & \frac{\gamma}{\alpha_{v_{gs}}} \\ \frac{\beta}{\alpha_{v_{ds}}} & \frac{-1}{\alpha_{v_{ds}}} & \frac{1}{\alpha_{v_{ds}}} \end{bmatrix}. \tag{A16}$$

The state-space matrices above all follow the form:

$$\dot{\boldsymbol{X}} = \boldsymbol{AX} + \boldsymbol{Bu}. \tag{A17}$$

Applying the backward Euler method, their state variables update matrices can be given by the following:

$$\boldsymbol{X}^{n+1} = (\boldsymbol{I} - h\boldsymbol{A})^{-1} X^n + h(\boldsymbol{I} - h\boldsymbol{A})^{-1} \boldsymbol{Bu}. \tag{A18}$$

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