Iterative Learning Adaptive Active Damping Based DC-Link Capacitor Ripple Current Suppression Strategy for PMSM Drives

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***Abstract*—Fixed damping strategies are inadequate for suppressing the dc-link capacitor ripple current in permanent magnet synchronous motor (PMSM) drives across a wide power range. Therefore, a ripple current suppression strategy based on adaptive active damping with iterative learning is proposed. The strategy indirectly characterizes the ripple current by the dc-link voltage, avoiding the need for additional sensors or current reconstruction algorithms. First, the limitation of fixed damping in suppressing the ripple current is revealed using the equivalent admittance model. Then, an adaptive suppression mechanism based on P-type iterative learning is constructed. The balance between the convergence speed and the disturbance rejection capability is achieved by introducing a forgetting factor. On this basis, the initial admittance parameters are dynamically matched to improve the iterative efficiency under variable-speed conditions. The analysis of convergence and parameter sensitivity demonstrates that the proposed strategy exhibits rapid convergence, high accuracy, and strong robustness. Finally, the effectiveness of the proposed strategy is verified on the experimental platform.**

***Index Terms*—Active damping, capacitor ripple current, parameter adaptation, permanent magnet synchronous motor (PMSM).**

I. Introduction

PERMANENT magnet synchronous motor (PMSM) has been extensively utilized in various fields, owing to its advantages of high power density, high power factor, and high efficiency [1], [2], [3], [4], [5]. In motor drive systems, electrolytic capacitors are typically used to balance power and stabilize dc-link voltage [6], [7], [8]. However, the poor tolerance of electrolytic capacitors to ripple current makes them a critical factor limiting system reliability. The statistics show that over 60% of drive failures are caused by the aging of electrolytic capacitors [9], [10]. Therefore, the suppression of capacitor ripple current is key to improving the operational reliability of the drive system.

The capacitor ripple current can be categorized into high-frequency and low-frequency components. Due to the decrease in equivalent series resistance (ESR) with increasing frequency, electrolytic capacitors exhibit relatively poor tolerance for low-frequency ripple current [11]. Typically, the suppression strategies for low-frequency ripple current can be categorized into hardware methods and software methods. The hardware methods suppress the ripple current by modifying the hardware topology [12], [13], [14], [15], [16]. In [15], a boost-based active power decoupling circuit (APDC) with voltage complementary was proposed, which suppressed the capacitor ripple current through complementary control of the decoupling capacitor and the output capacitor. On this basis, an APDC with a symmetric structure was proposed [16]. The APDC had the same mathematical model when absorbing or releasing the grid pulsating power, which reduced the control complexity. However, the additional hardware often leads to a reduction in system power density and cost-effectiveness.

In order to address the limitations of hardware methods, many scholars explore solutions based on software algorithms. The software methods can be categorized into harmonic injection methods and active damping methods. The harmonic injection methods suppress the ripple current by directly injecting harmonics [17], [18], [19]. In [17], a motor reactive power injection strategy based on the constant-torque trajectory was proposed, simultaneously suppressing both the ripple current and the torque fluctuation. In [18], the third and fifth harmonic currents were injected together into the input current. This approach reduced the peak-to-average ratio of the output current with a power factor above 0.9. In [19], an adaptive harmonic injection strategy for the power factor correction (PFC) converter was proposed, which reduced the ripple current under different power levels. However, the effectiveness of such strategies in suppressing ripple current is often limited by the controller bandwidth.

The active damping methods adjust the overall system characteristics by establishing the equivalent damping model, which offers clear physical insight and facilitates parameter design

Received 17 October 2025; revised 7 December 2025; accepted 21 December 2025. Date of publication 25 December 2025; date of current version 20 March 2026. This work was supported in part by the Research Fund for the National Natural Science Foundation of China under Grant 52421004, Grant 52125701, and Grant 52307198, in part by grants from the Delta Power Electronics Science & Technology Educational Development Program of Delta Group under Grant DREG2025008, and in part by the Open Fund Project of Key Laboratory of Electric Drives & Propulsion Technology, Ministry of Education (Harbin Institute of Technology). Recommended for publication by Associate Editor M. Monfared. *(Corresponding author: Gaolin Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3648140.

Digital Object Identifier 10.1109/TPEL.2025.3648140

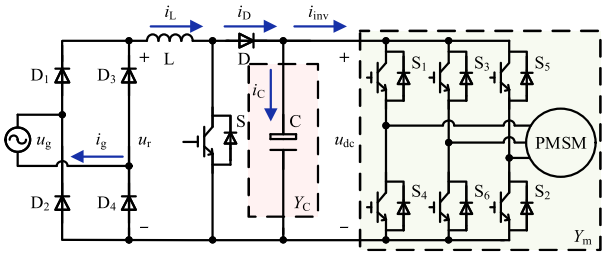

Fig. 1. Topology of PMSM drive fed by the boost PFC converter.

[20], [21], [22], [23]. In order to improve stability, an active damping strategy based on inductor current feedback was proposed, suppressing the LC resonance by connecting the virtual resistor in series [20]. In [21], the inverter input impedance was reshaped by connecting the virtual admittance in parallel, with the digital control delay reduced through the oversampling technology. On this basis, a super-twisting sliding mode-based disturbance observer was proposed to estimate the rectifier output current, thereby further reducing the hardware cost [22]. In [23], a high-admittance path for the capacitor ripple current was constructed by connecting the virtual admittance in parallel. However, the active damping methods with fixed parameters often lack adaptability under different power conditions.

Therefore, an adaptive regulation mechanism is necessary for the real-time adjustment of damping parameters under different operating conditions [24], [25], [26], [27], [28]. In [25], the grid current quality was characterized by the harmonic factor, and an *LC* resonance suppression strategy based on adaptive virtual admittance reshaping was proposed. In [26], a cooperative control strategy based on adaptive parameter tuning and virtual impedance injection was proposed, which could effectively suppress the harmonics under different power conditions. However, it is difficult for the fixed-step adjustment mechanism to balance the convergence speed and steady-state accuracy. Therefore, an adaptive parameter identification strategy based on gradient descent optimization was proposed, which alleviated the performance degradation caused by the model mismatch [27]. In [28], the compensation current was adaptively generated through the indirect iterative learning mechanism, thus effectively suppressing the torque ripple under different power conditions. They bring the inspiration for the adaptive suppression of capacitor ripple current. The core advantage of iterative learning control lies in its systematic use of historical data from repetitive tasks. This enables precise learning and compensation of periodic uncertainties, enhancing the system's transient performance and tracking accuracy.

Traditional strategies often struggle to suppress the capacitor ripple current effectively across a wide power range. To address this issue, an adaptive active damping strategy based on iterative learning controller (ILC) is proposed in this article. By establishing the system equivalent admittance model, the limitation of fixed damping in traditional strategies is revealed. The proposed strategy characterizes the ripple current through the dc-link voltage, thereby avoiding the need for complex current reconstruction. Meanwhile, a P-type ILC with the forgetting factor is constructed to balance the convergence speed and the disturbance rejection. On this basis, the initial admittance parameters are dynamically matched according to the motor power, thus improving the iterative efficiency under variable-speed conditions. In addition, the convergence and parameter sensitivity are analyzed to evaluate the convergence boundary and steady-state accuracy. Finally, the effectiveness of the proposed strategy is verified on the experimental platform of PMSM drive fed by the boost PFC converter.

II. Limitations Analysis in Ripple Current Suppression Strategies With Fixed Damping Parameters

The topology of PMSM drive fed by the boost PFC converter is shown in Fig. 1. Under the action of the PFC converter, the capacitor current fluctuates at twice the grid frequency. The amplitude of second-harmonic ripple current (SHRC) can be expressed as

$$I_{C2} = I_{D2}\left|\frac{Y_C(j\omega_2)}{Y_C(j\omega_2)+Y_m(j\omega_2)}\right| = \frac{P_m}{U_{\rm dc}}\left|\frac{j\omega_2 C}{j\omega_2 C+(1+j\omega_2 C R_C)Y_m(j\omega_2)}\right| \quad (1)$$

where Y_C, j, C, R_C, I_{D2}, ω_2, P_m, and $U_{\rm dc}$ represent the dc-link capacitor admittance, the imaginary unit, the capacitance, the ESR, the SHRC amplitude of diode, twice the grid angular frequency, the motor power, and the component of the dc-link voltage, respectively. Y_m represents the motor input admittance, as shown in (2), and the detailed derivation process of (2) is provided in [29]. In (2), $I_{\rm inv}$ and $U_{{\rm dc}\_e}$ represent the dc components of the inverter current and the equivalent sampled dc-link voltage (delay of $1.5T_s$), respectively. R_s, ω_e, and T_s represent the stator resistance, the electrical angular velocity, and the switching period, respectively. $L_{d,\ q}$ and $G_{d,\ q}$ represent the *dq*-axis inductances and the transfer functions of *dq*-axis current controllers, respectively. $U_{d,\ q{\rm ref}}$, $U_{d,\ q}$, and $I_{d,\ q}$ represent the dc components of *dq*-axis reference voltages, voltages, and currents, respectively,

$$Y_m(s) = -\frac{I_{\rm inv}}{U_{\rm dc}} + \frac{3\left(1-e^{-1.5T_s s}\right)}{2U_{\rm dc}U_{{\rm dc}\_e}} \left\{\begin{array}{l}\left[\frac{(R_s+L_d s)U_{d{\rm ref}}}{R_s+L_d s+G_d(s)} - \frac{\omega_e L_q U_{q{\rm ref}}}{R_s+L_q s+G_q(s)}\right] I_d + \frac{U_{d{\rm ref}}\ U_d}{R_s+L_d s+G_d(s)} + \\ \left[\frac{\omega_e L_d U_{d{\rm ref}}}{R_s+L_d s+G_d(s)} + \frac{(R_s+L_q s)U_{q{\rm ref}}}{R_s+L_q s+G_q(s)}\right] I_q + \frac{U_{q{\rm ref}}\ U_q}{R_s+L_q s+G_q(s)}\end{array}\right\}. \quad (2)$$

In order to suppress the SHRC, a high-admittance path for the ripple current was constructed by connecting the virtual admittance in parallel [23]. The equivalent model and control block diagram are shown in Fig. 2. The parallel virtual admittance is zero except for the second-harmonic component, and the virtual admittance at twice the grid frequency can be expressed as

$$Y_v(j\omega_2) = |Y_v|\cos\theta_v + j|Y_v|\sin\theta_v \quad (3)$$

where $|Y_v|$ and θ_v represent the amplitude and the phase of virtual admittance at twice the grid frequency, respectively.

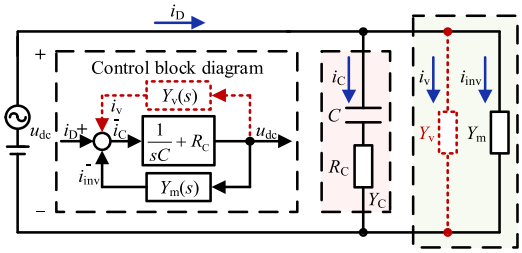

Fig. 2. Ripple current suppression strategy with the fixed virtual admittance.

TABLE I
PARAMETERS OF EXPERIMENTAL PLATFORM

Parameter	Value	Parameter	Value
Grid voltage	220 Vrms	Grid frequency	50 Hz
DC-link voltage	350 V	Switching frequency	10 kHz
Stator resistance	0.78 Ω	D-axis inductance	5.4 mH
Flux linkage	0.11 Wb	Q-axis inductance	8.4 mH
Rotational inertia	0.3 g·m²	Number of pole pairs	3
Rated power	1200 W	Controller bandwidth	500 Hz
Capacitance	379.32 μF	ESR	303.51 mΩ

According to (3), the virtual admittance current consists solely of the second-harmonic component, which can be expressed as

$$i_{\mathrm{v}} = |Y_{\mathrm{v}}| U_{\mathrm{dc2}} \cos(\omega_2 t + \theta_{\mathrm{v}} + \theta_{\mathrm{udc2}}) \tag{4}$$

where u_{dc}, U_{dc2}, and θ_{udc2} represent the dc-link voltage, the amplitude of dc-link second-harmonic voltage, and the phase of dc-link second-harmonic voltage, respectively.

Assuming the high-frequency components of dc-link voltage are neglected, the admittance power can be calculated as

$$p_v = i_v u_{\mathrm{dc}} = |Y_v| U_{\mathrm{dc}} U_{\mathrm{dc2}} \cos(\omega_2 t + \theta_v + \theta_{udc2}). \tag{5}$$

In order to generate the admittance power, the *dq*-axis admittance voltages are added to the original *dq*-axis reference voltages. In addition, the admittance voltage vector is aligned with the stator current vector, and the *dq*-axis admittance voltages can be derived as

$$\begin{cases} u_{v\_\mathrm{dref}} = \frac{2|Y_v| U_{\mathrm{dc2}} U_{\mathrm{dc}} i_d}{3(i_d^2+i_q^2)} \cos(\omega_2 t + \theta_v + \theta_{udc2}) \\ u_{v\_\mathrm{qref}} = \frac{2|Y_v| U_{\mathrm{dc2}} U_{\mathrm{dc}} i_q}{3(i_d^2+i_q^2)} \cos(\omega_2 t + \theta_v + \theta_{udc2}) \end{cases} \tag{6}$$

where i_d and i_q represent the *dq*-axis currents, respectively.

Combining (1) with (2), the SHRC amplitude of DC-link capacitors after admittance reshaping can be expressed as

$$I_{C2\_v} = \frac{P_m}{U_{\mathrm{dc}}} \left| \frac{Y_C(j\omega_2)}{Y_C(j\omega_2) + Y_m(j\omega_2) + Y_v(j\omega_2)} \right| \tag{7}$$

where i_d and i_q represent the *dq*-axis currents, respectively.

According to (7), the SHRC of dc-link capacitors can be effectively suppressed by selecting appropriate admittance parameters. With an adequate safety margin to ensure electrolytic capacitor longevity, the target SHRC amplitude I_{C2_T} is set to 50% (1.287 A) of the rated ripple current amplitude specified in the datasheet.

The drive parameters are given in Table I. The virtual admittance phase θ_v and the motor power P_m are normalized with base values set to 2 π and the rated power of 1200 W, respectively. According to (7), the SHRC amplitude after admittance reshaping

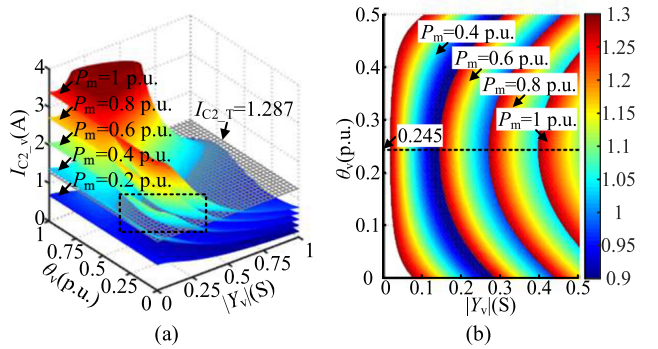

Fig. 3. Limitations of fixed damping parameters. (a) Overall view. (b) Zoomed top view.

can be obtained under different $|Y_v|$ and θ_v, as shown in Fig. 3. In order to reduce the influence of admittance power on the motor side, the virtual admittance parameters with the smallest amplitude are usually selected [23]. In Fig. 3(a), the suppression strategy is not needed because I_{C2_v} is less than I_{C2_T} under light load conditions. However, since I_{C2_v} increases with P_m, the ripple current suppression is progressively enhanced once I_{C2_v} exceeds I_{C2_T}. In Fig. 3(b), as P_m varies, the optimal admittance phase remains stable around 0.245 p.u., while the admittance amplitude changes significantly. Therefore, the suppression strategy with the fixed virtual admittance amplitude is difficult to meet the suppression requirements under different power conditions.

III. Ripple Current Suppression Strategy Based on Adaptive Active Damping

A. Adaptive Admittance Method for Drive System

The proposed SHRC suppression strategy based on adaptive active damping is shown in Fig. 4. The strategy mainly consists of three parts: the iterative learning mechanism construction, the initial admittance parameter matching, and the admittance voltage generation. First, the ripple current is indirectly characterized by the dc-link voltage, and an adaptive suppression mechanism based on the ILC is constructed. Then, the initial admittance parameters are dynamically matched to improve the iterative efficiency under different power conditions. On this basis, the admittance voltage is calculated based on the virtual admittance parameters. Finally, the admittance voltage commands are added to the original voltage commands, thereby achieving the SHRC suppression of dc-link capacitors.

In the proposed strategy, a power threshold corresponding to the target ripple current is predefined. During system operation, the input power is calculated and compared against this threshold. The proposed strategy is disabled when the power is below the threshold and enabled when the power exceeds it. In addition, the virtual admittance phase is set 0.245 p.u. based on the results in Fig. 3(b). It indicates that the phase of virtual admittance current leads the dc-link second-harmonic voltage. Therefore, in order to calculate the virtual admittance current, the future value of dc-link voltage is replaced with the historical value from the previous cycle.

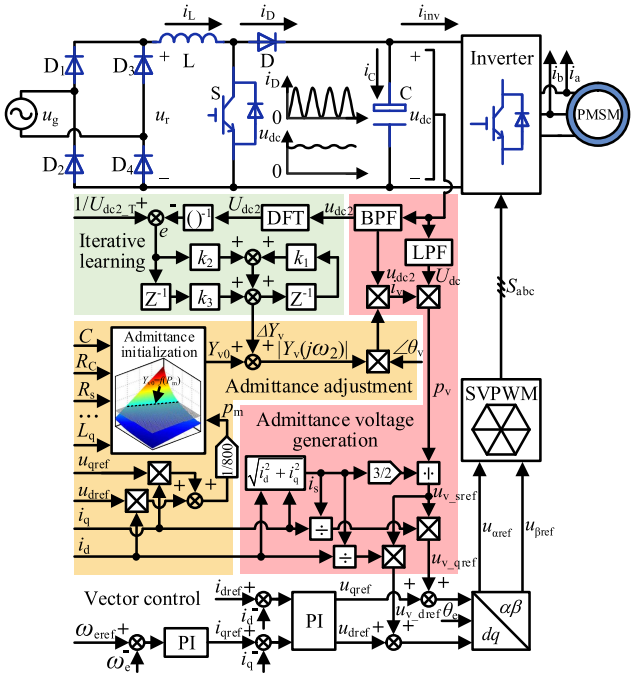

Fig. 4. Block diagram of the proposed SHRC suppression strategy based on adaptive active damping.

To avoid the increase in system complexity caused by the additional sensor or current reconstruction algorithm, the capacitor current can be characterized by the dc-link voltage. The target amplitude of the dc-link second-harmonic voltage can be calculated as

$$U_{\mathrm{dc2\_}T}=\frac{I_{C2\_T}}{|Y_C(j\omega_2)|}=I_{C2\_T}\left|\frac{1+j\omega_2CR_C}{j\omega_2C}\right|. \tag{8}$$

The optimal admittance phase is less affected by the power in the process of virtual admittance reshaping. Therefore, combining (7) with (8), the reciprocal of the dc-link second-harmonic voltage amplitude can be expressed as

$$\begin{aligned}\frac{1}{U_{\mathrm{dc2}}}&=\frac{U_{\mathrm{dc}}}{P_m}\left[|Y_C(j\omega_2)+Y_m(j\omega_2)+Y_v(j\omega_2)|\right]\\&=\frac{U_{\mathrm{dc}}}{P_m}\left[|Y_C(j\omega_2)+Y_m(j\omega_2)|+|Y_v|\right].\end{aligned} \tag{9}$$

On this basis, an ILC-based suppression mechanism for the dc-link second-harmonic voltage is constructed. The virtual admittance amplitude is adaptively adjusted under different power conditions by introducing the closed-loop feedback. In order to balance the convergence speed and the disturbance rejection, a P-type ILC with the forgetting factor is constructed, and its iterative learning law can be designed as

$$\begin{cases}\Delta Y_{vn}(t)=k_1\Delta Y_{vn-1}(t)+k_2e_n(t)+k_3e_{n-1}(t)\\ e_n(t)=\frac{1}{U_{\mathrm{dc2\_}T}}-\frac{1}{U_{\mathrm{dc2}n}(t)}\\ \frac{1}{U_{\mathrm{dc2}n}(t)}=\frac{U_{\mathrm{dc}}}{P_m}\begin{bmatrix}|Y_C(j\omega_2)+Y_m(j\omega_2)|+\\ Y_{\mathrm{v0}}+\Delta Y_{\mathrm{vn}}(t)\end{bmatrix}\end{cases} \tag{10}$$

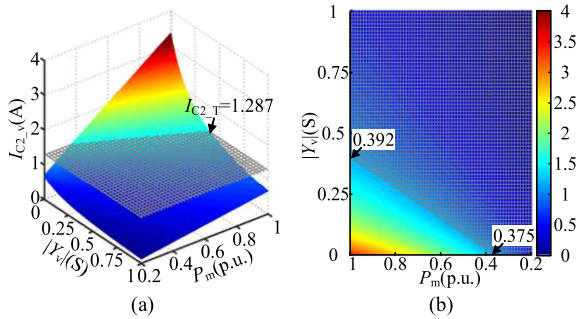

Fig. 5. Analysis of the virtual admittance amplitude initialization. (a) Overall view. (b) Top view.

where k_1 is the forgetting factor. k_2 and k_3 are the ILC gains. ΔY_{vn}, e_n, $U_{\mathrm{dc}2n}$, and Y_{v0} represent the nth admittance correction, iterative output, iterative error, amplitude of the dc-link second-harmonic voltage, and the initial admittance amplitude, respectively. n is the number of iterations.

To reduce the number of iterations, it is necessary to initialize the virtual admittance amplitude to an ideal value. The drive parameters are given in Table I. The virtual admittance phase is set to 0.245 p.u. According to (7), the SHRC amplitude after admittance reshaping can be obtained for different $|Y_v|$ and P_m, as shown in Fig. 5. In Fig. 5(a), when P_m remains unchanged, I_{C2_v} increases with $|Y_v|$. When $|Y_v|$ remains unchanged, I_{C2_v} increases with P_m. In Fig. 5(b), when I_{C2_v} is equal to I_{C2_T}, the ideal amplitude of the virtual admittance decreases approximately linearly as P_m increases. Thus, by applying the least squares method to fit the data points (P_{mi}, $|Y_{vi}|$), the initial amplitude of the virtual admittance can be expressed as

$$Y_{v0}=f(P_m)=\frac{\sum(P_{mi}-\bar{P}_m)(|Y_{vi}|-\bar{Y}_v)}{\sum(P_{mi}-\bar{P}_m)^2}(P_m-\bar{P}_m)+\bar{Y}_v \tag{11}$$

where $\bar{P}$ m and $\bar{Y}$ v represent the average values of P_{mi} and $|Y_{vi}|$, respectively. After normalization, the motor power P_{m} can be expressed as

$$P_m=\frac{3(u_{\mathrm{dref}}i_d+u_{\mathrm{qref}}i_q)}{2P_{\mathrm{based}}} \tag{12}$$

where P_{based} and $u_{d,\ \mathrm{qref}}$ represent the motor power base value and the dq-axis reference voltages, respectively.

B. Convergence Analysis of Suppression Algorithm

To analyze the convergence of the suppression algorithm, according to (10), the nth iterative error of the dc-link second-harmonic voltage can be expressed as

$$\begin{cases}e_n(t)=\frac{1}{U_{\mathrm{dc2\_}T}}-A(t)\begin{bmatrix}B(t)+k_1\Delta Y_{vn-1}(t)+\\ k_2e_n(t)+k_3e_{n-1}(t)\end{bmatrix}\\ A(t)=\frac{U_{\mathrm{dc}}}{P_m}\\ B(t)=|Y_C(j\omega_2)+Y_m(j\omega_2)|+Y_{v0}\end{cases}. \tag{13}$$

Combining (10) with (13), the nth iterative error of the dc-link second-harmonic voltage can be simplified as

$$\begin{cases} e_n(t) = C(t)e_{n-1}(t) + D(t) \\ C(t) = \frac{k_1 - k_3 A(t)}{1 + k_2 A(t)} \\ D(t) = \frac{1-k_1}{1+k_2 A(t)} E(t) \\ E(t) = \frac{1}{U_{\mathrm{dc2\_T}}} - A(t)B(t) \end{cases}. \tag{14}$$

The infinite norm on both sides of (14) can be further expressed as

$$\begin{aligned} &\|e_n(t)\|_\infty \\ &= \|C(t)e_{n-1}(t) + D(t)\|_\infty \\ &\le \|C(t)e_{n-1}(t)\|_\infty + \|D(t)\|_\infty \\ &= |C(t)|\,\|e_{n-1}(t)\|_\infty + |D(t)|_{\max} \\ &\le |C(t)|^2 \|e_{n-2}(t)\|_\infty + [1 + |C(t)|]\,|D(t)|_{\max} \\ &\le |C(t)|^n \|e_0(t)\|_\infty + \left[1 + \cdots + |C(t)|^{n-1}\right] |D(t)|_{\max} \\ &= |C(t)|^n \|e_0(t)\|_\infty + \frac{1 - |C(t)|^n}{1 - C(t)} |D(t)|_{\max}. \end{aligned} \tag{15}$$

According to (15), the sufficient condition for the convergence of the iterative learning algorithm can be expressed as

$$|C(t)| = \left|\frac{k_1 - k_3 A(t)}{1 + k_2 A(t)}\right| = \left|\frac{k_1 P_m - k_3 U_{\mathrm{dc}}}{P_m + k_2 U_{\mathrm{dc}}}\right| < 1. \tag{16}$$

Combining (13), (14), (15), and (16), when the number of iterations n tends to infinity, the steady-state error of the algorithm E_{ss} can be expressed as

$$\begin{cases} E_{\mathrm{ss}} = \lim\limits_{n\to\infty} \|e_n(t)\|_\infty = \frac{|D(t)|_{\max}}{1 - |C(t)|} = k_{\mathrm{ess}} |E(t)|_{\max} \\ k_{\mathrm{ess}} = \frac{(1-k_1)P_m}{|P_m + k_2 U_{\mathrm{dc}}| - |k_1 P_m - k_3 U_{\mathrm{dc}}|} \end{cases} \tag{17}$$

where k_{ess} represents the steady-state error coefficient, which is related to k_1, k_2, and k_3. Conversely, $|E(t)|_{\max}$ depends solely on the system admittance model accuracy and initial parameters.

The influence of the forgetting factor and the ILC gains on the algorithm convergence is analyzed as follows. The drive parameters are given in Table I. When the system operates at the rated power, the steady-state error coefficient for different k_2 and k_3 can be obtained from (17), as shown in Fig. 6(a). In Fig. 6(a), when k_2 and k_3 remain unchanged, k_{ess} decreases as k_1 increases. To ensure the steady-state convergence accuracy while maintaining satisfactory convergence speed, k_1 is set to 0.95, which is a typical empirical value in the ILC. On this basis, according to (16), the convergence range of the algorithm under different power conditions can be obtained as shown in Fig. 6(b). In Fig. 6(b), when k_2 and P_m remain unchanged, with k_3 increasing, $|C(t)|$ first decreases and then increases. When k_3 and P_m remain unchanged, $|C(t)|$ decreases as k_2 increases. When k_2 and k_3 remain unchanged, the convergence region gradually decreases as P_m decreases. Therefore, the convergence of the suppression algorithm can be guaranteed by reasonably setting the k_2 and k_3 parameters under light load conditions.

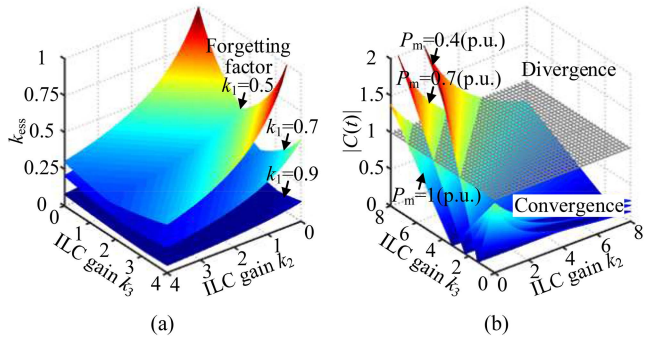

Fig. 6. Convergence analysis of the suppression algorithm. (a) Steady-state error. (b) Convergence range.

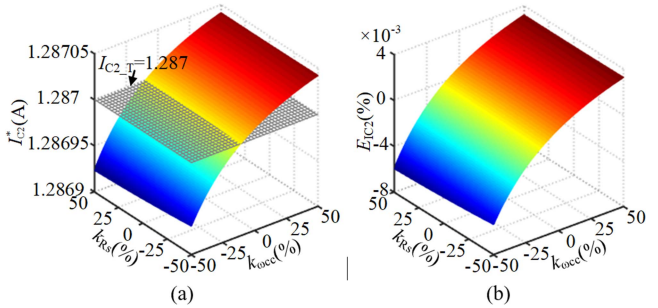

Fig. 7. Influence of ω_{cc} and R_s on the SHRC suppression. (a) SHRC amplitude. (b) Percentage error.

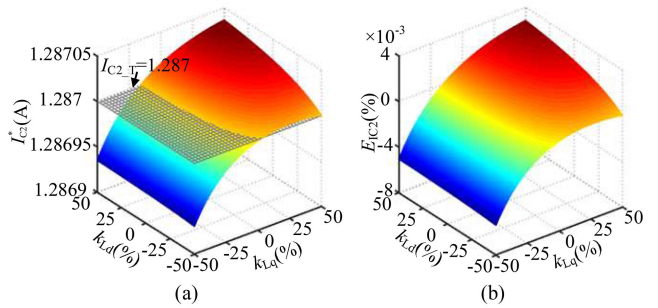

Fig. 8. Influence of L_d and L_q on the SHRC suppression. (a) SHRC amplitude. (b) Percentage error.

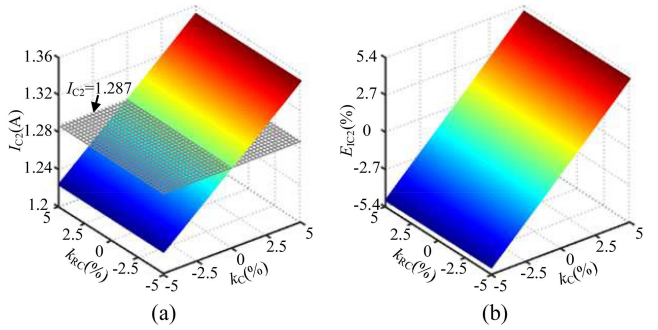

Fig. 9. Influence of C and R_C on the SHRC suppression. (a) SHRC amplitude. (b) Percentage error.

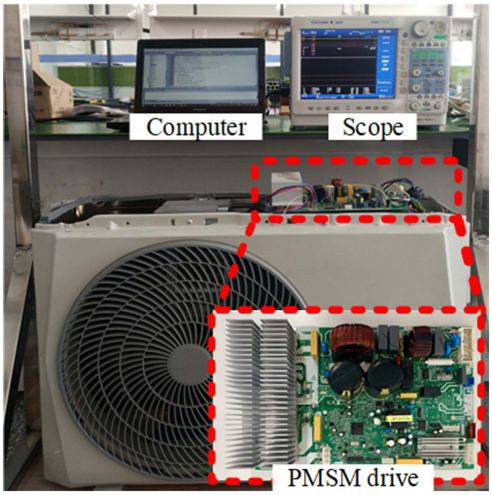

Fig. 10. Experimental platform of permanent magnet compressor system fed by the boost PFC converter.

C. Parameter Sensitivity Analysis

In practical systems, the established equivalent admittance model deviates from the actual system, owing to non-idealities including limited motor controller bandwidth and parametric nonlinearities. Therefore, it is necessary to analyze the impact of parameter sensitivity on the suppression performance for the SHRC. Combining (8), (10), and (17), the SHRC amplitude after convergence can be expressed as

$$I_{C2} = \frac{U_{\mathrm{dc2\_T}}\,|Y_{\mathrm{C}}(j\omega_2)|}{1 - U_{\mathrm{dc2\_T}} k_{\mathrm{ess}} |E(t)|_{\max}} = \frac{P_m U_{\mathrm{dc2\_T}}\,|Y_C(j\omega_2)|}{P_m - k_{\mathrm{ess}} \left| \begin{matrix} P_m - U_{\mathrm{dc2\_T}} U_{\mathrm{dc}} \times \\ [|Y_C(j\omega_2) + Y_m(j\omega_2)| + Y_{v0}] \end{matrix} \right|_{\max}}. \quad (18)$$

According to (18), the steady-state amplitude of the SHRC depends on the motor admittance accuracy. Therefore, to characterize the influence of non-ideal factors on the motor admittance, the related system parameter N_1 is defined as

$$N_1 = N(1 + k_N) \quad (19)$$

where N represents one of ω_{cc}, R_s, L_d, L_q, C, and R_C. k_N represents the change rate of N considering the influence of non-ideal factors. $k_{\omega cc}$, k_{Rs}, k_{Ld}, and k_{Lq} are set to $\pm 50\%$. k_C and k_{RC} are set to $\pm 5\%$.

Substituting (19) into (18), the steady-state amplitude of the SHRC considering the influence of non-ideal factors can be expressed as

$$I^*_{C2} = \frac{P_m U_{\mathrm{dc2\_T}}\,|Y_C(j\omega_2)|}{P_m - k_{\mathrm{ess}} \left| \begin{matrix} P_m - U_{\mathrm{dc2\_T}} U_{\mathrm{dc}} \times \\ [|Y_C(j\omega_2) + Y^*_m(j\omega_2)| + Y_{v0}] \end{matrix} \right|_{\max}}. \quad (20)$$

where Y^*_m represents the motor admittance considering the influence of nonideal factors.

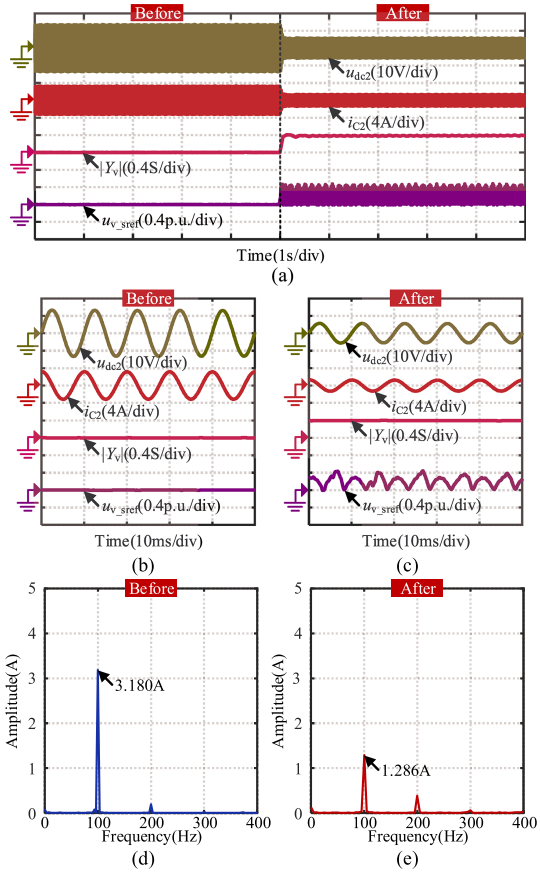

Fig. 11. Experimental results at the rated power (1200 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

According to (18) and (20), the percentage error caused by non-ideal factors can be expressed as

$$E_{\mathrm{IC2}} = \left(\frac{I^*_{C2}}{I_{C2\_\mathrm{T}}} - 1 \right) \times 100\%. \quad (21)$$

The parameter sensitivity of the algorithm is analyzed as follows. k_1, k_2, and k_3 are set to 0.95, 4, and 2, respectively. Under different $k_{\omega cc}$, k_{Rs}, k_{Ld}, k_{Lq}, k_C, and k_{RC}, according to (20) and (21), the SHRC amplitude I^*_{C2} and the percentage error E_{IC2} can be obtained, as shown in Figs. 7–9, respectively. In Fig. 7(a), when $k_{\omega cc}$ remains unchanged, I^*_{C2} is not significantly affected by k_{Rs}. When k_{Rs} remains unchanged, I^*_{C2} increases with $k_{\omega cc}$. In Fig. 7(b), when ω_{cc} and R_s change within $\pm 50\%$, the percentage error E_{IC2} is less than 0.004%. In Fig. 8(a), when k_{Ld} remains unchanged, with k_{Lq} increasing, I^*_{C2} first increases and then decreases. When k_{Lq} remains unchanged, I^*_{C2} increases with k_{Ld}. In Fig. 8(b), when L_d and L_q change within $\pm 50\%$, the percentage error E_{IC2} is less than 0.004%. In conclusion, the SHRC suppression algorithm is robust against nonideal factors such as controller bandwidth and motor parameter nonlinearity. Therefore, the constant nameplate values can be directly used for the motor parameters in the proposed strategy. However, since the ripple current is characterized by the dc-link voltage, the suppression effect is relatively sensitive to variation of dc-link

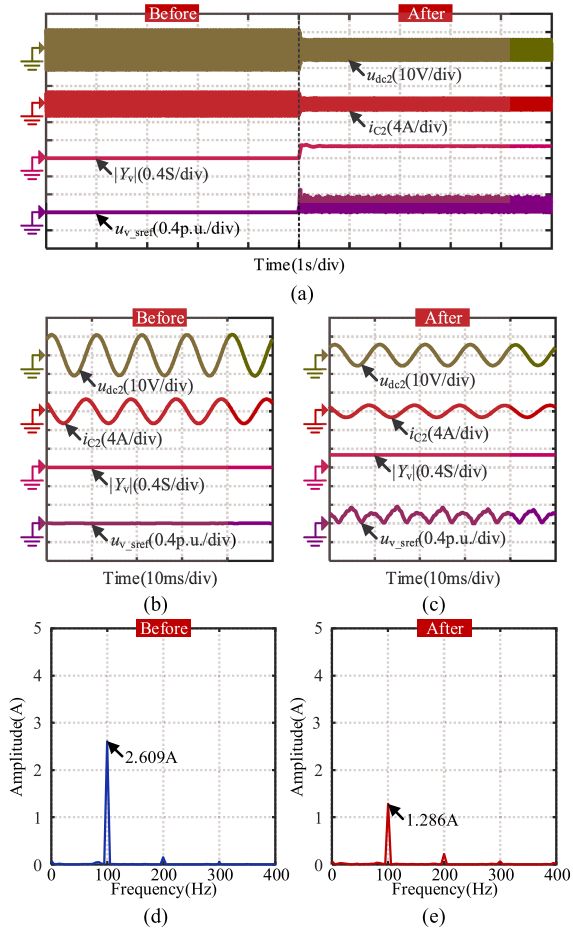

Fig. 12. Experimental results at 80% rated power (960 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

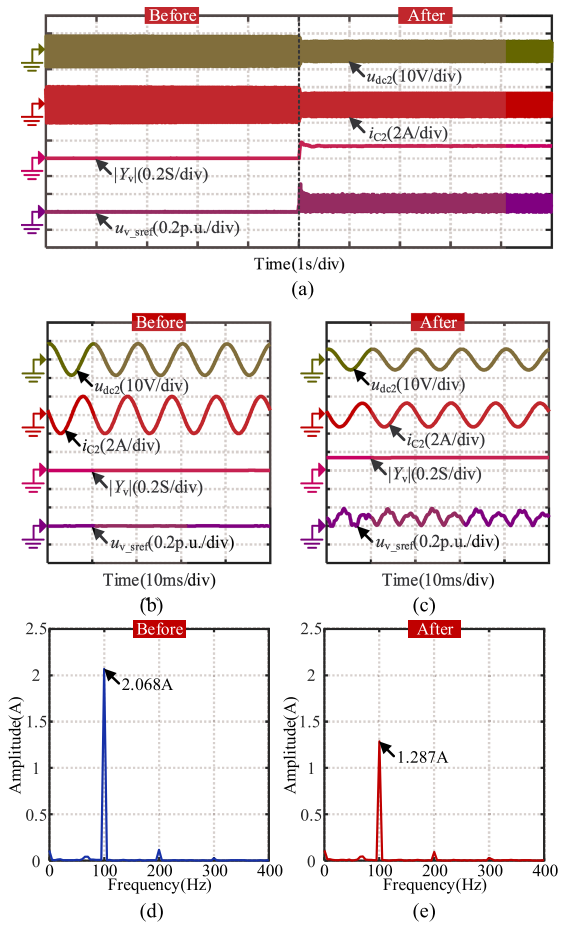

Fig. 13. Experimental results at 60% rated power (720 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

capacitor parameters. In Fig. 9(a), when k_C remains unchanged, I^*_{C2} is not significantly affected by k_{RC}. When k_{RC} remains unchanged, I^*_{C2} increases with k_C. In Fig. 9(b), when C and R_C change within $\pm 5\%$, the percentage error E_{IC2} is close to 5.5%. The problem can be mitigated by a capacitor current reconstruction algorithm.

IV. Experimental Results

To verify the effectiveness of the proposed suppression strategy, experiments under different conditions were carried out on the experimental platform of PMSM drive fed by the boost PFC converter, as shown in Fig. 10. The parameters of experimental platform are given in Table I. The control algorithm is executed by the R5F562T7DDF microcontroller of RX62T series. The switching frequency of the inverter is set to 10 kHz. The iterative learning parameters k_1, k_2, and k_3 are set to 0.95, 4, and 2, respectively.

In order to verify the effectiveness of the proposed strategy, the experimental results when the motor operates at the rated power (1200 W) are shown in Fig. 11. As shown in Fig. 11(a)–(c), after enabling the suppression strategy, the second-harmonic components of the capacitor current and dc-link voltage are significantly reduced, and the virtual admittance amplitude converges stably around 0.4 S. Comparing Fig. 11(d) and (e), before enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is 3.180 A. After enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.286 A, which is basically consistent with the target SHRC amplitude (1.287 A). This indicates that the proposed strategy is effective in suppressing SHRC at the rated power.

When the motor operating power is reduced to 80% rated power (960 W), the experimental results are shown in Fig. 12. As shown in Fig. 12(a)–(c), the fluctuations of the capacitor current and dc-link voltage increase as power decreases, so the virtual admittance amplitude required to achieve the target ripple current also decreases accordingly. After enabling the suppression strategy, the virtual admittance amplitude converges stably around 0.25 S. Comparing Fig. 12(d) and (e), before enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is 2.609 A. After enabling the proposed strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.286 A. Therefore, the proposed strategy can still effectively suppress the SHRC of dc-link capacitors at 80% rated power.

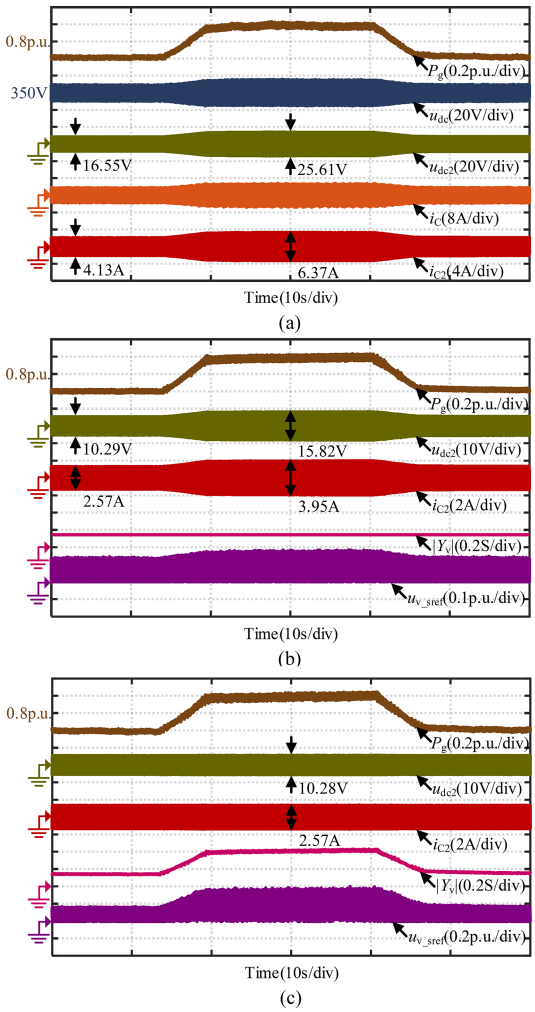

Fig. 14. Experimental results during power variations (720–1200 W). (a) Disabled strategy. (b) Enabled the fixed damping strategy. (c) Enabled the proposed adaptive damping strategy.

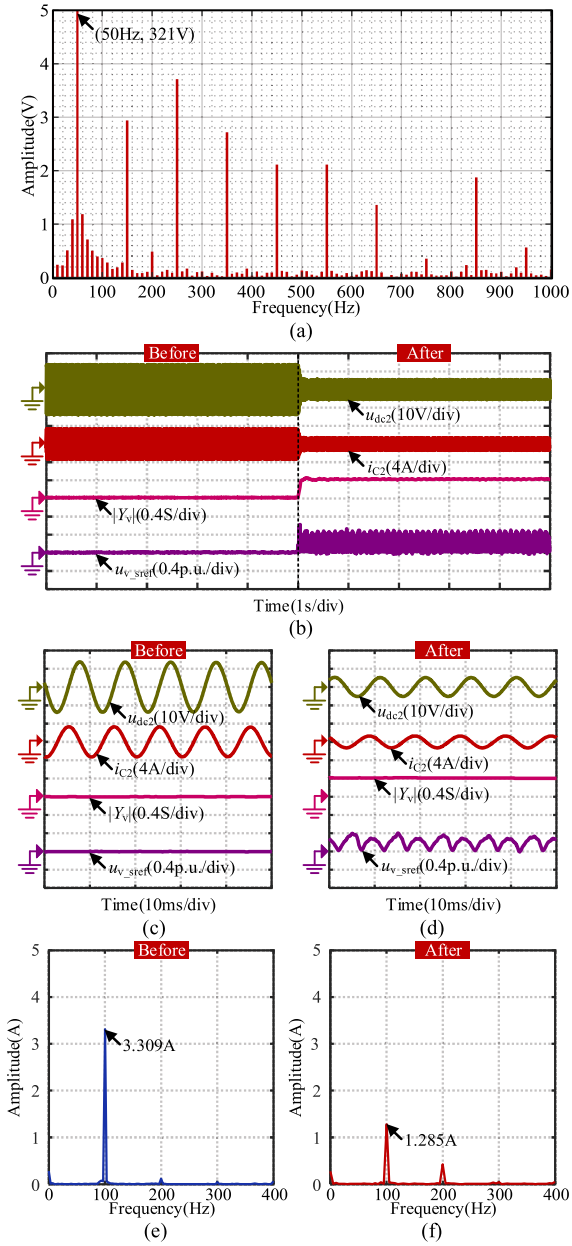

Fig. 15. Experimental results at the rated power (1200 W) under grid conditions. (a) FFT analysis of grid voltage. (b) Overall waveforms. (c) Zoomed waveforms (before). (d) Zoomed waveforms (after). (e) FFT analysis of capacitor current (before). (f) FFT analysis of capacitor current (after).

In order to verify the effectiveness of the proposed strategy under other power conditions, the experimental results when the motor operates at 60% rated power (720 W) are shown in Fig. 13. As shown in Fig. 13(a)–(c), after enabling the suppression strategy, the second-harmonic components of the capacitor current and dc-link voltage can still be effectively reduced, and the virtual admittance amplitude converges stably around 0.15 S. Comparing Fig. 13(d) and (e), before enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is 2.068 A. After enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.287 A. Therefore, the proposed strategy can stably converge and effectively suppress the SHRC of dc-link capacitors under various power conditions, demonstrating good adaptability.

To verify the effectiveness of the proposed strategy during power variations, Fig. 14 shows the experimental results obtained when the motor operates between 60% and 100% of the rated power (720–1200 W). In Fig. 14, P_g and u_{v_sref} represent the dc component of the grid power and the admittance voltage command, respectively. As shown in Fig. 13(a) and (b), the fixed damping strategy reduces the fluctuations in the capacitor current and dc-link voltage, but the suppression effect is limited under high power conditions. Comparing Fig. 14(a)–(c), after enabling the proposed adaptive damping strategy, the SHRC of dc-link capacitors can be effectively suppressed around the target amplitude during the wide-ranging power variations.

Fig. 15 presents the experimental results for motor operation at the rated power, verifying the effectiveness of the proposed strategy under grid conditions. In Fig. 15(a), the grid voltage is highly distorted with a fundamental component of 321 V, exceeding the theoretical value of 311 V. As shown in Fig. 15(b)–(d), the fluctuations of the capacitor current and

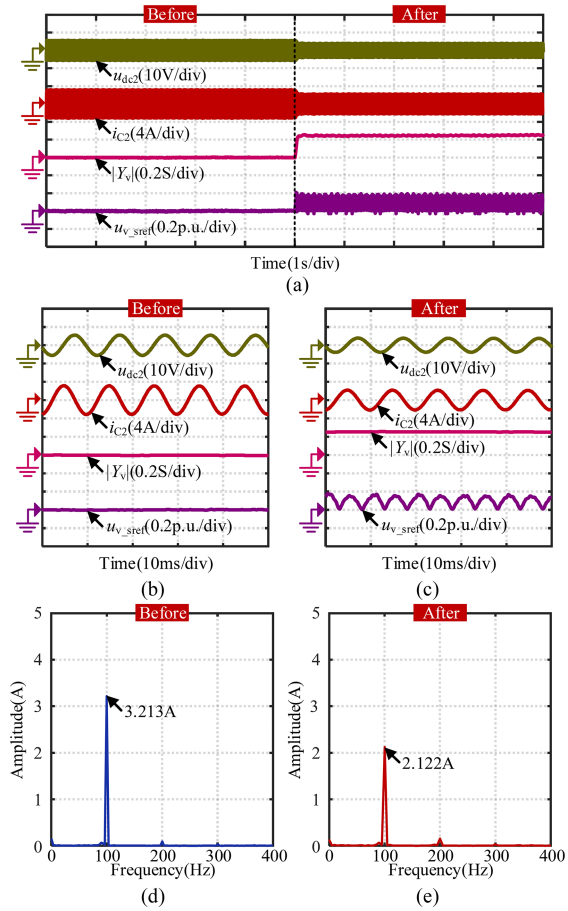

Fig. 16. Experimental results with other capacitor conditions (861.93 μF, 81.80 mΩ). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after). (d) FFT analysis of capacitor current (before). (e) FFT analysis of capacitor current (after).

dc-link voltage can still be effectively reduced. According to Fig. 15(e) and (f), before enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is 3.309 A; after enabling the suppression strategy, the SHRC amplitude of dc-link capacitors is reduced to 1.285 A. Therefore, the proposed strategy can effectively suppress the SHRC to the target amplitude (1.287 A) under grid conditions.

To verify the effectiveness of the proposed strategy under other capacitor conditions, Fig. 16 presents the experimental results for motor operation at the rated power. When the electrolytic capacitors (861.93 μF, 81.80 mΩ) are used to replace the original dc-link capacitors (379.32 μF, 303.51 mΩ), the corresponding target SHRC amplitude is 2.121 A. As shown in Fig. 16(a)–(c), the fluctuations of the capacitor current and dc-link voltage can still be effectively reduced. According to Fig. 16(d) and (e), enabling the proposed strategy, the SHRC amplitude of dc-link capacitors is reduced from 3.213 to 2.122 A. Therefore, the proposed strategy still exhibits satisfactory performance under different capacitance conditions.

In order to verify the robustness of the proposed strategy to temperature, the thermal imaging device (RM600F) is used to measure temperature. Fig. 17 presents the experimental results after 6-min continuous operation at the rated power (1200 W).

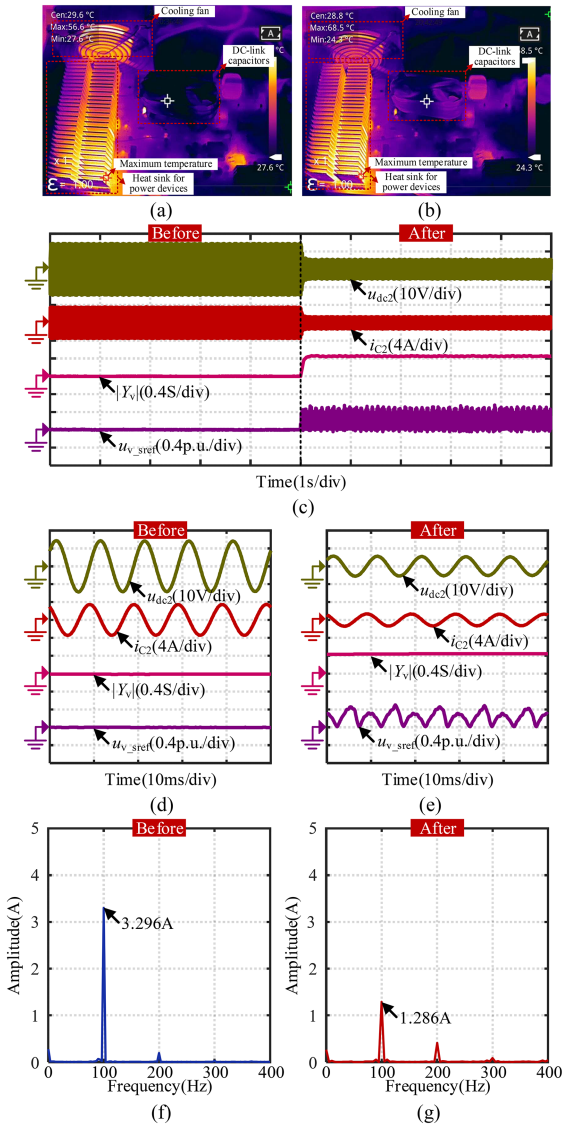

Fig. 17. Experimental results after 6-min continuous operation at the rated power (1200 W). (a) Thermal imaging (initial). (b) Thermal imaging. (c) Overall waveforms. (d) Zoomed waveforms (before). (e) Zoomed waveforms (after). (f) FFT analysis of capacitor current (before). (g) FFT analysis of capacitor current (after).

As shown in Fig. 17(a) and (b), the maximum temperature increases from 56.6 °C to 68.5 °C. According to Fig. 17(f) and (g), the SHRC amplitude of dc-link capacitors before enabling the proposed strategy during continuous operation for 6 min is 3.296 A. The SHRC amplitude of dc-link capacitors after enabling the proposed strategy during continuous operation for 6 min is 1.286 A. Therefore, the proposed strategy can effectively suppress the SHRC to the target amplitude (1.287 A) under different temperature conditions.

The admittance power fluctuations in (5) inevitably introduce *dq*-axis current harmonics, which increases the motor torque ripple. The influence of the proposed strategy on torque ripple is analyzed using experimental results at the rated power (1200 W), as presented in Fig. 18. In Fig. 18(a), consistent with the analysis, both the *dq*-axis current fluctuations and the torque

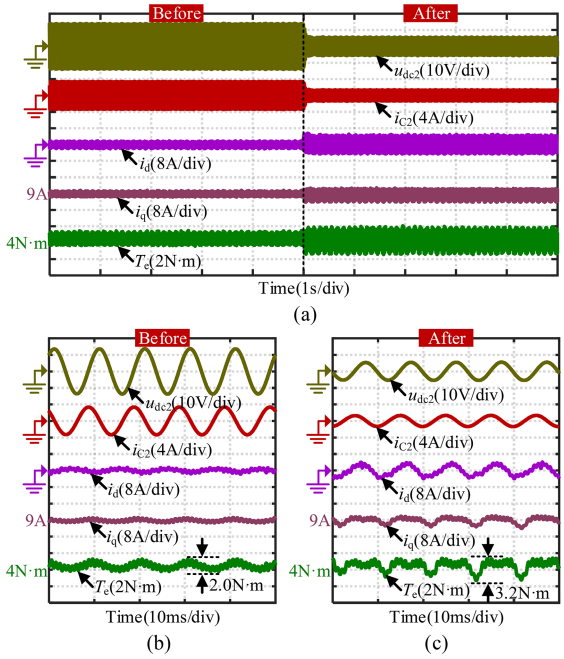

Fig. 18. Experimental results for the torque ripple (1200 W). (a) Overall waveforms. (b) Zoomed waveforms (before). (c) Zoomed waveforms (after).

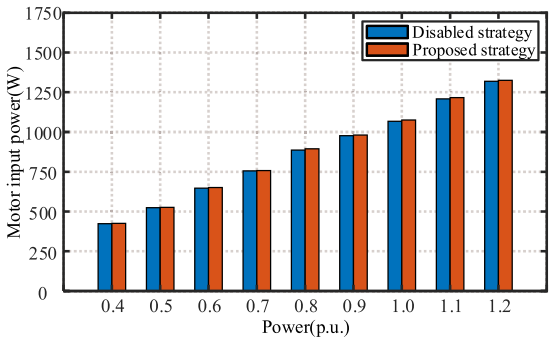

Fig. 19. Experimental results for the motor losses.

ripple increase after enabling the proposed strategy. As shown in Fig. 18(b) and (c), the peak-to-peak torque ripple before enabling the proposed strategy is 2.0 N·m. The peak-to-peak torque ripple after enabling the proposed strategy is 3.2 N·m. The peak-to-peak torque ripple increases to 1.6 times that of the initial value, but it is still within the acceptable limits.

In addition, the *dq*-axis current harmonics generated by the proposed strategy can increase the motor losses. In order to verify the influence of the proposed strategy on motor losses, Fig. 19 presents the experimental results at different power levels. Assuming that the motor output power remains unchanged in a short time, the motor losses can be analyzed by the changes in the motor input power. As shown in Fig. 19, the motor input power increases slightly after enabling the proposed strategy. The experimental results are consistent with the theoretical analysis, and the increase in motor losses is within an acceptable range.

To further verify the effectiveness of the proposed strategy under different power conditions, when the grid power changes

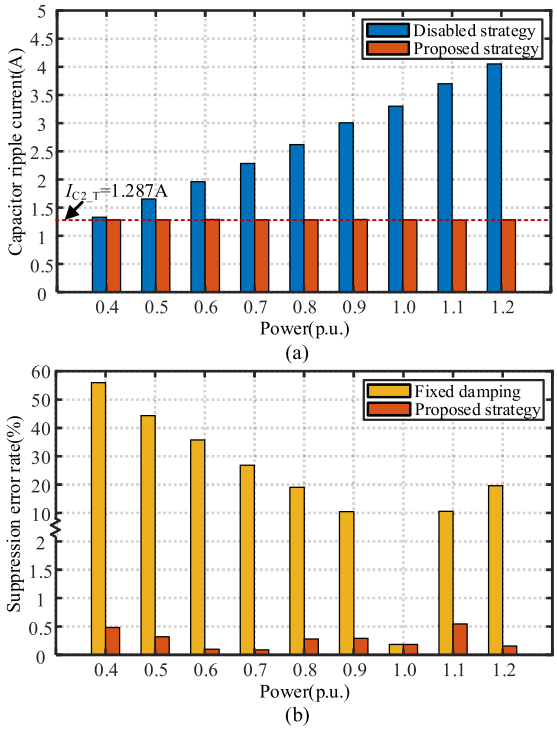

Fig. 20. Experimental comparison results under different power conditions. (a) Capacitor ripple current. (b) Suppression error rate.

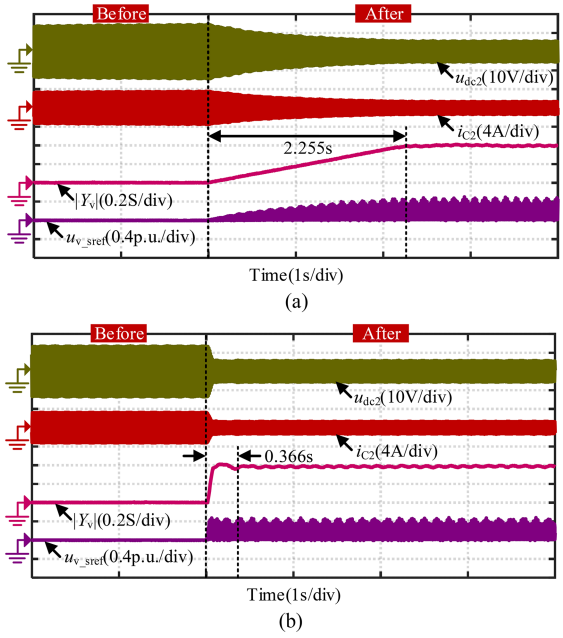

Fig. 21. Experimental comparison results of convergence times. (a) Strategy in [25]. (b) Proposed strategy.

from 40% to 120% of the rated power (480–1440 W) in steps of 120 W, the experimental comparison results are shown in Fig. 20. As shown in Fig. 20(a), the proposed strategy can suppress the SHRC amplitude, maintaining it around the target value of 1.287 A. As shown in Fig. 20(b), the fixed damping strategy exhibits the significant suppression error rate of the SHRC under

non-rated power conditions. Since the damping parameters of this strategy are designed based on the rated power, they cannot be adaptively adjusted during power variations. In contrast, the proposed adaptive damping strategy maintains the error suppression rate within 1% under different power conditions. Therefore, the proposed strategy has better adaptability and ripple current suppression effect.

Since convergence time is a critical metric for adaptive strategies, Fig. 21 compares the convergence times of the strategy in [25] and the proposed strategy. In [25], since the step size for adjusting the admittance amplitude is fixed, the convergence time is relatively long. Fig. 21(a) presents the experimental waveforms using the strategy in [25], where the admittance amplitude stabilizes 2.255 s after the strategy is enabled. In contrast, the proposed strategy achieves the faster convergence speed by constructing the adaptive admittance amplitude mechanism based on the iterative learning algorithm. Fig. 21(b) presents the experimental waveforms using the proposed strategy, where the admittance amplitude stabilizes just 0.366 s after the strategy is enabled.

V. Conclusion

In this article, a ripple current suppression strategy of dc-link capacitors for PMSM drives based on adaptive active damping has been proposed. The strategy characterizes the ripple current using the dc-link voltage without the need for additional hardware or current reconstruction algorithms. Based on the system admittance modelling, the inherent limitations of fixed damping parameters in the traditional strategy are revealed. To overcome the limitation of fixed damping parameters, a P-type iterative learning mechanism with the forgetting factor is constructed. On this basis, the initial admittance parameters are dynamically matched according to the motor power, further improving the iterative efficiency. The theoretical analysis and experimental results show that the proposed strategy can effectively suppress the ripple current under different power conditions, with a suppression error rate within 1% across a wide power range. Compared with the traditional strategies, the proposed strategy offers better adaptability and faster convergence speed.

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