High Step-Up DC–DC Converter Based on Switched Boost Impedance Source Network and Ladder Switched Capacitor

Tooraj Sabetfar, Majid Hosseinpour, *Member, IEEE*, Ali Seifi, and Hamed Heydari-doostabad, *Senior Member, IEEE*

***Abstract*—This article proposes a new step-up dc–dc converter based on a switched boost impedance source network (SB-ZSN) with high voltage gain for application in renewable energy sources. In addition to maintaining the advantages of recent impedance source converters, such as continuous input current, the absence of inrush current, and a common ground between the input and output, the proposed converter increases the voltage gain. In this converter, the switched boost impedance source network and ladder switched capacitor (Ladder-SC) are used simultaneously to achieve high boosting capability. The voltage gain is enhanced in the first stage by the switched boost impedance network and further increased in the second stage by the Ladder-SC block. The performance of the converter is analyzed in continuous conduction mode and discontinuous conduction mode under steady-state conditions, and the real voltage gain is calculated by incorporating parasitic elements, comparing it with recently introduced dc–dc converters. The voltage stress on the switches, capacitors, and diodes in the proposed converter is low. In addition, the input current ripple is minimal and can be neglected. The proposed converter also shares a common ground with the load, and one of its advantages is low electromagnetic interference. Other features include high efficiency and the small size of both passive and active components. To investigate the key characteristics of the proposed converter, a steady-state analysis has been conducted, and a comprehensive comparison has been made with similar converters. Small-signal analysis and controller design for output voltage regulation have been carried out. To validate the mathematical analyses, two laboratory prototypes rated at (40–372 V, 400 W) and (50–614 V, 1 kW) have been constructed and evaluated.**

***Index Terms*—High efficiency, ladder switched capacitor (Ladder-SC), low voltage stress, step-up dc-dc converter, switched boost impedance source network (SB-ZSN).**

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I. Introduction

DUE to environmental damage and the depletion of fossil energy resources, renewable energy sources such as wind energy, solar energy, and fuel cells are suitable alternatives to fossil fuels. The low voltage output of renewable energy sources has led to the use of step-up dc–dc converters in renewable applications [1]. In conventional step-up converters, the output voltage can increase significantly at high duty cycles, but under these conditions, efficiency decreases, and the voltage stress of the switch increases. Therefore, to reduce the voltage stress of the switch, diode, and capacitor, and to improve system efficiency, advanced and novel step-up dc–dc converters are being researched [2]. By employing techniques such as switched inductor (SL) [3], switched capacitor (SC) [4], combined switched inductor and SC [5], voltage lift cells (voltage Lift) [6], and the cascade connection technique [7], the voltage gain of the dc–dc converter can be increased. The use of coupled inductors also enhances the voltage gain of the converter, but it leads to higher input current ripple, power losses, and increased electromagnetic interference (EMI) [8].

Ladder-switched capacitor converters (Ladder-SC) offer high power density due to the absence of magnetic components. High voltage gain and compact size are among the key advantages of Ladder-SC converters [9]. These converters divide the output voltage across two capacitors, which reduces the nominal voltage requirements of the capacitors [10]. In studies [11] and [12], the combination of coupled inductors and Ladder-SC is employed in applications requiring very high voltage gain, and the low voltage stress on the capacitors cited as one of the advantages of these converters.

Impedance source dc–dc converters are classified into two main categories: isolated and nonisolated. Isolated converters are larger and more expensive due to the inclusion of a transformer. Nonisolated converters are further classified into two subcategories: those with coupled inductors and those with normal inductors [13]. Converters based on coupled inductors achieve higher voltage gain, but this type of converter experiences higher voltage drops due to leakage inductance, resulting in lower efficiency. Snubber circuits are requires to reduce the voltage drop, which increases system complexity and volume [14]. Conventional impedance source dc–dc converters, including impedance source converters and quasi-impedance source

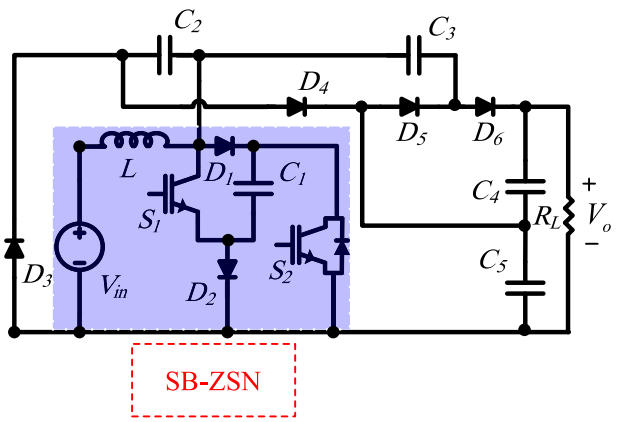


Fig. 1. Proposed DC–DC converter.

converters, have a low voltage gain, which limits their use [15]. In these converters, the voltage gain can be increased by adding passive and active components to the impedance network, such as replacing conventional impedance quasi-source converter inductors with SL [16], adding an SC [17], using a combination of SL and SC) [18] methods, or incorporating a voltage lift cell (Voltage Lift) [19]. Each of these solutions, while offering some advantages, also has drawbacks, such as a limited switching cycle, increased voltage stress on the switch and diodes, and increased output voltage ripple. Another type of impedance source converter uses both passive and active components, an active switch is also presented in impedance network [20]. While the traditional switched boost impedance source converter retains all the advantages of the conventional impedance source converter, it lacks a high voltage gain, which has led to further research and development of such converters [21], [22]. In the step-up converter (SL-DS-DC) [23], a combination of switched inductor and switched boost is used simultaneously, resulting in high voltage gain with a compact converter size.

New structures with high voltage gain are obtained by combining the impedance quasi-source converter and active SC. One of the features of these converters is continuous input current with reduces ripple and a common ground between input and output, though the current through the switches is high [24]. Another type of impedance quasi-source converter with an active SC, which has one fewer diode compared to the converter presented in study [24], has lower current through the switch, lower voltage gain, and lacks a common ground between the input and output [25]. In study [26], two converters based on an impedance source network with an active SC (ASC-ZSN1-ASC-ZSN2) with high voltage gain are presented; both converters offer continuous input current and a compact design. Power loss in the inductor is categorized into two types: core loss and winding or conductive loss. Coli loss is proportional to the current passing through the inductor and the material of the coil conductor, while core loss depends on the material of the core using higher quality metals reduces the loss. The more inductors a converter has, the greater the inductor losses and the higher the converter cost [27], [28].

By increasing the number of active and passive components in the impedance network, the voltage gain of the converter can be enhanced. However, this also limits the duty cycle of the converter switch and increase the voltage stress on the components. To stabilize the switch's duty cycle and the voltage stress of the components, a two-stage method based on the impedance source has been employed. In study [29], adding a SC to the conventional impedance source converter increases the voltage gain, stabilizes the voltage stress of the components at the previous level, and establishes a common ground between the source and the load. However, a disadvantage of this converter is its discontinuous input current. In study [30], adding a capacitor and a diode to the conventional impedance source converter enhances the voltage gain while maintaining the switching interval and voltage stress of the components. Nonetheless, this converter also suffers from discontinuous input current. In study [31], to leverage the impedance quasi-source converter, an SC is incorporated into it. Although this converter offers improvements, its volume is large and the voltage gain is not sufficiently high. The converter described in study [32] adds an inductor, along with an SC, to the impedance quasi-source converter to store energy and enhance voltage gain capability. Its disadvantages include high input current ripple, a lack of common ground between input and output, and a large volume.

In Reference [33], a high voltage gain dc–dc converter is presented, which integrates a switched-boost quasi-impedance network with an SC configuration. This topology features a continuous input current and a common-ground structure. However, it experiences substantial current stress on the diodes, which can adversely affect their reliability.

This article presents a nonisolated dc–dc converter based on an impedance source network that achieves high voltage gain without limiting the duty cycle of the switch. The proposed converter simultaneously utilizes the switched boost impedance source network (SB-ZSN) and a Ladder-SC to achieve high voltage boosting capability. The voltage stress of the active and passive devices in the switched boost impedance source network remains unchanged, while the voltage gain of the converter is enhanced in the first stage by the switched boost impedance source network and in the subsequent stage by the Ladder-SC. The converter components include five capacitors, six diodes, two switches, and an inductor. High voltage gain coefficient at low duty cycles, continuous input current with low ripple and no inrush current, a common ground between the source and load, high efficiency, small size of passive and active devices, easy control, expandability for increasing voltage gain, and low EMI is one of the features of the proposed converter.

This article is organized into the following sections: Section II covers the converter's operating modes, the converter's voltage gain extraction, and the voltage stress and current of the components in their ideal state. Section III compares the proposed converter with recently presented converters, focusing on ideal and real voltage gain, as well as the voltage stress and current of the components. Section IV addresses the converter's small-signal analysis and the analysis of state equations. Section V deals with calculating the efficiency of the proposed converter and comparing it with similar converters. Section VI presents the design of the inductor and capacitor of the proposed converter. Section VII pertains to simulation and laboratory results, followed by the conclusion of this article.

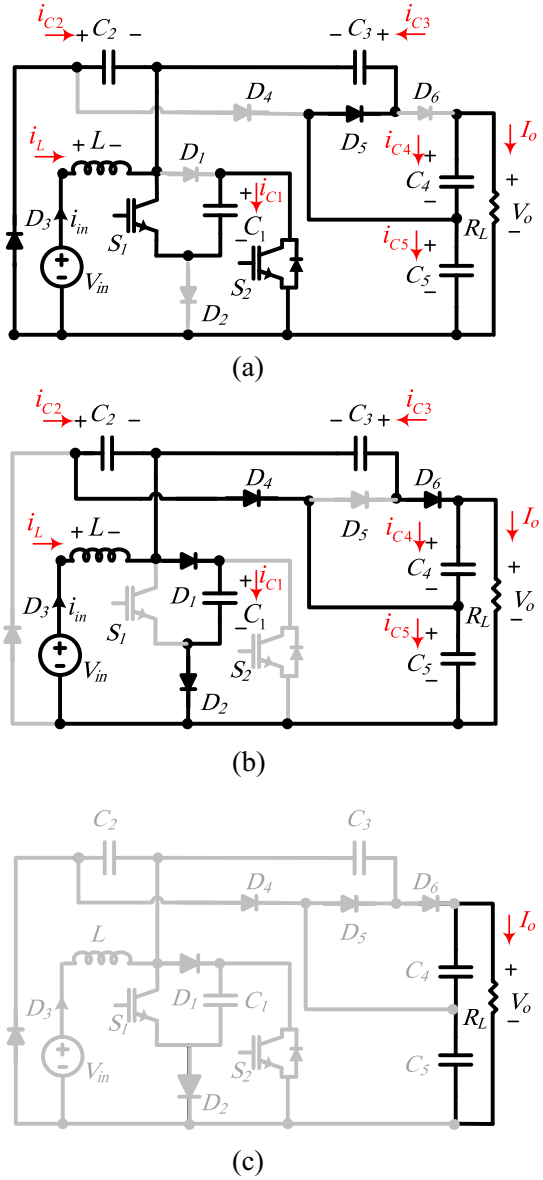


Fig. 2. (a) First operating mode (S_{on}). (b) Second operating mode (S_{off}). (c) Third operating in DCM.

II. Theoretical Analysis of the Proposed Converter

Fig. 1 shows the power circuit of the step-up dc–dc converter based on the SB-ZSN. To significantly increase the input voltage at the converter's, the SB-ZSN and the Ladder-SC are used simultaneously. The SB-ZSN consists of the inductor (L), capacitor (C_1), diodes (D_1 and D_2), and switches (S_1 and S_2) and the Ladder-SC network includes capacitors (C_2, C_3, C_4, and C_5) and diodes (D_3, D_4, D_5, and D_6). Since the output voltage in the proposed converter is divided between two capacitors (C_4 and C_5), the nominal voltage of the output capacitors is reduced. For simplification, it is assumed that all the components in the converter are ideal and the proposed converter operates in continuous conduction mode (CCM) and discontinuous conduction mode (DCM)

A. Operating Modes of the Proposed Converter

The operating modes of the proposed converter are determined by simultaneous switching S_1 and S_2. The switch's ON state is indicated as "ON" and its OFF state is indicated as "OFF." In the circuit analysis of the proposed converter, the parameter D represents the duty cycle of switch, which is the ratio of the switch's ON-time to the switching period (T_s). DT_s represents the ON-time interval, while (1-D)T_s represent the OFF-time interval for the switch. The equivalent circuit of the proposed converter is shown in Fig. 2 in two operating modes, including the ON and OFF modes of the switches.

1) First Operating Mode ($0 < t < DT_s$): The equivalent circuit of the converter in the first operating mode is shown in Fig. 2(a) This mode begins when switches S_1 and S_2 are turned on simultaneously during the time interval (DT_s). According to the polarity of the voltage across the diodesD_3 and D_5 are forward-biased, and diodes D_1, D_2, D_4, and D_6 are reverse-biased. Based on the path created by conducting diodes (D_3 and D_5), the inductor (L) is charged by the capacitor C_1 and the input voltage source (V_{in}). In the proposed converter, capacitors C_2 and C_3 behave similarly to inductors in terms of charging and discharging, and in this operating mode, capacitors C_2 and C_3 are charged while capacitors C_1, C_4, and C_5 are discharged. Capacitors C_2 and C_3 are charged by capacitors C_1 and C_5. Meanwhile, capacitor C_5 in addition to charging capacitors C_2 and C_3, along with capacitor C_4, also supplies power to the load.

By applying KVL to the equivalent circuit in Fig. 2(a), three equations for the voltage across the inductor L according to the following equation are obtained:

$$\begin{cases} v_{L,\text{on}} = V_{C_1} + V_{\text{in}} \\ v_{L,\text{on}} = V_{C_2} + V_{\text{in}} \\ v_{L,\text{on}} = V_{C_3} - V_{C_5} + V_{\text{in}}. \end{cases} \tag{1}$$

By applying KCL in the equivalent circuit of Fig. 2(a), the current of capacitors can be expressed according to the following equation:.

$$\begin{cases} i_{C_1,\text{on}} = -I_{L1} - i_{C_2,\text{on}} + i_{C_5,\text{on}} + I_o \\ i_{C_2,\text{on}} = -I_{L1} - i_{C_1,\text{on}} - i_{C_3,\text{on}} \\ i_{C_3,on} = -I_{L1} - i_{C_1,\text{on}} - i_{C_2,\text{on}} \\ i_{C_4,\text{on}} = -I_o \\ i_{C_5,\text{on}} = -i_{C_3,\text{on}} + i_{C_4,\text{on}} \end{cases}. \tag{2}$$

2) Second Operating Mode ($DT_s < t < (1\text{-}D)T_s$): The equivalent circuit of the proposed converter in the second operating mode is shown in Fig. 2(b) This mode begins when switches S_1 and S_2 are turned OFF during the time interval (1-D)T_s. According to the polarity of the voltage across the diodes, diodes D_3 and D_5 are reverse-biased, while diodes D_1, D_2, D_4, and D_6 are forward-biased. Through the path created by conducting diodes D_1, D_2, D_4, and D_6, capacitor C_1 is charged by the inductor L and the input voltage source V_{in}, while capacitors C_2 and C_3 transfer their energy to capacitors C_1, C_4, and C_5.

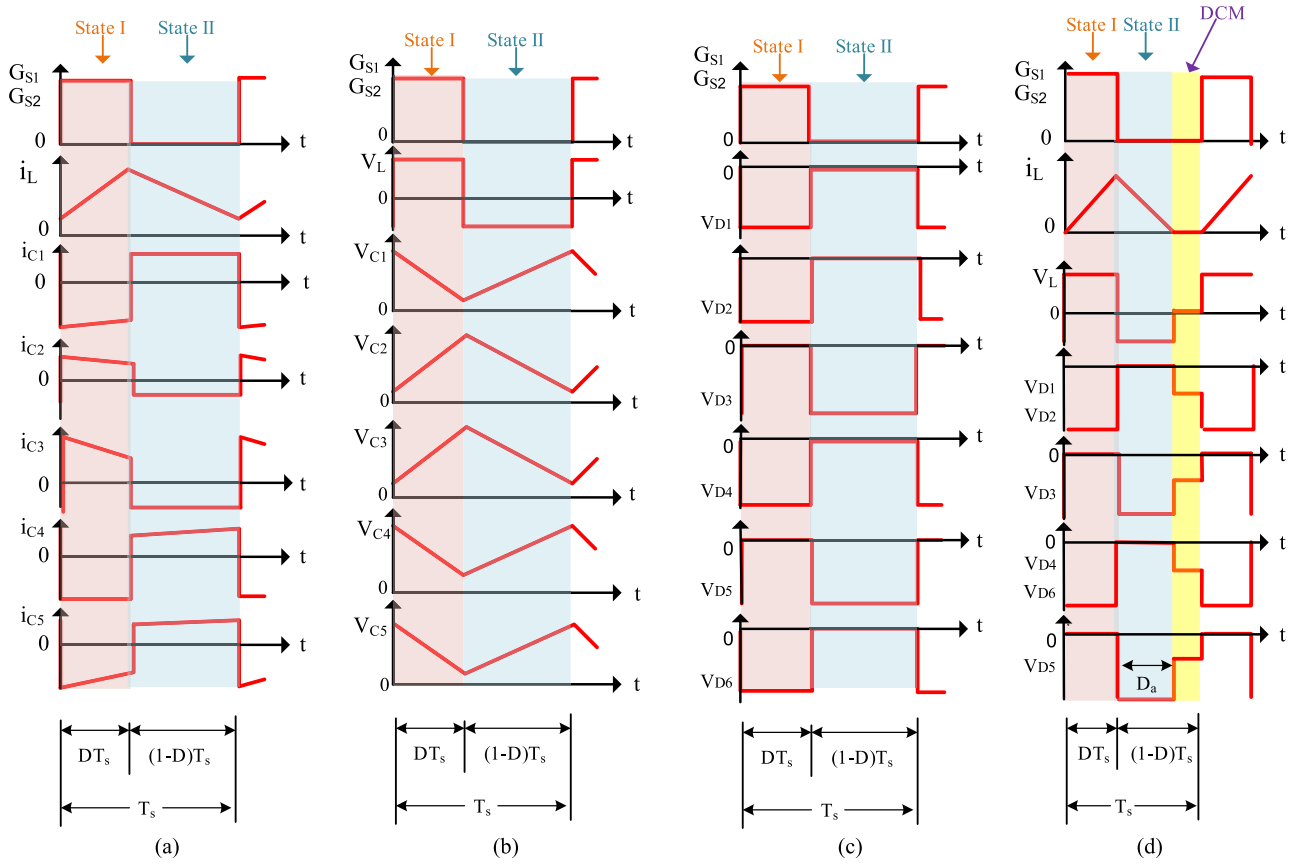


Fig. 3. Voltage and current waveforms of the proposed converter components. (a) Inductor and capacitors current. (b) Inductor and capacitors voltage. (c) Diodes voltage. (d) Inductor voltage and current and diode voltage in DCM.

The load is powered by the voltage source and capacitors C_4 and C_5.

By applying KVL to the equivalent circuit in Fig. 2(b), three relationships for the voltage are obtained. The voltage across the inductor L can be expressed as shown in (3). By applying KCL in the equivalent circuit of Fig. 2(b), the current of capacitors is obtained according to (4).

The typical voltage waveforms of the capacitor, inductor, and diode and the current waveforms of the capacitor and inductor in the ideal state to confirm the operating modes are shown in Fig. 3

$$\begin{cases} v_{L,off} = -V_{C_1} + V_{in} \\ v_{L,off} = V_{C_2} - V_{C_5} + V_{in} \\ v_{L,off} = V_{C_3} - V_{C_4} - V_{C_5} + V_{in} \end{cases} \tag{3}$$

$$\begin{cases} i_{C_1,\text{off}} = I_L - i_{C_5,\text{off}} - I_o \\ i_{C_2,\text{off}} = -I_L + i_{C_1,\text{off}} - i_{C_3,\text{off}} \\ i_{C_3,\text{off}} = -I_L + i_{C_1,\text{off}} - i_{C_2,\text{off}} \\ i_{C_4,\text{off}} = -I_o - i_{C_3,\text{off}} \\ i_{C_5,\text{off}} = -i_{C_2,\text{off}} + i_{C_4,\text{off}} \end{cases} . \tag{4}$$

According to Fig. 3(a), the inductor current increases during the first operating mode, while in the second operating mode, the inductor current decreases and discharges. Similarly, capacitors C_2 and C_3 are charged in the first operating mode and discharged in the second operating mode. Capacitors C_1, C_4, and C_5 maintain their typical behavior, discharging in the first operating mode and charging in the second. Due to the increase in inductor current during the first operating mode, the inductor voltage is positive, while in the second operating mode, the inductor voltage becomes negative the current decreases, as shown in Fig. 3(b). In the first operating mode, diodes D_3 and D_5 are reverse biased and diodes D_1, D_2, D_4, and D_6 are forward biased. The voltage across the diodes is shown in Fig. 3(c).

B. Extracting the Voltage Gain of the Proposed Converter

In this section, in addition to calculating the ideal gain of the proposed converter, the voltage stress of switches, diodes, and capacitors will also be calculated.

According to the balance principle (Volt-sec), the average voltage of the inductor in a switching period is equal to zero, which is shown as follows:

$$\int_0^{DT_S} v_L dt + \int_{DT_S}^{T_S} v_L dt = 0. \tag{5}$$

By using relations (1), (3) and (5) and inserting in relation (5), the voltage of the converter capacitors is obtained in terms of duty cycle and input voltage according to the following:

$$\begin{cases} V_{C_1} = V_{C_2} = \frac{1}{1-2D} V_{\text{in}} \\ V_{C_3} = \frac{3}{1-2D} V_{\text{in}} \\ V_{C_4} = V_{C_5} = \frac{2}{1-2D} V_{\text{in}} \end{cases}. \tag{6}$$

Since, in both operating modes of the converter, the output voltage (V_o) is equal to the sum of the voltages across capacitors C_4 and C_5, by using the voltage relations of the capacitors in (6), V_o can be obtained, as shown in the following:

$$V_o = V_{C_3} + V_{C_4} = \frac{4}{1-2D} V_{\text{in}}. \tag{7}$$

The boosting factor of the converter is defined as the ratio of the output voltage to the input voltage. Therefore, the boosting factor in the proposed converter can be expressed as shown in (8). The presence of a factor of 4 in the numerator of the gain term significantly enhances the boosting capability of the proposed converter. According to (8), the duty cycle changes in the proposed converter can range from zero to 0.5

$$G = \frac{V_o}{V_{\text{in}}} = \frac{4}{1-2D}. \tag{8}$$

According to Fig. 2(a), when switches S_1 and S_2 are ON, diodes D_1, D_2, D_4, and D_6 are reverse biased, and their voltage stress can be expressed as shown in (9). In addition, according to Fig. 2(b), when the switches S_1 and S_2 are OFF, diodes D_3 and D_5 are reverse biased. The voltage stress on switches S_1 and S_2 and diodes D_3 and D_5, can be expressed as shown in (10). According to these relations, the voltage stress on switches and diodes D_1 and D_2 is one-quarter of the output voltage and the voltage stress on diodes D_3, D_4, D_5, and D_6 is half of the output voltage. Due to the low and appropriate voltage stress on the power electronic devices in the proposed converter, the nominal ratings of the switches and diodes are not high, which results in a lower volume and cost for the proposed converter

$$\begin{cases} V_{D_1} = V_{D_2} = \frac{1}{1-2D} V_{\text{in}} \\ V_{D_4} = V_{D_6} = \frac{2}{1-2D} V_{\text{in}} \end{cases} \tag{9}$$

$$\begin{cases} V_{D_3} = V_{D_5} = \frac{2}{1-2D} V_{\text{in}} \\ V_{S_1} = V_{S_2} = \frac{1}{1-2D} V_{\text{in}}. \end{cases} \tag{10}$$

C. Extracting the Current Stress of Active and Passive Devices

In this section, we will calculate not only the input current of the proposed converter but also the current through the switches, diodes, and capacitors.

According to the capacitor current-second (Ampere-sec) balance principle, the average current through the capacitor over a switching period, as described by (11), is equal to zero

$$\int_0^{DT_S} i_C dt + \int_{DT_S}^{T_S} i_C dt = 0. \tag{11}$$

By using relations (2) and (4) and substituting them into relation (11), the peak current of the capacitors during the switch's on and off periods can be determined, as shown in (12). Using relations (2), (4), and (12), the average current through the inductor, in terms of the duty cycle and the output current of the converter, can be expressed by relation (13)

$$\begin{cases} i_{C_1,\text{on}} = -\frac{I_L}{2D} \\ i_{C_1,\text{off}} = \frac{I_L}{2(1-D)} \end{cases} \quad \begin{cases} i_{C_5,\text{on}} = -\frac{(1+D)}{D} I_o \\ i_{C_5,\text{off}} = \frac{(1+D)}{(1-D)} I_o \end{cases}$$

$$\begin{cases} i_{C_2,\text{on}} = i_{C_3,\text{on}} = \frac{1}{D} I_o \\ i_{C_2,\text{off}} = i_{C_3,\text{off}} = -\frac{1}{(1-D)} I_o \end{cases}$$

$$\begin{cases} i_{C_4,\text{on}} = -I_o \\ i_{C_4,\text{off}} = \frac{D}{(1-D)} I_o \end{cases} \tag{12}$$

$$I_L = \frac{4}{(1-2D)} I_o. \tag{13}$$

According to Fig. 2(a), when switches S_1 and S_2 are on, diodes D_3 and D_5 are forward-biased. The current passing through these diodes and switches can be expressed using (14). According to Fig. 2(b), when switches S_1 and S_2 are off, diodes D_1, D_2, D_4 and D_6 are forward biased. The current passing through these diodes can be expressed according to (15)

$$\begin{cases} i_{D_3} = \frac{1}{D} I_o \\ i_{D_5} = -\frac{1}{D} I_o \\ i_{S_1} = i_{S_2} = \frac{2}{D(1-2D)} I_o \end{cases} \tag{14}$$

$$\begin{cases} i_{D_1} = i_{D_2} = \frac{2}{(1-D)(1-2D)} I_o \\ i_{D_4} = i_{D_6} = \frac{1}{(1-D)} I_o. \end{cases} \tag{15}$$

According to the above relations, the current stress on diodes D_1, D_2, D_4, and D_6 is low and the current stress on the switches and diodes D_1 and D_2 is higher compared to diodes D_3 and D_6.

D. Discontinuous Conduction

The DCM of the proposed converter occurs when the inductor current becomes zero. The proposed converter in discontinuous conduction has three operating modes, the first and second operating modes are similar to CCM conduction. In the third operating mode, the inductor current decreases and becomes zero, which is shown in Fig. 3(b).

In the first operating modes ($0 < t < \text{DT}_\text{s}$) both switches ($\text{S}_1$ and S_2) are ON, the inductor current increases according to the first operating mode in the CCM, the peak value of the inductor current is obtained as follows:

$$I_{L(\text{peak})} = \frac{2(1-D) V_{\text{in}} D}{(1-2D) L f_s}. \tag{16}$$

In the second operating modes ($DT_S < t < D_a T_S$) both switches (S_1 and S_2) are OFF and the inductor is discharged. The inductor current decreases similar to the second operating mode in CCM, the peak value of the inductor current in terms

of Da is given by the following::

$$I_{L(\text{peak})} = \frac{2\left(1-D\right)V_{\text{in}} - \left(1-2D\right)V_o}{\left(1-2D\right)Lf_s} D_a. \tag{17}$$

In the third operating mode ($D_aT_S < t < T_S$), both switches (S_1 and S_2) remain in the OFF state and the diodes (D_1, D_2, D_3, D_4, D_5 and D_6) are reverse biased and no current flows through the inductor. During this time, the load current is supplied by the capacitors (C_4 and C_5). Using (16), and (17), (D_a) is obtained as follows:

$$D_a = \frac{2\left(1-D\right)V_{\text{in}}D}{2\left(1-D\right)V_{\text{in}} - \left(1-2D\right)V_o}. \tag{18}$$

The equivalent circuit of the converter in the third operating mode is shown in Fig. 2(c). In the third operating mode, the current of capacitor C_4 is equal to the current of capacitor C_5 ($i_{C4} = i_{C5} = i_{Co}$) and the average output current is obtained as follows:

$$i_{Co} = \frac{1}{2}D_a I_{L(\text{peak})} - I_o. \tag{19}$$

By substituting (16) and (18) into (19), the current i_{Co} is obtained as follows:

$$i_{Co} = \frac{2(1D)^2V^2D^2}{\left[2\left(1-D\right)V_{\text{in}} - \left(1-2D\right)V_o\right]\left(1-2D\right)Lf_s} - \frac{V_o}{R_L}. \tag{20}$$

The voltage gain of the proposed converter in DCM can be obtained by further simplifying (20)

$$M_{\text{DCM}} = \frac{(1D)}{(12D)}\left[1 \pm \sqrt{1 + \frac{2R_LD^2}{Lf_s}}\right]. \tag{21}$$

E. Boundary Conditions Between CCM and DCM

To check the performance of the converter, it is necessary to determine the boundary conditions. In general, in the boundary conditions of the converter, the maximum inductor current ripple (ΔI_L) should be twice the average inductor current (I_L). The boundary conditions can be defined as follows:

$$\begin{cases} \tau > \tau_B : \text{CCMmode} \\ \tau < \tau_B : \text{DCMmode} \\ \tau = \tau_B : \text{Boundarymode} \end{cases}. \tag{22}$$

Using (13), the average inductor current and inductor current ripple are obtained as follows:

$$\begin{cases} I_L = \frac{4}{(1-2D)}I_o \\ \Delta I_L = \frac{2(1-D)DV_{\text{in}}}{(1-2D)Lf_s} \\ I_{L1-\text{min}} = I_L - \frac{\Delta I}{2} \\ L \geq \frac{(1-D)(1-2D)DR_L}{16f_S} \end{cases}. \tag{23}$$

Using (23), the normalized time constant of the inductor is obtained as follows:

$$\tau = \frac{16Lf_S}{R_L}. \tag{24}$$

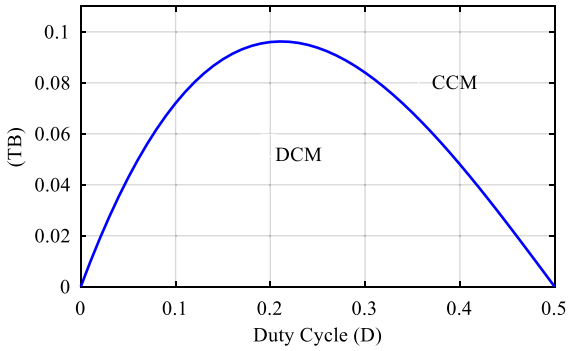


Fig. 4. Boundary condition of the proposed converter.

Using (23), the normalized boundary time constant of the inductor is obtained as follows:

$$\tau_B = \left(1-D\right)\left(1-2D\right)D. \tag{25}$$

The boundary conditions of the proposed converter to determine the CCM and DCM operating modes are shown in Fig. 4.

III. Comparative Study

To provide a comprehensive comparison of the number of passive and active components, voltage stress and current of passive and active devices, and finally, the voltage gain of the proposed converter and converters [2], [6], [13], [18], [32] and [33] are shown in Table I. For a fair comparison, similar structures were used for comparison, with no significant variances in the number of components and the type of inductor compared to the proposed converter. The total number of passive and active devices in the proposed converter is similar to converter [33] and is less than in converters [13] and [32] and more than in converters [2], [6], and [18]. The proposed converter and converters [6], [18] and [33] uses two switches, whereas converters [2], [13], and [32] use only one switch. The number of inductors and capacitors in the proposed converter is similar to that in converter [6] and [33] and fewer than in converters [2], [13], [18], and [32]. The proposed converter similar to converter [33] have more diodes than the converters [2], [6], [13], [18], and [32].

According to Table I, the voltage stress on capacitor C_o in converters [6] and [32] and capacitor C_6 in converter [13] is equal to the output voltage of the converter, resulting in a high value. In the proposed converter, although the voltage stress on capacitor C_3 is higher than that on capacitors C_1, C_2, C_4, and C_5, it remains lower than the voltage stress on capacitor C_o in converters [6] and [32], capacitor C_4 in converter [2], capacitor C_6 in converter [13], and capacitor C_3 in converter [18]. Capacitors C_1 and C_2 in the proposed converter exhibit the lowest voltage stress. In general, the voltage stress on capacitors in the proposed converter is lower compared to converters [2], [6], [13], [18], and [32].

The operating modes of the converters are determined by turning the diodes ON and OFF. The lower the voltage stress on a diode, the lower nominal voltage diode that can be used.

TABLE I
COMPARISON OF CONVERTER COMPONENTS, COMPONENT VOLTAGE STRESS, AND VOLTAGE GAIN

	Converter of reference [2]	Converter of reference [6]	Converter of reference [13]	Converter of reference [18]	Converter of reference [32]	Converter of reference [33]	Proposed converter
Capacitor	4	4	6	4	5	5	5
Inductor	3	2	4	3	3	1	1
Diode	4	4	5	3	5	6	6
Switch	1	2	1	2	2	2	2
Sum of components	12	12	16	12	15	14	14
Common ground	☑	☒	☑	☒	☑	☑	☑
Type of clamping	Common ground	Active clamping	Common ground	Passive clamping	Common ground	Common ground	Common ground
Voltage gain (G)	$\frac{(1+D)}{(1-D)^2}$	$\frac{4}{(1-D)}$	$\frac{1+2D-2D^2}{(1-D)^2}$	$\frac{3-D}{1-2D}$	$\frac{2}{(1-2D)(1-D)}$	$\frac{4}{1-2D}$	$\frac{4}{1-2D}$
Capacitor voltage stress (V_C/V_{in})	$V_{C_1}=\frac{1}{(1-D)}$ $V_{C_2}=\frac{D}{(1-D)^2}$ $V_{C_3}=\frac{1}{(1-D)^2}$ $V_{C_4}=\frac{(3D-D^2)}{(1-D)^2}$	$V_{C_1}=V_{C_3}=\frac{G}{2}$ $V_{C_B}=1$ $V_{C_o}=G$	$V_{C_1}=\frac{1}{(1-D)}$ $V_{C_2}=\frac{1}{(1-D)^2}$ $V_{C_3}=\frac{(2D-D^2)}{(1-D)^2}$ $V_{C_4}=V_{C_5}=\frac{D}{(1-D)}$ $V_{C_6}=G$	$V_{C_1}=\frac{(1-D)G}{(3-D)}$ $V_{C_2}=\frac{DG}{(3-D)}$ $V_{C_3}=\frac{2G}{(3-D)}$ $V_{C_4}=\frac{(1+D)G}{(3-D)}$	$V_{C_1}=\frac{1-D}{(1-2D)}$ $V_{C_2}=\frac{D}{(1-2D)}$ $V_{C_3}=\frac{1}{(1-2D)}$ $V_{C_4}=V_{C_5}=\frac{1}{(1-2D)(1-D)}$	$V_{C_1}=V_{C_2}=\frac{G}{4}$ $V_{C_3}=V_{C_4}=$ $V_{C_5}=\frac{G}{2}$	$V_{C_1}=V_{C_2}=\frac{G}{4}$ $V_{C_3}=\frac{3G}{4}$ $V_{C_4}=V_{C_5}=\frac{G}{2}$
Diode voltage stress (V_D/V_{in})	$V_{D_1}=\frac{4}{(1-D)}$ $V_{D_2}=\frac{D}{(1-D)^2}$ $V_{D_3}=V_{D_4}=$ $\frac{1}{(1-D)^2}$	$V_{D_1}=V_{D_2}$ $=V_{D_o}=\frac{G}{2}$ $V_D=\frac{G}{4}$	$V_{D_1}=V_{D_4}=V_{D_5}$ $=\frac{1}{(1-D)}$ $V_{D_2}=V_{D_3}$ $=\frac{1}{(1-D)^2}$	$V_{D_1}=\frac{G}{(3-D)}$ $V_{D_2}=V_{D_3}$ $=\frac{2G}{(3-D)}$	$V_{D_1}=V_{D_2}=$ $\frac{1-D}{(1-2D)}$ $V_{D_3}=V_{D_4}=$ $V_{D_5}=\frac{G}{2}$	$V_{D_1}=V_{D_2}=$ $V_{D_6}=\frac{G}{4}$ $V_{D_3}=V_{D_4}=$ $V_{D_5}=\frac{G}{2}$	$V_{D_1}=V_{D_2}=\frac{G}{4}$ $V_{D_3}=V_{D_4}=$ $V_{D_5}=V_{D_6}=$ $\frac{G}{2}$
Switch voltage stress (V_S/V_{in})	$V_S=\frac{D}{(1-D)^2}$	$V_{S_1}=V_{S_2}=\frac{G}{4}$	$V_S=\frac{1}{(1-D)^2}$	$V_{S_1}=V_{S_2}=\frac{G}{(3-D)}$	$V_{S_1}=\frac{1-D}{(1-2D)}$ $V_{S_2}=\frac{DG}{2}$	$V_{S_1}=\frac{G}{4}$ $V_{S_2}=\frac{G}{2}$	$V_{S_1}=V_{S_2}=\frac{G}{4}$
Current through the inductor (i_L/I_o)	$I_{L_1}=G$ $I_{L_2}=\frac{(1+D)}{(1-D)}$ $I_{L_3}=1$	$I_{L_1}=I_{L_2}$ $=\frac{G}{2}$	$I_{L_1}=G$ $I_{L_2}=\frac{1}{(1-D)}$ $I_{L_3}=I_{L_4}=1$	$I_{L_1}=\frac{(2-2D+D^2)G}{(1-D)(3-D)}$ $I_{L_2}=\frac{1}{(1-D)}$ $I_{L_3}=\frac{(2+D)G}{(3-D)}$	$I_{L_1}=I_{L_2}=G$ $I_{L_3}=\frac{2}{(1-D)}$	$I_L=G$	$I_L=G$
Current through the switch (i_S/I_o)	$i_S=\frac{(3-D)}{(1-D)^2}$	$i_{S_1}=i_{S_2}=$ $\frac{(3+D)}{D(1-D)}$	$i_S=\frac{(4-3D)}{(1-D)^2}$	$i_{S_1}=\frac{1+D-D^2}{D(1-D)(1-2D)}$ $i_{S_2}=\frac{1}{D(1-D)}$	$I_{S_1}=$ $\frac{(1+3D)G}{2}$ $I_{S_2}=$ $\frac{(1-D-2D^2)}{(1-D)}$	$i_{S_1}=\frac{G}{2D}$ $i_{S_2}=\frac{(1+2D)G}{4D}$	$i_{S_1}=i_{S_2}=\frac{G}{2D}$
Current through the diode (i_D/I_o)	$i_{D_1}=i_{D2}=G$ $i_{D_3}=i_{D_4}=\frac{1}{(1-D)}$	$i_{D_1}=i_{D2}=\frac{G}{4}$ $i_D=\frac{G}{2D}$ $i_{D_o}=\frac{1}{D}$	$i_{D_1}=i_{D_3}=i_{D_4}$ $=i_{D_5}=\frac{1}{(1-D)}$ $i_{D_2}=\frac{(3-2D)}{(1-D)^2}$	$i_{D_1}=\frac{G}{(1-D)}$ $i_{D_2}=\frac{1}{(1-D)}$ $i_{D_3}=\frac{1}{D}$	$i_{D_1}=G$ $i_{D_2}=\frac{2}{(1-D)}$ $i_{D_3}=i_{D_4}=i_{D_5}=1$	$i_{D_1}=i_{D_6}=$ $\frac{G}{2(1-D)}$ $i_{D_2}=\frac{G}{2D}$ $i_{D_3}=i_{D_5}=$ $\frac{1}{(1-D)}$ $i_{D_4}=\frac{1}{D}$	$i_{D_1}=i_{D_2}=$ $\frac{G}{2(1-D)}$ $i_{D_3}=i_{D_5}=\frac{1}{D}$ $i_{D_4}=i_{D_6}=$ $\frac{1}{(1-D)}$

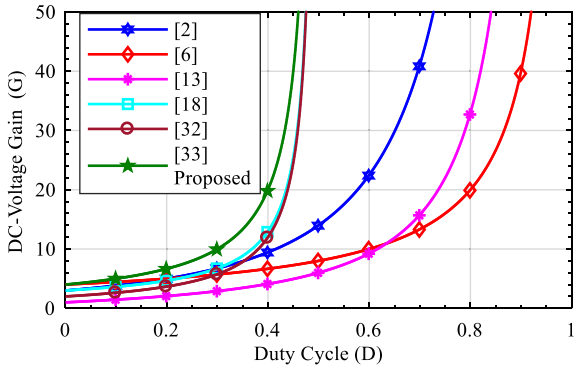


Fig. 5. Comparison of the voltage boosting factor of the proposed converter with converters [2], [6], [13], [18], [32], and [33].

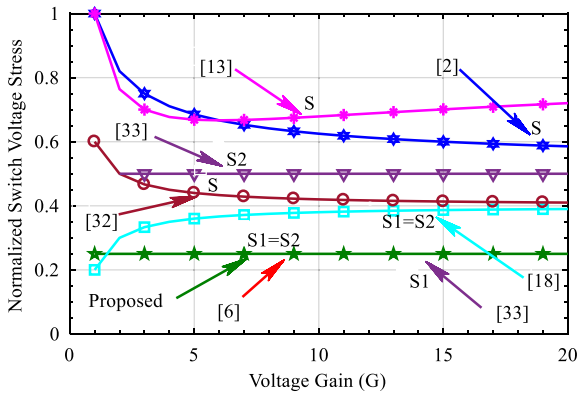


Fig. 6. Comparison of the voltage stress of the proposed converter's switch with comparative converters.

Table I shows that diodes D_3 and D_4 in converter [13], D_3 and D_4 in converter [18], and D_4 in the converter [2] have the highest voltage stress. In the proposed converter, the voltage stress of diodes D_3, D_4, D_5, and D_6 Similar to the voltage stress of diodes D_3, D_4, and D_5 in the converter [33] and is half of the gain factor, while for diodes D_1 and D_2, proposed converter it is a quarter of the gain factor. In general, the voltage stress on the diodes in the proposed converter is lower compared to converters [2], [6], [13], [18], and [32].

The current stress of active and passive devices, based on the gain factor of the converter, is shown in Table I. The current stress of the inductor L_3 in converters [2], [13], [18], and [32] is lower compared to the proposed converter. The current stress of the inductor L in the proposed converter is similar to the current stress of the inductor L_1 in converters [2] and [13] and the inductors L_1 and L_2 in converter [32]. The current stress of the switch S_2 in converter [18] is relatively high. In the proposed converter, the current stress of switches S_1 and S_2 is equal and comparable to the current stress of the switch S in converters [2] and [13] and the current stress of switches S_1 and S_2 in converter [6].

Diode D_1 in converter [32], diode D_1 in converter [18], diode D_2 in converter [13], and diodes D_1 and D_2 in converter [2] have the highest diode current stress. In the proposed converter, although the current stress of diodes D_1 and D_2 is higher, it remains lower than the current stress of diode D_1 in converters [18], [32].and [33] The current stress of diodes D_3 and D_5 in the proposed converter is lower than the current stress of diodes D_1, D_2, and D_3 in converter [2], diodes D_1, D_2, and D in converter [6], diodes D_1, D_2, D_3, D_4, and D_5 in converter [13], diodes D_1 and D_3 in converter [18], and diodes D_1, D_2, and D_5 in converter [32]. The current stress of diodes D_4 and D_6 in the proposed converter and diodes D_3 and D_4in converter [32] are similar and lower than the current stress of diodes D_3 and D_5 in the proposed converter.

A. Comparison of Voltage Boosting Factor

According to Table I and Fig. 5, the voltage gain factor of the proposed converter is higher than converters [2], [6], [13], [18], [32], and [33]. It is noteworthy that in this comparison, the range of changes in the duty cycle of the proposed converter is similar to converters [18] and [32] and different from converters [2], [6], and [13]. A fair comparison is possible for different values of the duty cycle, which will be done further by considering the parasitic resistances and real gain. One of the important features of the proposed converter is that it can produce high voltage gain in low switching intervals.

B. Comparison of Switch Voltage Stress

Power semiconductor switches are critical components of dc–dc converters. The lower the voltage across the switches during the off state, the more feasible it becomes to use switches with lower rated voltage and power, which in turn reduces the cost and size of the switch and its associated components. Fig. 6 compares the voltage stress of the proposed converter's switch with those in converters [2], [6], [13], [18], [32], and [33]. The switch (S) in converter [13] experiences the highest voltage stress. The voltage stress of the switches S_1 and S_2 in the proposed converter is similar to that of the switches S_1 and S_2 in converter [6] and switches S_1 converter [33] and one-quarter of the converter's voltage gain. Since the proposed converter combines a quasi-impedance source network with a Ladder-SC and places the switches on the side of the impedance source network, the voltage stress on both switches is lower than that of the switches in converters [2], [13], [18], [32] and S_2 in converter [33].

C. Comparison of the Real Gain Factor

In this section, the effect of parasitic elements on the output voltage and efficiency is analyzed. The proposed converter circuit with parasitic elements is shown in Fig. 7. The parasitic parameters of the proposed converter include the equivalent series resistance of the inductor (r_L), the equivalent series resistance of the capacitors (r_{C1}, r_{C2}, r_{C3}, and r_{C4}), the equivalent resistance during the conduction state of the switches (r_{S1} and r_{S2}), the internal resistances in the on the state of the diodes (r_{D1}, r_{D2}, r_{D3}, r_{D4}, r_{D5}, and r_{D6}), and the forward bias voltages of the diodes (V_{D1}, V_{D2}, V_{D3}, V_{D4}, V_{D5}, and V_{D6}). The operation

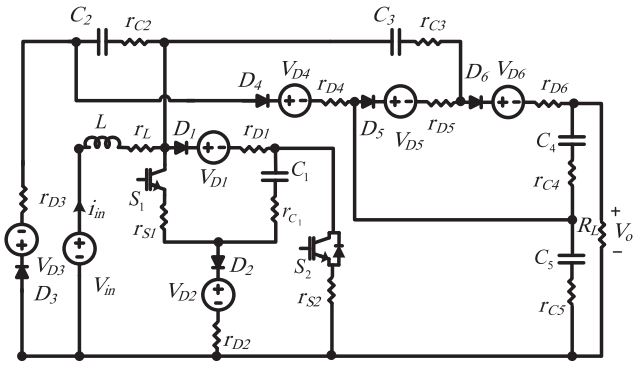


Fig. 7. Proposed converter circuit with parasitic elements.

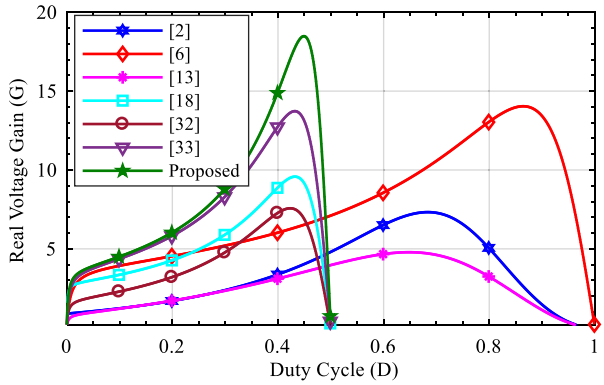


Fig. 8. Comparison of the real gain factor of the proposed converter with comparative converters.

TABLE II
SERIES RESISTORS OF THE PROPOSED CONVERTER

	Parameters	value
1	Inductor series resistance	0.04 Ω
2	Capacitor series resistance	0.07 Ω
3	Switch series resistance	0.04 Ω
4	Diode series resistance	0.02 Ω
5	Diode forward bias voltage	0.73 V

analysis of the converter in the real state is similar to that in the ideal state, with the addition of the equivalent series resistances.

Table II shows the equivalent series resistances of the inductor, capacitor, switch, and diode and the forward bias voltage of the diode. Considering the parasitic parameters, the inductor voltage can be expressed during the time interval (DT_s) using (26) and during the time interval (1–D)T_s using (27). The voltage boosting factor of the proposed converter is the real state is obtained according to (28) shown at the bottom of the next page.

$$\begin{cases} v_L = -r_L I_L + r_{S_1} i_{C_1,\text{on}} + V_{C_1} + r_{C_1} i_{C_1,\text{on}} + r_{S_2} i_{C_1,\text{on}} + V_{\text{in}} \\ v_L = -r_L I_L + r_{C_2} i_{C_2,\text{on}} + V_{C_2} + V_{D_3} + r_{D_3} i_{C_2,\text{on}} + V_{\text{in}} \\ v_L = -r_L I_L + r_{C_3} i_{C_3,\text{on}} + V_{C_3} + V_{D_5} + r_{D_5} i_{C_3,\text{on}} \\ \quad -r_{C_5} i_{C_5,\text{on}} - V_{C_5} + V_{\text{in}} \end{cases} \tag{26}$$

$$\begin{cases} v_L = -r_L I_L - V_{D_1} - r_{D_1} i_{C_1,\text{off}} - V_{C_1} - r_{C_1} i_{C_1,\text{off}} \\ -V_{D_2} - r_{D_2} i_{C_1,\text{off}} + V_{\text{in}} \\ v_L = -r_L I_L + V_{C_2} + r_{C_2} i_{C_2,\text{off}} - V_{D_4} + r_{D_4} i_{C_2,\text{off}} \\ -r_{C_5} i_{C_5,off} - V_{C_5} + V_{\text{in}} \\ v_L = -r_L I_L + r_{C_3} i_{C_3,\text{off}} + V_{C_3} - V_{D_6} + r_{D_6} i_{C_3,\text{off}} \\ \quad -r_{C_4} i_{C_4,\text{off}} - V_{C_4} - r_{C_5} i_{C_5,\text{off}} - V_{C_5} + V_{\text{in}} \end{cases} \tag{27}$$

The comparison of the real voltage gain of the proposed converter with that of the reference converters is illustrated in Fig. 8. Although the switching duty cycle range of the proposed converter differs from those of the reference

TABLE III
COST COMPARISON OF THE PROPOSED STRUCTURE AND COMPARATIVE CONVERTERS

	Price ($)				Total cost ($)
	C	L	D	M	
[2]	9.37	23.7	6.58	3. 2	42.85
[6]	5.32	11.96	7.21	3. 2	27.69
[13]	5.48	27.64	7.91	2.63	43.66
[18]	2.44	22.04	5.25	3. 2	32.93
[32]	7.64	28.57	8.57	3. 2	47.98
[33]	3.62	8.11	10.54	6.38	28.65
Proposed	3.12	8.11	10.54	5.9	27.67

M: Mosfets, D: Diodes, C: Capacitors, L: Inductor, The price of components from www.mouser.com

Converters [2], [6], and [13], the maximum real voltage gain achieved by the proposed topology is higher than that of the other structures. Specifically, compared to the reference converters [2], [6], [13], [18], [32], and [33], the proposed converter exhibits real voltage gain improvements of 252%, 131%, 386%, 193%, 244%, and 134%, respectively. These results clearly demonstrate the superiority of the proposed converter in voltage boosting capability over the aforementioned structures.

D. Cost Comparison

Table III presents the calculated cost results of the proposed converter and converters [2], [6], [13], [18], [32], and [33], based on the total cost of active and passive components. The purpose of this comparison is to provide a more detailed analysis and highlight the economic advantages of the proposed converter. According to the obtained results, the total cost of the proposed converter is lower than that of the other compared converters.

IV. SMALL-SIGNAL ANALYSIS

The small-signal method is used to analyze the dynamic behavior of the converter and also to design the closed-loop control to stabilize the output voltage at the desired value. In

the small-signal model, the inductor current (I_L) and capacitor voltage (V_C) are considered as state variables. The state-space equations are expressed as follows:

$$\begin{cases} X' = [DA_1 + (1-D)A_2]\,X + [DB_1 + (1-D)B_2]\,u \\ y = [DE_1 + (1-D)E_2]\,X + [DF_1 + (1-D)F_2]\,u \end{cases} \tag{29}$$

where *X* represents the state vector of the proposed converter, *u* is the input vector, which includes the independent inputs of the system, and *y* is the output vector, including any dependent variables in the converter. In the first operating mode when the switches are on, capacitors (C_1, C_3, and C_5) and capacitors (C_1 and C_2) form a loop together. Considering that an invalid state variable is generated for each loop, therefore, the resistance ($R_3 = 0.1\ \Omega$) in the first ring and in series with capacitor C_3 and the resistance ($R_2 = 0.1\ \Omega$) in the second ring and in series with capacitor C_2 are considered as the sum of the equivalent series resistance of the capacitors in each ring and in this way, the invalid state variables are removed [31]. The state equations for the time interval of turning on the switches can be expressed as follows:

$$A_1 = \begin{bmatrix} 0 & \frac{1}{L} & 0 & 0 & 0 & 0 \\ -\frac{1}{C_1} & -\frac{R_2+R_3}{C_1R_2R_3} & \frac{1}{C_1R_2} & \frac{1}{C_1R_3} & 0 & -\frac{1}{C_1R_3} \\ 0 & \frac{1}{C_2R_2} & -\frac{1}{C_2R_2} & 0 & 0 & 0 \\ 0 & \frac{1}{C_3R_3} & 0 & -\frac{1}{C_3R_3} & 0 & \frac{1}{C_3R_3} \\ 0 & 0 & 0 & 0 & -\frac{1}{C_4R_L} & -\frac{1}{C_4R_L} \\ 0 & -\frac{1}{C_5R_3} & 0 & \frac{1}{C_5R_3} & -\frac{1}{C_5R_L} & -\frac{R_3+R_L}{C_5R_3R_L} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad E_1 = [0\ \ 0\ \ 0\ \ 0\ \ 1\ \ 1] \quad F_1 = [0]. \tag{30}$$

In the second operating mode when the switches are off, capacitors (C_1, C_3, C_4, and C_5) and capacitors (C_1, C_2, and C_5) form a loop together. So there are two invalid state variables in this situation. As in the first operating mode, consider the resistance ($R_3 = 0.1\ \Omega$) in the first ring and in series with capacitor C_3 and the resistance ($R_2 = 0.1\ \Omega$) in the second ring and in series with capacitor C_2 as the sum of the series resistances of the capacitors in the rings and in this way, the invalid state variables are removed. The state equations for the time interval of turning off the switches can be expressed as (31) shown at the bottom of the next page. The state variables, input variable, output variable, and switching interval of the converter, in addition to a constant dc value, also have an ac fluctuation value, which is shown in (32)

$$\begin{cases} i_L = I_L + \hat{i}_L \\ v_{C1} = V_{C1} + \hat{v}_{C1} \\ v_{C2} = V_{C2} + \hat{v}_{C2} \\ v_{C3} = V_{C3} + \hat{v}_{C3} \\ v_{C4} = V_{C4} + \hat{v}_{C4} \\ v_{C5} = V_{C5} + \hat{v}_{C5} \\ v_{\text{in}} = V_{\text{in}} + \hat{v}_{\text{in}} \\ v_o = V_o + \hat{v}_o \\ d(t) = D + \hat{d}(t) \end{cases} . \tag{32}$$

The ac fluctuation of the state variables in the proposed converter is $\hat{x} = [\hat{i}_L \quad \hat{v}_{C1} \quad \hat{v}_{C2} \quad \hat{v}_{C3} \quad \hat{v}_{C4} \quad \hat{v}_{C5}]^T$, $\hat{u} = [\hat{v}_{\text{in}}]$, $\hat{y} = [\hat{v}_o]$ and the duty cycle of the switch is $(\hat{d})$. The small-signal equations for the proposed converter are obtained by removing the dc component and the second-order ac component using the following:

$$\begin{aligned} A &= (D)\,A_1 + (1-D)\,A_2 \\ B &= (D)\,B_1 + (1-D)\,B_2 \\ E &= (D)\,E_1 + (1-D)\,E_2 \\ F &= (D)\,F_1 + (1-D)\,F_2 \\ C &= [(A_1 - A_2)\,X + (B_1 - B_2)\,u] \\ &\quad + [(E_1 - E_2)\,X + (F_1 - F_2)\,u] \end{aligned}$$

$$\begin{cases} \hat{x}' = A\hat{x} + B\hat{u} + C\hat{d}(t) \\ \hat{y} = E\hat{x} + F\hat{u} \end{cases} . \tag{33}$$

By substituting (30) and (31) into (33), the small-signal converter equations can be expressed according to (34) shown at the bottom of the next page. By applying Laplace in (34), the transfer function of the output voltage ($\hat{v}_o(s)$) in terms of the duty cycle ($\hat{d}(s)$) in the proposed system can be expressed according to (35).

The transfer function of the output voltage ($\hat{v}_o(s)$) in terms of the duty cycle ($\hat{d}(s)$) of the proposed converter has six poles all of which are in the left half of the imaginary axis, which includes four real poles and two complex poles close to the imaginary axis. Also, this transfer function contains four zeros, which include two real zeros and two complex zeros.

$$G_{\text{real}} = \frac{\frac{4}{1-2D}\left(1 - \frac{V_{D_1}+V_{D_2}}{2V_{\text{in}}}\right) - \left(\frac{V_{D_3}+V_{D_4}+V_{D_5}+V_{D_6}}{V_{in}}\right)}{\begin{bmatrix} a_1 r_L + a_2(r_{S_1} + r_{S_2}) + a_3 r_{C_1} + a_4(r_{C_2} + r_{C_3}) + a_5 r_{C_4} + a_6 r_{C_5} + a_7\,(r_{D_1} + r_{D_2}) + a_8(r_{D_3} + r_{D_5}) \\ + a_9\,(r_{D_4} + r_{D_6}) \end{bmatrix} \frac{1}{R_L} + 1}$$

$$\begin{cases} a_1 = \frac{16}{(1-2D)^2}, a_2 = \frac{4}{D(1-2D)^2}, a_4 = \frac{1}{D(1-D)}, a_3 = \frac{4}{D(1-D)(1-2D)^2} \\ a_5 \frac{D}{(1-D)}, a_6 = \frac{(1+D)^2}{D(1-D)}, a_7 = \frac{4}{(1-D)(1-2D)^2}, a_8 = \frac{1}{D}, a_9 = \frac{1}{(1-D)}. \end{cases} \tag{28}$$

Like most high-boost converters, the proposed converter has a right-hand zero. This right-hand zero leads to the nonminimum phase behavior of boost converters. The right-hand zero limits the bandwidth of the modeled system. As a result, the system's phase margin (PM) decreases and the dephasing time or dynamic response of the output voltage becomes slower

$$G_c(s) = \frac{2.5 \times 10^{-6} \times (s+220)^2}{s}. \tag{36}$$

The bode diagram of the system is shown in Fig. 9(a). This system has a gain margin of –56.4 dB and a phase margin of –85.8°. Because the gain margin and phase margin of the system are negative, therefore the closed-loop feedback of the system will become unstable. To improve the dynamic performance and also stabilize the closed-loop system, a controller should be designed to stabilize the closed-loop system and improve the dynamic performance of the system. Based on (35) and

$$A_2 = \begin{bmatrix} 0 & -\frac{1}{L} & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & -\frac{R_2+R_3}{C_1R_2R_3} & -\frac{1}{C_1R_2} & -\frac{1}{C_1R_3} & \frac{1}{C_1R_3} & \frac{R_2+R_3}{C_1R_2R_3} \\ 0 & -\frac{1}{C_2R_2} & -\frac{1}{C_2R_2} & 0 & 0 & \frac{1}{C_2R_2} \\ 0 & -\frac{1}{C_3R_3} & 0 & -\frac{1}{C_3R_3} & \frac{1}{C_3R_3} & \frac{1}{C_3R_3} \\ 0 & \frac{1}{C_4R_3} & 0 & \frac{1}{C_4R_3} & -\frac{R_3+R_L}{C_4R_3R_L} & -\frac{R_3+R_L}{C_4R_3R_L} \\ 0 & \frac{R_2+R_3}{C_5R_2R_3} & \frac{1}{C_5R_2} & \frac{1}{C_5R_3} & -\frac{R_3+R_L}{C_5R_3R_L} & -\frac{R_3R_2+R_2R_L+R_3R_L}{C_5R_2R_3R_L} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad E_2 = [0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1] \quad F_2 = [0]. \tag{31}$$

$$A = \begin{bmatrix} 0 & -\frac{(1-2D)}{L} & 0 & 0 & 0 & 0 \\ \frac{(1-2D)}{C_1} & -\frac{R_2+R_3}{C_1R_2R_3} & -\frac{(1-2D)}{C_1R_2} & -\frac{(1-2D)}{C_1R_3} & \frac{(1-D)}{C_1R_3} & \frac{R_2(1-2D)+R_3(1-D)}{C_1R_2R_3} \\ 0 & -\frac{(1-2D)}{C_2R_2} & -\frac{1}{C_2R_2} & 0 & 0 & \frac{(1-D)}{C_2R_2} \\ 0 & -\frac{(1-2D)}{C_3R_3} & 0 & -\frac{1}{C_3R_3} & \frac{(1-D)}{C_3R_3} & \frac{1}{C_3R_3} \\ 0 & \frac{(1-D)}{C_4R_3} & 0 & \frac{(1-D)}{C_4R_3} & -\frac{R_3+(1-D)R_L}{C_4R_3R_L} & -\frac{R_3+(1-D)R_L}{C_4R_3R_L} \\ 0 & \frac{R_2(1-D)+R_3(1-2D)}{C_5R_2R_3} & \frac{(1-D)}{C_5R_2} & \frac{1}{C_5R_3} & -\frac{R_3+(1-D)R_L}{C_5R_3R_L} & -\frac{R_3R_2+R_2R_L+R_3R_L(1-D)}{C_5R_2R_3R_L} \end{bmatrix}$$

$$B = DB_1 + (1-D)B_2$$

$$B = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

$$C = [(A_1 - A_2)X + (B_1 - B_2)u] + [(E_1 - E_2)X + (F_1 - F_2)u]$$

$$\mathrm{C} = \begin{bmatrix} 0 & \frac{2}{L} & 0 & 0 & 0 & 0 \\ \frac{-2}{C_1} & 0 & \frac{2}{C_1R_2} & \frac{2}{C_1R_3} & \frac{-1}{C_1R_3} & \frac{-2R_2-R_3}{C_1R_2R_3} \\ 0 & \frac{2}{C_2R_2} & 0 & 0 & 0 & \frac{-1}{C_2R_2} \\ 0 & \frac{2}{C_3R_3} & 0 & 0 & \frac{-1}{C_3R_3} & 0 \\ 0 & \frac{-1}{C_4R_3} & 0 & \frac{-1}{C_4R_3} & \frac{R_L}{C_4R_3R_L} & \frac{R_L}{C_4R_3R_L} \\ 0 & \frac{-2R_3-R_2}{C_5R_2R_3} & -\frac{1}{C_5R_2} & 0 & \frac{R_L}{C_5R_3R_L} & \frac{R_3R_L}{C_5R_2R_3R_L} \end{bmatrix}$$

$$E = DE_1 + (1-D)E_2$$

$$E = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

$$F = DF_1 + (1-D)F_2$$

$$F = [0] \tag{34}$$

$$G_{v_o,d}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{V}_{in}(s)=0}$$

$$\frac{-9.004 \times 10^{10}S^4 - 4.48 \times 10^{16}S^3 - 6.15 \times 10^{21}S^2 - 1.083 \times 10^{26}S + 2.159 \times 10^{30}}{S^6 + 2.393 \times 10^6 S^5 + 9.462 \times 10^{11}S^4 + 1.078 \times 10^{17}S^3 + 3.212 \times 10^{21}S^2 + 3.457 \times 10^{23}S + 2.163 \times 10^{27}}. \tag{35}$$

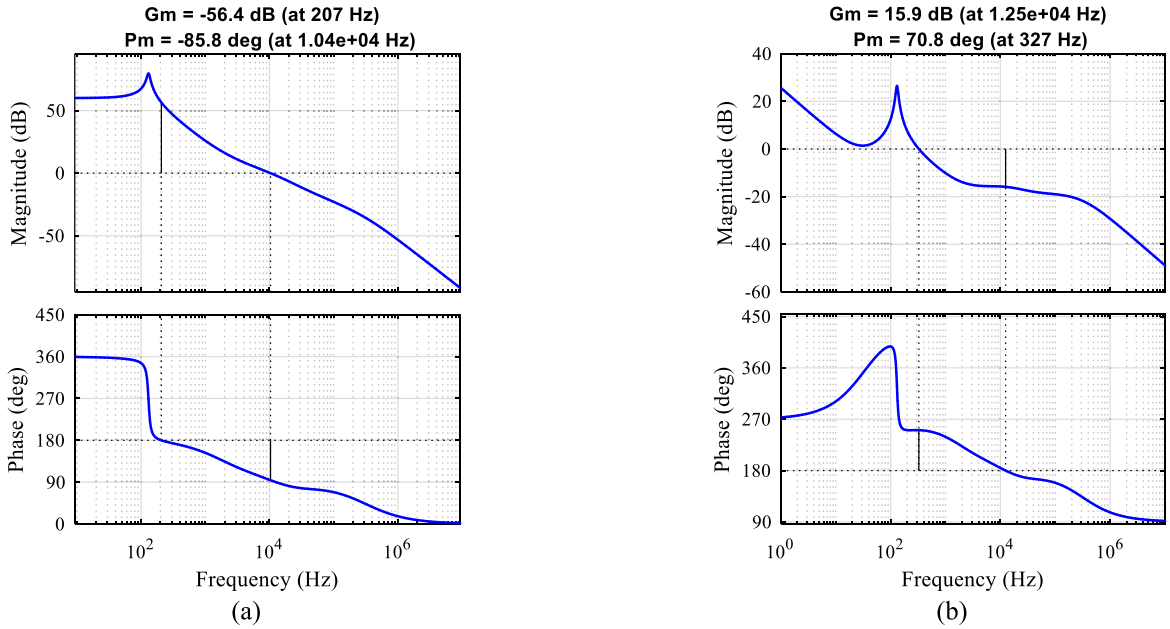


Fig. 9. System transfer function bode diagram. (a) Before applying the controller. (b) After applying the controller.

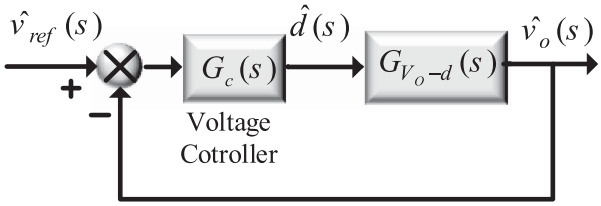


Fig. 10. Control block diagram of the proposed system.

using MATLAB software SISOTOOL and considering the system control requirements including gain margin (Gm>6) and phase margin (75°>Pm>45°), the controller can be obtained according to (36). The bode diagram of the system after applying the controller is shown in Fig. 9(b). The gain margin and phase margin of the system are 15.9 dB and 70.8°, respectively. The positive values of these parameters confirm the stability of the closed-loop system.

The voltage loop control scheme for the proposed converter is shown in Fig. 10, where G_c is the system controller and $G_{VO\text{-}d}$ is the system transfer function.

V. Calculation of Efficiency

The efficiency of the converter is determined by calculating the losses of active elements, including switches and diodes, and passive elements, including inductors and capacitors. To calculate losses in the proposed structure, the

following assumptions are made.

1) Diode losses include conduction losses and turn-OFF losses. The conduction of diodes is modeled as a resistance r_D and a voltage source $V_{F,D}$, which represent the resistance in the conduction state and the voltage drop during diode conduction, respectively.
2) Internal resistance of inductors (r_L) and internal resistance of capacitors (r_C) are considered in series with inductor and capacitor.
3) Power switches are considered an ideal switch in series with resistance (r_S). r_S represents the conduction mode resistance of the switch.

A. Switch Losses

Semiconductor switch losses include conduction losses and switching losses, which will be discussed as follows.

1) Switch Conduction Losses: Conduction loss is caused by the resistance in the conducting state of semiconductor elements, which is calculated by multiplying the RMS current passing through the semiconductor during its conduction state. Assuming the current variations in the switches during the switching period are linear, the conduction loss of the switch is expressed as follows:

$$P_{\text{cond}} = \frac{1}{T_s}\int_0^{T_S} r_S i_{S,\text{rms}}^2 dt. \tag{37}$$

Using (14), the RMS current passing through switches (S_1 and S_2) is as follows:

$$I_{S_1,\text{rms}} = I_{S_2,\text{rms}} = \sqrt{D}\left(\frac{2}{D(1-2D)}I_o\right). \tag{38}$$

Using relations (37) and (38), the conduction losses of switches (S_1 and S_2) are obtained as follows:

$$P_{S_1,\text{cond}} = P_{S_2,\text{cond}} = D\left[r_S\left(\frac{2I_o}{D(1-2D)}\right)^2\right]. \tag{39}$$

2) Switching Losses: Switching losses occur due to the presence of nonzero current and voltage at the moments when semiconductor elements are turned ON and OFF. These losses are

calculated as the product of the voltage and current waveforms during the switching period, as follows:

$$P_{\text{sw}}^{\text{on}} = \frac{1}{T_s}\int_0^{t_{\text{on}}} V_s(t)\, i_s(t)\, dt = \frac{1}{6} f_s V_s i_s t_{\text{on}}$$
$$P_{\text{sw}}^{\text{off}} = \frac{1}{T_s}\int_0^{t_{\text{off}}} V_s(t)\, i_s(t)\, dt = \frac{1}{6} f_s V_s i_s t_{\text{off}}. \quad (40)$$

Using relations (10), (14), and (40), switching losses in the ON-state of switches (S_1 and S_2) as well as in the OFF-state are obtained according to the following:

$$P_{\text{sw},s_1}^{\text{on}} = \frac{1}{T_s}\int_0^{t_{\text{on}}} V_{s_1}(t)\, i_{s_1}(t)\, dt = \frac{V_{\text{in}} I_o t_{\text{on}} f_s}{3D(12D)^2}$$
$$P_{\text{sw},s_2}^{\text{on}} = \frac{1}{T_s}\int_0^{t_{\text{on}}} V_{s_2}(t)\, i_{s_2}(t)\, dt = \frac{V_{\text{in}} I_o t_{\text{on}} f_s}{3D(12D)^2} \quad (41)$$
$$P_{\text{sw},s_1}^{\text{off}} = \frac{1}{T_s}\int_0^{t_{\text{off}}} V_{s1}(t)\, i_{s1}(t)\, dt = \frac{V_{\text{in}} I_o t_{\text{off}} f_s}{3D(12D)^2}$$
$$P_{sw,s_2}^{\text{off}} = \frac{1}{T_s}\int_0^{t_{\text{off}}} V_{s2}(t)\, i_{s2}(t)\, dt = \frac{V_{\text{in}} I_o t_{\text{off}} f_s}{3D(12D)^2}. \quad (42)$$

B. Diode Losses

Diode losses also include conduction losses and switching losses, which will be discussed further.

1) Diode Conduction Losses: The conduction loss of the diode is caused by the resistance in the conduction state of the diode, which is obtained by multiplying the square power of the RMS current passing through the diode and its ON-state resistance (r_D). Also, the diode has a voltage drop in conduction mode and the threshold voltage of the diode ($V_{F,D}$) also causes losses. The conduction loss of the diode is obtained from the following relationship:

$$P_{\text{cond},D} = \frac{1}{T_s}\int_0^{T_S} \left(V_{F,D} i_{D,\text{avg}} + r_D i_{D,\text{rms}}^2\right) dt. \quad (43)$$

Using (15), the average current and RMS current passing through diodes D_1 and D_2 in a switching period are obtained, respectively, according to the following equations:

$$i_{D_1,\text{avg}} = i_{D_2,\text{avg}} = \left(\frac{2}{1-2D}\right) I_o \quad (44)$$

$$i_{D_1,\text{rms}} = i_{D_2,\text{rms}} = \sqrt{1-D}\left(\frac{2}{(1-D)(1-2D)} I_o\right). \quad (45)$$

Using relations (43), (44), and (45), the conduction losses of diodes D_1 and D_2 are obtained as follows:

$$P_{\text{cond},D_1} = P_{\text{cond},D_2} = (1-D)\times$$
$$\left[V_{F,D}\left(\frac{2}{(1-D)(1-2D)} I_o\right) + r_D\left(\frac{2}{(1-D)(1-2D)} I_o\right)^2\right]. \quad (46)$$

Using (14), the average current and RMS current passing through diodes D_3 and D_5 in a switching period are obtained, respectively, according to (46) and (48)

$$i_{D_3,\text{avg}} = i_{D_5,\text{avg}} = I_o \quad (47)$$

$$i_{D_3,\text{rms}} = i_{D_5,\text{rms}} = \sqrt{D}\left(\frac{1}{D} I_o\right). \quad (48)$$

Using relations (43), (47), and (48), the conduction losses of diodes D_3 and D_5 are obtained as follows:

$$P_{\text{cond},D_3} = P_{\text{cond},D_5} = D\left[V_{F,D}\left(\frac{I_o}{D}\right) + r_D\left(\frac{I_o}{D}\right)^2\right]. \quad (49)$$

Using (15), the average current and RMS current passing through diodes D_4 and D_6 in a switching period are obtained, respectively, according to the following:

$$i_{D_4,\text{avg}} = i_{D_6,\text{avg}} = I_o \quad (50)$$

$$i_{D_4,\text{rms}} = i_{D_6,\text{rms}} = \sqrt{1-D}\left(\frac{1}{1-D} I_o\right). \quad (51)$$

Using relations (43), (50), and (51), the conduction losses of diodes D_4 and D_6 are obtained as follows:

$$P_{\text{Cond},D_4} = P_{\text{Cond},D_6} =$$
$$(1-D)\left[V_{F,D}\left(\frac{I_o}{1-D}\right) + r_D\left(\frac{I_o}{1-D}\right)^2\right]. \quad (52)$$

2) Diode Switching Losses: Turning on the diode can be considered like an ideal switch, because it turns on quickly and according to the conditions of the power circuit. Therefore, diode turn-ON losses are neglected ($P_{\text{SW},D}^{\text{on}} 0$). When the diode turns OFF, the diode current changes for a reverse recovery time (t_{rr}), and t_{rr} is divided into two-time intervals ($t_{rr} = t_a + t_b$). In the period t_a, the diode voltage is zero but in the period t_b, the voltage of the diode changes linearly and reaches from zero to the reverse voltage of the two ends of the diode (V_D). The switching loss of the diode at the moment of turning OFF is obtained from the following relationship:

$$P_{\text{sw},D}^{\text{off}} = \frac{1}{T_s}\int_0^{t_{rr}} P_D(t)\, dt = \frac{1}{6} V_D I_{rr} t_{rr} f_s. \quad (53)$$

Using relations (9) and (53), the switching losses of diodes D_1 and D_2 are obtained as follows:

$$P_{\text{sw},D_1}^{\text{off}} = P_{\text{sw},D_2}^{\text{off}} = \frac{V_{\text{in}} I_{rr} t_{rr} f_s}{6(1-2D)}. \quad (54)$$

Using relations (10) and (53), the switching losses of diodes D_3 and D_5 are obtained as follows:

$$P_{\text{sw},D_3}^{\text{off}} = P_{\text{sw},D_5}^{\text{off}} = \frac{V_{\text{in}} I_{rr} t_{rr} f_s}{3(1-2D)}. \quad (55)$$

Using relations (9) and (53), the switching losses of diodes D_4 and D_6 are obtained as follows:

$$P_{\text{sw},D_4}^{\text{off}} = P_{\text{sw},D_6}^{\text{off}} = \frac{V_{\text{in}} I_{rr} t_{rr} f_s}{3(1-2D)}. \quad (56)$$

C. Capacitor Losses

The loss of the capacitor is due to the RMS current passing through the equivalent resistance of the capacitor (r_C) and is expressed as follows:

$$\mathrm{P}_{r_C} = i^2_{C,\mathrm{rms}}.r_C. \tag{57}$$

Using (12), the RMS current of capacitor C_1 is as follows:

$$i_{C_1,\mathrm{rms}} = \sqrt{D\left(\frac{4I_o}{2D\,(1-2D)}\right)^2 + (1-D)\left(\frac{4I_o}{2\,(1-D)\,(1-2D)}\right)^2}. \tag{58}$$

Using relations (57) and (58), the loss of capacitor C_1 is obtained as follows:

$$\mathrm{P}_{r_{C1}} = \left(\frac{4I_o^2}{D\,(1-D)\,(12D)^2}\right).r_C. \tag{59}$$

Using (12), the RMS current of capacitors C_2 and C_3 is as follows:

$$i_{C_2,\mathrm{rms}} = i_{C_3,\mathrm{rms}} = \sqrt{D\left(\frac{I_o}{D}\right)^2 + (1-D)\left(\frac{I_o}{(1D)}\right)^2}. \tag{60}$$

Using relations (57) and (60), losses of capacitors C_2 and C_3 are obtained as follows:

$$\mathrm{P}_{r_{C_2}} = \mathrm{P}_{r_{C_3}} = \left(\frac{I_o^2}{D\,(1-D)}\right).r_C. \tag{61}$$

Using (12), the RMS current of capacitor C_4 is as follows:

$$i_{C_4,\mathrm{rms}} = \sqrt{D(I_o)^2 + (1-D)\left(\frac{DI_o}{1-D}\right)^2}. \tag{62}$$

Using relations (57) and (62), the loss of capacitor C_4 is obtained as follows:

$$\mathrm{P}_{r_{C_4}} = \left(\frac{DI_o^2}{1-D}\right).r_C. \tag{63}$$

Using (12), the RMS current of capacitor C_5 is as follows:

$$i_{C_5,\mathrm{rms}} = \sqrt{D\left(\frac{(1+D)\,I_o}{D}\right)^2 + (1-D)\left(\frac{(1+D)\,I_o}{1-D}\right)^2}. \tag{64}$$

Using relations (57) and (64), the loss of capacitor C_5 is obtained as follows:

$$\mathrm{P}_{r_{C_5}} = \left(\frac{((1+D)\,I_o)^2}{D\,(1-D)}\right).r_C. \tag{65}$$

D. Inductor Losses

Inductor losses include winding losses and core losses, which are discussed as follows.

Inductor winding loss (copper loss) is obtained from the following equation:

$$P_{cu} = r_L I^2_{L,\mathrm{rms}}. \tag{66}$$

Using relations (13) and (66), the winding loss of the inductor (L) is obtained as follows:

$$P_{cu} = r_L\left(\frac{4I_o}{1-2D}\right)^2. \tag{67}$$

The loss of the inductor core is obtained from the following equation:

$$P_{\mathrm{core}} = k f_s^m B_{\mathrm{mag}}^u V_e \tag{68}$$

where k is a constant coefficient and depends on the type of magnetic material, n is a coefficient in the range ($1.5 \le n \le 2.5$) and m is a coefficient in the range ($1 \le m \le 2$), B_{mag} is the magnetic flux density, f_s is the switching frequency, and V_e is the core volume [27], [28].

The following relationship exists between the current passing through the inductor and the magnetic flux (φ):

$$\varphi = \frac{NI_L}{R_C}. \tag{69}$$

Inductance is defined as the ratio of linkage flux (λ) to winding current (I_L):

$$L = \frac{\lambda}{I_L} = \frac{N\varphi}{I_L}. \tag{70}$$

The magnetic flux density (B_{mag}) is obtained as follows:

$$B_{\mathrm{mag}} = \frac{\varphi}{A_e} \tag{71}$$

where φ is the magnetic flux and A_e is the cross section.

By inserting (69), (70) and (71) in (68), the core losses are obtained as follows:

$$P_{\mathrm{core}} \tilde{-} k f_s^m \left(\frac{LI_L}{NA_e}\right)^u V_e. \tag{72}$$

To reduce the losses of the inductor core, high-quality metals should be used, which leads to an increase in the price. Because only one inductor is used in the proposed converter, the loss of the inductor core is very low and the price of the inductor will be lower compared to converters [2], [6], [13], [18], and [32].

By calculating the losses mentioned above, the total losses of the converter can be calculated according to (73). Converter efficiency is also obtained by using (74).

$$P_{\mathrm{loss}}^{\mathrm{total}} = \sum\left(P_{\mathrm{loss}}^{\mathrm{Switch}} + P_{\mathrm{loss}}^{\mathrm{diode}} + P_{\mathrm{loss}}^{\mathrm{capacitor}} + P_{\mathrm{loss}}^{\mathrm{inductor}}\right) \tag{73}$$

$$\eta = \frac{P_o}{P_o + P_{\mathrm{loss}}^{\mathrm{total}}} \times 100\%. \tag{74}$$

Fig. 11(a) shows the efficiency of the proposed converter in the duty cycle (D) at different output powers (P_o) from 100 to 400 W. According to this figure, as the duty cycle (D) increases from 0.1 to 0.4, the efficiency of the converter also rises, with the highest efficiency achieved in the duty cycle range of 0.3 $< D <$ 0.4. Fig. 11(b) compares the efficiency of the proposed converter with that of converters [2], [6], [13], [18], [32], and [33] for an input voltage of 40 V and an output power of 400 W, considering similar parasitic elements as specified in Table II. This figure shows that the proposed converter offers higher

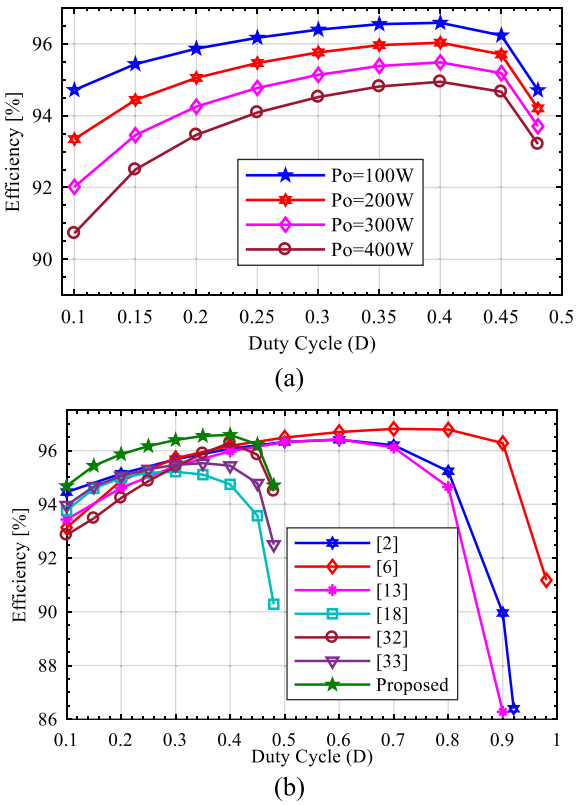


Fig. 11. Efficiency in different conditions. (a) Efficiency of the proposed converter at different powers. (b) Comparison of the efficiency of the proposed converter with similar converters in the power of 100 W.

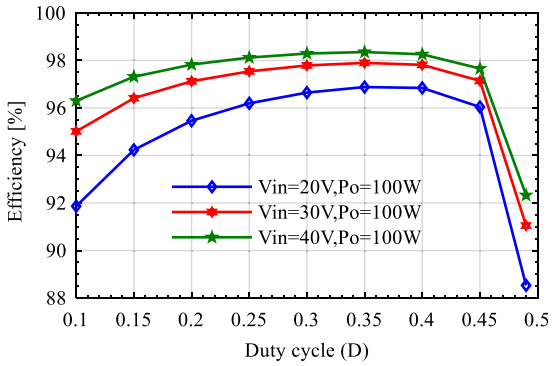


Fig. 12. Efficiency of the proposed converter with parasitic elements of the converter [1].

efficiency compared to similar structures at low duty cycles of the switch.

In the laboratory construction of the proposed converter, active and passive devices with relatively high parasitic resistance have been used, which has led to a relative decrease in the efficiency of the laboratory sample. Fig. 12 shows the efficiency of the proposed converter using reference parasitic parameters [1] for different values of input voltage (V_{in}) at an output power (P_{o}) of 100 W. As V_{in} increases, the efficiency of the converter also rises, exceeding 98% at a voltage of 40 V, which indicates the high efficiency of the proposed converter.

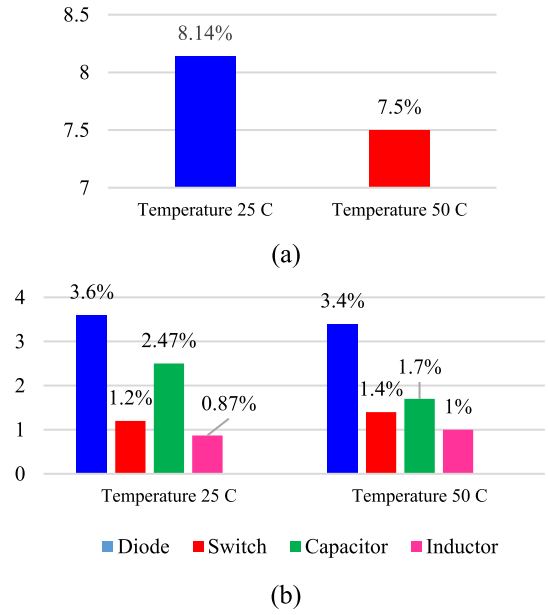


Fig. 13: Losses of active and passive components at 25 and 50 °C for an output power of 400 W. (a) Total losses. (b) Losses of each active and passive component.

E. Power Loss Analysis With Increasing Temperature

In the process of analyzing power losses with increasing temperature, parasitic values were taken based on the components used in the laboratory circuit. According to the datasheet of the switch, as the temperature rises, the switch equivalent series resistance ($R_{\text{DS(on)}}$) increases, leading to higher conduction losses at elevated temperatures. Similarly, datasheet information for the diode indicates that with increasing temperature, the diode's series resistance (r_D) and forward bias voltage (V_F) decrease. This reduction improves conduction conditions, thereby reducing diode power losses at higher temperatures. For electrolytic capacitors, increasing temperature lowers the viscosity of the electrolyte, reducing the equivalent series resistance (ESR) of the capacitor. However, excessive temperature rise can lead to capacitor failure. In contrast, film capacitors exhibit greater thermal stability, and their ESR shows minimal change with temperature increase. As temperature rises, core copper losses also increase. Fig. 13 illustrates the active and passive device losses of the proposed circuit at 25 and 50 °C. Although the total power losses of the proposed converter at 50 °C are approximately 8% lower than those at 25 °C, excessive temperature can still cause failure of certain components. Therefore, it is essential to prevent excessive temperature rise in the circuit.

F. Power Density

To calculate the power density, the converter volume must first be determined, after which the rated output power is divided by this volume. Based on the data obtained from the datasheets of the active and passive components, the volume of each element has been calculated and summarized in Table IV. The power density (ρ) can be determined as the ratio of the rated output

TABLE IV
CALCULATING THE VOLUME OF PROPOSED CONVERTER

Components	Specification	Volume
Switches	Length:36.8 mm Width:15.87 mm Thickness:5.31 mm	$2 \times 3101.12 = 6202.24$ mm^3
Diodes	Length:16.40 mm Width:10.40 mm Thickness:4.60 mm	$6 \times 784.5 = 4707$ mm^3
Capacitors	C_1 Diameter:16 mm C_1 Height:32 mm C_2 Diameter:13 C_2 Height:25 C_3 Diameter:16 C_3 Height:25 C_4 Length:31 mm C_4 Width = 15 mm C_4 Height:25 C_5 Diameter:13 C_5 Height:20	(6430.72) + (3316.6) + (5024) (11625) + (2653.3) = 29152.48 mm^3
Inductor	EE42/15/20 core	23000 mm^3
	Total volume:	63.06 cm^3

power to the total volume of the proposed converter, expressed as follows:

$$\rho = \frac{P_{\text{out}}}{V_e} \tag{75}$$

where P_{out} represents the output power and V_e denotes the total volume of the converter. Using (75) together with the data in Table III, the power density of the proposed converter is calculated as follows:

$$\rho = \frac{400}{63.06} \text{W/cm}^3 \tag{76}$$

VI. INDUCTOR AND CAPACITOR DESIGN

In general, the design of inductor and capacitor parameters depends on the voltage and current passing through them. The inductor current ripple and capacitor voltage ripple significantly affect converter performance. Therefore, the inductors and capacitors of the converter are designed while considering these ripples.

A. Inductor Design

The relationship between the current and voltage of the inductor is as follows:

$$V_L = L\frac{\Delta i_L}{\Delta t} \tag{77}$$

where V_L is the voltage across the inductor during the switch-ON period, $\Delta t = DT_s$ is the duration of the switch-ON, and $f_s = 1/T_s$ is the switching frequency, also, Δi_L is the permissible ripple of the current passing through the inductor in the time interval Δt and Δi_L is defined as the percentage of allowed ripple ($X_L\%$) as follows:

$$\Delta i_L = I_L X_L\%. \tag{78}$$

Using the (78), the value of the inductor considering the input current ripple is obtained as follows:

$$L = \frac{V_L D}{\Delta i_L f_s}. \tag{79}$$

1) Inductor Core Design: One of the most critical steps in designing an inductor core is selecting an appropriate magnetic material. Among available options, iron powder cores are considered ideal for high-current applications due to their softer magnetic characteristics and high saturation resistance. These cores, with a uniformly distributed magnetic gap in their structure, can store greater amounts of energy and are particularly suitable for high-power inductors, especially in dc–dc converters. For the design of the inductor, the following specifications were considered:

1) inductance: 280 μH;
2) current rating: ($I_{\text{DC}} = 10$ A);
3) ripple current: ($\Delta I = 2$ A);
4) switching frequency: (50 kHz);
5) calculation of peak current: ($I_{\text{peak}} = I_{\text{DC}} + \frac{\Delta I}{2}$); and
6) calculation of the number of turns: $N = \sqrt{\frac{L \times l_e}{\mu_0 \times \mu_r A_e}}$

where l_e is the effective magnetic length of the core and A_e is the effective cross-sectional area of the core.

For high-frequency applications, iron powder cores are suitable. An iron powder core with a permeability of $\mu_r = 60$ was selected for the proposed converter. An EE42 core was used for the proposed converter, and to ensure that core saturation does not occur, the saturation calculations were performed as follows:

First, the number of turns is calculated:

$$N = \sqrt{\frac{280 \times 10^{-6} \times 0.0978}{4\pi \times 10^7 \times 60 \times 2.35 \times 10^{-4}}} = 39. \tag{80}$$

For iron powder cores, the maximum allowable flux density is $B_{\max} = 0.7$ T. The peak flux density (B_{peak}) is calculated using the following relation:

$$B_{\text{peak}} = \frac{L \times I_{\text{peak}}}{N \times A_e} = \frac{280 \times 10^{-6} \times 11}{39 \times 2.35 \times 10^{-4}} = 0.33T < 0.7T. \tag{81}$$

The calculated peak flux density indicates that the designed inductor operates well below the saturation region, and the probability of core saturation is very low.

B. Capacitor Design

The relationship between the current and voltage of the Capacitor is as follows:

$$i_C = C\frac{\Delta V_C}{\Delta t} \tag{82}$$

where i_C is the current across the capacitor during the switch-ON period, $\Delta t = DT_s$ is the duration of the switch-ON, and $f_s = 1/T_s$ is the switching frequency, also, ΔV_C is the permissible ripple of the voltage passing through the capacitor in the time interval

Δt. ΔV_C is defined as the percentage of allowed ripple ($X_C\%$) as follows:

$$\Delta V_C = V_C X_C\%. \tag{83}$$

Using the (83), the capacitance of the capacitor is obtained by considering the voltage ripple of the capacitor as follows:

$$C = \frac{i_C D}{\Delta V_C f_s}. \tag{84}$$

C. Comparison of Inductor and Capacitor Values

Table V shows the exact comparison of inductors and capacitors in terms of inductor current ripple, capacitor voltage ripple, and the same gain factor. Considering that the gain factor of the converters is different, the duty cycle (D) will be different to achieve a specific gain factor (G). Two parameters $K_L = V_{\text{in}}/f_s \bar{i}_{\text{in}} X_L\%$ and $K_C = \bar{i}_{\text{in}}/f_s V_{\text{in}} X_C\%$ are defined to simplify the values of inductors and capacitors. V_{in} is the value of the input voltage, $\bar{i}_{\text{in}}$ is the average input current, and f_s is the switching frequency. According to Table V, at the same voltage gain, the size of the inductor and capacitors of the proposed converter is smaller compared to the converters [2], [6], [13], [18], and [32], so the proposed converter will have a lower volume and price.

Considering the similarity in the number of components and the ideal voltage gain between the proposed converter and the reference converter [33], A summary of the various comparisons conducted between the two converters is consolidated here. Despite the similarity in active and passive elements and the ideal voltage gain, the actual voltage gain of the proposed converter is higher than that of converter [33]. Moreover, the switch voltage stress in the proposed converter is lower, and its efficiency is noticeably higher compared to converter [33]. These comparisons are illustrated in Figs. 8, 5, and 11(b), respectively. Furthermore, based on the results provided in Table IV, the total component cost of the proposed converter is lower than that of converter [33]. In summary, the higher actual voltage gain, better efficiency, lower voltage stress on some components, and lower overall cost demonstrate the technical and economic superiority of the proposed structure over converter [33].

VII. Laboratory Results

To confirm the theoretical (mathematical) analysis of the proposed converter in a nonideal state and to demonstrate its performance under practical conditions, a test sample was constructed in the power range of 400 W, as shown in Table VI and Fig. 14.

The input and output voltage waveforms are shown in Fig. 15(a), measuring 40 and 372 V, respectively. With a duty cycle of 0.3 and an input voltage of 40 V, the experimental value of the voltage gain factor is approximately 9.3, which aligns with the voltage boosting factor of the proposed converter in real conditions, as per (28). The output voltage and current are shown in Fig. 15(b), measuring 372 V and 10.72 A, respectively. According to (7), the output voltage under ideal conditions is equal to 400 V for an input voltage of 40 V and a duty cycle of 0.3. Due to the parasitic values, a drop of about 9.3% in the output voltage was observed.

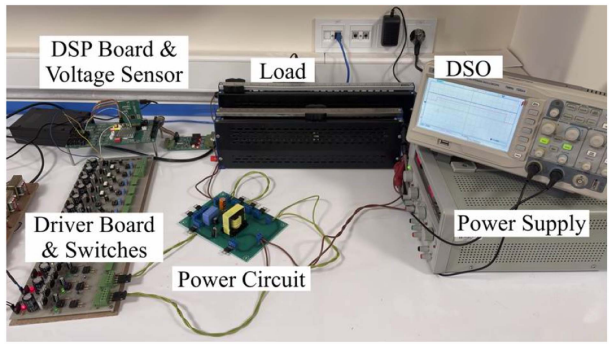
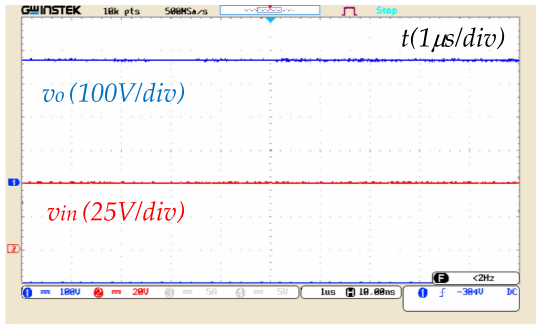
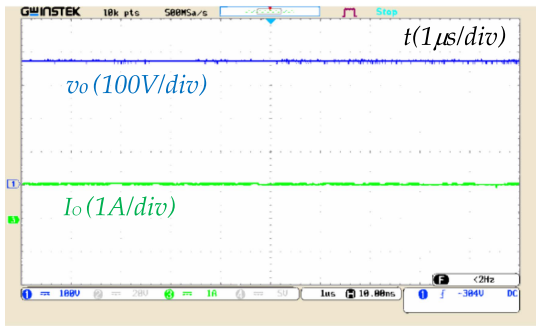


Fig. 14. Laboratory image of the proposed converter.



(a)



(b)

Fig. 15. Laboratory results of the proposed converter. (a) Input and output voltage. (b) Output voltage and current.

The input current waveform of the proposed converter, along with the power switch pulse command, is shown in Fig. 16. According to this figure, when the power switch is turned ON, the current through the inductor increases as it charges and stores energy. When the switch is turned OFF, the inductor discharges its current, releasing the stored energy. The continuous current of the converter's inductor, which is the same as the input current of the converter, confirms its suitability for renewable energy sources such as solar arrays. The figure also indicates that the inductor current ripple is less than 20%, demonstrating good agreement between the experimental results and the simulation.

The voltage waveform across diodes D_3 and D_4 and capacitor C_2 is shown in Fig. 17(a). According to this figure, when the switch is turned on, diode D_3 is forward biased while diode D_4

TABLE V
COMPARISON OF INDUCTOR AND CAPACITOR OF THE PROPOSED CONVERTER AND COMPARATIVE CONVERTERS

	Converter of reference [2]	Converter of reference [6]	Converter of reference [13]	Converter of reference [18]	Converter of reference [32]	Converter of reference [33]	Proposed converter
Inductors	$L_1 = K_L D$ $L_2 = K_L \frac{D}{(1-D)}$ $L_3 = K_L \frac{D(1+D)}{(1-D)^3}$	$L_1 = L_2 = K_L 2D$	$L_1 = K_L D$ $L_2 = L_3 = L_4 = K_L \frac{(1+2D-2D^2)}{(1-D)^2}$	$L_1 = K_L \frac{D(3-D)(1-D)^2}{(D^2-2D+2)(1-2D)}$ $L_2 = K_L \frac{D(3-D)(1-D)^2}{(1-2D)^2}$ $L_3 = K_L \frac{D(3-D)(1-D)}{(2+D)(1-2D)}$	$L_1 = L_2 = K_L \frac{D(1-D)}{1-2D}$ $L_3 = K_L \frac{D(1-D)(2+D)}{(1-2D)^2}$	$L = K_L \frac{2D(1-D)}{1-2D}$	$L = K_L \frac{2D(1-D)}{1-2D}$
Capacitors	$C_1 = K_C D(1-D)$ $C_2 = K_C \frac{(1-D)^4}{(1+D)}$ $C_3 = K_C \frac{D(1-D)^4}{(1+D)}$ $C_4 = K_C \frac{D(1-D)^4}{(1+D)(3D-D^2)}$	$C_1 = C_2 = K_C \frac{(1-D)^2}{8}$ $C_B = K_C \frac{(1-D)}{2}$ $C_o = K_C \frac{(1-D)^3}{16}$	$C_1 = K_C \frac{D(1-D)^2}{(1+2D-2D^2)}$ $C_2 = K_C \frac{2D(1-D)^4}{(1+2D-2D^2)}$ $C_3 = K_C \frac{2D(1-D)^4}{(1+2D-2D^2)(2D-D^2)}$ $C_4 = C_5 = K_C \frac{(1-D)^3}{(1+2D-2D^2)}$ $C_6 = K_C \frac{D(1-D)^4}{(1+2D-2D^2)^2}$	$C_1 = K_C \frac{(-D^2+D+1)(1-2D)}{(1-D)(3-D)}$ $C_2 = K_C (1-2D)$ $C_3 = K_C \frac{(1-D)(1-2D)}{2(3-D)}$ $C_4 = K_C \frac{(1-2D)^2}{(3-D)(1+D)}$	$C_1 = K_C \frac{D(1-2D)}{(1-D)}$ $C_2 = K_C (1-2D)$ $C_3 = K_C \frac{(1+D)(1-2D)^2}{(2+D)}$ $C_4 = K_C \frac{(1-2D)^2}{(2+D)}$ $C_5 = K_C \frac{(1-2D)^2}{D(2+D)}$ $C_6 = K_C \frac{(1-2D)^2}{2D(2+D)}$ $C_o = K_C (1-D) \times \left(\frac{(1-2D)}{(2+D)}\right)^2$	$C_1 = K_C \frac{(1-2D)^2}{2}$ $C_2 = K_C \frac{(1-2D)}{2}$ $C_3 = K_C \frac{(1-2D)^2}{8}$ $C_4 = K_C \frac{D(1-2D)^2}{8}$ $C_5 = K_C \frac{(1+D)(1-2D)^2}{8}$	$C_1 = K_C \frac{(1-2D)}{2}$ $C_2 = K_C \frac{(1-2D)^2}{4}$ $C_3 = K_C \frac{(1-2D)^2}{12}$ $C_4 = K_C \frac{D(1-2D)^2}{8}$ $C_5 = K_C \frac{(1+D)(1-2D)^2}{8}$
Switching interval Duty Ratio, D	0.5	0.34	0.5	0.273	0.3078	0.1667	0.1667
Voltage gain, G	6	6	6	6	6	6	6
Inductor value	$L_1 = 0.2mH$ $L_2 = 0.4mH$ $L_3 = 2.4mH$	$L_1 = L_2 = 0.272mH$	$L_1 = 0.2mH$ $L_2 = L_3 = L_4 = 2.4mH$	$L_1 = 0.227mH$ $L_2 = 0.743mH$ $L_2 = 0.209mH$	$L_1 = L_2 = 0.221mH$ $L_3 = 1.33mH$	$L = 0.167mH$	$L = 0.167mH$
Capacitor value	$C_1 = 125\mu F$ $C_2 = 21\mu F$ $C_3 = 10.5\mu F$ $C_o = 8.34\mu F$	$C_1 = C_2 = 27.3\mu F$ $C_2 = 165\mu F$ $C_o = 8.95\mu F$	$C_1 = 42\mu F$ $C_2 = 21\mu F$ $C_3 = 28\mu F$ $C_4 = C_5 = 42\mu F$ $C_6 = 6.94\mu F$	$C_1 = 137.3\mu F$ $C_2 = 227\mu F$ $C_3 = 30.3\mu F$ $C_4 = 29.7\mu F$	$C_1 = 85\mu F$ $C_2 = 192.2\mu F$ $C_3 = 41\mu F$ $C_4 = 32\mu F$ $C_5 = 104\mu F$ $C_6 = 52\mu F$ $C_o = 9.6\mu F$	$C_1 = 111\mu F$ $C_2 = 167\mu F$ $C_3 = 27\mu F$ $C_4 = 4.6\mu F$ $C_5 = 32\mu F$	$C_1 = 167\mu F$ $C_2 = 55\mu F$ $C_3 = 18\mu F$ $C_4 = 4.6\mu F$ $C_5 = 32\mu F$

TABLE VI
VALUE OF THE PARAMETERS OF THE PROPOSED CONVERTER

Parameters	Value
Input voltage	40 V
Inductor	$L = 280$ mH , $r_L = 0.03\ \Omega$, $N = 39$turn EE42, $L_e = 97.8$ mm, $A_e = 235$ mm^2, $u_r = 60$
Capacitors	C_1: Rubycon, 220 μf, ESR = 0.07 Ω C_2: Rubycon, 68 μf, ESR = 0.12 Ω C_3: Panasonic, 47 μf, ESR = 0.1 Ω C_4: film, 5.6 μf, ESR = 5.6 mΩ C_5: Panasonic, 33 μf, ESR = 0.06 Ω
Switching frequency(f_s)	50 kHz
Duty cycle (D)	0.3
Diode (D_1,D_2,D_3,D_4,D_5,D_6,D_7) (STTH2002C)	$R_D = 0.02\ \Omega$ $V_F = 0.73$ V $t_{rr} = 22$ns
Power switch (S_1, S_2) (IRFP150NPbF)	$R_{DS(on)} = 0.04\ \Omega$ $t_{on} = 11$ns, $t_{off} = 45$ ns
Gate drive	ICL7667 Optocoupler 6N137
Controller	DSP(TMSF28335)
Load	348 Ω

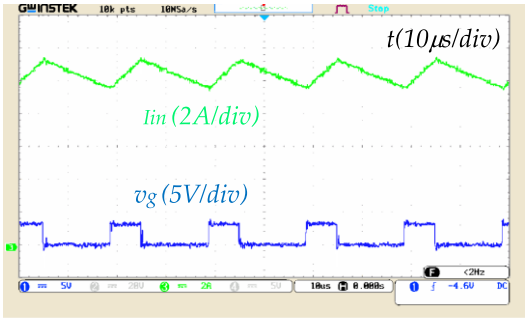
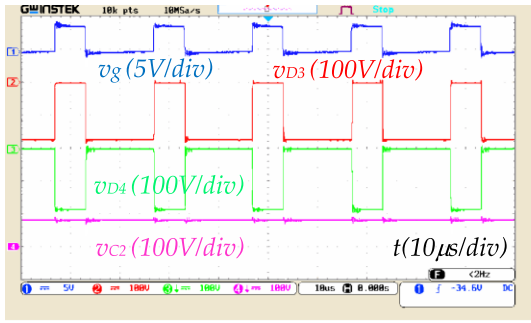
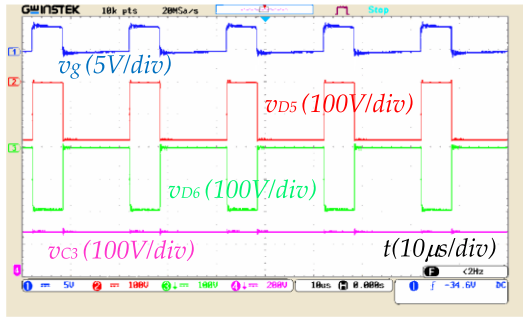


Fig. 16. Laboratory results of the proposed converter; Input current of the proposed converter.



(a)



(b)

Fig. 17. Experimental results of voltage of the diodes and capacitors of the proposed converter. (a) Voltage across D3, D4, C2. (b) Voltage across D5, D6, C3.

is reverse biased. The voltage across both diodes is 187 V, and the voltage of capacitor C_2 is 92 V. The voltage waveform of diodes D_5 and D_6 and capacitor C_3 is shown in Fig. 17(b). In this case, when the switch is turned on, diode D_5 is forward biased and diode D_6 is reverse biased; the voltage across both diodes remains 186.5 V, and the voltage of capacitor C_3 is 278 V.

According to relations (9) and (10), for the duty cycle 0.3, the voltage across diodes D_3, D_4, D_5, and D_6 should ideally be equal to 200 V. However, due to parasitic conditions, about a 9.34% drop in the voltage of these diodes is observed. Under ideal conditions, (6) indicates that the voltage of capacitor C_2 should be equal to 100 V and the voltage of capacitor C_3 should be equal to 300 V. Again, due to parasitic conditions, about a 9.3% drop in the voltage of these capacitors is observed. when the switch is turned on, diode D_2 is reverse biased, with the voltage across it measuring 94 V.

The voltage of switch S_1 is 96 V in the OFF state, while the voltage of capacitor C_1 is 95.5 V. The voltage waveform of diode D_1 and the voltage of switch S_2 are shown in Fig. 18. In this case, when the switch is turned ON, diode D_1 is also reverse biased, with a reverse voltage of 93.5 V across both ends of the diode, and the voltage of switch S_2 is 96 V in the OFF state. The voltage waveforms of capacitors C_4 and C_5 in relation to the switch function are shown in Fig. 18(c), where the voltage across both capacitors is 186 V. The waveforms presented in Fig. 18 indicate a good agreement between the simulation results under real conditions and the laboratory results. However, due to the parasitic values of the components used in the laboratory circuit, there is a noticeable difference between the ideal voltage calculated in the theory section and the actual voltages of the power switches, diodes, and capacitors. This difference could be reduced by using equipment with lower parasitic values.

The results of the dynamic response tests under variations in input voltage, load resistance, and reference voltage are shown in Fig. 19. Initially, the converter was started with an input voltage of 40 V, and by tuning the control parameters, a stable output voltage of 372 V was achieved across a 348 Ω load. When the input voltage drops from 40 to 25 V, the controller is able to maintain the output voltage steadily at 372 V, as illustrated in Fig. 19(a). Under conditions of 40 V input and 372 V output, the load resistance is then decreased. Despite the increase in load current, the controller maintains the output voltage at 372 V, demonstrating robust and stable performance. This behavior, indicative of the high capability of the control system to handle load variations, is shown in Fig. 19(b). Furthermore, the system's flexibility and tracking accuracy were evaluated by varying the

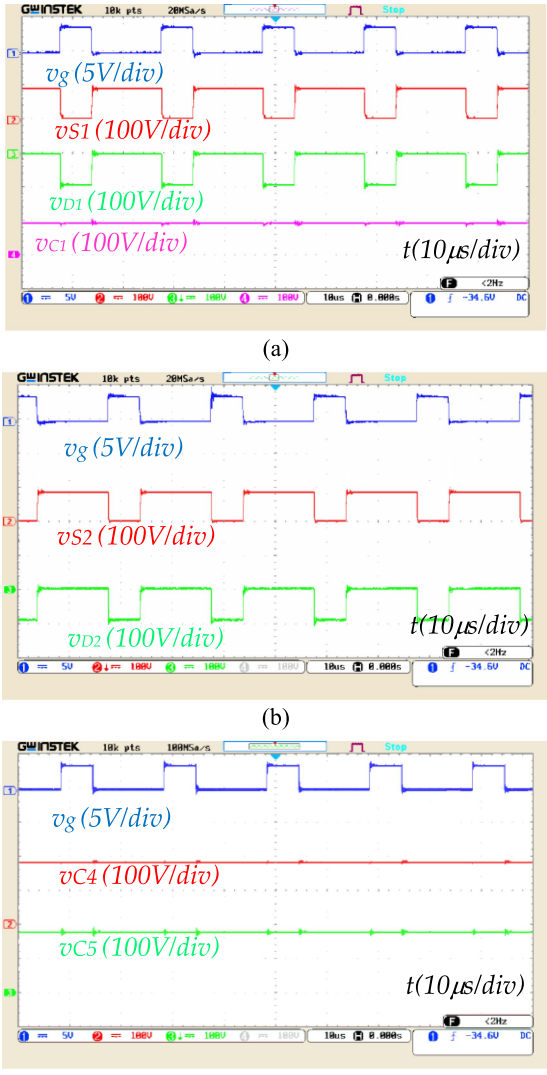


Fig. 18. Experimental results of the voltage of the switches, diodes, and capacitors of the proposed converter. (a) Voltage across S1, D1, C1. (b) Voltage across S2, D2. (c) Voltage across C4, C5.

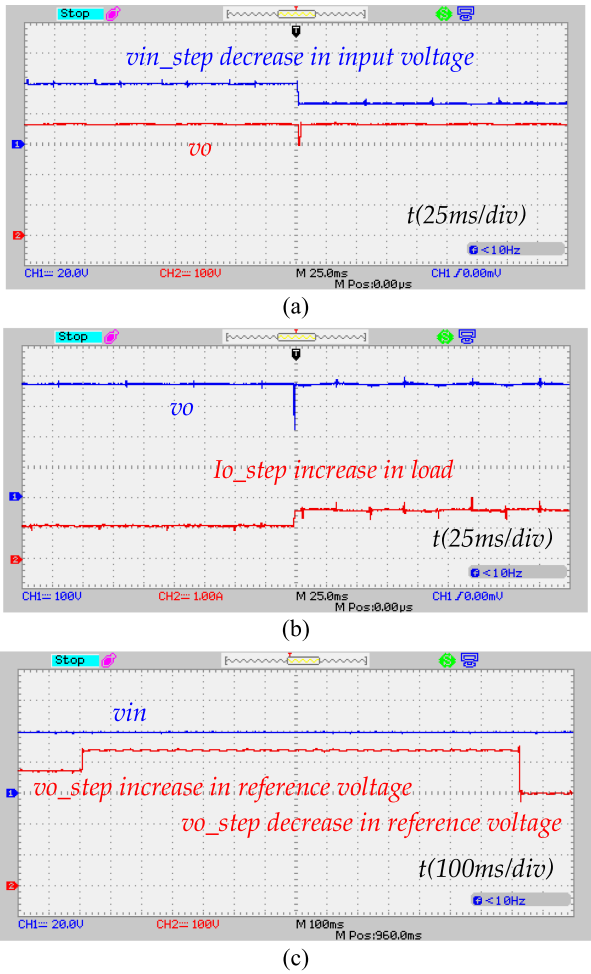


Fig. 19: Dynamic response of the proposed converter. (a) Step decrease in input voltage. (b) Step increase in load current. (c) Step increase and decrease in reference voltage.

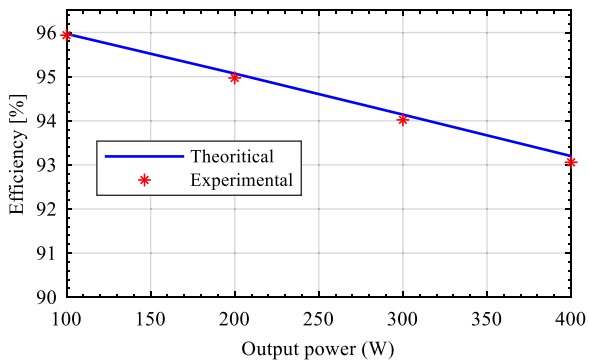


Fig. 20. Efficiency versus output power in theoretical as well as experimental setup.

reference voltage, as presented in Fig. 19(c). The reference voltage, initially set at 372 V, was increased to 440 V after a specific time interval. Under this new condition, the control system accurately maintained the output voltage at 440 V, demonstrating its ability to track reference changes effectively. Subsequently, when the reference voltage was reduced to 300 V, the system responded promptly and precisely, adjusting the output voltage to the desired level. It should be noted that during these tests, the input voltage was kept constant to create controlled conditions. The results confirm the reliable and accurate performance of the proposed converter and its control system in response to changes in the reference voltage.

Fig. 20 illustrates both the theoretical and experimental efficiency of the proposed converter as a function of output power. As shown, the theoretical calculations exhibit good agreement with the experimental data. This close correspondence is attributed to the careful determination of the parasitic parameters in the model. During the modeling process, the parasitic values of the active and passive components were selected based on realistic conditions and the actual characteristics of the circuit elements in the laboratory environment. This approach enabled the theoretical analysis to accurately predict the real behavior of the converter.

TABLE VII
VALUE OF THE PARAMETERS FOR 1 KW PROTOTYPE OF THE PROPOSED CONVERTER

Parameters	Value
Input voltage	50 V
Inductor	$L = 380$ mH , $r_L = 0.04\ \Omega$, $N = 15$turn EE55, $L_e = 124$ mm, $A_e = 282$ mm^2, $u_r = 60$
Capacitors	C_1: Rubycon, 150 μf, ESR = 0.14 Ω C_2: Rubycon, 33 μf, ESR = 0.7 Ω C_3: film, 8 μf, ESR = 4.4 mΩ C_4: film, 4.7 μf, ESR = 6.6 mΩ C_5: Rubycon, 22 μf, ESR = 1 Ω
Switching frequency(f_s)	50 kHz
Duty cycle (D)	0.35
Diode (D_1,D_2,D_3,D_4,D_5,D_6,D_7) (STTH3003CW)	$R_D = 0.017\ \Omega$ $V_F = 0.75$ V $t_{rr} = 30$ ns
Power switch (S_1,S_2) (IRFP260NPbF)	$R_{DS(on)} = 0.04\ \Omega$ $t_{on} = 17$ ns $t_{off} = 55$ ns
Gate drive	ICL7667 Optocoupler 6N137
Controller	DSP(TMSF28335)
Load	363 Ω

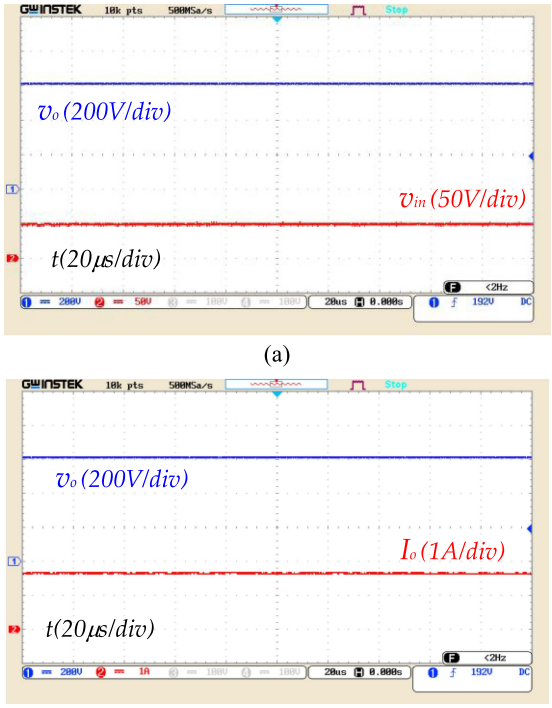


Fig. 21. Laboratory results of the proposed converter at 1 kW prototype. (a) Input and output voltage. (b) Output voltage and current.

To evaluate the capability of the proposed converter for higher-power applications, a 1 kW prototype of the converter was designed and tested. For this purpose, an input voltage of 50 V and a duty cycle of $D = 0.35$ were selected, and the tests were carried out based on the parameters listed in Table VII.

Fig. 21(a) shows the input and output voltage waveforms, measured at 50 and 614 V, respectively. Fig. 21(b) presents the

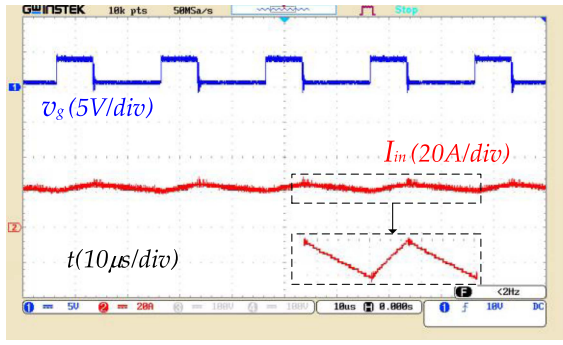


Fig. 22. Laboratory results of input current at 1 kW prototype.

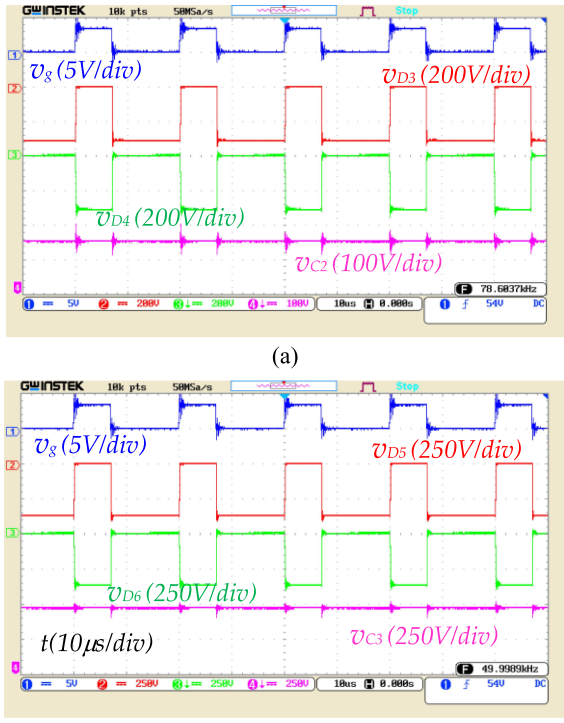


Fig. 23. Experimental results of voltage of the diodes and capacitors at 1 kW prototype. (a) Voltage across D3, D4, C2. (b) Voltage across D5, D6, C3.

output voltage and output current waveforms of the converter, measured at 614 Vand 1.69 A, respectively. The experimental voltage gain under these conditions, with a duty cycle of $D = 0.35$, was approximately 12.28, which is in good agreement with the voltage gain of the proposed converter under practical conditions, calculated according to (28). Furthermore, based on (5), the ideal output voltage for an input of 50 V and duty cycle $D = 0.35$ is 666 V. The observed discrepancy of about 8% in the experimental output voltage is attributed to parasitic effects in the circuit.

In Fig. 22, the waveform of the inductor current (L_1) along with the power switch pulse signal is shown. The inductor current (i_{L1}), which also serves as the input current (i_{in}) of the converter, is continuous and exhibits a limited ripple of less than 20%. In Fig. 23, the voltage stress on diodes (D_3, D_4, D_5, and

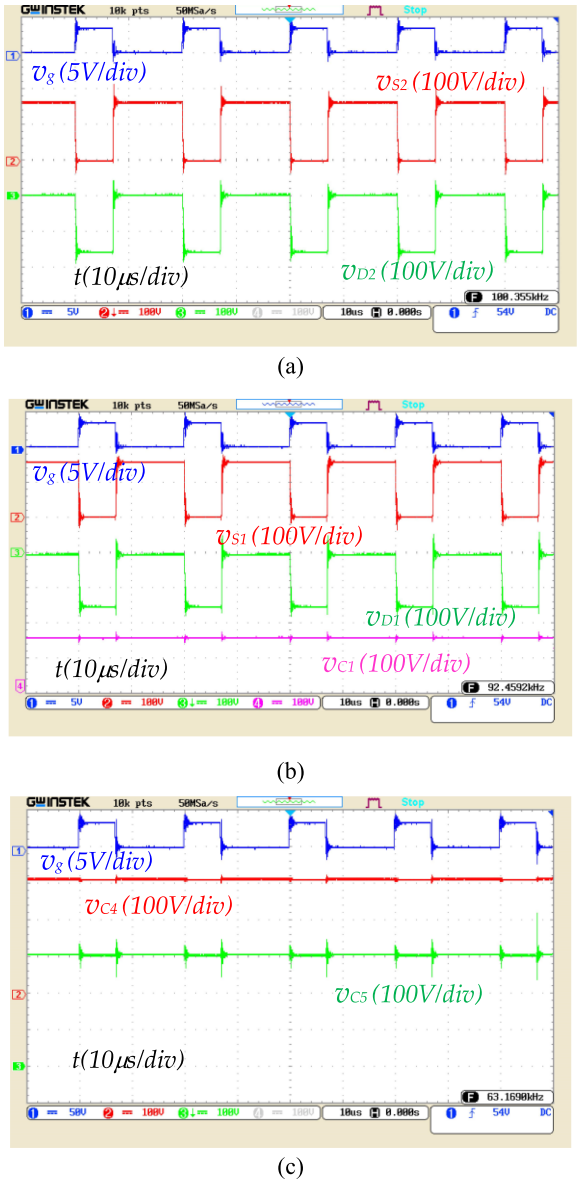


Fig. 24. Experimental results of the voltage of the switches, diodes, and capacitors at 1 kW prototype. (a) Voltage across S2, D2. (b) Voltage across S1, D1, C1. (c) Voltage across C4, C5.

D_6) along with the voltage stress on capacitors (C_2 and C_3) is presented. The voltage stress across diodes D_3 and D_4 is half of the output voltage, measured at 306.5 V, while the voltage across capacitor C_2 is 152 V. Similarly, the voltage stress across diodes D_5 and D_6 is 306.5 V, and the voltage across capacitor C_3 is 458 V.

In Fig. 24, the voltage stress across diodes (D_1 and D_2), switches (S_1 and S_2), as well as capacitors (C_1, C_4, and C_5), along with the power switch pulse signals, are shown. The measured voltage stress values are as follows: diode D_2 and switch $\mathbf{S_2}$ at 154. and 158.5 V, respectively; diode D_1 and switch S_1 at 153. and 158.5 V, respectively; capacitor C_1 at 156.5 V, and capacitors C_4 and C_5 at 307 V. By comparing the measured values of switch and diode voltage stress and capacitor voltages with the ideal theoretical values, it can be observed that, due to parasitic effects, the measured values are approximately 4.9–8% lower than the theoretical predictions under ideal conditions. These results indicate that the proposed converter not only performs well at a 400 W output but also maintains appropriate operational characteristics at higher power levels, making it suitable for higher power applications.

VIII. Conclusion

In this research, a nonisolated high-voltage-gain converter based on a switched boost impedance source network and a switched ladder capacitor was proposed. Analytical expressions for the voltage stress across active and passive elements, as well as the converter's voltage gain function, were derived. For comparison, both ideal and practical voltage gain curves as a function of the switching duty cycle were plotted for the proposed converter and reference topologies. The results demonstrated that the actual voltage gain of the proposed converter exceeds that of the reference converters, while the switch voltage stress is significantly lower. The proposed topology, featuring continuous input current, high voltage gain, common-ground configuration, and low voltage stress across active and passive devices, is particularly suitable for photovoltaic systems. The continuous input current not only improves the efficiency of the photovoltaic array but also mitigates its degradation rate, thereby extending its service lifetime but also enables more precise and stable MPPT algorithm design. Although the use of additional diodes in most converters increases circuit size and losses, the proposed topology mitigates these limitations through appropriate low-voltage stress distribution across the diodes. Due to the use of active devices with relatively high ON-state resistance, the efficiency of the proposed converter is slightly reduced. Therefore, employing advanced semiconductors such as SiC and gallium nitride, which offer high switching frequency, low ON-state resistance, and optimal performance at elevated voltages and temperatures, can significantly reduce switching losses.

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