Dual-Mode Operation of Quasi-Square-Wave Modulated DC–DC Converter for Enhanced Efficiency Across a Wide Operating Range

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***Abstract*—Extending the use of dc–dc converters, such as the dual active bridge (DAB) to high voltage applications, will require voltage sharing among series-connected power devices. Initial solutions used snubber capacitors to limit voltage rise and balance the turn-OFF voltage. However, this mechanism is not viable at low currents, which leads to high capacitor discharge currents. The quasi-square-wave modular multilevel dc–dc converter (QSW-MMC) has been proposed as an option for high voltage DAB converters. This circuit employs an additional switch in series with the capacitor, which acts as a controlled voltage clamp. This avoids problems at low loading but loses the benefit of switching loss reduction at high currents. In this article, a dual-mode operation based on the QSW-MMC is proposed, which actively controls the auxiliary switch to use the submodule capacitor as a clamping component at low currents and as a snubber component at high currents. In addition, the presented control strategy can achieve smooth transitions between two modes. Finally, simulation and experimental results from a scaled test rig validate the efficiency improvement achieved by the proposed dual-mode operation.**

***Index Terms*—DC transformer, dc–dc power conversion, dual-active bridge (DAB), modular multilevel converter (MMC), zero-voltage switching (ZVS).**

I. Introduction

Medium-voltage dc (MVdc) power networks are increasingly being adopted as alternatives to conventional ac systems with the growing integration of renewable energy sources. This trend is driven by the advantages of MVdc systems, which includes higher efficiency and reliability, reduced size, improved controllability, and lower overall cost [1], [2], [3], [4]. A key enabler for integrated dc networks is the ability to transform voltage and current levels in a manner similar to that of conventional ac power networks. This functionality can be readily achieved in lower power systems, such as data centers and automotive platforms, which operate at voltage levels compatible with well-established dc–dc converter technologies [5], [6], [7], [8], [9]. In high-power applications with conversion from MVdc to high-voltage dc (HVdc) levels, high-gain dc–dc converters also offer a more compact and cost-effective solution compared to original ac systems, making them a promising alternative for future high-power applications, such as offshore wind farms [10], [11], [12].

Several key requirements exist for high gain dc–dc converters, which include high power, galvanic isolation, bidirectional power transfer, and a high step-up ratio. A range of solutions has been proposed, among which dual-active-bridge (DAB) dc–dc converters serve as a core converter unit [12]. DAB converters can be implemented using various connection strategies, for example, the input-parallel output-series (IPOS) configurations, as shown in Fig. 1(a) [13], [14], [15]. Nevertheless, the straightforward setup of DAB arrays requires the distributed transformers to block the system's maximum voltage, which leads to a complex transformer core design under MV [16]. In addition, the high voltage and power levels require the DAB converter unit capable of operating beyond the voltage rating of single power semiconductor devices.

An early solution employed the series connection of power switches, such as insulated gate bipolar transistors (IGBTs). This approach has been proven viable, which uses a reduced number of passive components and simplified circuit structures. However, achieving proper voltage sharing among series-connected power switches remains concerned [17], [18]. To address this issue, two main approaches have been proposed: active gate drive techniques and passive snubber circuits. Dedicated active gate drives control the switching speed of each power switch by regulating the gate voltage [17], [19], [20], [21]. However, this implementation requires high bandwidth current and voltage feedback to realize the synchronization among power switches, which increase the circuit complexity and cost.

Passive snubber circuits utilize a simple, component-based topology connected in parallel with power switches to slow down the switching transients. A common configuration consists of a resistor, capacitor, and diode, forming a reliable and widely adopted snubber circuit [16], [22], [23], [24], [25]. In DAB converters, soft turn-ON is typically achieved, as the snubber capacitor voltage reaches 0 V before the power switches are

Received 27 July 2025; revised 3 November 2025; accepted 10 December 2025. Date of publication 17 December 2025; date of current version 20 March 2026. This work was supported in part by the China Scholarships Council under Grant CSC202008510125 and in part by the Engineering and Physical Sciences Research Council under Wind2DC Grant EP/X035867/1. Recommended for publication by Associate Editor F. Dijkhuizen. *(Corresponding author: Peizhou Xia.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3645213.

Digital Object Identifier 10.1109/TPEL.2025.3645213

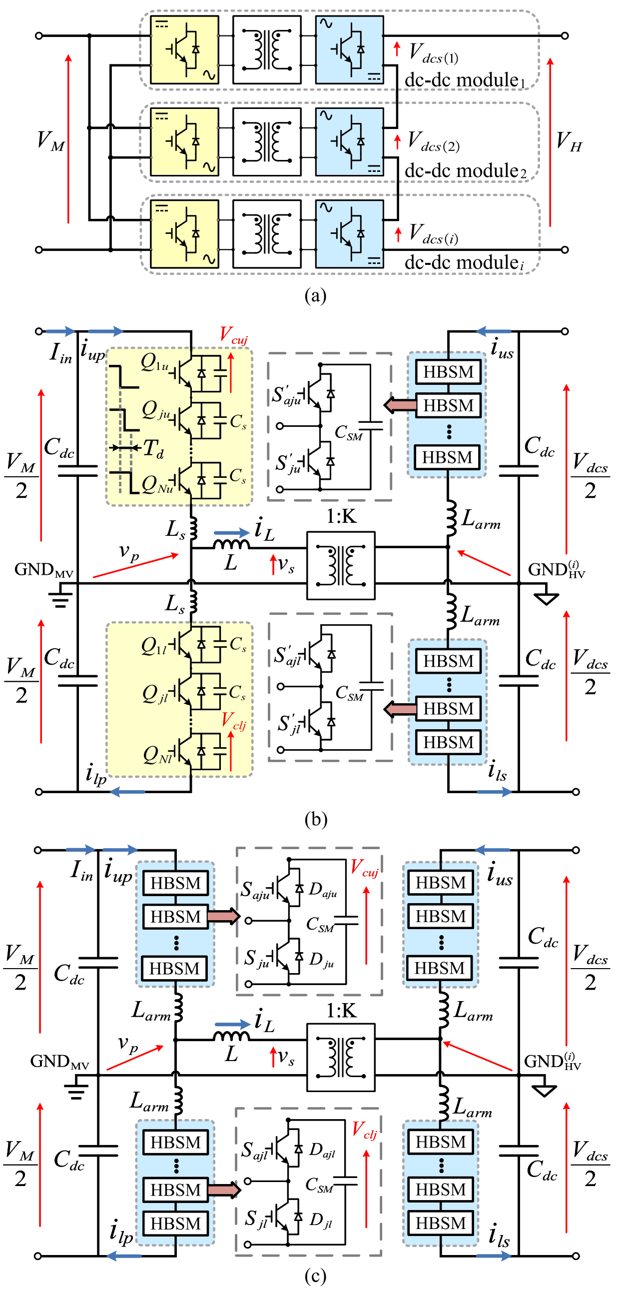

Fig. 1. Schematics of (a) IPOS based high-gain DC–DC converter. (b) DC–DC module with SCDCT topology. (c) DC–DC module with MMDCT topology.

turned ON [25]. As a result, the snubber resistor is not required to limit the inrush current and an individual snubber capacitor is sufficient. However, the energy stored in stray inductance can resonate with the snubber capacitor, resulting in switching-frequency related power losses [26].

Another drawback of passive snubber circuits is the increased power loss under light-load conditions, which is especially critical in applications with a high peak-to-average power ratio, such as wave energy systems [27]. In such cases, the snubber capacitor may not fully discharge during the dead-time interval and can experience a short-circuit at the turn-ON instant of the power switch, leading to excessive losses [16]. Therefore, the snubber capacitor must be carefully designed: a capacitance value that is too low may result in inadequate voltage sharing, while an excessively large value can cause substantial losses during low-current operation.

In addition to the series connection of power switches, numerous studies have explored the use of quasi-square-wave (QSW) modulated modular multilevel converters (MMCs), which extend conventional two-level DAB converters by incorporating trapezoidal transition edges. Unlike traditional MMC implementations, the submodule capacitors under QSW modulation conduct only at switching transients, during which they are dealing with voltage overshoot caused by the commutation of arm inductor current [28], [29], [30], [31]. Dwell transition times are typically on the order of microseconds, allowing for a significant reduction in submodule capacitance and consequently a decrease in overall capacitor volume. Similar strategies have been proposed in [26] and [32], commonly referred to as active clamping circuits. The integration of auxiliary switches within MMC submodules enables consistent clamping voltages across power switches, thereby alleviating voltage sharing challenges in series-connected configurations. Meanwhile, snubber-related losses at low-current levels are significantly reduced as the submodule capacitors remain charged.

Although the studies in [29] and [30] present a comprehensive analysis of submodule capacitance sizing to mitigate excessive voltage overshoot, high switching losses during turn-OFF events remain a significant concern. In [33] and [34], additional snubber capacitors are introduced for both the main and auxiliary power switches. However, this approach does not address snubber-related losses under low-current conditions. Furthermore, to recover the energy losses originating from the arm inductance, a low submodule capacitance is often desirable to generate high-frequency oscillations [30]. Nevertheless, this also leads to increased voltage overshoot at high-current levels. The reduced submodule capacitance, made feasible by QSW-modulated MMC operation, allows the submodule capacitors to function as snubber elements for series-connected power switches. This article also demonstrates that the auxiliary switch can be actively controlled to suppress the ringing during switching periods. In addition, given the variable load demands of dc–dc converter units, the required power transfer can be used to determine the appropriate operating mode of the QSW-modulated MMC stack.

In this article, a control methodology featuring dual-mode operation is proposed to control the auxiliary switch within the submodules. This determines whether the QSW-modulated MMC arm operates as a series-connected switch stack with complete zero-voltage switching (ZVS) under high-current conditions, or reverts to its original QSW-modulated mode under low-current operation to minimize snubber-related losses. The boundary transferred power between these two modes is investigated, which considers both the minimum load current required to fully achieve ZVS and the allowable voltage overshoot across the power switches.

The rest of this article is organized as follows. Section II reviews the operation of dc–dc modules based on series-connected power switches and QSW-modulated MMCs.

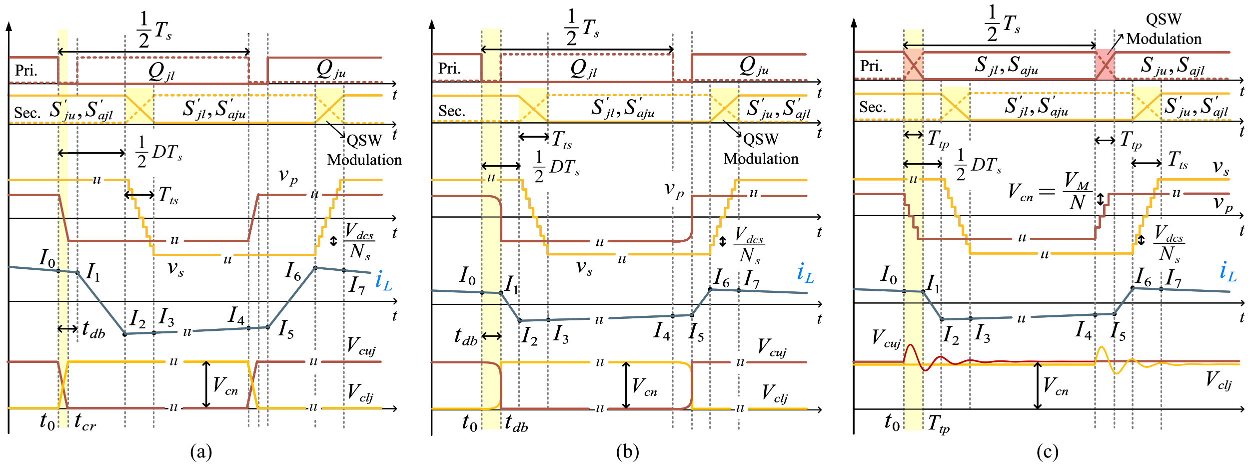

Fig. 2. Voltage and current waveforms of the SCDCT under (a) heavy load and (b) light load. (c) Voltage and current waveforms of the MMDCT under light load.

Section III analyzes the proposed dual-mode operation and the boundary conditions between the two modes. Section IV presents the practical implementation, including the design of a hybrid controller and the analysis of mode transitions. Sections V and VI provide simulation and scaled experimental results to validate the effectiveness of the dual-mode operation in QSW-modulated dc–dc converters, demonstrating their capability to improve conversion efficiency over a wide operating range. Finally, Section VII concludes this article.

II. Structure and Operating Principle of Analyzed High-Gain DC–DC Converter.

This section introduces the high-gain dc–dc converter based on two configurations, with an IPOS layout, as shown in Fig. 1, which enables current sharing on the MV side and voltage sharing on the HV side. For each dc–dc module, the individual power switch used in a conventional two-level DAB converter is replaced by an arm structure. This arm can be implemented using either series-connected power switches, as shown in Fig. 1(b), or MMC submodules, as depicted in Fig. 1(c).

Between the primary and secondary sides, a low-frequency or medium-frequency ac transformer is used to provide galvanic isolation and high-gain voltage conversion. This transformer can be modeled as a leakage inductance L in series with an ideal transformer.

A. Series-Connected Power Switches

In this article, the series-connected power switch configuration is referred to as the *series-connected dc transformer* (SCDCT). The power switches are denoted as Q_{1u} to Q_{Nu}, and Q_{1l} to Q_{Nl}, with subscripts u and l indicating the upper and lower arms, respectively. L_s represents the equivalent arm inductance, which is primarily attributed to the stray or parasitic inductance of the power modules and busbar connections. C_s denotes the snubber capacitor, which is implemented to enable ZVS and voltage sharing for power switches.

The operational modes of the proposed SCDCT are categorized into four distinct conditions based on the dead-band duration and the relationship between the switch voltages and currents: forward power flow under light load, forward power flow under heavy load, backward power flow under light load, and backward power flow under heavy load. Given the application of the discussed SCDCT, this article primarily focuses on forward power flow. The light-load and heavy-load conditions are analyzed, as illustrated in Fig. 2.

The heavy-load condition can be characterized by the fact that all power switches achieve ZVS. Q_{1u}–Q_{Nu} of the upper arm (represented by Q_{ju} in Fig. 2) are turned OFF at t_0, with snubber capacitors C_s slowly ramp to realize ZVS of turn-OFF switches. At t_{cr}, every snubber capacitors are charged to nominal voltage V_{cn}. $Q_{1l} - Q_{Nl}$ (represented by Q_{jl} in Fig. 2) will then be turned ON at t_1, after the dead-band time t_{db}. Due to the inductive loading, the turn-ON of $Q_{1l} - Q_{Nl}$ will see ZVS. Therefore, under heavy-load conditions, the switching losses from series-connection side are completely removed.

The voltage imbalance among power switches can be derived based on the maximum delay time between the turn-OFF events of the first and last power switches, denoted as T_d, and the load current at the switching instant, represented by I_0 for the upper arm of the primary bridge. Since T_d is short relative to the entire switching period, the arm current responsible for generating the voltage imbalance can be assumed to remain constant during this interval. Accordingly, the voltage imbalance ΔV can be expressed as

$$\Delta V = \frac{T_d I_0}{C_s} \tag{1}$$

Under light-load condition, as shown in Fig. 2(b), snubber capacitors C_s cannot be fully discharged during the dead-band time t_{db}. Therefore, at the turn-ON instant t_1 of $Q_{1l} - Q_{Nl}$, the output voltage v_p will drop abruptly to $-V_M/2$ and the snubber capacitors release the remaining stored energy, which causes significant losses. The maximum losses can be calculated as

$$P_{\text{snub}} = \frac{f_s}{N} C_s V_M^2. \tag{2}$$

where f_s is the switching frequency of the SCDCT.

B. QSW Modulated MMC

To mitigate the excessive losses encountered under low-current conditions in the SCDCT, the QSW-modulated MMC stack, as depicted in Fig. 1(c), can be adopted as an active clamping circuit. This configuration is referred to as the *modular multilevel dc transformer* (MMDCT).

To ensure a consistent comparison between the SCDCT and MMDCT, both topologies employ a QSW-modulated MMC stack on the low-current secondary side, so the loss analysis can be concentrated on the high-current primary side of two topologies. The voltage change under QSW modulation at each level is limited to the nominal voltage of a half-bridge submodule (HBSM), denoted as V_{cn}. This voltage is ideally equal to V_M/N on the primary side and $V_{\text{dc}}s/N_s$ on the secondary side. The parameters T_w and T_{ws} define the dwell time for each intermediate voltage level in the two bridges, enabling precise control of the output voltage's dv/dt.

The series arm inductance, L_{arm}, helps limit the inrush arm current and protects the converter components. Each HBSM consists of two semiconductor devices, S_{ju} and S_{aju}, along with their antiparallel diodes, D_{ju} and D_{aju}. As for the lower arm, the switches are denoted as S_{jl} and S_{ajl}. S_{ju} and S_{jl} are positioned in the main power path, while S_{aju} and S_{ajl}, together with the HBSM capacitor C_{SM}, are connected in an auxiliary path to provide the clamping voltage V_{cuj} and V_{clj}, where u and l denote the upper and lower arm, respectively.

During the transitions T_{tp}, T_{ts} defined in (3), the SMs will be switched ON in sequence according to their voltage sorting

$$T_{tp} = (N-1)\,T_w \tag{3a}$$

$$T_{ts} = (N_s-1)\,T_{ws}. \tag{3b}$$

C. Current and Power Derivation of DC–DC Module

The authors in [28], [30] and [33] provided a comprehensive analysis of the inductor current profile of a DAB converter employing QSW-modulated MMC stacks. The arm current observed in the upper arm of the MV side at the inserted switching instant is denoted as I_0, which can be derived as

$$I_0 = \frac{KV_M + 2DV_{\text{dcs}-V_{\text{dcs}}}}{8KLf_s} - \frac{KV_M T_{tp} - V_{\text{dcs}T_{ts}}}{4KL}. \tag{4}$$

where K denotes the turns ratio of the ac transformer. Furthermore, the dc voltage ratio ρ is defined as the ratio between the voltages across the equivalent series inductance (ESL) L, where

$$\rho = \frac{V_{\text{dcs}}}{KV_M}. \tag{5}$$

Then, I_0 in (4) can be reformulated using the dc voltage ratio ρ, and I_1 can be derived as

$$I_0 = \frac{(1+2D\rho-\rho)\,V_M}{8Lf_s} - \frac{V_M T_{tp} - \rho V_M T_{ts}}{4L} \tag{6a}$$

$$I_1 = \frac{(1+2D\rho-\rho)\,V_M}{8Lf_s} - \frac{V_M\,(T_{tp} + 2\rho T_{tp} - \rho T_{ts})}{4L}. \tag{6b}$$

When operating in reverse power transfer mode, with $D \in [-0.5, 0]$, the current seen by the primary bridge at the inserted switching instant on the MV side becomes

$$I_0 = \frac{(-\rho-2D\rho+1)\,V_M}{8Lf_s} + \frac{V_M T_{tp} + \rho V_M T_{ts}}{4L}. \tag{7}$$

The value of this current is close to that in forward power transfer when operating at the same absolute values of phase shift D and dc voltage ratio ρ, except for the difference introduced by staircase transitions.

In the QSW-modulated MMC stacks, the additional current points can be derived using symmetry, where

$$I_4 = -I_0,\quad I_5 = -I_1,\quad I_6 = -I_2,\quad I_7 = -I_3 \tag{8}$$

and the transferred power in the forward direction can be computed as

$$P = \frac{\rho V_M^2}{8Lf_s}\left[D(1-D) - \Delta\right]. \tag{9}$$

The duty ratios of staircase transitions are defined as $D_{tp} = T_{tp}/T_s$ and $D_{ts} = T_{ts}/T_s$, thus the power degradation factor Δ in (9) can be derived as

$$\Delta = \frac{4}{3}\left(D_{tp}^2 + D_{ts}^2 - \frac{3}{2}D_{tp}D_{ts}\right) + (1-2D)\,(D_{tp} - D_{ts})\,. \tag{10}$$

From (9), by introducing the base values, the normalized power transfer in the dc–dc module can be expressed as in the following equation:

$$P_{\text{base}} = \frac{V_M^2}{8Lf_s},\quad V_{\text{base}} = V_M,\quad Z_{\text{base}} = 8Lf_s \tag{11a}$$

$$P^* = \rho\left[D(1-D) - \Delta\right],\qquad D \in [0, 0.5] \tag{11b}$$

$$P^* = \rho\left[D(1+D) + \Delta_R\right],\quad D \in [-0.5, 0] \tag{11c}$$

where the power degradation factor for reverse power transfer, Δ_R, is different from Δ, as

$$\Delta_R = \frac{4}{3}\left(D_{tp}^2 + D_{ts}^2 - \frac{3}{2}D_{tp}D_{ts}\right) + (1+2D)\,(D_{ts} - D_{tp})\,. \tag{12}$$

To avoid high power degradation caused by increased transitions D_{tp} and D_{ts}, a boundary equation is introduced to limit the maximum power drop within 10% of transferred power as $(\Delta/D(1-D) < 0.1)$, where

$$P^* > P_{Bd}(\rho, D)$$
$$= \frac{40\rho}{3}\left(D_{tp}^2 + D_{ts}^2 - \frac{3}{2}D_{tp}D_{ts}\right) + 10\rho\,(1-2D)\,(D_{tp} - D_{ts}) \tag{13}$$

and for reverse power flow, (13) becomes

$$P_{Bd}(\rho, D) = 10\rho\Delta_R. \tag{14}$$

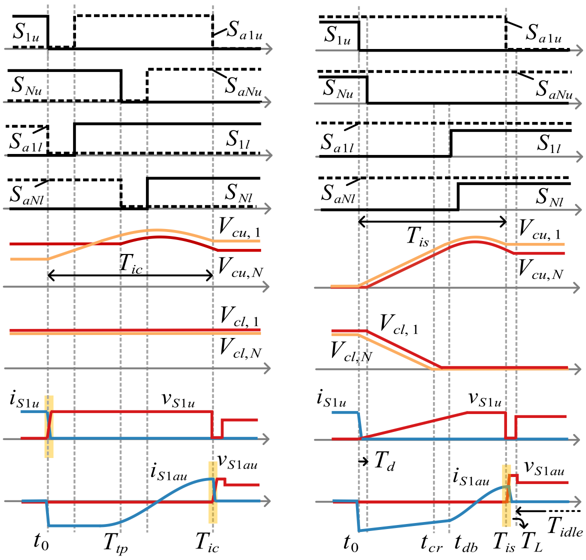

Fig. 3. Switching signals, capacitor voltages, switch voltages, and currents of the operating submodule (S_{1u}, S_{a1u}) under. (a) Clamping mode at low currents. (b) Snubber mode at high currents.

III. Dual-Mode Operation of MMDCT

This article proposes a dual-mode operation strategy for QSW-modulated MMC stacks. At high-current levels, the auxiliary switch is turned ON, allowing the submodule capacitor to function as a snubber component for the main power switch. Under this condition, the MMDCT exhibits a structure and operating behavior similar to that of the SCDCT. The auxiliary switch is actively controlled based on the current magnitude without interrupting the operation of the DAB converter.

At low-current levels, to avoid excessive losses caused by the snubber capacitors, such as in SCDCT, the proposed dual-mode MMDCT reverts to its original clamping mode, which corresponds to a typical QSW-modulated MMC stack, where the submodule capacitor maintains a nominal voltage. During this low-current operation, both the switching losses and the capacitor voltage overshoot are effectively limited.

A. Clamping Mode

Clamping mode will be utilized at low currents, where Fig. 3(a) provides a detailed sketches of switching signals, HBSM voltages V_{cu} and V_{cl}, along with switching waveforms of power-semiconductor devices.

According to [30], under the clamping mode of a QSW-modulated MMC stack, one of the HBSMs switchesOFFits auxiliary switch to block the oscillatory circulating current, thereby improving conversion efficiency by recovering the energy stored in the arm inductance. The switch-OFF delay time in clamping mode, denoted as T_{ic}, can be derived as

$$T_{ic} = \frac{(N_p - 1)\,T_w}{2} + \frac{\pi}{\omega_d} \tag{15}$$

where ω_d indicates the oscillation frequency, which can be computed as

$$\omega_d = \frac{1}{\sqrt{2L_{\text{arm}}\dfrac{C_{\text{SM}}}{N}}}. \tag{16}$$

The work in [29] and [30] analyze the HBSM capacitor voltage overshoot, denoted as γ and defined as

$$\gamma = \frac{V_{c,\max} - V_{cn}}{V_{cn}} \tag{17}$$

and the voltage overshoot with different loading conditions is given as

$$\gamma = \frac{N\,(N-1)\,\omega_d T_w I_0 + 2NI_0}{2\omega_d C_{\text{SM}} V_M}. \tag{18}$$

Based on the voltage overshoot limit criteria, the operating range of clamping mode with different HBSM capacitance can be investigated. By combining (4), (11), and (18), the boundary of transferred power can be derived as

$$\begin{aligned} &P^* > P_{B\gamma}(\rho, D)\\ &\quad = D + \rho D + \rho D^2 - \frac{\gamma\omega_d D C_{\text{SM}} V_{cn} Z_{\text{base}}}{(\omega_d C_{\text{SM}}/N + 1)\,V_{\text{base}}}. \end{aligned} \tag{19}$$

B. Snubber Mode

As the MMDCT primary bridge always sees inductive loading under forward power flow, the stack arm current is suitable for realizing zero-voltage turn-ON in MMDCT. Under heavy-load conditions, HBSM capacitor can be used as snubber capacitance for the main switches S_{ju} and S_{jl} to realize zero-voltage turn-OFF, with auxiliary switches S_{aju} and S_{ajl} being turned ON during all operating time.

Fig. 3(b) gives an illustration of the switching signals, along with the voltage and current waveforms under the snubber mode of MMDCT. At the turn-OFF instant, it can be noted that $V_{cu,j} = 0$ and will be charged relatively slowly compared to the turn-OFF of the main power switch, hence ZVS is realized. Consequently the submodule capacitor C_{SM} is allowed to be fully discharged during the dead-band between two bridges and the MMDCT operates similar to the SCDCT.

Fig. 4 depicts the equivalent circuit of the MMC stack under snubber mode, during the inserted interval of upper arm. At t_0, the main switches $S_{1u} - S_{Nu}$ of upper arm are turned OFF with the maximum time delay T_d, as shown in Fig. 3(b). The upper arm capacitors start to be charged from 0 V and the lower arm start to be discharged from nominal voltage V_{cn}. The average capacitor voltages of the upper and lower arms are denoted as V_{cu} and V_{cl}, respectively. During $[t_0 - t_{cr}]$, by applying Kirchhoff's voltage law (KVL) we have

$$\begin{aligned} &V_{cu} + V_{cl} + L_{\text{arm}}\frac{di_{\text{up}}}{dt} + L_{\text{arm}}\frac{di_{lp}}{dt} = V_{cn}\\ &i_{\text{up}} - i_{lp} = I_0, \quad C_{\text{SM}}\frac{dV_{cu}}{Ndt} = i_{\text{up}}, \quad C_{\text{SM}}\frac{dV_{cl}}{Ndt} = i_{lp}. \end{aligned} \tag{20}$$

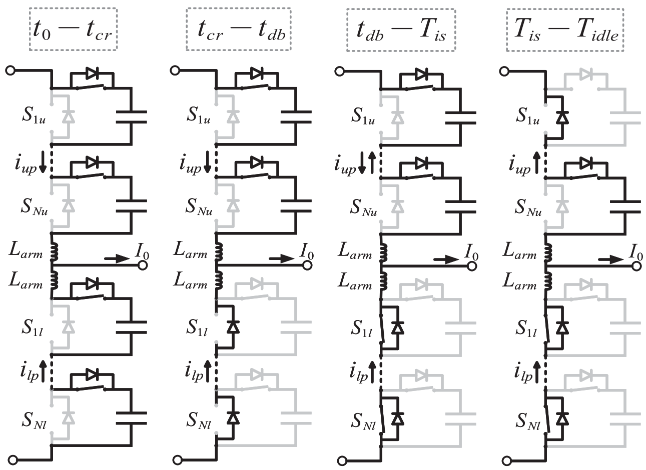

Fig. 4. Equivalent circuit and current commutation path of the snubber mode.

Rearrange (20) leads to a third-order differential equation

$$\frac{d^3V_{cl}}{dt^3} + \frac{N}{L_{\mathrm{arm}}C_{\mathrm{SM}}}\frac{dV_{cl}}{dt} + \frac{N^2}{2L_{\mathrm{arm}}C_{\mathrm{SM}}^2}I_0 = V_{cn} \quad (21)$$

and it can be solved as

$$V_{cu} = \frac{NI_0}{2\sqrt{2}\omega_d C_{\mathrm{SM}}}\sin\left(\sqrt{2}\omega_d t\right) + \frac{NI_0 t}{2C_{\mathrm{SM}}} \quad (22a)$$

$$V_{cl} = \frac{NI_0}{2\sqrt{2}\omega_d C_{\mathrm{SM}}}\sin\left(\sqrt{2}\omega_d t\right) - \frac{NI_0 t}{2C_{\mathrm{SM}}} + V_{cn}. \quad (22b)$$

After the lower arm capacitors are completely discharged, the arm current will conduct the auxiliary diode D_{aju} and keep charging upper arm capacitors. Meanwhile the output current is commutating through the diodes of lower arm D_{jl}. The arm current now becomes

$$\frac{d^2 i_{\mathrm{up}}}{dt^2} + \frac{2R_{\mathrm{arm}}}{L_{\mathrm{arm}}}\frac{di_{\mathrm{up}}}{dt} + \frac{N}{L_{\mathrm{arm}}C_{\mathrm{SM}}}i_{\mathrm{up}} = 0. \quad (23)$$

The upper arm current i_{up} will then show a oscillatory behavior with the oscillation frequency of ω_d, and damping factor of $\alpha = R_{\mathrm{arm}}/2L_{\mathrm{arm}}$.

This oscillation also occurs on the SCDCT structure. With the auxiliary switches S_{aju} and S_{ajl} implemented in the MMDCT structure, this oscillation can be interrupted by switching OFFthe auxiliary switch at the correct time, which is referred to as switch-OFF delay time T_{is}. During $[t_{\mathrm{db}}, T_{is}]$, the upper arm capacitors are first charged and then discharged and ideally at T_{is} the voltage across upper arm submodule capacitors are discharged back to nominal voltage V_{cn}.

After T_{is}, a brief time interval T_L follows, during which D_{1u} conducts and causes a nominal voltage drop in the output voltage. The duration of T_L is short, and once the arm current drops to zero, the submodule enters an idle state, denoted as T_{idle}, providing a clamped submodule voltage. Since the negative current commutation path is blocked by the idle HBSM, no arm current and conduction loss will occur in the auxiliary switches of the inserted arm.

During the inserted interval, as shown in Fig. 4, the upper arm HBSM capacitors experience a lower voltage overshoot than in clamping mode when operating under the same power transfer. This is because the HBSM capacitors are charged from 0 V. Instead of numerically solving (20) and (22), the voltage overshoot in snubber mode can be approximated by considering the energy transferred from the arm inductors and lower arm capacitors to the upper arm capacitors. Therefore

$$\frac{1}{2}NC_{\mathrm{SM}}V_{c,\max}^2 = \frac{1}{2}\left(2L_{\mathrm{arm}}I_0^2 + NC_{\mathrm{SM}}V_{cn}^2\right)$$

$$V_{c,\max} = \sqrt{\frac{2L_{\mathrm{arm}}I_0^2 + NC_{\mathrm{SM}}V_{cn}^2}{NC_{\mathrm{SM}}}}. \quad (24)$$

C. Required Load Current for Snubber Mode

For varying dead-band time t_{db}, the minimum required load current, noted as I_{BL}, can be derived by letting $V_{cl} = 0$ in (22) as

$$I_{BL} = \frac{2C_{\mathrm{SM}}V_{cn}}{Nt_{\mathrm{db}} - \dfrac{N}{\omega_d}\sin\left(\sqrt{2}\omega_d t_{\mathrm{db}}\right)} \quad (25)$$

t_{db} here is designed to cover the discharging time of C_{SM} for bypassed arms, which also specifies the duty ratio of staircase transition of primary bridge, yielding $D_{tp} = t_{\mathrm{db}}/T_s$. According to (10), higher D_{tp} results in transferred power drop, which has to be compensated by higher phase shift D and subsequently higher current. In this article, D_{tp} is designed to be lower than 0.05 to avoid power degradation and the load current I_0 must satisfy

$$I_0 > I_{BL}. \quad (26)$$

The initial computation toward T_{is} can be based on the approximation of using the addition of discharging time with the half cycle of oscillation period, where

$$T_{is} = \frac{2C_{\mathrm{SM}}V_{cn}}{NI_{BL}} + \frac{\pi}{\omega_d}. \quad (27)$$

This time would be used as the feedback control to regulate the steady state turn-OFF voltages of main power switches.

As for a specified D_{tp}, by combining (4), (11), (25), and (26), the required power transfer in per unit P_{Bm} of boundary for minimum phase shift can be obtained, and mathematically the normalized power P^* has to satisfy the power requirement of (28), where

$$P^* < P_{Bm}(\rho, D) = D + \rho D^2 - \frac{DI_{BL}Z_{\mathrm{base}}}{V_{\mathrm{base}}} - \frac{DD_{tp} - \rho DD_{ts}}{4Lf_s}. \quad (28)$$

According to the derivation of transferred power in (9)–(11), the power under snubber mode is highly sensitive to passive components as the selection of C_{SM} will determine D_{tp}. In Fig. 5, the transferred power in terms of various normalized HBSM capacitance, C_{SM}^*, and phase shift D is demonstrated. The HBSM capacitance is normalized using

$$C_{\mathrm{SM}}^* = 2\pi f_s Z_{\mathrm{base}} C_{\mathrm{SM}}. \quad (29)$$

As shown in Fig. 5, under the same D, the transferred power is degraded with the increasing C_{SM}, as larger C_{SM} leads to higher

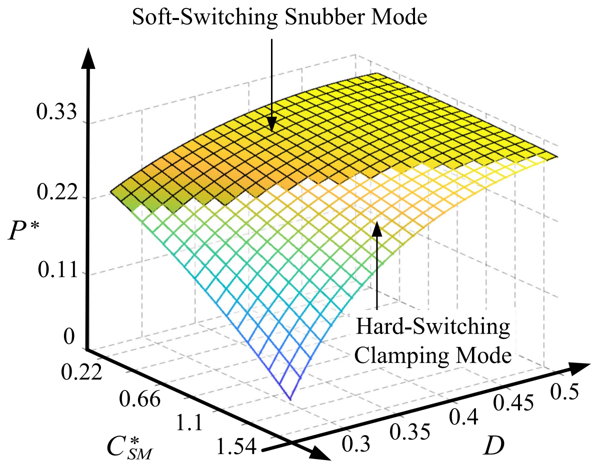

Fig. 5. Normalized transferred power P^* in terms of normalized HBSM capacitance, C^*_{SM}, and phase shift D.

D_{tp}. Therefore, D is required to be greater than a certain value by solving (25) to guarantee that the proposed snubber mode is applicable. Otherwise, only clamping mode can be employed.

After t_{db}, the turn-ON of complementary switch, for example, the S_{jl} at $t = t_{\mathrm{db}}$ in Fig. 4, is expected to see soft turn-ON, which indicates that i_{lp} at this instant is negative and conducting D_{jl}. This criteria can be translated to $I_1 > 0$, thus by combining (4) and (11) we have

$$\begin{aligned} P^* &< P_{Bp}(\rho, D) \\ &= -2DD_{tp} - 2\rho D\left(2D_{tp} - D_{ts}\right) + D + \rho D^2. \end{aligned} \tag{30}$$

Based on the aforementioned analysis, Fig. 6 illustrates the boundary region along with the normalized power transfer P^* (black dashed line) for snubber mode across different values of C_{SM}. It can be observed that as C_{SM} decreases, the snubber mode region expands while the clamping mode region becomes more constrained due to the voltage overshoot exceeding the specified limits.

Under reverse power transfer, where the phase shift $D \in [-0.5, 0]$, the criteria for operating the two modes are identical to those in forward power transfer. The successful operation of the proposed snubber mode depends on the minimum required power, where the current seen by the primary bridge on the MV side, I_0, is positive and higher than the boundary current I_{BL}. Recall the current derivation in (7), the boundary power transfer is then given by

$$P_{Bm}(\rho, D) = \rho D^2 - D + \frac{DI_{BL}Z_{\mathrm{base}}}{V_{\mathrm{base}}} + \frac{DD_{tp} + \rho DD_{ts}}{4Lf_s}. \tag{31}$$

In addition, the criterion $I_1 > 0$ still applies under reverse power flow to ensure that the complementary arm experiences a negative current while enabling soft turn-ON. Therefore

$$P_{Bp} = \rho D^2 - D + 2DD_{ts} + 2\rho D\left(D_{tp} - 2D_{ts}\right). \tag{32}$$

Fig. 7 depicts the boundary curves of the operating modes for the MMDCT as functions of the dc voltage ratio ρ and phase shift D. In deriving Fig. 7, the normalized submodule capacitance is set to $C^*_{\mathrm{SM}} = 0.8$. The figure indicates that at lower dc ratios, the snubber mode is easier to implement for both forward and reverse power transfer, since the MV side experiences a higher positive current at the inserted instant. The cross-sectional area of $|P_{Bm}| < |P^*| < |P_{B\gamma}|$ indicates regions where both modes are valid. However, as the dc voltage ratio ρ further decreases, a region appears where neither mode is feasible, indicating that the dc–dc module can only operate at partial load, or that the passive component sizes may need to be redesigned.

IV. Switching Sequence Control

The control system for the proposed dual-mode MMDCT consists of two parts: a high-level controller that manages the behavior of the two MMC stacks, and a low-level controller that regulates the arm behavior of each MMC stack. The proposed controller in this section can shift between the clamping and snubber mode according to the current magnitude.

A. High-Level Controller

The robust control method proposed in [9] for conventional DAB converters can be adapted for the MMDCT, as the control objective remains the regulation of phase shift in response to voltage or power references. In this article, the power transfer of the MMDCT is regulated using this method, as illustrated in Fig. 8(a). This approach enhances the robustness of phase shift D regulation in the presence of perturbations and step changes in the reference signal.

The generated phase shift D determines the inductor current magnitude seen by the submodules. According to the defined region for the operating sequence provided in Fig. 6, whether clamping mode or snubber mode will be determined for the MMC stack, while a hysteresis band is introduced to avoid consecutive transition between switching modes.

B. Low-Level Controller

The snubber mode is activated when the operating point lies within the boundary region defined by (28), which typically corresponds to high load current conditions. Under light-load conditions, the clamping mode is applied.

A voltage balancing algorithm (VBA) is required when operating in clamping mode to regulate the submodule voltage seen by the power switches, by determining the inserted order of HBSMs. However, when the snubber mode is applied, it is unnecessary to determine the inserted order through VBA, since the HBSM capacitor voltages are fully discharged before insertion, and all HBSMs are inserted simultaneously.

Unlike the switch-OFF delay time of clamping mode T_{ic}, which is independent with the load current, the switch-OFF delay time for snubber mode, T_{is}, varies under different loading conditions. Therefore, a feedback control, as shown in Fig. 8(a), is implemented to regulate the voltage of the submodule capacitors and ensures that the voltage imbalance among the main power switches remains within safe limits.

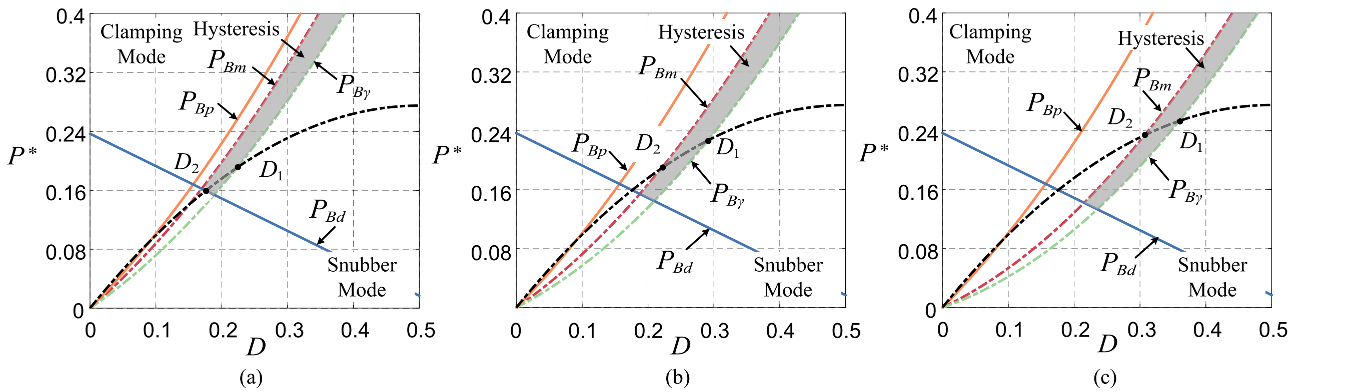

Fig. 6. Boundary curves for mode selection of the dual-mode MMDCT primary bridge under $\rho = 1.1$: P_{Bm} representing the required minimum power for snubber mode, and $P_{B\gamma}$ indicating the maximum power for clamping mode. The curves are presented for different values of submodule capacitance with (a) $C^*_{\mathrm{SM}} = 0.2$, (b) $C^*_{\mathrm{SM}} = 0.5$, and (c) $C^*_{\mathrm{SM}} = 0.8$.

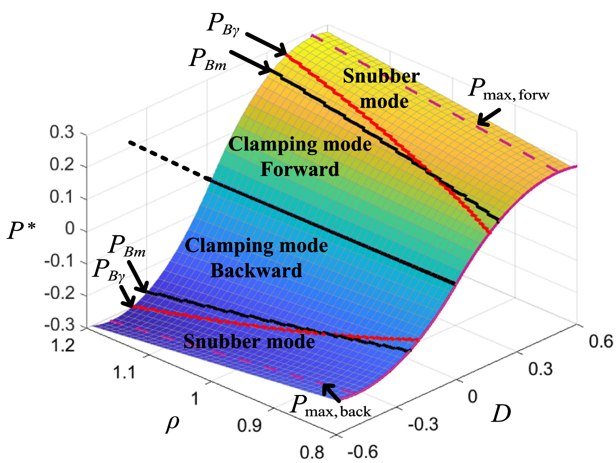

Fig. 7. Boundary curves and normalized transferred power of the operating modes with respect to the DC voltage ratio ρ and phase shift D.

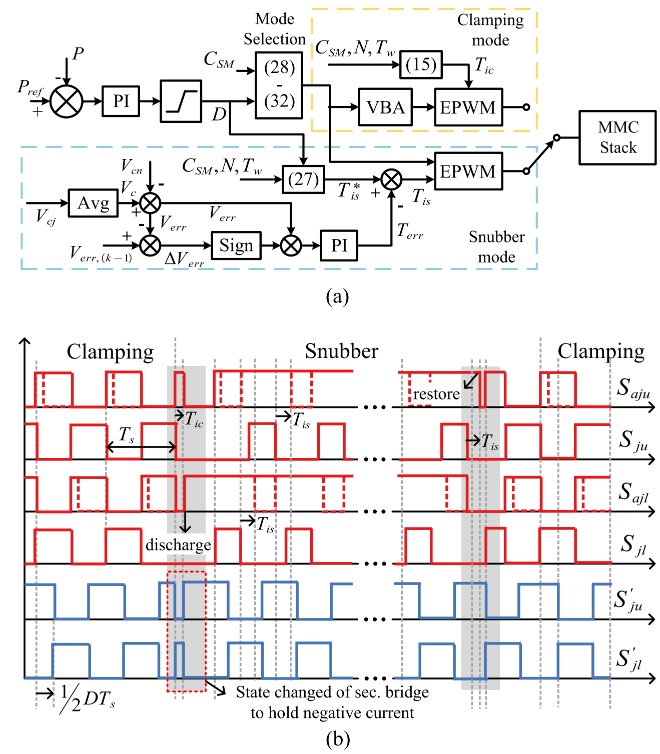

Fig. 8. (a) Controller diagram of the proposed dual-mode MMDCT. (b) Switching signals of state transitions.

To achieve that, the initial T^*_{is} is calculated based on (27). Subsequently, the error voltage signal, V_{err}, is used to determine a corrective time delay, T_{err}, which adjusts T_{is} as

$$T_{is} = T^*_{is} - T_{\mathrm{err}}. \tag{33}$$

However, both lower and higher T_{is} result in increased capacitor voltages. Therefore, the trend of the voltage error signal is incorporated into the calculation of T_{err}, which determines the adjustment direction of T_{is}.

Moreover, implementing a variable switch-OFF delay time in both clamping (T_{ic}) and snubber modes (T_{is}) provides flexibility in addressing issues, such as passive component uncertainties or in particular the capacitance variations, which may negatively affect converter operation.

In high-power, high-gain dc–dc converters, film capacitors are generally preferred over electrolytic or ceramic capacitors for achieving high-efficiency conversion, due to their superior characteristics of low ESL and low equivalent series resistance [35], [36]. Specifically, film capacitors typically exhibit a tolerance of $\pm 10\%$, and their capacitance may decrease by about 5% due to aging [37].

In clamping mode, a decrease in capacitance can lead to a higher oscillation frequency and greater voltage overshoot, as indicated by (16) and (18). For example, considering the worst case of a 15% reduction in total submodule capacitance, the voltage overshoot γ would increase by approximately 17% compared to its original value. This implies that if the original γ is 20%, the final voltage overshoot after the capacitance drop could reach to 23.5%.

The integrated VBA can mitigate potential voltage imbalances caused by capacitance reduction by adjusting the switching order so that the capacitor with the lowest voltage is inserted first. In addition, for the energy recovery technique, T_{ic} can be slightly reduced in response to the capacitance drop to ensure that the steady-state voltages of the submodule capacitors remain close to their nominal values.

In snubber mode, a total decrease in submodule capacitance does not significantly affect the voltage overshoot, as indicated by (24). A 5% reduction in the inserted arm capacitance results in only a 2.6% increase in voltage overshoot, and the steady-state voltages can be controlled by regulating the switch-OFF delay time T_{is}. However, if there is capacitance drop of an individual submodule, then this can cause voltage imbalance since this individual capacitor will see a faster charging than the remaining capacitors. This can result in a 5.3% voltage imbalance according to $CdV/dt = i$. Although this deviation is tolerable relative to the nominal voltage, an additional delay T_d can be introduced for the submodule with the lowest capacitance, which can be detected as having a higher voltage than the other capacitors.

C. Transitions Between Different Modes

The transitions between clamping and snubber modes must be completed within fewer cycles to avoid disruptions in power transfer. Meanwhile, it is necessary to make sure that the inductor current is stable during the transition without any current distortion, which can subsequently result in over-voltage of submodule capacitors and power switches.

The transition from clamping to snubber mode requires the HBSM capacitors to be fully discharged before the next switching edge, while the transition from snubber to clamping mode requires the HBSM capacitors to be restored to their nominal voltage. A hysteresis band is shown in Fig. 6, which is applied to facilitate transitions and prevent frequent toggling between different switching sequences. Fig. 8(b) depicts the transitions between these states.

In the proposed control strategy, the inserted period of upper arm will be used as the execution cycle of mode transition. Once the transition from clamping to snubber mode triggers, all submodules in the upper arm of the primary bridge are switched to idle, after switch-OFF delay time T_{ic}. Then, the lower arm submodules are inserted and discharged, taking advantage of the negative arm current of i_{lp}.

In some applications where a high-frequency operated MMDCT is required, during the transition it would be required to regulate the ac output voltage of the secondary bridge to ensure that the inductor current i_L remains negative, allowing for the continued discharge of the primary lower arm submodule capacitors.

The transition from snubber to clamping mode requires all the lower arm submodules to remain idle, while charging all the primary upper arm capacitors to their nominal voltage at the moment the upper arm is inserted. The detailed gate signals are provided in Fig. 8(b).

V. Simulation of the MMDCT Under Dual-Mode Operation

This section presents the simulation results of the dc–dc converter module based on the proposed dual-mode MMDCT, which is configured for a step-up conversion from MVdc to HVdc in Simulink, with the corresponding circuit parameters listed in Table I. The subsequent loss analysis is done with the use of 1700 V 1800 A FF1800R17IP5P IGBT for medium-voltage high-current primary side.

TABLE I
Parameters of the Proposed Dual-Mode MMDCT

	Primary bridge	Secondary bridge
DC voltage (V_M, V_{dcs})	10 kV	25 kV
Number of HBSMs per arm	10	25
HBSM capacitance (C_{SM})	15 μF	20 μF
Arm inductance (L_{arm})	10 μH	5 μH
Arm resistance (R_{arm})	5 mΩ	30 mΩ
Dwell transition time (T_w)	1 μs	500 ns
Output voltage (V_H)	100 kV	
Number of dc–dc modules (n)	4	
Rated duty ratio (D)	0.4	
Rated power (P)	10 MW	
Operating frequency (f_s)	1 kHz	
Equivalent inductance (L)	1.2 mH	
Coupling transformer	11 kV/25 kV—power: 3 MVA series inductance: 10% series resistance:0.3% Base impedance: 40.3 Ω (primary)	

Fig. 9 compares the ac outputs v_p and v_s, inductor current i_L, HBSM capacitor voltages V_{cj}, and upper arm current $i_{\rm up}$ under different loading conditions and switching patterns of the proposed dual-mode MMDCT. Under the light-load condition with clamping mode, as illustrated in Fig. 9(a), QSW modulation is achieved in v_p and v_s. With the implementation of switch-OFF delay time T_{ic}, the oscillations in the HBSM capacitor voltage and arm current are eliminated, which ensures a high conversion efficiency.

According to the (28) and Fig. 6, the phase shift D is expected to be greater than 0.35 for MMDCT operating under snubber mode. The submodule capacitors are fully discharged during the turn-ON period of main power switches. At turn-OFF switching instant, the submodule capacitor voltage slowly ramps, acting as a snubber capacitor to the main power switches. Under this condition, the MMDCT operates similar to SCDCT. The regulation of switch-OFF delay time, T_{is}, blocks the ringing commencing on the power switch voltages and arm currents. Meanwhile, the steady-state voltage is controlled to be close to nominal voltage, V_{cn}.

The transitions between two modes are finished within a few cycles, as shown in Fig. 10. The energy stored in the submodule capacitors from clamping action is smoothly released to the secondary bridge during the transition with the negative arm current, which prevents the high circulating current caused by sudden voltage change of submodule capacitors. In addition, the inductor current shows a stable transition, which ensures there is no overvoltage for both clamping and snubber modes.

In order to validate the efficiency improvement of the proposed dual-mode MMDCT, a loss analysis is applied to SCDCT and MMDCT of the high-gain MV/HV dc–dc converter, under different transferred power. The conduction losses of the main power switches $P_{c,S}$ and diodes $P_{c,D}$ can be calculated as

$$P_{c,S} = nNV_{\rm ce(on)}\left(i_{L,p} + i_{{\rm up},p}\right) \tag{34a}$$

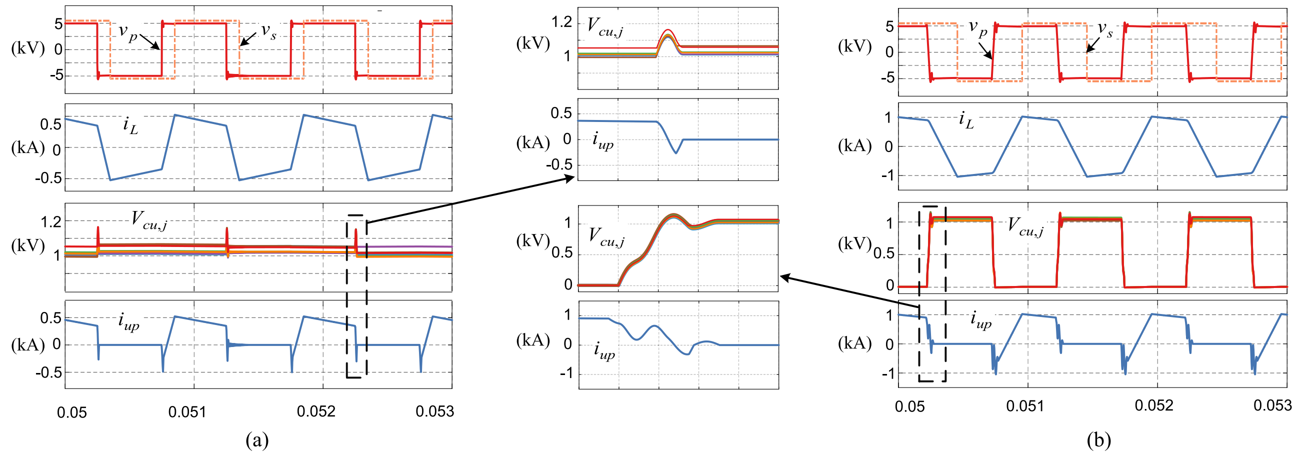

Fig. 9. AC output v_p and v_s, inductor current i_L, HBSM capacitor voltages V_{cj}, arm current of upper arm i_{up} under (a) light load with clamping mode, and (b) heavy load with snubber mode.

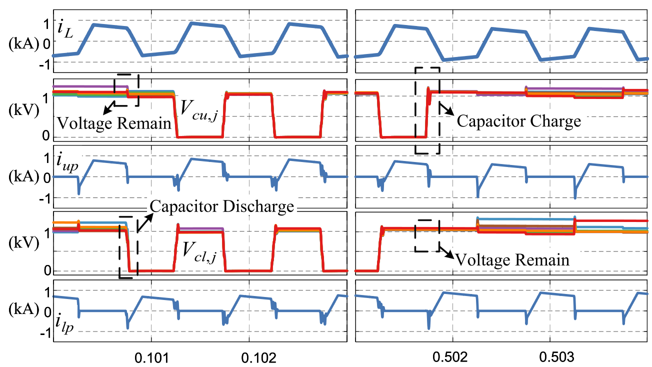

Fig. 10. Inductor current, capacitor voltages, and arm currents under mode transition from clamping to snubber mode (left), and from snubber to clamping mode (right).

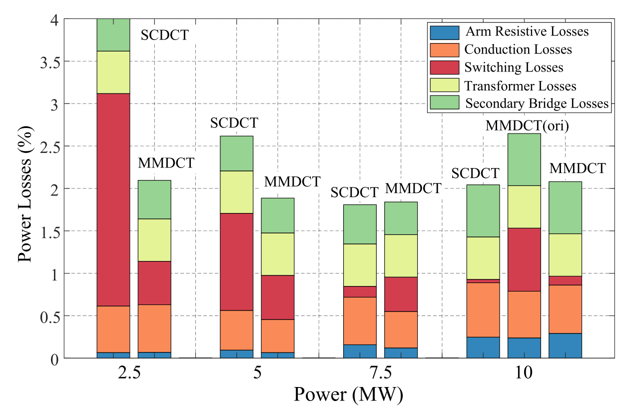

Fig. 11. Percentage of total losses in DC–DC converters employing SCDCT and the proposed dual-mode MMDCT under varying transferred power levels.

$$P_{c,D} = nNV_f\left(i_{L,n} + i_{\mathrm{up},n}\right) \tag{34b}$$

where $i_{L,p}$ and $i_{L,n}$ denote the positive and negative inductor current, respectively, and $i_{\mathrm{up},p}$ and $i_{\mathrm{up},n}$ represent the upper arm circulating current when it is positive and negative, respectively. Moreover, the resistive losses are calculated as

$$P_{\mathrm{res}} = R_{\mathrm{arm}}\left(i^2_{L,p,\mathrm{rms}} + i^2_{\mathrm{up},p,\mathrm{rms}}\right). \tag{35}$$

Under clamping mode, the switching losses of power switches and antiparallel diodes can be calculated as

$$P_{\mathrm{sw},S} = 2nNf_sE_{off}\frac{I_0V_{cn}}{I_{\mathrm{ref}}V_{\mathrm{ref}}} \tag{36a}$$

$$P_{\mathrm{sw},D} = 2nNf_sE_{rr}\frac{I_0V_{cn}}{I_{\mathrm{ref}}V_{\mathrm{ref}}} \tag{36b}$$

where I_{ref} and V_{ref} are the rated current and voltage under the test conditions from the datasheet, respectively. Under snubber mode, the switching losses $P'_{\mathrm{sw},S}$ and $P'_{\mathrm{sw},D}$ becomes $1/N$ of the clamping mode since only one auxiliary switch will see a hard turn-OFF to enter the idle state, which gives

$$P'_{\mathrm{sw},S} = \frac{1}{N}P_{\mathrm{sw},S},\; P'_{\mathrm{sw},D} = \frac{1}{N}P_{\mathrm{sw},D}. \tag{37}$$

The conduction losses associated with resistive losses are computed using the current values from simulated model, while the switching losses are from mathematical derivations. The snubber-related losses of SCDCT at low currents are calculated using (2), with the simulated capacitor voltage at the turn-ON instant of the main power switches.

Since the current through the transformer remains similar across different cases, the transformer losses are expected to be comparable. In the simulation, these losses are estimated to be approximately 0.5% of the transferred power [12]. In addition, the losses of the secondary bridge are lower than those of the primary bridge due to the reduced current on the secondary side.

As shown in Fig. 11, loss analysis is conducted for both the SCDCT and the MMDCT under various loading conditions. Under light-load conditions at 2.5 and 5 MW, the SCDCT exhibits significant snubber-related losses, as the snubber capacitors cannot be fully discharged within the dead-band interval. In

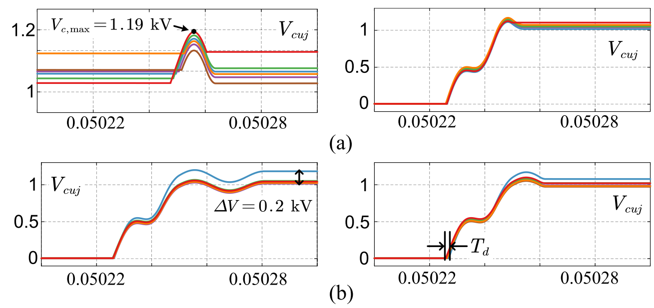

Fig. 12. Impact of submodule capacitance variations under (a) total capacitance drop and (b) single-capacitor variation in snubber mode operations.

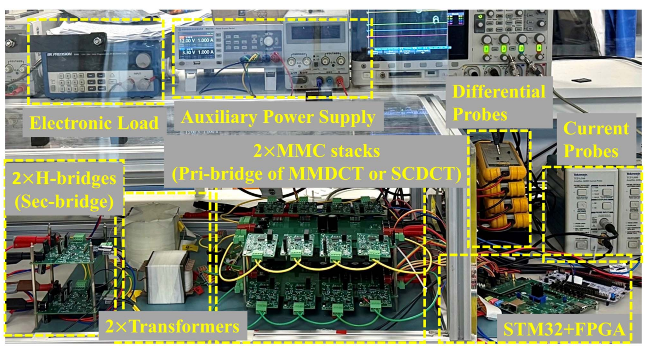

Fig. 13. Overall experimental setup of the scaled MMDCT, with IPOS connections.

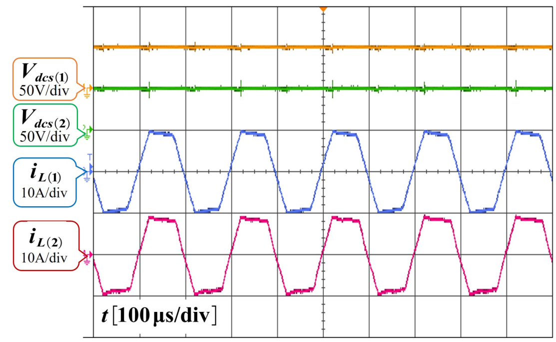

Fig. 14. Experimental waveforms of the IPOS connected DC–DC converter.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP FOR THE PROPOSED DUAL-MODE MMDCT

DAB parameters	Values	Arm parameters	Values
V_{dc}	100 V	C_{SM}	4.7 μF
ρ	[0.8 , 1]	L_{arm}	10 μH
D	[-0.5 , 0.5]	N	4
L_s	220 μH	T_w	2 μs
f_s	5 kHz	T_{tp}	6 μs
K	1:1	V_{cn}	25 V

contrast, the clamping mode of the MMDCT effectively avoids this loss and improves conversion efficiency.

Under medium-load conditions at 7.5 MW, the overall losses of the SCDCT and the MMDCT are comparable. The SCDCT exhibits higher conduction losses due to current ringing, whereas the MMDCT incurs higher switching losses. Under heavy-load conditions at 10 MW, the MMDCT operates in snubber mode and behaves similarly to the SCDCT. As a result, both converters present similar total losses. The charging current through the auxiliary switch in the MMDCT does not lead to significant additional losses, as it is interrupted upon the turn-OFF of the auxiliary switch. Furthermore, compared to the original QSW-modulated MMDCT, the dual-mode operation significantly reduces switching losses.

Fig. 12(a) presents the capacitor voltage overshoots of both clamping and snubber modes under the 15% total capacitance reduction. It can be observed that in clamping mode, the voltage overshoot increases from 1.16 to 1.19 kV, corresponding to an 18.75% increment. In contrast, the effect on voltage overshoot in snubber mode remains limited.

As discussed in previous sections, capacitance mismatches or single capacitance drop can introduce voltage imbalance under snubber mode. Fig. 12(b) illustrates the voltage overshoot in snubber mode with a single capacitance reduction. Without compensation, a voltage imbalance of up to 20% of the nominal voltage can occur. However, by introducing a corrective delay time T_d through the low-level controller, this imbalance can be effectively minimized.

VI. EXPERIMENTAL RESULTS

A scaled test rig of the MMDCT with a rated power of 500 W was constructed to validate and analyze the practical performance of the proposed dual-mode operation. As shown in Fig. 13, the test rig consists of two MMC stacks, which serve as the primary sides of the MMDCT, and the MMDCTs are configured in an IPOS connection, with two H-bridges connected in series on the output side. Each MMDCT achieves voltage step-down conversion from 100 V at a switching frequency of 5 kHz, with a ferrite transformer providing galvanic isolation. An STM32H7-based microcontroller is used as the high-level controller, performing phase shift generation between bridges. Each MMC arm contains $N = 4$ submodules, and a 100-MHz Artix-7 FPGA is employed to implement the MMC arm switching control and dual-mode operation.

Table II lists the selected circuit parameters of the primary bridge in detail. The submodule capacitance $C_{\rm SM}$ is selected to emulate the required discharging time, which maintains a similar ratio of nominal voltage V_{cn} to load current I_0 as in the simulated medium-voltage MMDCT.

A scaled SCDCT test-rig was also constructed for comparison purposes. The snubber capacitor C_s is chosen as 1 μF to emulate practical medium-voltage converter behavior and ensure proper voltage sharing by following (1) across four series-connected MOSFETs. Both the snubber capacitance and arm inductance in the SCDCT setup are lower than those in the dual-mode MMDCT, ensuring a fair comparison between the two topologies under appropriately scaled conditions.

Fig. 14 depicts the experimental waveforms of the IPOS-connected dc–dc module units with ρ set to 1. The output voltages of the two converters, $V_{dcs(1)}$ and $V_{dcs(2)}$, are both regulated at 50 V. The inductor current waveforms, $i_{L(1)}$ and

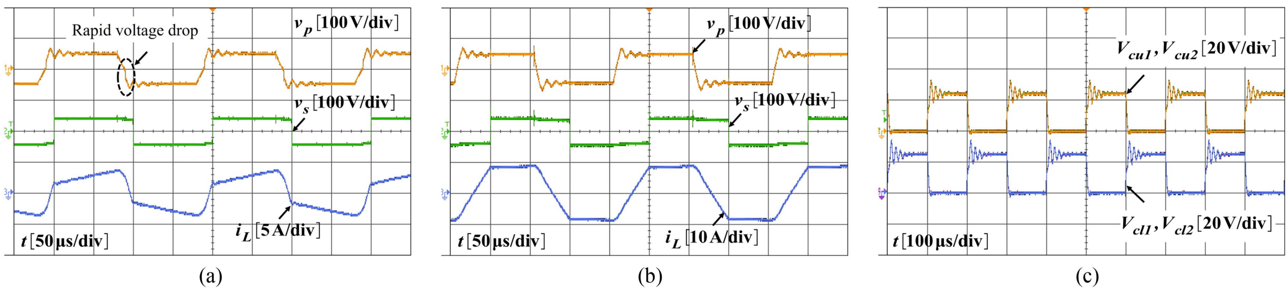

Fig. 15. Experimental waveforms of SCDCT under (a) light load and (b) heavy load. (c) Drain–source voltages of series-connected power switches of SCDCT under heavy-load conditions.

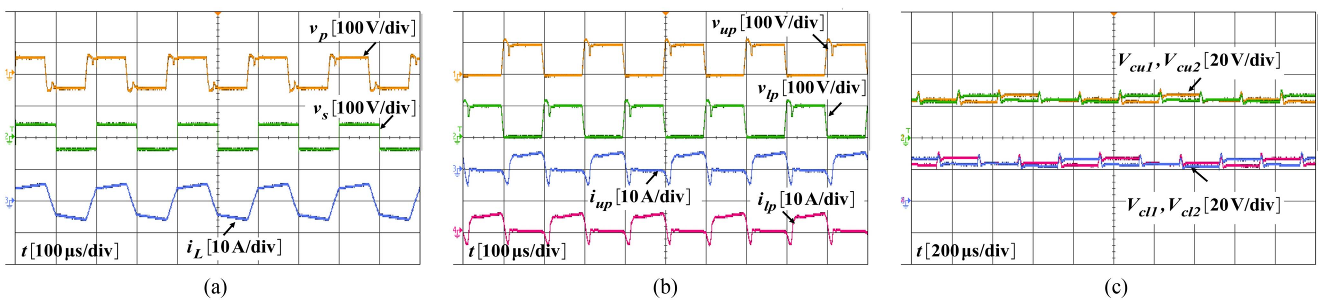

Fig. 16. MMDCT operation under clamping mode during light loads. (a) Output voltages of two bridges, and inductor current. (b) Stack arm voltages and currents. (c) Capacitor voltages of upper and lower arms.

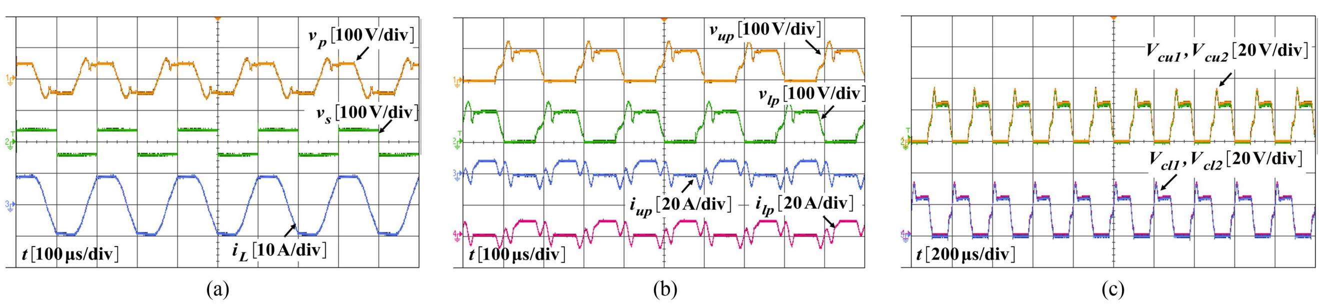

Fig. 17. MMDCT operation under snubber mode during heavy loads. (a) Output voltages of two bridges, and inductor current. (b) Stack arm voltages and currents. (c) HBSM capacitor voltages of upper and lower arms.

$i_{L(2)}$, as shown in Fig. 14, confirm that the power conversion is evenly shared between the two dc–dc modules.

Fig. 15 presents the experimental waveforms of the output voltages from both bridges in the SCDCT topology with $\rho = 0.8$. Under light-load conditions with a duty cycle of $D = 0.2$, a rapid change in the output voltage v_p can be observed in Fig. 15(a). This is resulted from the insufficient current to fully discharge snubber capacitors during the dead-band period, leading to considerable snubber-related losses.

Under heavy-load conditions, snubber-related losses are negligible, as the higher current enables full discharge of the snubber capacitors before the main power switches turn ON, thereby achieving ZVS at all turn-OFF instants. However, efficiency degradation still occurs due to the ringing, which results from the interaction between stray inductance and snubber capacitance.

The proposed dual-mode MMDCT operates in the original clamping mode during light-load conditions, as shown in Fig. 16, where turn-OFF of the auxiliary switch suppresses oscillatory circulating currents [30]. In this mode, the submodule capacitors remain charged to their nominal voltage, which ensures uniform voltage sharing across the main power switches. In addition, snubber-related losses at low currents are effectively avoided, in contrast to the SCDCT.

Under heavy-load conditions with a high phase shift value D, the proposed dual-mode MMDCT operates in snubber mode, as illustrated in Fig. 17(a). In this mode, the auxiliary switch is turned ON to enable the submodule capacitors to be fully discharged under high-current conditions, facilitating effective energy transfer and ZVS. To suppress undesired oscillations, one submodule selectively turns OFF its auxiliary switch during the inserted state, thereby blocking circuit ringing and reducing conduction losses caused by the inserted arm currents. This behavior is evidenced by the near-zero values of i_{up} and i_{lp} during insertion, as shown in Fig. 17(b). Furthermore, the snubber mode ensures sufficient voltage sharing across the main

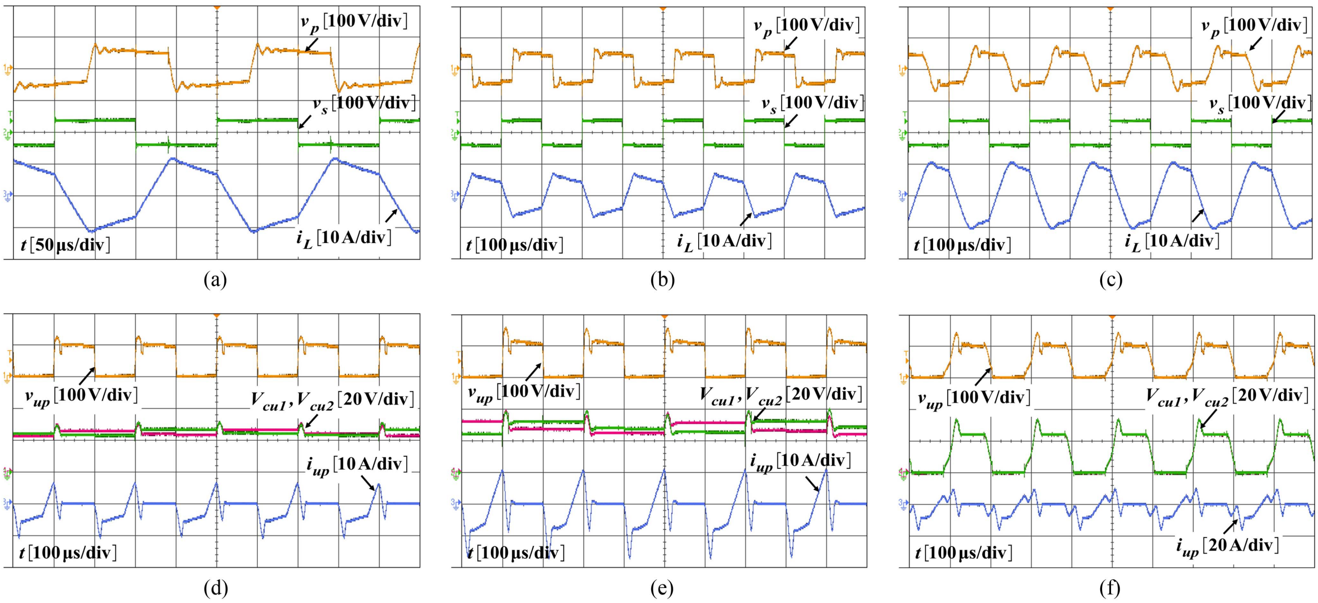

Fig. 18. Experimental results under reverse power transfer. Output voltages of the primary and secondary sides and inductor current for (a) SCDCT. (b) MMDCT with clamping mode. (c) MMDCT with snubber mode. Arm behaviors of stack voltage, two upper arm capacitor voltages, and upper arm currents for MMDCT with clamping mode under (d) light load, (e) heavy load, and (f) MMDCT with snubber mode under heavy load.

power switches by using the submodule capacitors as passive voltage-balancing components, as demonstrated in Fig. 17(c).

Compared to the original MMDCT, the implementation of snubber mode is able to further reduce the voltage overshoot at high currents, since the capacitor voltage is charged from 0 V instead of the nominal voltage. Moreover, the nonnegligible switching losses are significantly reduced at high currents, as the submodule capacitors slow down the voltage rise across the main power switches.

Both SCDCT and MMDCT are bidirectional dc–dc converters, as their high-level architectures are derived from the DAB converter. Fig. 18(a)–(c) illustrates the reverse power flow operation of SCDCT and MMDCT by showing the output voltages and inductor currents. It can be observed that the output voltage of the secondary bridge leads that of the primary bridge, indicating reverse power flow. SCDCT still exhibits ringing during the turn-OFF of the power switches, as shown in Fig. 18(a), which contributes to oscillation losses.

For MMDCT, the clamping mode is used under light-load conditions and the snubber mode under heavy-load conditions, as shown in Figs. 18(b) and 1(c), respectively. The results confirm stable operation of the proposed dual-mode MMDCT under reverse power flow. In addition, the arm behaviors, including the stack voltage, capacitor voltages, and the upper arm current, are tested under reverse power flow. As shown in Fig. 18(d)–(f), the MMC arm still experiences inductive loading at turn-OFF because the absolute phase shift exceeds the boundary condition, which also ensures proper operation of the snubber mode.

Compared with SCDCT, no oscillation occurs in the dual-mode MMDCT, which confirms that the integrated energy recovery technique remains effective during reverse power flow. Moreover, Fig. 18(e) shows the arm behavior of the original MMDCT with clamping mode under heavy-load conditions. It can be noted that, compared with the original MMDCT, the proposed snubber mode of MMDCT, as shown in Fig. 18(f), further reduces the capacitor voltage overshoot by approximately 20%.

The proposed dual-mode operation ensures that the high-current side of the MMDCT adopts an optimized switching mode based on the instantaneous current level. During the transition from clamping mode to snubber mode, as illustrated in Fig. 19, the lower arm submodule capacitors [see Fig. 19(c)] are fully discharged while the upper arm remains in the inserted state. This is accomplished by switching the upper arm submodules to the idle state and then reinserting the lower arm submodules. In high-frequency operation, the output of the secondary bridge [see Fig. 19(a)] is regulated to provide sufficient positive load current, enabling the full discharge of the lower arm submodule capacitors.

Fig. 20 illustrates the reverse transition from snubber mode to clamping mode, during which the voltages of the lower arm submodule capacitors are restored using the positive current in the arm. Once the target voltage is reached, the lower arm submodules are switched to the idle state to prevent further discharge of the capacitors, even as the upper arm is being charged, as shown in Fig. 20(c).

The transition between the two operating modes is completed within approximately one switching cycle, and the inductor currents remain stable throughout the process. Therefore, it can be concluded that the mode transitions introduce no current distortion or overvoltage, and enable fast, smooth switching between modes without interrupting power transfer in the MMDCT.

Fig. 21 presents the measured efficiency η across the full operating range for the SCDCT, the original MMDCT employing only clamping mode, and the proposed dual-mode MMDCT. Under light-load conditions with low-current levels, the MMDCT achieves higher conversion efficiency than the SCDCT due to the elimination of snubber-related losses. This improvement is verified under both forward and reverse power

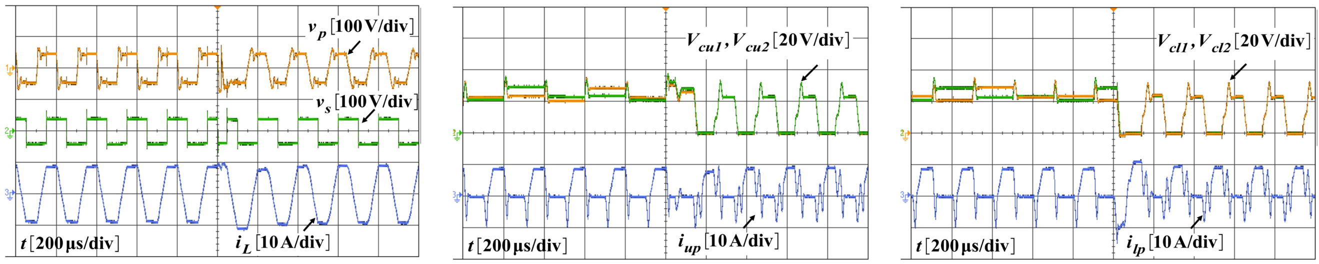

Fig. 19. Transition from clamping to snubber mode, showing (a) the output voltage and inductor current, (b) the submodule voltages and arm current of the upper arm, and (c) the submodule voltages and arm current of the lower arm.

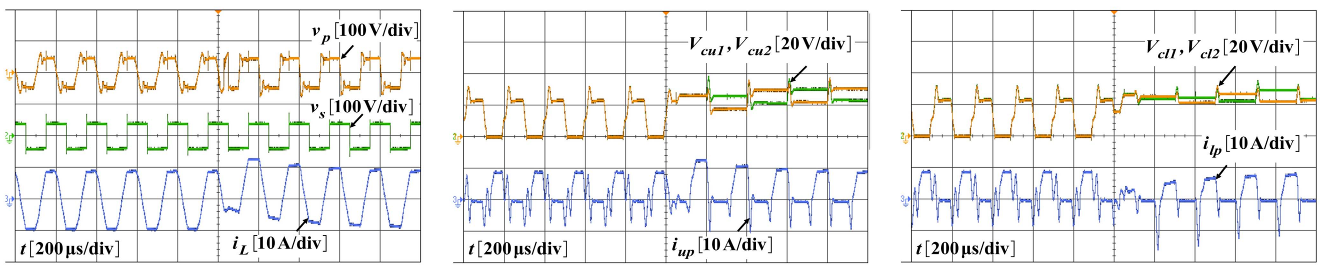

Fig. 20. Transition from snubber to clamping mode, showing (a) the output voltage and inductor current, (b) the submodule voltages and arm current of the upper arm, and (c) the submodule voltages and arm current of the lower arm.

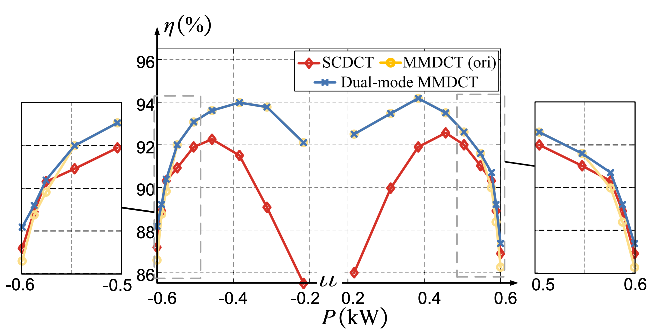

Fig. 21. Conversion efficiency η of the SCDCT, MMDCT, and the proposed dual-mode MMDCT under different transferred power levels with bidirectional power flow.

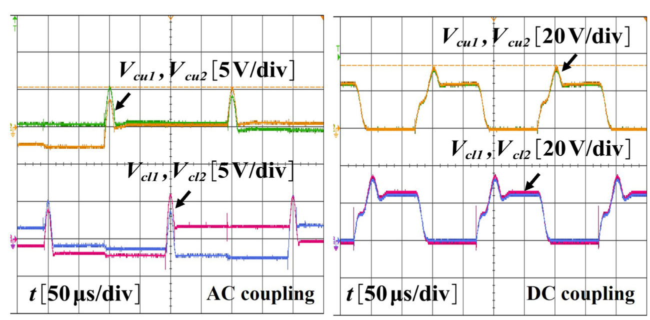

Fig. 22. Experimental waveforms of submodule capacitor voltages under capacitance variations.

flow. The original MMDCT exhibits a similar efficiency to the dual-mode MMDCT in this region, as both operate in the same switching mode.

Under heavy-load conditions with high-current levels, the zoomed-in view of Fig. 21 shows that the dual-mode MMDCT exhibits a higher efficiency than the original MMDCT, indicating a clear tendency of efficiency improvement due to the reduction of switching losses. Moreover, the dual-mode MMDCT maintains a higher efficiency than the SCDCT, as the snubber mode effectively suppresses circuit ringing and mitigates oscillation losses associated with the energy stored in the arm inductors. This efficiency improvement trend is consistently observed under both forward and reverse power flow conditions.

Fig. 22 illustrates the impact of submodule capacitance variations on the submodule capacitor voltages. In this test, the original 4.7 μF capacitors in the lower arm were replaced with 3.9 μF capacitors, corresponding to a reduction of approximately 17%. Under clamping mode, the overall capacitance decrease leads to a higher capacitor voltage overshoot, with the measured value increasing from 20.8% to 24%. In contrast, the snubber mode shows limited sensitivity to the total capacitance reduction, as previously analyzed. To further evaluate this, a single submodule capacitor was replaced with a 3.9 μF capacitor to investigate potential voltage imbalance under steady-state operation. With the implemented low-level controller, a compensating delay is introduced to the submodule exhibiting higher steady-state voltage, which effectively minimizes the voltage imbalance during snubber mode operation.

VII. Conclusion

This article first presents a comparative analysis of modular dc–dc converters for medium- to high-voltage applications, based on the series-connected power switches (SCDCT) and the QSW modulated MMC (MMDCT). The analysis indicates that the SCDCT exhibits relatively low efficiency due to snubber-related losses at light loads, but demonstrates improved performance under high-current conditions owing to the realization of ZVS.

Therefore, a dual-mode operation for the MMDCT is proposed in this article. At low-current levels, the submodule capacitors are utilized as active clamping components for the main power switches, thereby eliminating snubber-related losses observed in the SCDCT. At high-current levels, a newly introduced snubber mode leads to a reduction in switching losses compared to the original MMDCT. In this mode, the auxiliary switch is actively controlled to suppress circuit ringing, further enhancing overall efficiency compared to SCDCT.

The operational regions of the two modes are investigated, along with the transition mechanism between them. The auxiliary switch is dynamically controlled based on the instantaneous current magnitude without interrupting power transfer. Simulation and scaled-down experimental results confirm the improved conversion efficiency of the proposed dual-mode MMDCT across the entire operating range.

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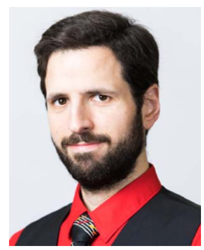

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