Design and Implementation of a Dual-Mode Fast Charger for Supercapacitors

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***Abstract*—Supercapacitors can be charged or discharged by pulse currents with much higher magnitudes compared to the maximum continuous current for limited periods of time. To exploit this characteristic, this article proposes a dual-mode fast charger for supercapacitors that utilizes both continuous and fine-tuned pulse currents by modifying the conventional forward converter. Specifically, the proposed charger introduces two energy storage capacitors to tune the rising and falling edges of the pulse current, respectively. By establishing and maintaining relatively high voltages on the two capacitors, the pulse rising and falling processes are significantly accelerated and the charging time is shortened. To evaluate the proposed charger, a prototype is designed and implemented, which is then used to charge a 12 V/1.5 F supercapacitor moddule from 4 to 8 V. The charging times are 1.68 and 2.04 s when the prototype is configured to operate in the dual-mode and the continuous current mode, respectively. Therefore, the charging time is reduced by 17.6% . Moreover, the pulse characteristics of the proposed charger are significantly improved compared to the conventional forward converter. Specifically, the pulse rising and falling times are dramatically reduced: 4.4 versus 150 μs and 4.2 versus 100 μs, respectively.**

***Index Terms*—Continuous current, dual-mode charging, fast charger, pulse current, supercapacitor.**

I. Introduction

SUPERCAPACITORS are usually characterized as an energy storage technology with a high power density, a long cycle life, and a wide operating temperature range while their downsides include a low energy density and a high self-discharge rate [1]. In fact, supercapacitor-based energy storage systems have been adopted in various electrified transportation systems [2], [3], [4], [5], [6], [7], [8], renewable energy systems [9], [10], [11], [12], [13], [14], [15], low-power systems [16], [17], and defense systems [18], [19].

Supercapacitors can be charged in the constant current (CC), constant voltage (CV), or constant power (CP) modes and multiple aspects of their charging mechanisms have been investigated [20], [21], [22]. For example, as a critical relaxation process of supercapacitors, charge redistribution has been studied [23], [24], [25]. In particular, an optimal charging protocol is proposed to minimize the voltage decay during the charge redistribution process [26]. In addition, advanced charging strategies have been proposed for supercapacitors. For example, a model predictive control (MPC)-based charging strategy is proposed to minimize the charging time for lithium-ion capacitors [27]. As another example, the temperature of the supercapacitor module is utilized to tune the maximum charging current [28]. Moreover, when the supercapacitor charging time is specified, the charging process can be optimized accordingly [29]. Furthermore, an optimal charging method is proposed to maximize the capacity utilization of a hybrid energy storage system incorporating supercapacitors [30].

Other than investigating the supercapacitor charging mechanisms, different types of supercapacitor charging circuits have also been designed, implemented, and tested. For example, a charging circuit dividing a supercapacitor bank into two parts is proposed [31]. A push converter is utilized to implement CC and CP charging modes for supercapacitors [32]. Matrix converters are adopted to charge supercapacitor banks from the power grid [33], [34]. A coordinated charging strategy is proposed for supercapacitor banks [35]. For wireless power transfer (WPT) systems, supercapacitor charging has also been investigated [36]. A WPT system is developed to charge the onboard supercapacitors of a sightseeing car [37]. A converter with a current-controlled semiactive rectifier is proposed to enhance the supercapacitor charging efficiency [38]. A method based on a variable resistance is proposed to design a WPT system for the onboard supercapacitors in an electric vehicle [39].

While the mechanisms, strategies, and circuits above explore different aspects of the supercapacitor charging process, the fact that supercapacitors can be charged by a relatively large pulse current for a limited period of time has not been fully utilized to develop fast and even ultra fast chargers. Supercapacitor datasheets typically specify a continuous current and a pulse current. For example, a 3 V/6 F supercapacitor (manufacturer: Eaton, part number: TV1020-3R0605-R) can sustain a continuous current of 2.4 A and a pulse current of 7.4 A [40]. Based on this fact, a dual-mode fast charger employing both continuous and pulse currents has been proposed for supercapacitors [41], which is developed based on a conventional forward converter [42]. The key feature of this charger is that its pulse characteristics are significantly improved compared to the conventional forward converter. Specifically, by introducing an energy storage capacitor and a branch resistor, the rising and

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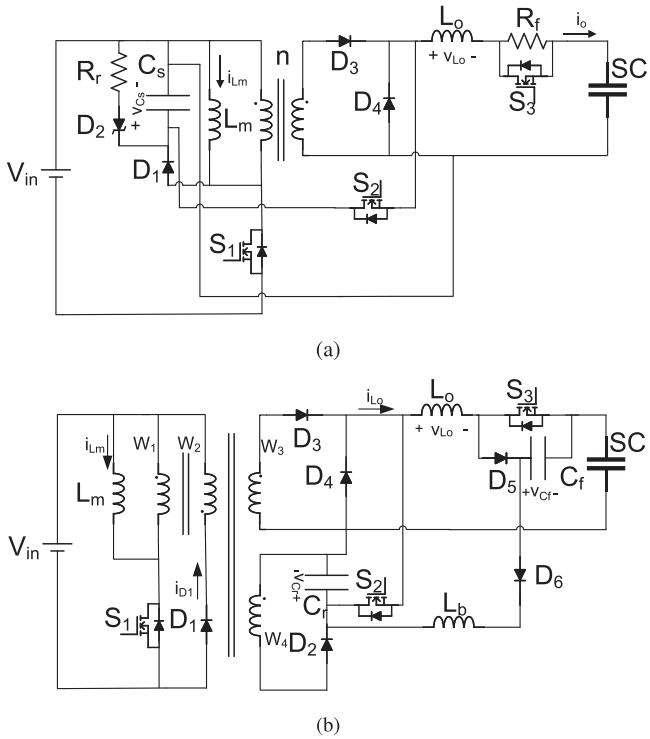


Fig. 1. Dual-mode fast chargers. (a) Topology proposed in [44]. (b) Topology proposed in this article.

falling edges of the pulse current generated by this charger are much sharper than those of the conventional forward converter. Therefore, the transitions between the continuous and pulse current modes are much faster in this charger. Ultimately, this charger shortens the charging time compared to the conventional forward converter. To reduce the circuit complexity and facilitate the circuit implementation, this charger is improved by removing two switches and introducing one diode [43]. Then, a prototype is designed, implemented, and evaluated to demonstrate the feasibility of the dual-mode operation and the impressive pulse characteristics of the improved charger [44].

This article further enhances the work of [44] in the following three aspects.

1) First, the pulse falling process is further accelerated. Figs. 1(a) and 1(b) show the fast charger topologies proposed in [44] and in this article, respectively. The branch resistor R_f in Fig. 1(a) is replaced by the energy storage capacitor C_f in Fig. 1(b). Compared to the voltage across R_f, the C_f voltage (i.e., V_{C_f}) is higher, which leads to a sharper pulse falling edge. An additional benefit of introducing C_f is that energy is stored in C_f instead of being dissipated by R_f, which reduces the loss and improves the efficiency of the charger.
2) Second, the pulse rising process is further optimized. As shown in Fig. 1(b), to establish and maintain the high voltage across the energy storage capacitor C_r, two auxiliary transformer windings W_2 and W_4 are added. Specifically, C_r is charged through W_4. When the C_r voltage (i.e., V_{C_r}) reaches the predefined threshold, the charging process is terminated to ensure that its voltage is maintained at a proper level. On the other hand, Fig. 1(a) shows that the voltage of the energy storage capacitor C_s [i.e., the counterpart of C_r in Fig. 1(b)] is established by L_m. If its voltage is above the threshold, C_s is discharged through the Zener diode D_2 and the discharging resistor R_r, which introduces additional losses and reduces the charger efficiency.
3) Third, energy recycling is introduced to further improve the charger efficiency. Specifically, if $V_{C_f} > V_{C_r} - V_{\text{SC}}$, where V_{SC} is the voltage across the supercapacitor, D_6 is turned ON. In this case, energy is transferred from C_f to C_r through D_6 and L_b to achieve energy recycling.

The rest of this article is organized as follows. Section II presents the topology of the proposed charger and analyzes its operation modes. Section III analyzes the voltage and current stresses of the switches in the proposed charger. Section IV discusses the design considerations for the proposed charger. Section V shows the experimental setup and results. Section VI evaluates the proposed charger against other converters. Finally, Section VII concludes this article.

II. Topology and Operation of Proposed Charger

The topology of the supercapacitor dual-mode fast charger proposed in this article is shown in Fig. 1(b). Similar to the one shown in Fig. 1(a), the charger proposed in this article is also built on the conventional forward converter [42]. As elaborated in [44], while both continuous and pulse currents can be generated using the conventional forward converter, the transitions between these two types of currents may be too slow. To accelerate such transitions, the charger shown in Fig. 1(b) introduces two energy storage capacitors C_r and C_f to tune the rising and falling edges of the pulse current, respectively. The supercapacitor is denoted as SC in Fig. 1(b), which could be a supercapacitor cell, a supercapacitor module, or even a supercapacitor pack depending on its ratings. For the four transformer windings W_1, W_2, W_3, and W_4, their turns ratio is written as $n_1 : n_2 : n_3 : n_4$. The input power source is denoted as V_{in}. The operation of the proposed charger is elaborated as follows. The key waveforms are plotted in Fig. 2.

A. Steady Current Modes

When the output current of the charger is stabilized at either the continuous current or the peak value of the pulse current and no transitions between the continuous and pulse currents are needed, the charger operates in a steady current mode. In this case, the charger behaves as a forward converter. Fig. 2 shows that S_1 is turned ON at t_0. Correspondingly, Fig. 3 shows the equivalent circuit. Clearly, energy is transferred from the power source V_{in} to the supercapacitor through W_1 and W_3. In the meantime, the current of the magnetizing inductor L_m rises linearly.

To enable a fast transition from the continuous current mode to the pulse current mode, the energy storage capacitor C_r associated with the pulse rising process needs to establish and

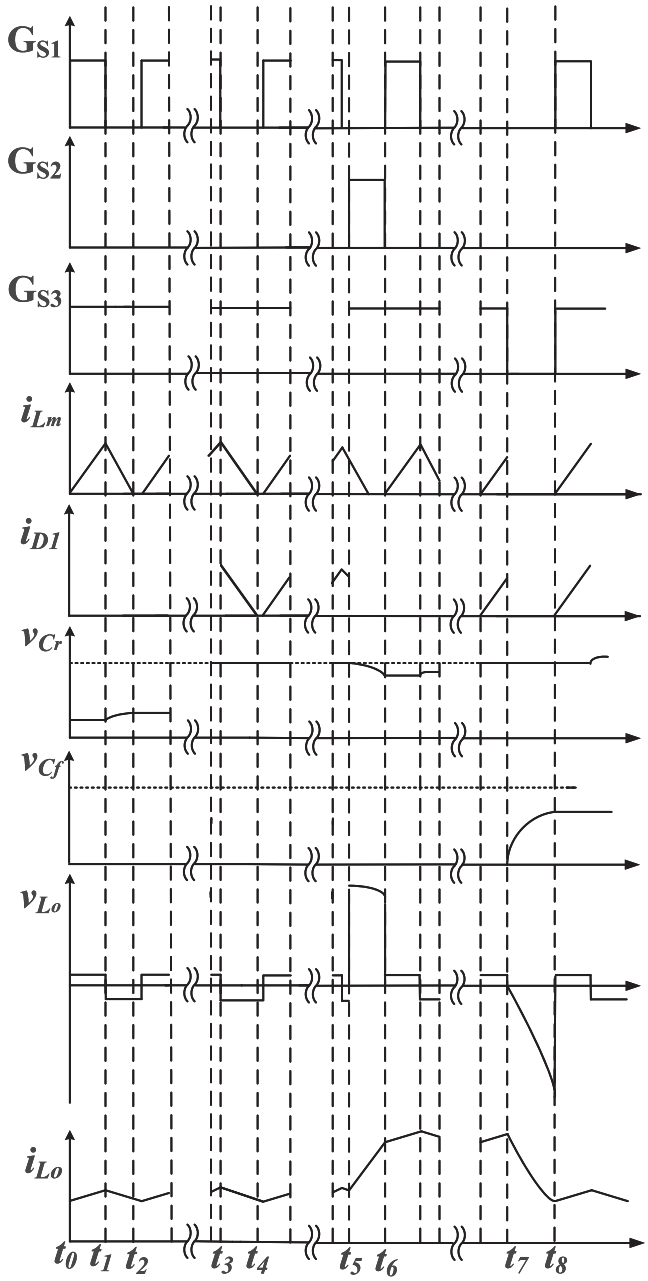


Fig. 2. Key waveforms of proposed charger.

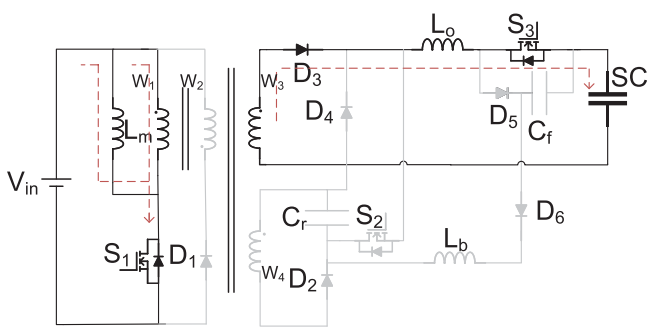


Fig. 3. Steady current mode I: transferring energy from source to supercapacitor through transformer and storing energy in L_m.

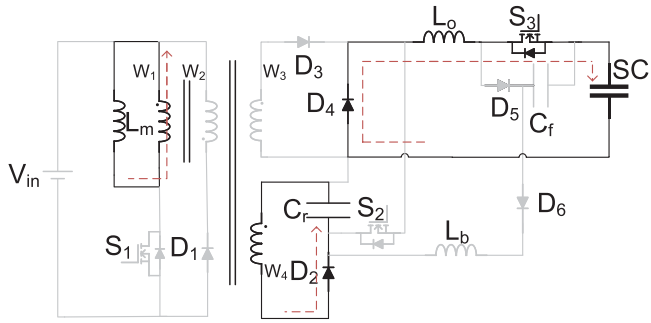


Fig. 4. Steady current mode II: charging of C_r to establish its voltage.

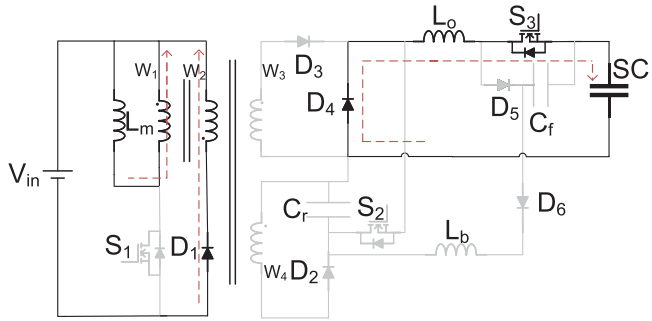


Fig. 5. Steady current mode III: resetting of transformer magnetizing current through D_1.

maintain a high voltage V_t:

$$V_t = V_{\text{in}} \frac{n_4}{n_2}. \tag{1}$$

As illustrated in Figs. 2 and 4, if the voltage of C_r (i.e., V_{C_r}) is lower than V_t, when S_1 is turned OFF at t_1, D_2 is turned ON. Consequently, L_m charges C_r through W_4 and D_2 till the L_m current is reset to zero at t_2.

On the other hand, if V_{C_r} exceeds V_t, when S_1 is turned OFF at t_3, D_1 is turned ON to reset the L_m current to zero through W_2, as shown in Figs. 2 and 5. During this process, the currents of L_m and D_1 decrease linearly to zero at t_4. In the meantime, C_r is not charged by L_m and its voltage is maintained around V_t.

B. Pulse Rising Mode

When the conventional forward converter switches from the continuous current mode to the pulse current mode, the rising rate of its output current is written as

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = \frac{\frac{V_{\text{in}}}{N} - V_{D_3} - V_{\text{SC}}}{L_o} \tag{2}$$

where $N = n_1/n_3$, V_{D_3} is the forward voltage of D_3, and V_{SC} is the supercapacitor voltage.

For the proposed charger, when its output current needs to change from the continuous current to the pulse current, S_1 is turned OFF while S_2 and S_3 are turned ON at t_5, as illustrated in Fig. 2. The corresponding equivalent circuit is shown in Fig. 6. The high voltage of C_r established in the steady current modes is applied to L_o and the supercapacitor. Assuming that V_{C_r} is

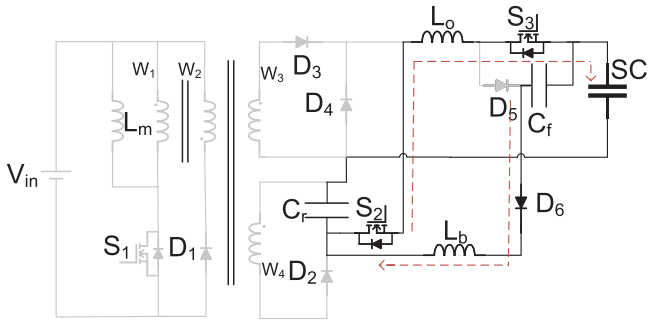


Fig. 6. Pulse rising mode.

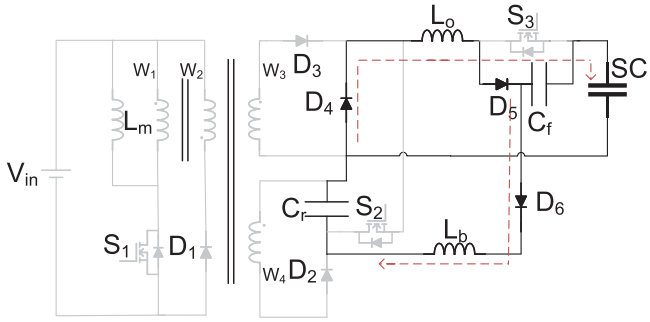


Fig. 7. Pulse falling mode.

constant, the rising rate of the output current is

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = \frac{V_{C_r} - V_{\mathrm{SC}}}{L_o}. \tag{3}$$

Note that $V_{C_r} >> V_{\mathrm{in}}/N$. Therefore, (2) and (3) indicate that the output current rising rate of the proposed charger is much higher than that of the forward converter. Consequently, the proposed charger realizes a much faster transition from the continuous current mode to the pulse current mode. Once the pulse rising process is completed at t_6, the proposed charger returns to a steady current mode.

C. Pulse Falling Mode

As for the pulse falling mode, the conventional forward converter makes a relatively slow transition from the pulse current mode to the continuous current mode because its current falling rate is relatively low:

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = -\frac{V_{D_4} + V_{\mathrm{SC}}}{L_o} \tag{4}$$

where V_{D_4} is the forward voltage of D_4.

For the proposed charger, Fig. 7 shows the equivalent circuit in the pulse falling mode. In this case, S_3 is turned OFF at t_7, as shown in Fig. 2. Moreover, D_5 and C_f are introduced into the output loop. Consequently, C_f is charged to build a high voltage. Ultimately, a sharp pulse falling edge is generated:

$$\frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = -\frac{V_{C_f} + V_{D_4} + V_{D_5} + V_{\mathrm{SC}}}{L_o} \tag{5}$$

where V_{C_f} is the voltage of C_f. Clearly, $V_{C_f} + V_{D_4} + V_{D_5} + V_{\mathrm{SC}} >> V_{D_4} + V_{\mathrm{SC}}$. Therefore, (4) and (5) show that the current falling rate is much higher for the proposed charger compared to the forward converter. Once the pulse falling process is completed at t_8, the charger switches to a steady current mode.

When $V_{C_f} > V_{C_r} - V_{\mathrm{SC}}$, D_6 is turned ON. Energy is transferred from C_f to C_r through D_6 and L_b to achieve energy recycling until the current of L_b is reset to zero. During this process, the charging current for the supercapacitor is $i_{\mathrm{SC}} = i_{L_o} - i_{L_b}$, where i_{L_b} is the current of L_b. Since i_{L_b} is relatively small, i_{SC} is approximately equal to i_{L_o}. It should be noted that energy recycling can still be implemented even without L_b. In this case, i_{L_o} is shared by two branches: 1) the branch with C_f and the supercapacitor and 2) the branch with C_r and D_6. Therefore, i_{SC} is approximately equal to $i_{L_o} C_f/(C_f + C_r)$. Also note that when the proposed charger works stably, V_{C_r} and $V_{C_f} + V_{\mathrm{SC}}$ are both approximately equal to V_t. Therefore, C_r and C_f are maintained at a high voltage to enable fast transitions between the continuous and pulse current modes.

III. Voltage and Current Stresses of Switches

This section analyzes the voltage and current stresses of the switches in the proposed charger. The continuous and pulse currents are denoted as I_C and I_P, respectively.

The voltage stresses of S_2, S_3, D_2, D_3, D_4, D_5, and D_6 are all V_t. For S_1 and D_1, their voltage stresses are $V_t n_4/n_1 + V_{\mathrm{in}}$ and $V_{\mathrm{in}}(1 + n_2/n_1)$, respectively.

The current stresses are determined when the output current is I_P because I_P is much higher than I_C. Specifically,

$$I_{S_3\_\mathrm{rms}} = I_P \tag{6}$$

$$I_{D_3\_\mathrm{rms}} = \sqrt{D} I_P \tag{7}$$

$$I_{D_4\_\mathrm{rms}} = \sqrt{1 - D} I_P \tag{8}$$

where D is the duty cycle of S_1.

When S_1 is turned ON, its current equals the sum of I_P/N and the L_m current. Assuming that the L_m current has been reset to zero before S_1 is turned ON and this current rises linearly after S_1 is turned ON, the current stress of S_1 is

$$\begin{aligned} I_{S_1\_\mathrm{rms}} &= \sqrt{\frac{1}{T_s}\int_0^{DT_s} \left(\frac{I_P}{N} + \frac{V_{\mathrm{in}}}{L_m} t\right)^2 dt} \\ &= \sqrt{\frac{V_{\mathrm{in}}^2 D^3}{3{L_m}^2 f^2} + \frac{V_{\mathrm{in}} I_P D^2}{N L_m f} + \frac{{I_P}^2 D}{N^2}} \end{aligned} \tag{9}$$

where T_s is the switching period, f is the switching frequency, and $T_s = 1/f$.

When V_{C_r} is lower than V_t and S_1 is just turned OFF, a current flows through D_2. During this process, V_{C_r} is considered to be constant and the current through L_m decreases linearly to zero. The current stress of D_2 is

$$\begin{aligned} I_{D_2\_\mathrm{rms}} &= \frac{n_4}{n_1}\sqrt{\frac{1}{T_s}\int_0^{\frac{DV_{\mathrm{in}}T_s}{V_{C_r}}} \left(\frac{DV_{\mathrm{in}}T_s}{L_m} - t\frac{V_{C_r}}{L_m}\right)^2 dt} \\ &= \frac{n_4}{n_1}\sqrt{\frac{{V_{\mathrm{in}}}^3 D^3}{3V_{C_r}{L_m}^2 f^2}}. \end{aligned} \tag{10}$$

Similarly, when V_{C_r} is higher than V_t and S_1 is just turned OFF, a current flows through D_1. The current stress of D_1 is

$$I_{D_1\_\text{rms}} = \frac{n_2}{n_1}\sqrt{\frac{1}{T_s}\int_0^{\frac{DV_{\text{in}}T_s}{V_t}}\left(\frac{DV_{\text{in}}T_s}{L_m} - t\frac{V_t}{L_m}\right)^2 dt} = \frac{n_2}{n_1}\sqrt{\frac{{V_{\text{in}}}^3 D^3}{3V_t{L_m}^2 f^2}}. \tag{11}$$

Since S_2 is only turned ON during the pulse rising process and it is a relatively short process compared to the steady current modes, the maximum value of the S_2 current is a more meaningful metric compared to its root-mean-square (rms) value. Therefore, the current stress of S_2 is determined as

$$I_{S_2\_\text{peak}} = I_P. \tag{12}$$

Similarly, D_5 is only turned ON during the pulse falling process and its current stress is determined as

$$I_{D_5\_\text{peak}} = I_P. \tag{13}$$

The current stress of D_6 is determined as follows. During the pulse falling process, C_f absorbs energy from L_o and the change of V_{C_f} can be written as

$$\Delta V_{C_f} = \frac{L_o(I_P^2 - I_C^2)}{2C_f V_{C_f}}. \tag{14}$$

As for D_6, it is turned ON when $V_{C_f} > V_{C_r} - V_{\text{SC}}$. Assuming that V_{C_r} is constant, the instantaneous v_{C_f} can be determined by solving

$$L_b C_r {V_{C_f}}'' + v_{C_f} = V_{C_r}. \tag{15}$$

In fact,

$$v_{C_f} = \Delta V_{C_f}\cos\frac{t}{\sqrt{L_b C_f}} + V_{C_r}. \tag{16}$$

Therefore, the current through D_6 and L_b can be written as

$$i_{D_6} = i_{L_b} = C_f\frac{\mathrm{d}v_{C_f}}{\mathrm{d}t} = \Delta V_{C_f}\sqrt{\frac{C_r}{L_b}}\sin\frac{t}{\sqrt{L_b C_f}}. \tag{17}$$

By integrating (17) over one pulse period, the current stress of D_6 is determined as

$$I_{D_6\_\text{rms}} = \sqrt{\frac{1}{T_P}\int_0^{\frac{\pi\sqrt{L_b C_f}}{2}}\left(\Delta V_{C_f}\sqrt{\frac{C_r}{L_b}}\sin\frac{t}{\sqrt{L_b C_f}}\right)^2 dt} = \frac{\Delta V_{C_f}^2 {C_f}^{\frac{3}{2}}}{4T_P(L_b)^{\frac{1}{2}}} \tag{18}$$

where T_P is the period of the pulse current.

IV. Design Considerations

To design, implement, and test a prototype for the proposed charger, a supercapacitor module is built by connecting four 3 V/6 F supercapacitor cells in series. The supercapacitor cell (manufacturer: Eaton, part number: TV1020-3R0605-R) can sustain a continuous current of 2.4 A and a pulse current of 7.4 A [40]. While the supercapacitor cell can be charged or discharged by a continuous current of 2.4 A for a long time, it can only be charged or discharged by a pulse current of 7.4 A for a limited period of time to ensure that its temperature rise is under control. Therefore, instead of setting the pulse current as 7.4 A during the prototype design, implementation, and test processes, a 7.1 A pulse current is utilized, which means that a 0.3 A margin is introduced. As for the continuous current, it is set as 2.4 A without introducing a margin. The rated voltage and capacitance of the supercapacitor module are 12 V and 1.5 F, respectively. The supercapacitor module is charged from the initial voltage of $V_i = 4$ V to the final voltage of $V_e = 8$ V. The output branch resistance, including the resistances of L_o, S_3, and the supercapacitor module, is denoted as R_{on}. The key parameters of the prototype are designed as follows, which are also listed in Table I.

TABLE I
Prototype Parameters

Parameters/Components	Symbols	Values
Input voltage	V_{in}	80 V
High voltage	V_t	200 V
Transformer	$n_1 : n_2 : n_3 : n_4$	40:16:10:40
Magnetizing inductor	L_m	0.64 mH
Resonant inductor	L_b	3.3 mH
Output inductor	L_o	168 μH
Switching frequency	f	100 kHz
Energy storage capacitor	C_r	4.7 μF
Energy storage capacitor	C_f	2.2 μF
Diode forward voltage	V_D	1.1 V
Output branch resistance	R_{on}	200 mΩ
Switches 1 and 2	$S_{1,2}$	NVBG160N120SC1
Switch 3	S_3	CI90N120SM
Diodes 1, 2, and 6	$D_{1,2,6}$	S8NC-13
Diodes 3, 4, and 5	$D_{3,4,5}$	SDUR30Q60

A. Transformer

For the transformer, the turns ratio n_4/n_2 is first determined as

$$\frac{n_4}{n_2} = \frac{V_t}{V_{\text{in}}}. \tag{19}$$

A higher V_t means a faster dynamic response and a higher voltage stress at the same time, which is finalized as 200 V.

Then, to ensure the volt–second balance for L_m, the maximum duty cycle is calculated as

$$D_{\text{lim}} = \frac{V_t n_4}{V_{\text{in}}n_1 + V_t n_4}. \tag{20}$$

To extend the duty cycle range, $n_1 = n_4$.

Finally, to ensure that the supercapacitor module can be charged within the specified voltage range between V_i and V_e, the turns ratio n_1/n_3 is determined as

$$\frac{n_1}{n_3} = N = \frac{V_{\text{in}}D_{\text{lim}}}{V_e + V_D + I_P R_{\text{on}}}. \tag{21}$$

B. Output Inductor

The duty cycle of S_1 can be found as

$$D = \frac{N(V_{\text{SC}} + V_D + I_o R_{\text{on}})}{V_{\text{in}}} \tag{22}$$

where I_o is the output current. Since the prototype works in the steady current modes most of the time, the output current should remain almost constant. Specifically, its ripple Δi_o is designed to be less than 17% of the output current. When the supercapacitor module is charged to V_e with I_C, the current ripple reaches the maximum value. Therefore, the requirement for the output inductor is

$$L_o > \frac{D(V_{\text{in}}N - V_D - I_C R_{\text{on}} - V_{\text{SC}})}{2\Delta i_o f}. \tag{23}$$

C. Energy Storage Capacitors

For the energy storage capacitor C_r, its voltage should remain almost constant during the pulse rising process. Assuming that its voltage drop is within 2% of V_t, C_r is sized as

$$C_r > \frac{L_o({I_P}^2 - {I_C}^2)}{({V_t}^2 - 0.9604{V_t}^2)}. \tag{24}$$

Similarly, the voltage of the energy storage capacitor C_f should remain almost constant during the pulse falling process. Assuming that its voltage rise is within 3% of V_t, C_f is sized as

$$C_f > \frac{L_o({I_P}^2 - {I_C}^2)}{({V_t}^2 - 0.9409{V_t}^2)}. \tag{25}$$

D. Resonant Inductor

To size L_b, it is assumed that during a pulse period, the energy stored in C_f during the pulse falling process can be transferred to C_r. According to (17), L_b is sized as

$$L_b < \frac{T_P}{\pi C_f}. \tag{26}$$

E. Magnetizing Inductor

For the pulse rising process, assuming that V_{C_r} remains constant, the energy provided by C_r can be written as

$$E_p = \frac{({I_P}^2 - {I_C}^2)V_t L_o}{2(V_t - V_{\text{SC}})}. \tag{27}$$

Similarly, for the pulse falling process, assuming that V_{C_f} remains constant, the energy absorbed by C_f can be written as

$$E_a = \frac{({I_P}^2 - {I_C}^2)(V_t - V_{\text{SC}})L_o}{2V_t}. \tag{28}$$

Clearly, E_a is less than E_p. To maintain the voltage of C_r, for every pulse period, the energy transferred from L_m to C_r should be greater than $E_p - E_a$. To determine L_m, it is required that the C_r voltage can still be maintained at V_t when the output current is I_C at V_i and D takes the minimum value of D_{min}:

$$L_m < \frac{V_{\text{in}}^2 D_{\text{min}}^2}{2f f_P(E_p - E_a)} \tag{29}$$

where f_P is the frequency of the pulse current and $f_P = 1/T_P$.

F. Loss Analysis

This section analyzes the losses of the proposed charger, which mainly include the diode losses, switch losses, transformer losses, and conduction losses.

The diode losses are mainly contributed by D_3 and D_4. During the charging process, the forward voltages of D_3 and D_4 share voltage with the supercapacitor module. The total loss associated with D_3 and D_4 is

$$P_{\text{loss\_diode}} = [D_{\text{pulse}} I_P + (1 - D_{\text{pulse}})I_C]V_D \tag{30}$$

where D_{pulse} is the duty cycle of the pulse current, which is the ratio of the pulse width to the pulse period. As for D_1, D_2, D_5, and D_6, their forward voltages are relatively low compared to the other components (e.g., C_r and C_f) in their conduction loops. Therefore, their losses are ignored.

To analyze the switch losses, S_1 is taken as an example. The turn-ON switching loss E_{on} and the turn-OFF switching loss E_{off} can be obtained under specific test conditions. However, these values need to be corrected to estimate the actual switching losses. For E_{on}, the correction factor is $I_{S_{1\_\text{on}}} V_{\text{in}}/(V_{DS} I_{DS})$, where $I_{S_{1\_\text{on}}}$ is the current of S_1 after S_1 is just turned ON and its value is I_o/N. V_{DS} and I_{DS} are two parameters of S_1. For E_{off}, the correction factor is $I_{S_{1\_\text{off}}} V_t/(V_{DS} I_{DS})$, where $I_{S_{1\_\text{off}}}$ is the current of S_1 after S_1 is just turned OFF and its value is $I_o/N + V_{\text{in}} D T_s/L_m$. Consequently, for S_1, the total switching loss per switching cycle is

$$E_{\text{sw\_}S_1} = E_{\text{on}} \frac{\left(\frac{I_o}{N}\right) V_{\text{in}}}{V_{DS} I_{DS}} + E_{\text{off}} \frac{\left(\frac{I_o}{N} + \frac{V_{\text{in}} D T_s}{L_m}\right) V_t}{V_{DS} I_{DS}}. \tag{31}$$

Similarly, the total switching losses per switching cycle for S_2 and S_3 can be determined as $E_{\text{sw\_}S_2}$ and $E_{\text{sw\_}S_3}$, respectively. Therefore, for all the three switches, the total switching loss is

$$P_{\text{loss\_sw}} = f E_{\text{sw\_}S_1} + f_P(E_{\text{sw\_}S_2} + E_{\text{sw\_}S_3}). \tag{32}$$

The transformer losses include the core loss and the copper loss. Specifically, the core loss [42] can be expressed as

$$P_{\text{core}} = K_{fe} \left(\mu \frac{n_1 V_{\text{in}} D}{f L_m l_m}\right)^{\beta} A_c l_m \tag{33}$$

where l_m, β, and A_c are the transformer parameters while K_{fe} and μ are constants. The copper loss is associated with the winding resistance. When the charger works stably, the energy transferred from L_m to C_r through W_4 is minimal, which means that the current through W_4 is also low. Therefore, the copper loss associated with W_4 can be ignored. The copper loss of the transformer is mainly contributed by the other three windings:

$$P_{\text{copper}} = R_{W1}\left(\frac{V_{\text{in}}^2 D^3}{3{L_m}^2 f^2} + \frac{V_{\text{in}} {I_o}^2 D^2}{N L_m f} + \frac{{I_o}^2 D}{N^2}\right) + R_{W2}\left(\frac{{n_2}^2}{{n_1}^2} \frac{{V_{\text{in}}}^3 D^3}{3 V_t {L_m}^2 f^2}\right) + R_{W3} D {I_o}^2 \tag{34}$$

where R_{W1}, R_{W2}, and R_{W3} are the resistances of the W_1, W_2, and W_3 windings, respectively. Note that the currents of W_1,

W_2, and W_3 are equal to the currents of S_1 in (9), D_1 in (11), and D_3 in (7) when I_P is replaced by the output current I_o, respectively.

The conduction losses are analyzed as follows. Since S_2 is only turned ON during the pulse rising process and this is a relatively short process, the conduction loss during this process can be ignored. On the other hand, the current through L_b is small and this conduction loss is also ignored. In fact, the conduction losses are mainly associated with S_1 and the output loop:

$$P_{\text{loss\_con}} = R_{S_1}\left(\frac{V_{\text{in}}^2 D^3}{3{L_m}^2 f^2} + \frac{V_{\text{in}} I_o D^2}{N L_m f} + \frac{{I_o}^2 D}{N^2}\right) + R_{\text{on}}{I_o}^2 \tag{35}$$

where R_{S_1} is the drain–source ON-state resistance of S_1.

Compared to the conventional forward converter, the proposed charger experiences more losses such as the switching losses of S_2 and S_3 as well as the forward conduction losses of D_2 and D_5. However, such losses are not major contributors to the total loss of the proposed charger. Therefore, the total loss of the proposed charger can be assumed to be at the same level as the conventional forward converter.

G. Component Selection

The key components of the prototype are selected as follows. For all the three switches especially S_1 and S_2, the turn-ON and turn-OFF times need to be short for fast switching. As listed in Table I, S_1 and S_2 are implemented using an SiC MOSFET NVBG160N120SC1 [45] with a turn-ON time of 11 ns and a turn-OFF time of 15 ns. Since S_3 is turned ON most of the time and included in the output loop, an SiC MOSFET CI90N120SM [46] with a low drain–source ON-state resistance of 27 mΩ is selected to improve the charger efficiency.

To implement the transformer, an EC2834 core is selected. The numbers of turns for the W_1, W_2, W_3, and W_4 windings are 40, 16, 10, and 40, respectively. For L_m, L_o, and L_b, their inductances are finalized as 0.64 mH, 168 μH, and 3.3 mH, respectively.

For the two energy storage capacitors C_r and C_f, polypropylene film capacitors of 4.7 and 2.2 μF are selected because of their low equivalent series resistances (ESRs) and good pulse characteristics.

H. Control Scheme

The control scheme of the proposed charger is shown in Fig. 8. To simply the control process, only the voltage of the supercapacitor module is sampled. Once the sampled voltage V_{fd} is greater than the preset threshold, the pulse width modulation (PWM) signal is set to zero and the charging process is terminated. In the meantime, the duty cycle of S_1 is also controlled based on V_{fd}.

For S_2 and S_3, they are not controlled by sampling the current because the pulse rising and falling processes are fast. Instead, they are controlled based on the pulse rising and falling times,

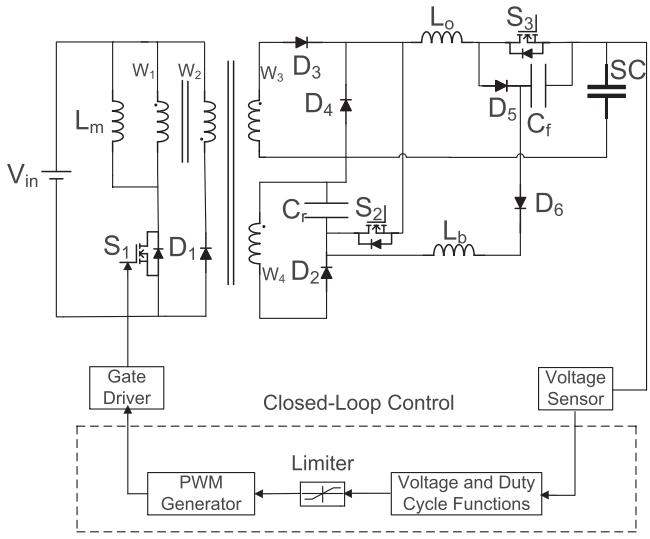


Fig. 8. Control scheme of proposed charger.

which can be written as

$$t_r = \frac{(I_P - I_C)L_o}{V_{C_r} - V_{\text{SC}}} \tag{36}$$

$$t_f = \frac{(I_P - I_C)L_o}{V_{C_f} + V_{\text{SC}} + V_{D_4} + V_{D_5}}. \tag{37}$$

Specifically, S_2 is turned ON during a period of time equal to the pulse rising time t_r and then turned OFF. On the other hand, S_3 is turned OFF during a period of time equal to the pulse falling time t_f and then turned ON. Moreover, to ensure that the transitions between the steady current modes and the pulse rising/falling modes are safe, a 1 μs dead time is added.

The stability of the proposed charger is analyzed as follows. For the steady current modes, the small signal equations can be written as

$$\begin{cases} L_o \frac{\mathrm{d}\hat{i}_{L_o}}{\mathrm{d}t} = \frac{V_{\text{in}}}{N}\hat{d} - \hat{v}_{\text{SC}} - \hat{i}_{L_o} R_{\text{esr}} \\ C_{\text{SC}} \frac{\mathrm{d}\hat{v}_{\text{sc}}}{\mathrm{d}t} = \hat{i}_{L_o} \end{cases} \tag{38}$$

where $\hat{d}$ is the duty cycle of S_1, R_{esr} is the ESR of the supercapacitor module, and C_{SC} is the capacitance of the supercapacitor module. The transfer function from the duty cycle of S_1 to the output current is determined as

$$G_{id}(s) = \frac{\hat{i}_{L_o}(s)}{\hat{d}(s)} = \frac{s\frac{V_{\text{in}}}{N}C_{\text{SC}}}{s^2 L_o C_{\text{SC}} + s R_{\text{esr}} C_{\text{SC}} + 1}. \tag{39}$$

The Bode plot of the transfer function is shown in Fig. 9. Since the phase margin is 90°, the charger is stable.

V. Experimental Setup and Results

A. Experimental Setup

The proposed charger is evaluated using the experimental setup shown in Fig. 10. Specifically, the front and back views of the prototype are shown in Figs. 10(a) and 10(b), respectively. The test setup is illustrated in Fig. 10(c). As elaborated in Section IV, the supercapacitor module is built by connecting

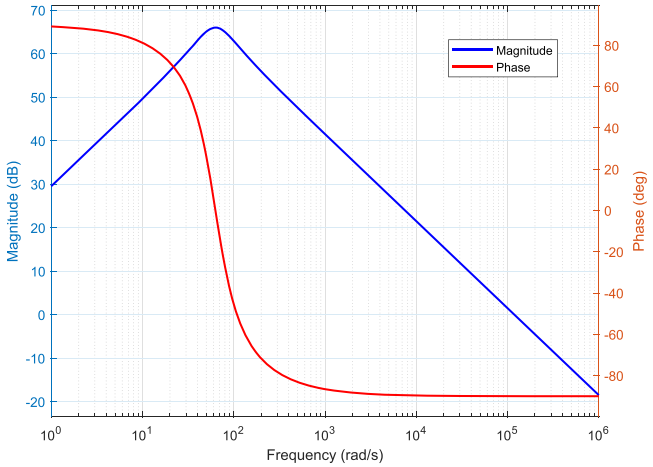


Fig. 9. Bode plot of transfer function.

four 3 V/6 F supercapacitor cells in series. The continuous and pulse currents are set as 2.4 and 7.1 A, respectively. The pulse width and period are set as 0.25 and 2.5 ms, respectively.

B. Dual-Mode Operation

The dual-mode operation of the proposed charger is demonstrated in this section. The supercapacitor module is charged from the initial voltage of $V_i = 4$ V to the final voltage of $V_e = 8$ V. Note that the rated and surge voltages of the supercapacitor cell are 3 and 3.3 V, respectively. Consequently, the rated and surge voltages of the supercapacitor module are 12 and 13.2 V, respectively. To demonstrate the dual-mode operation of the proposed charger, the middle part (i.e., between 4 and 8 V) of the operating voltage range of the supercapacitor module is utilized. In real-world applications, to avoid overcharging the supercapacitor module, the pulse current mode can be simply disabled when the voltage is approaching the upper bound.

The experimental results are shown in Fig. 11. In particular, the supercapacitor module voltage $V_{\rm SC}$ and the corresponding charging current i_{L_o} are illustrated in Fig. 11(a). When the charging current is active, the supercapacitor module voltage increases. The charging process continues until the sampled voltage reaches a specific threshold determined in the following manner. The maximum ESR of the supercapacitor cell is 35 mΩ [40], which suggests that the maximum ESR of the supercapacitor module is 140 mΩ. When the pulse current of 7.1 A is considered, the maximum instantaneous voltage change due to the ESR is approximately 1 V. Therefore, when the final voltage of the supercapacitor module is set as 8 V, the charging process can be terminated if the sampled voltage reaches approximately 9 V. For the experiment shown in Fig. 11(a), the charging process is terminated when the sampled voltage reaches 8.9 V. The charging time corresponding to this termination voltage is approximately 1.68 s.

To more clearly observe the dual-mode operation, Fig. 11(b) shows a zoomed-in view of Fig. 11(a). Both the continuous and pulse currents are generated properly. The current ripples are 0.33 A at 2.4 A and 0.36 A at 7.1 A, respectively. The pulse characteristics are listed in Table II. Specifically, the pulse rising and falling times are 4.4 and 4.2 μs, respectively. The pulse duration is approximately 0.24 ms.

TABLE II
PULSE CHARACTERISTICS OF PROPOSED CHARGER AND FORWARD CONVERTER

	Proposed Charger	Forward Converter
Rising time	4.4 μs	150 μs
Falling time	4.2 μs	100 μs
Peak current	7.1 A	6.4 A
Duration of peak current	0.24 ms	Not applicable

To illustrate the benefits of the dual-mode operation, a comparative study is performed. Specifically, the pulse current mode is disabled and the prototype is configured to operate in the continuous current mode only. To implement this configuration, S_2 is turned OFF and S_3 is turned ON. The experimental results are shown in Fig. 12. The supercapacitor module is charged from 4 to 8 V in 2.04 s using only a continuous current of 2.4 A with a ripple of 0.33 A. If 2.04 s is set as the baseline, the charging time is reduced by approximately 17.6% to 1.68 s when the prototype operates in the dual-mode. Therefore, the charging process is indeed accelerated by employing both the continuous and pulse current modes.

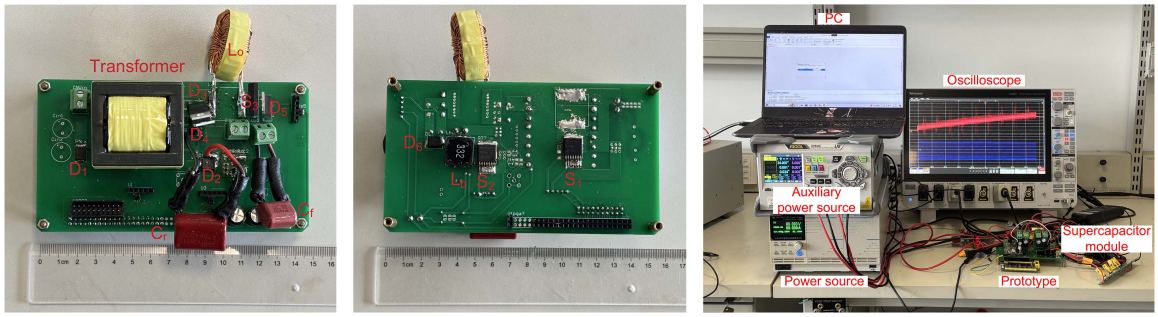
Since the proposed charger is derived based on the conventional forward converter, another comparative study is performed to further demonstrate its features. Again, S_2 is turned OFF and S_3 is turned ON to configure the prototype to operate as a forward converter. The charging current is illustrated in Fig. 13. Note that within the pulse width of 0.25 ms, the pulse fails to reach the preset peak value of 7.1 A. As a matter of fact, the peak value of the current is only 6.4 A. The pulse rising and falling times associated with this peak value are 150 and 100 μs, respectively. The duration of the pulse current cannot be determined in this case because the predefined peak value of the pulse current is never reached. The pulse characteristics of this configuration are listed in the "Forward Converter" column in Table II.

In summary, this section demonstrates the dual-mode operation of the proposed charger, its benefits in reducing the charging time by introducing the pulse current mode, and its enhanced pulse characteristics in terms of much shorter pulse rising and falling times compared to the conventional forward converter.

C. Pulse Rising Process

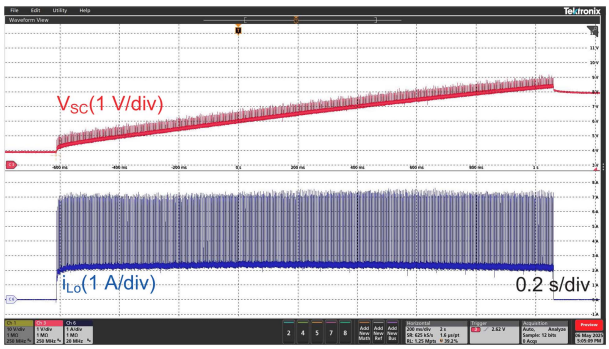
This section elaborates on the pulse rising process of the proposed charger. An overview of such a process is shown in Fig. 14(a), which includes the waveforms of V_{C_r}, V_{C_f}, $V_{\rm SC}$, i_{L_o}, i_{L_b}, and $i_{\rm SC}$. In fact, i_{L_b} is close to zero and $i_{\rm SC}$ is approximately equal to i_{L_o}. In the meantime, V_{C_f} remains almost constant.

In particular, V_{C_r} and i_{L_o} are shown in Fig. 14(b). Before i_{L_o} rises, C_r has established a high voltage of 202 V, which is close to V_t of 200 V. As shown in the circled areas, i_{L_o} ramps up quickly from 2.5 to 7.1 A within 4.4 μs. Therefore, a sharp pulse rising edge is generated. During this process, V_{C_r} only drops by 5 V because C_r is large. Moreover, Fig. 14(c) shows the voltage

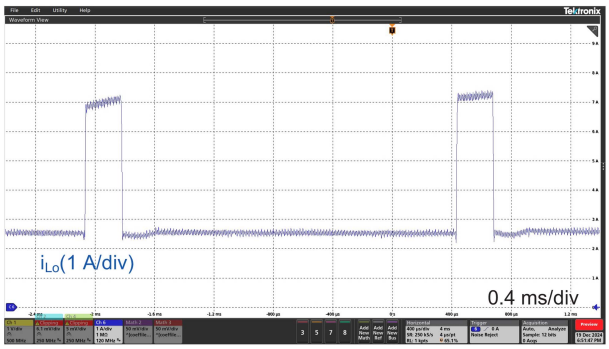


(a) (b) (c)

Fig. 10. Experimental setup. (a) Charger prototype: front view. (b) Charger prototype: back view. (c) Test setup.



(a)



(b)

Fig. 11. Proposed charger: dual-mode operation. (a) Supercapacitor module voltage and charging current during charging process. (b) Continuous and pulse currents.

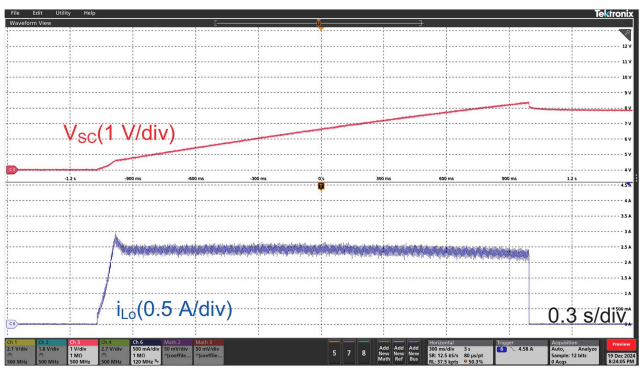


Fig. 12. Proposed charger: continuous current mode operation.

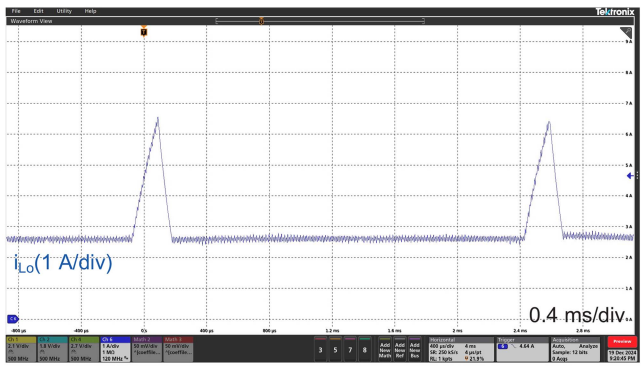


Fig. 13. Forward converter: continuous and pulse currents.

across L_o during this process, which is also high. For instance, V_{L_o} is 192 V in the circled area.

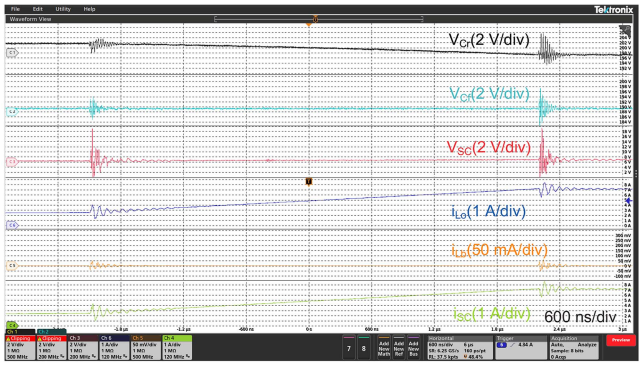
For comparison, Fig. 15 shows V_{L_o} for the forward converter, which is only 13 V. Correspondingly, the current ramps up much more slowly in this case. In summary, this section illustrates the pulse rising process of the proposed charger and shows the significant difference between the proposed charger and the forward converter in terms of the pulse current ramping-up rate.

D. Pulse Falling Process

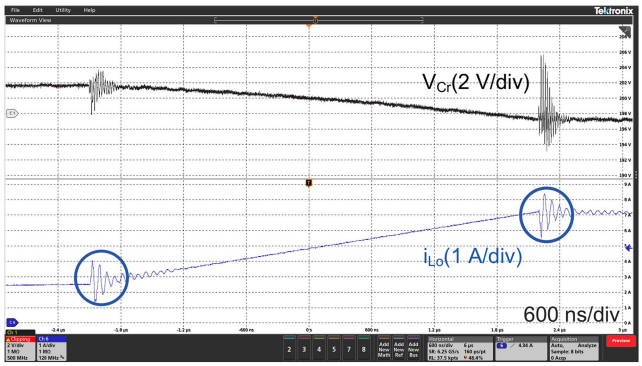
For the pulse falling process, an overview is shown in Fig. 16(a). Again, i_{L_o} and i_{SC} are approximately equal because i_{L_b} is almost zero. In this case, V_{C_r} remains almost constant. Fig. 16(b) shows V_{C_f} and i_{L_o}. As indicated in the circled areas, i_{L_o} drops quickly from 7 to 2.4 A within 4.2 μs, which leads to a sharp pulse falling edge. In the meantime, V_{C_f} increases from 188 to 197 V and enables a fast transition from the pulse current mode to the continuous current mode. Moreover, Fig. 16(c) shows that V_{L_o} is -180 V in the circled area. On the other hand, Fig. 17 shows that V_{L_o} is only -5.6 V for the forward converter. Once again, this section demonstrates the impressive pulse characteristics of the proposed charger in terms of the fast pulse falling process compared to the forward converter.

E. Energy Recycling

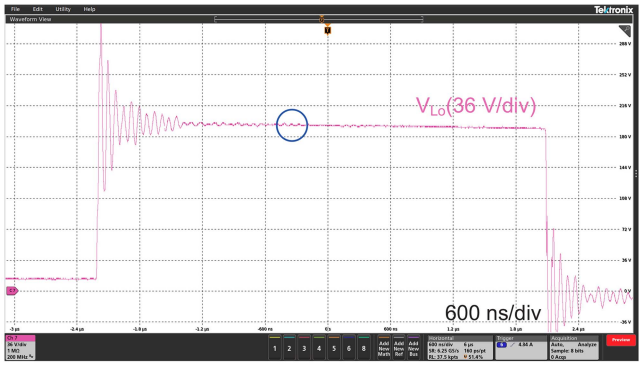
This section illustrates the energy recycling process. First, as analyzed in Section II-C, if $V_{C_f} > V_{C_r} - V_{\mathrm{SC}}$, D_6 is turned



(a)



(b)



(c)

Fig. 14. Proposed charger: pulse rising process. (a) Overview. (b) Voltage across C_r and current through L_o. (c) Voltage across L_o.

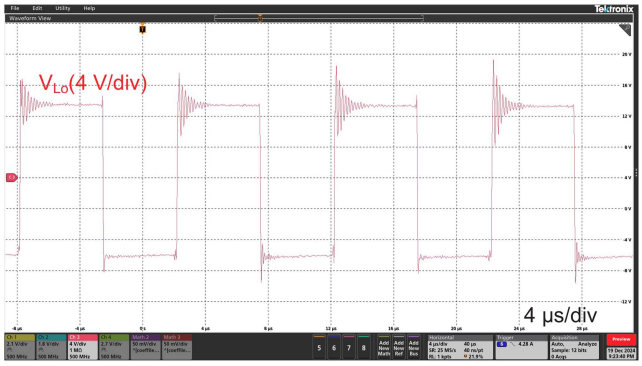
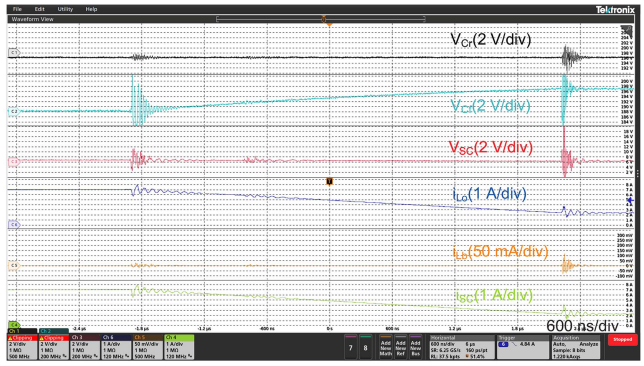
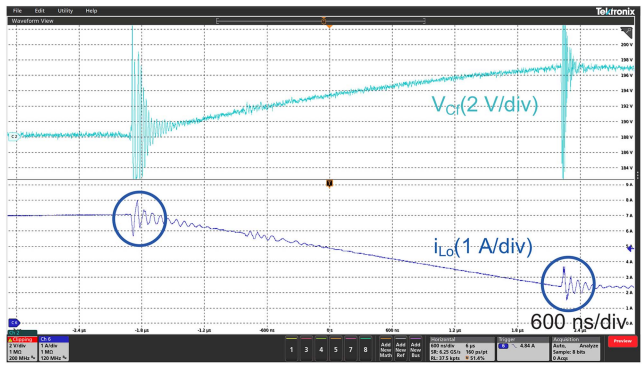


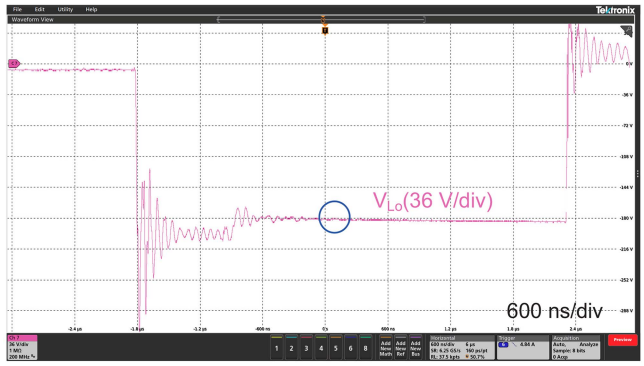
Fig. 15. Forward converter: voltage across L_o during pulse rising process.



(a)



(b)



(c)

Fig. 16. Proposed charger: pulse falling process. (a) Overview. (b) Voltage across C_f and current through L_o. (c) Voltage across L_o.

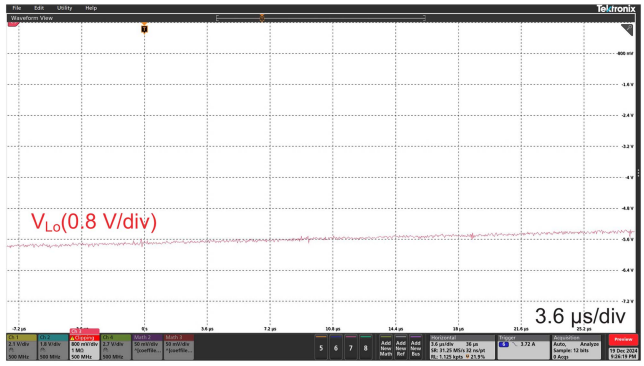


Fig. 17. Forward converter: voltage across L_o during pulse falling process.

TABLE III
COMPARISON OF PROPOSED CHARGER WITH OTHER CONVERTERS

Topologies	Number of Switches	Number of Diodes	Number of Transformers	Voltage Stress	Efficiency	Dynamic Response	Charging Speed
Proposed charger	3	6	1	High	Medium	Fast	Fast
[44]	3	4	1	High	Low	Fast	Fast
Buck	1	1	0	Medium	Medium	Medium	Medium
Full-bridge	4	4	1	Low	Medium	Medium	Medium
Half-bridge	2	2	1	Medium	Medium	Medium	Medium
[47]	4	10	1	Low	Medium	Medium	Medium
[48]	1	2	0	High	High	Medium	Medium
[49]	2	0	0	Medium	Medium	Medium	Medium
[50]	8	0	0	Medium	Medium	Medium	Medium

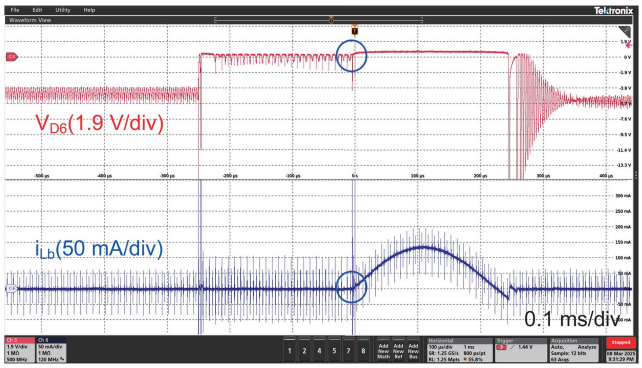


Fig. 18. Proposed charger: energy recycling.

ON. Energy is transferred from C_f to C_r through D_6 and L_b to achieve energy recycling. Fig. 18 shows such a process. Specifically, D_6 is turned ON, as indicated in the circled area. In the meantime, a sinusoidal current flows through L_b, as suggested by (17). The amplitude of i_{L_b} is 0.13 A. Compared to i_{L_o} with the preset values of 2.4 A for the continuous current and 7.1 A for the pulse current, i_{L_b} is indeed a small current. Therefore, i_{SC} is approximately equal to i_{L_o}, which is consistent with the analysis elaborated in Section II-C.

F. Effects of Pulse Period on Charging Time

In Sections V-A–V-E, the pulse width and period are set as 0.25 and 2.5 ms, respectively, which are selected arbitrarily to illustrate the operation of the proposed charger. In fact, to exploit the pulse current mode to minimize the charging time, a rigorous study needs to be conducted to optimize the pulse width and period while properly addressing the thermal management issues of the charger and the supercapacitor module. As a first attempt, a comparative experiment is performed in which the pulse width is still set as 0.25 ms while the pulse period is changed to 5 ms. Intuitively, the charging time is extended, which is indeed the case. As shown in Fig. 19, it takes the prototype 1.78 s to charge the supercapacitor module from 4 to 8 V. Clearly, the charging time is longer compared to 1.68 s when the pulse period is set as 2.5 ms. Still, this charging time is shorter compared to 2.04 s when the prototype is configured to operate in the continuous current mode only.

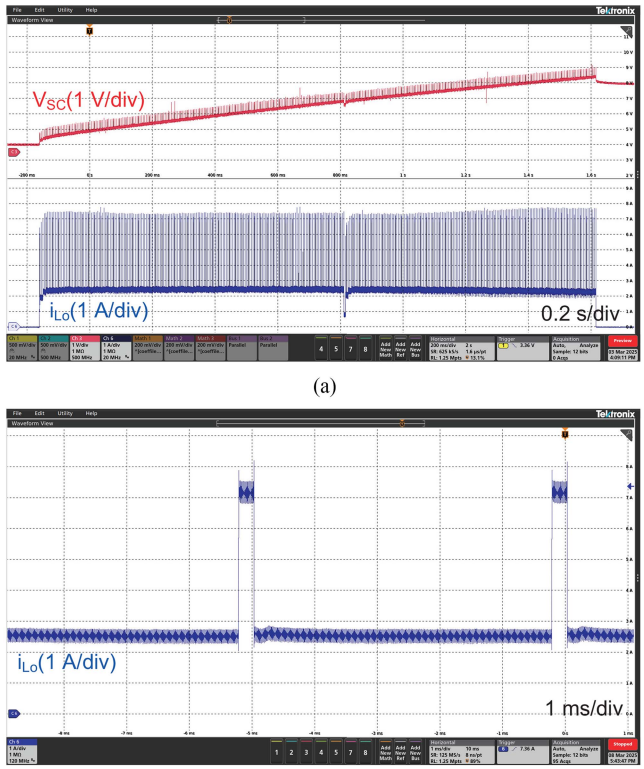


Fig. 19. Proposed charger: effects of pulse period on charging time. (a) Supercapacitor module voltage and charging current during charging process. (b) Continuous and pulse currents.

VI. EVALUATION OF PROPOSED CHARGER

A more comprehensive evaluation of the proposed charger against other converters is listed in Table III. The charging speed of the proposed charger is faster than those of various conventional converters, such as the buck, full-bridge, and half-bridge converters, as well as those proposed for specific applications [47], [48], [49], [50]. Compared to the dual-mode fast charger proposed in [44], the charger proposed in this article shows a faster dynamic response in terms of a shorter pulse falling time and a higher efficiency at the cost of a higher hardware complexity as it utilizes more diodes and transformer windings, as elaborated below.

A. Dynamic Response

Compared to the charger proposed in [44], the charger proposed in this article leads to a faster dynamic response when it comes to the pulse falling process. The pulse falling times of the proposed charger and the charger proposed in [44] are compared as follows. For the proposed charger, the pulse falling time can be calculated using (37), which can be illustrated using the setup elaborated in Sections V-A and V-B. The pulse and continuous currents are set as $I_P = 7.1$ and $I_C = 2.4$ A, respectively. Table I lists the following parameters: $L_o = 168$ μH and $V_{D_4} = V_{D_5} = 1.1$ V. Referring to Section II-C, $V_{C_f} + V_{\rm SC}$ is approximately equal to V_t, which is set as 200 V. Therefore, t_f is calculated as 3.9 μs, which is close to the experimental result of 4.2 μs elaborated in Section V-D. For the charger proposed in [44], the pulse falling time is determined as

$$t_f = \frac{L_o}{R_f} \ln\left(\frac{I_P}{I_C}\right). \tag{40}$$

For a fair comparison, the voltage stresses of S_3 are assumed to be equal in the two chargers to determine R_f. As mentioned in Section III, the voltage stress of S_3 is V_t for the charger proposed in this article. In [44], the voltage stress of S_3 is $I_P R_f$. Therefore, $R_f = V_t/I_P = 28.17\ \Omega$. Consequently, t_f is determined as 6.5 μs using (40). Clearly, the charger proposed in this article results in a shorter pulse falling time compared to the charger proposed in [44]: 3.9 versus 6.5 μs. This is because the charger proposed in this article introduces an energy storage capacitor [i.e., C_f in Fig. 1(b)] to establish a relatively high voltage to accelerate the pulse falling process, while the charger proposed in [44] utilizes a branch resistor [i.e., R_f in Fig. 1(a)] instead.

The pulse rising time is considered as well. For the proposed charger, the pulse rising time corresponding to the setup elaborated in Sections V-A and V-B is determined using (36). Specifically, $V_{C_r} = V_t = 200$ V and $V_{\rm SC} = V_e = 8$ V. Therefore, t_r is calculated as 4.1 μs, which is close to the experimental result of 4.4 μs elaborated in Section V-C. For the charger proposed in [44], the pulse rising time is determined as

$$t_r = \frac{(I_P - I_C)L_o}{V_Z - V_{\rm SC}}. \tag{41}$$

Again, for a fair comparison, the voltage stresses of S_2 are assumed to be equal in the two chargers, which means that $V_Z = V_t = 200$ V. Therefore, (41) also leads to a pulse rising time of 4.1 μs. The pulse rising processes are equally fast in the two chargers because they both adopt an energy storage capacitor [i.e., C_r in Fig. 1(b) and C_s in Fig. 1(a)] to establish a relatively high voltage.

B. Efficiency

The efficiency of the proposed charger is swept when the load voltage varies from 4 to 8 V. An electronic load instead of the supercapacitor module is used in this sweep. The continuous and pulse currents are set as 2.4 and 7.1 A, respectively. The pulse width and period are set as 0.25 and 2.5 ms, respectively. The efficiency is calculated as the ratio of the power received by the electronic load to the power delivered by the power source. For instance, Table IV shows that when the load voltage is 8 V, the load power is 21.46 W and the source power is 31.15 W. The efficiency is then determined as $21.46/31.15 * 100\% = 68.9\%$. In general, Fig. 20 shows that the efficiency of the proposed charger increases from 62.9% to 68.9% when the load voltage increases from 4 to 8 V. On the other hand, the charger proposed in [44] shows an efficiency around 40% when the load voltage varies from 2 to 2.9 V. While it is unfair to perform a side-by-side comparison of the efficiencies of these two chargers as their load voltages significantly differ, it is beneficial to analyze the losses of various components to reveal the differences between these two chargers. Therefore, Table IV lists the component losses of the charger proposed in this article when the load voltage is 8 V and the charger proposed in [44] when the load voltage is 2.9 V.

TABLE IV
COMPONENT LOSSES OF TWO CHARGERS

	Proposed Charger		[44]	
	Power (W)	Percentage (%)	Power (W)	Percentage (%)
Source Power	31.15	100.0	21.00	100.0
Load Power	21.46	68.9	8.42	40.1
Diodes' Loss	3.16	10.1	3.16	15.0
Conduction Loss	2.19	7.0	0.66	3.1
Branch Resistor Loss	–	–	0.89	4.2
Zener Diode Loss	–	–	6.65	31.7
Other Loss	4.34	14.0	1.22	5.9

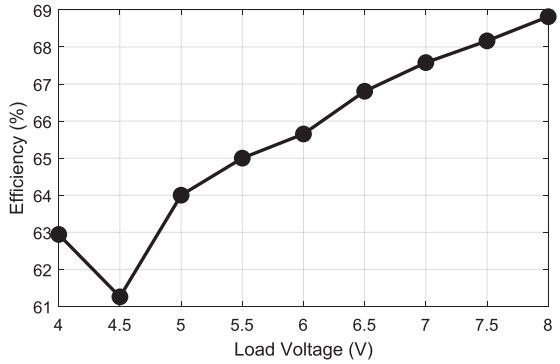


Fig. 20. Proposed charger: efficiency versus load voltage.

For the proposed charger, the loss of the diodes and the conduction loss are calculated as follows. As elaborated in Section IV-F, the loss of the diodes can be calculated using (30). When the duty cycle of the pulse current is $D_{\rm pulse} = 0.25/2.5 = 0.1$, the loss of the diodes is determined as 3.16 W, which is 10.1% of the source power. To determine the conduction loss, the continuous current and the pulse current are considered separately first. Specifically, when the output current is set as the continuous current (i.e., $I_o = I_C = 2.4$ A), the duty cycle of S_1 is calculated as $D_{I_C} = 0.479$ using (22) with $N = n_1/n_3 = 4$ and $V_{\rm SC} = V_e = 8$ V. Consequently, the conduction loss associated with the continuous current is determined as $P_{I_C} = 1.25$ W using (35) with $R_{S_1} = 239$ mΩ [45]. Similarly, when the output current is set as the pulse current (i.e., $I_o = I_P = 7.1$ A), the duty cycle of S_1 is calculated as $D_{I_P} = 0.526$ and the corresponding conduction loss is determined as $P_{I_P} = 10.64$ W. Finally, the total conduction loss is

determined as $D_{\text{pulse}}P_{I_P} + (1 - D_{\text{pulse}})P_{I_C} = 2.19$ W, which is 7.0% of the source power. The losses associated with other components, such as the transformer, are aggregated as a single item, which is determined by deducting the load power, the loss of the diodes, and the conduction loss from the source power. As listed in Table IV, this item is 4.34 W, or 14.0% of the source power.

For the charger proposed in [44], the component losses are also calculated. For instance, the loss of the diodes is also determined as 3.16 W because the same model of diodes with the same V_D is adopted. Note that the branch resistor loss and the Zener diode loss total 35.9% of the source power. By removing these two components and introducing energy recycling, the efficiency of the charger proposed in this article is improved compared to the charger proposed in [44].

In summary, although the hardware complexity of the charger proposed in this article is higher, it shows a faster dynamic response in terms of a shorter pulse falling time and a higher efficiency compared to the charger proposed in [44].

VII. Conclusion

This article proposes a dual-mode fast charger for supercapacitors that utilizes both continuous and fine-tuned pulse currents. The proposed charger is derived from the conventional forward converter. By introducing two energy storage capacitors, the rising and falling edges of the pulse current are significantly sharpened. Specifically, the energy storage capacitor C_r is charged through the transformer winding W_4 to build a high voltage, which is then applied to the output inductor L_o to generate a sharp pulse rising edge. On the other hand, the high voltage established on the energy storage capacitor C_f is utilized to sharpen the pulse falling edge. Therefore, the transitions between the continuous and pulse current modes are significantly accelerated, which ultimately shortens the charging time.

A prototype of the proposed charger is designed, implemented, and tested. To charge a 12 V/1.5 F supercapacitor module from 4 to 8 V, it takes the prototype 1.68 and 2.04 s when it is configured to operate in the dual-mode and the continuous current mode, respectively, which leads to a 17.6% reduction in the charging time. Moreover, the pulse characteristics of the proposed charger are significantly improved compared to the conventional forward converter. In fact, the pulse rising and falling times are dramatically reduced: 4.4 versus 150 μs and 4.2 versus 100 μs, respectively. When the load voltage increases from 4 to 8 V, the prototype efficiency increases from 62.9% to 68.9% . In summary, this article demonstrates the feasibility and effectiveness of employing both continuous and fine-tuned pulse currents to develop fast chargers for supercapacitors.

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