Design and Control of an Electrolytic Capacitorless Three-Phase On-Board Charger Based on Active Third-Harmonic Current Injection

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***Abstract*—On-board chargers (OBCs) with conventional two-stage architecture, consisting of an active front-end (AFE) converter and an isolated dc–dc stage, require bulky line filters and dc-link capacitors, resulting in low volumetric efficiency. Active third-harmonic injection and current unfolding methods offer significant improvement in terms of efficiency and power density in power factor correction (PFC) applications. However, existing unfolding-based topologies require two isolated dc–dc converters capable of handling the rated power for PFC and output voltage regulation. This article presents a three-phase ac–dc converter with a third-harmonic current injection circuit that processes a fraction of the total power and a single isolated dc–dc converter for galvanic isolation. Line frequency switching in the rectifier produces varying dc-link voltages, eliminating the requirement of bulky electrolytic capacitors. The article discusses detailed operation and design procedures along with an elaborate comparative analysis between the proposed topology and the conventional two-stage and Swiss rectifier-based isolated topologies. A 6.6-kW prototype is developed and tested for experimental validation of the system in both balanced and unbalanced grid conditions. The experimental results demonstrate unity power factor operation throughout the operating range, achieving a peak efficiency above 97%.**

***Index Terms*—Line frequency switching, power factor correction, third-harmonic current injection, variable dc-link.**

I. Introduction

THE growing battery capacity of electric vehicles (EVs) has necessitated higher charging power levels of on-board chargers (OBCs) to enable faster charging. The charging levels are categorized according to the output power of the charger [1].

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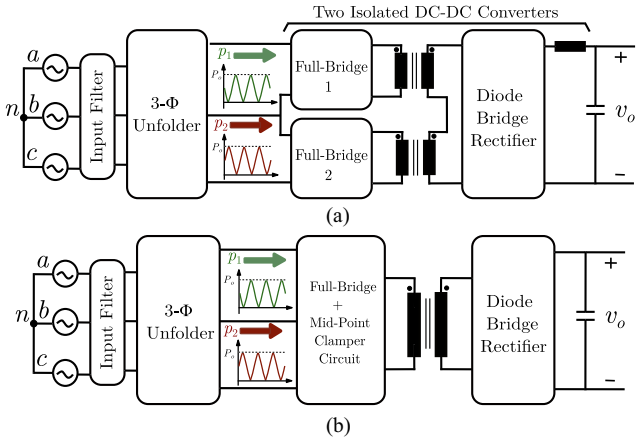

Fig. 1. Swiss rectifier-based isolated AC–DC converters [11], [14].

Usually, single-phase grid-connected OBCs are used for level 1 ($<$ 3.7 kW) and level 2 ($<$ 7 kW) charging, suitable for low-power applications. However, EVs with higher battery capacity employ 11 or 22 kW chargers that require three-phase grid connection [2]. The most common configuration of a three-phase OBC is a two-stage system comprising an AFE followed by an isolated dc–dc stage. The active front-end (AFE) is operated at high frequency for power factor correction (PFC) operation to comply with the power quality standard according to the IEEE 519 [3] guidelines, while the dc–dc stage regulates the output power. The bulky *LCL* line filters used to attenuate the switching frequency harmonics [4] deteriorate the power density of the converter. Although the passive size can be reduced by selecting a higher switching frequency, the efficiency of the system is compromised.

Topologies based on third-harmonic current injection have been proposed in the literature, offering several advantages in terms of efficiency improvement and passive size reduction [5]. Usually, a three-level converter, often termed as "three-phase unfolder," is employed at the front-end, and it is switched at line frequency to obtain variable piecewise sinusoidal dc-link voltages. The PFC and output voltage regulation are realized by two dc–dc converters capable of processing the varying input powers. Swiss rectifier [6] is a nonisolated buck-type PFC converter that utilizes third-harmonic current injection concept by modulating two buck converters connected with the split dc links. The two active switches in the positive and negative

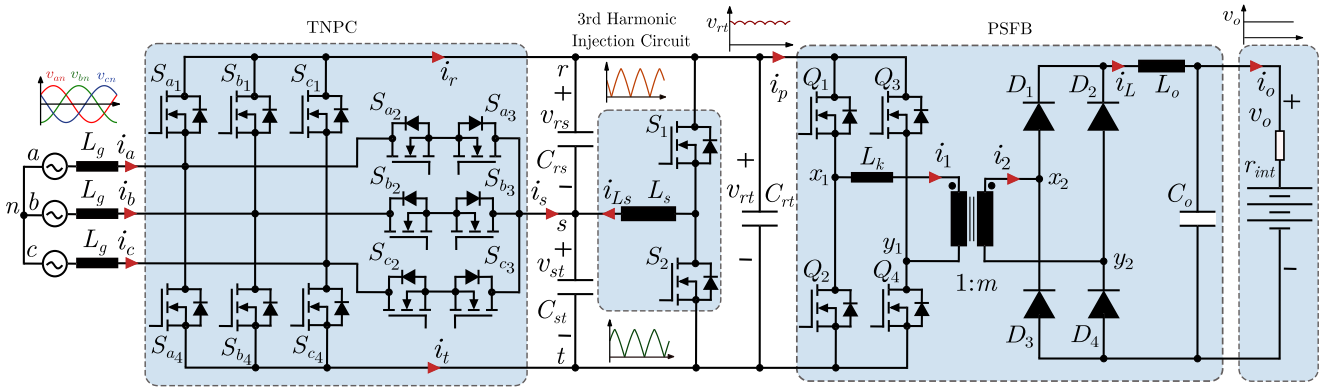

Fig. 2. Three-phase grid-tied isolated EV charger consisting of line frequency switched T-type neutral point clamped (TNPC) and active third-harmonic current injection circuit.

dc rails are controlled to maintain the positive and negative dc-link currents proportional to the maximum and minimum grid voltages, respectively. Other variants of the Swiss rectifier are proposed in [7], [8]. Interleaved dc–dc converters are employed in [7] to reduce the total harmonic distortion (THD) of the input current. The current unfolding principle is used in [8] along with a boost operation for solar photovoltaic applications. However, the topologies discussed above are not isolated and galvanic isolation is mandatory for EV chargers according to the IEC 61851 standard [9].

Three-phase current unfolding concept has been applied to Swiss rectifier-based isolated ac–dc converters for grid integration of energy storage systems. In [10], two dual bridge series resonant converters (DBSRC) are used in the input parallel output series configuration to produce the variable dc-link currents that are unfolded by a line frequency switched neutral point clamped (NPC) converter. The modular DBSRC system is capable of operating in dc–dc, dc–ac and ac–dc modes. A similar approach is explored in [11], [12] where phase-shifted full-bridge (PSFB) and forward converter are used respectively, as the dc–dc stages. The input power to each dc–dc converter varies from zero to peak power over one-third of a grid cycle. Hence, each dc–dc converter must be designed for the rated power, which results in underutilization of the dc–dc converters. In order to simplify the complex structure of the two full-bridges and improve the overall efficiency, a single full-bridge with a mid-point clamper circuit is proposed to process the fluctuating power resulting from the unfolding operation in [13] and [14]. A high-low high-low (HLHL) modulation scheme is introduced in [14] to facilitate zero voltage switching (ZVS). In addition, a hybrid frequency control is implemented in [14] to reduce input current distortion. A T-type structure with an LCC compensation network is used in [15] for a wireless charging application. Although employing a T-type converter reduces the number of active devices, it requires a more complex modulation scheme. The block diagram of the topologies proposed in [11] and [14] is depicted in Fig. 1. Three-phase unfolding-based single-stage dc–ac converters are proposed in [16] and [17]. However, these topologies require multiple high-frequency transformers for galvanic isolation, resulting in increased loss and volume.

Besides Swiss rectifier-derived topologies, a buck/boost type active third-harmonic current injection circuit, also referred as "Integrated-Active-Filter," has been developed. A buck-type PFC rectifier consisting of a diode bridge rectifier and a third-harmonic current injection circuit is proposed in [18]. A buck converter at the back-end is modulated to draw constant power from the input. A two-stage matrix converter based on third-harmonic current injection is presented in [19] for ac–ac application proposing a strategy to enhance the control range of reactive power. The effect of volt-second imbalance in the active filter inductor on grid current quality is explored in [20] for 115 V/400 Hz aircraft system. This article presents an isolated three-phase ac–dc converter for EV charging application utilizing a line frequency switched rectifier and partial power processing current injection circuit for PFC [21]. Line frequency switching of the front-end converter produces piecewise sinusoidal dc-link voltages. The total dc-link voltage has a six-pulse shape, and its maximum value is equal to the peak of the line-to-line grid voltage. Hence, the voltage stress on the devices is lower compared to the AFE where the dc-link voltage is maintained at a higher value than the peak line-to-line voltage. In order to provide galvanic isolation and regulation of output current, a PSFB converter is used. PSFB is chosen for its simple control and inherent ZVS capability [22]. The main contributions of the article are as follows.

1) The article presents an isolated PFC converter with a modulation strategy that requires relatively low implementation effort. The buck/boost-based current injection circuit can be controlled as a simple dc–dc converter. Feedforward duties are incorporated to modulate the dc–dc stage to reduce the controller burden.
2) A detailed comparison is presented with the conventional two-stage AFE and Swiss rectifier-based topologies. The proposed converter exhibits superior performance in terms of efficiency and passive size reduction compared to AFE. The topology presented in this article has the minimum total active device stress compared to existing third-harmonic current injection-based isolated topologies.
3) The performance of the system is validated in a 6.6-kW laboratory prototype in balanced and unbalanced grid conditions. Balanced, sinusoidal input currents are maintained while a negative sequence component of 10 V is injected in the grid voltages. The THD is maintained below 5% in both balanced and unbalanced conditions.

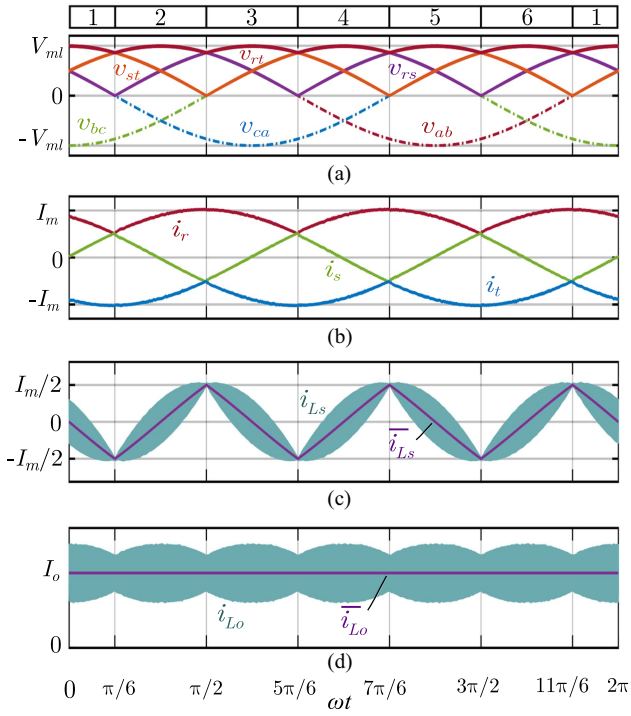

Fig. 3. Waveforms of the TNPC and current injection circuit. (a) Piecewise sinusoidal dc-link voltages (v_{rs}, v_{st}, v_{rt}). (b) DC-link currents (i_r, i_s, i_t). (c) Current injection inductor current (i_{L_s}) and its low-frequency component ($\bar{i}_{L_s}$). (d) PSFB output inductor current (i_{L_o}) and its average ($\bar{i}_{Lo}$).

The experimental results demonstrate a peak efficiency of 97.93% and an efficiency above 95% for 15% to 100% load range.

The article is organized as follows: Section II discusses the operating principle of the system. The closed-loop control strategy is presented in Section III. Section IV presents the analytical expressions of voltage and current stresses on the semiconductor devices and the design of passive components. A comparative analysis between the conventional two-stage converter, the Swiss rectifier-based converters, and the proposed converter is discussed in Section V. Section VI presents the loss analysis of the three-phase charger. The experimental results are presented in Section VII. Section VIII concludes the article.

II. Operating Principle

The complete circuit diagram of the three-phase isolated ac–dc converter is shown in Fig. 2. A T-type neutral point clamped (TNPC) converter is employed at the front-end for rectification. The TNPC is switched at grid frequency and, therefore, is not capable of regulating the grid currents. Hence, an active third-harmonic current injection circuit is incorporated for PFC. The current injection circuit is connected as a shunt branch and operates as a partial power processing converter. The third-harmonic current pushed by the current injection inductor (L_s) is proportional to the phase voltage having the minimum absolute magnitude. The dc-link currents (i_r, i_s, and i_t) and the third-harmonic current (i_{L_s}) are shown in Fig. 3. Further, a PSFB converter is integrated at the back-end to provide galvanic isolation as well as to ensure sinusoidal input currents from the grid. The primary of the PSFB is a H-bridge whose two legs

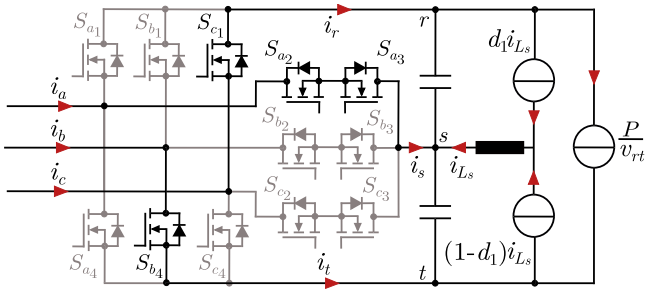

Fig. 4. Equivalent circuit of the system in sector 1 ($v_{cn} > v_{an} > v_{bn}$).

are phase shifted to transfer power to the load. The secondary circuit consists of a diode-bridge rectifier. There are two main operating modes in a switching cycle: the power delivery mode (mode 1 as shown in Fig. 7) where two diagonal devices (Q_1, Q_4 or Q_2, Q_3) are ON and power is transferred from the input to the load, and the free-wheeling mode (mode 2) where the two high-side (Q_1, Q_3) or low-side devices (Q_2, Q_4) are ON. There is also a duty loss period (mode 3) when the transformer current changes its direction with a finite slope. The PSFB is controlled to draw a constant power to maintain the sinusoidal shape of the grid currents. The input current to the PSFB needs to be varied in the opposite phase of the six-pulse dc-link so that the power drawn by the PSFB is constant.

The detailed operating principle of the system with relevant voltage and current equations is presented below. The three line-to-neutral grid voltages are defined by

$$\begin{aligned} v_{an} &= V_m \sin(\omega t) \\ v_{bn} &= V_m \sin(\omega t - 2\pi/3) \\ v_{cn} &= V_m \sin(\omega t + 2\pi/3) \end{aligned} \tag{1}$$

where V_m is the amplitude and $\omega = 2\pi f_g$ is the fundamental angular frequency. One grid cycle is divided into six equal sectors, as depicted in Fig. 3. In each sector, the phases having maximum and minimum instantaneous voltages are clamped to the positive and negative dc-buses, respectively, while the remaining phase is connected to the mid dc-bus by appropriate switching of the TNPC devices, The resultant dc-link voltages (v_{rs}, v_{st}, and v_{rt}) are piecewise sinusoidal. The maximum and minimum values of v_{rt} are $V_{ml}(=\sqrt{3}V_m)$ and $(\sqrt{3}/2)V_{ml}$, respectively, and its frequency is six times the grid frequency. The voltages v_{rs} and v_{st} vary from 0 to $(\sqrt{3}/2)V_{ml}$. Due to the pulsating nature of the voltages, bulky electrolytic capacitors can be eliminated from the dc link. Small filter capacitance is sufficient to attenuate the switching frequency ripples.

The desired ac input currents for unity power factor operation are given by

$$\begin{aligned} i_a &= I_m \sin(\omega t) \\ i_b &= I_m \sin(\omega t - 2\pi/3) \\ i_c &= I_m \sin(\omega t + 2\pi/3) \end{aligned} \tag{2}$$

where I_m is the current amplitude. If the active power drawn from the grid is P, the value of I_m is $(2P/3V_m)$. The current injection circuit and PSFB are modulated in a way so that i_r and i_t are proportional to the maximum and minimum phase

TABLE I
DC-LINK VOLTAGES AND CURRENTS IN DIFFERENT SECTORS

Sector	v_{rs}	v_{st}	v_{rt}	i_r	i_s	i_t
1	v_{ca}	v_{ab}	v_{cb}	i_c	i_a	i_b
2	v_{ac}	v_{cb}	v_{ab}	i_a	i_c	i_b
3	v_{ab}	v_{bc}	v_{ac}	i_a	i_b	i_c
4	v_{ba}	v_{ac}	v_{bc}	i_b	i_a	i_c
5	v_{bc}	v_{ca}	v_{ba}	i_b	i_c	i_a
6	v_{cb}	v_{ba}	v_{ca}	i_c	i_b	i_a

voltages. The mid dc-link current i_s is proportional to the phase voltage having smallest absolute value. The relationship between the ac line voltages and line currents with the dc-link voltages and currents is provided in Table I.

The equivalent circuit for sector 1 $[\omega t : 0 - \pi/6, 11\pi/6 - 2\pi]$ $(v_{cn} > v_{an} > v_{bn})$ is depicted in Fig. 4. As phase c is maximum in this sector, it is clamped to positive dc-link via switch S_{c_1}. Phase b is connected to the negative dc-link through S_{b_4} and phase a is connected to the mid dc-bus via S_{a_2} and S_{a_3}. The switching cycle average of the third-harmonic current i_{L_s} in sector 1 is expressed in the following:

$$\bar{i}_{L_s} = -i_a + \bar{i}_{C_{st}} - \bar{i}_{C_{rs}}. \tag{3}$$

Here, the low-frequency component of the currents $(\bar{i}_{C_{rt}}, \bar{i}_{C_{st}})$ through the capacitors C_{rs} and C_{st} can be ignored as the capacitance values are very small. Hence, the third-harmonic current can be approximated as

$$\bar{i}_{L_s} = -i_a = -(2P/3V_m)\sin(\omega t). \tag{4}$$

The average voltage (v_{Ls}) across the current injection inductor is zero to maintain volt-second balance. When switch S_1 is ON, the voltage across L_s is v_{ca}. Similarly, the voltage is v_{ba} when S_2 is ON. The voltage drop v_{Ls} can be written as

$$v_{L_s} = d_1 v_{ca} + (1 - d_1) v_{ba} = 0 \tag{5}$$

where d_1 is the duty ratio. Therefore, the duty ratio for sector 1 is given by

$$d_1 = v_{ab}/v_{cb} = \sin(\omega t + \pi/6)/\cos\omega t \tag{6}$$

The same approach can be used to derive the duty ratio for the other sectors. Further, the average currents through S_1 and S_2 can be written as

$$\begin{aligned} \bar{i}_{S_1} &= d_1 \bar{i}_{Ls} = -d_1 i_a \\ \bar{i}_{S_2} &= (1 - d_1)\bar{i}_{Ls} = -(1 - d_1) i_a. \end{aligned} \tag{7}$$

The average input current to the isolated dc–dc converter is given by

$$\bar{i_p} = P/v_{rt} = P/v_{cb} \tag{8}$$

The current through the positive dc-bus is obtained from the summation of $\bar{i_p}$ and $\bar{i}_{S_1}$

$$\bar{i_r} = \bar{i_p} + \bar{i}_{S_1}. \tag{9}$$

The instantaneous power in a balanced three-phase system is constant. To achieve sinusoidal controllability of the ac currents,

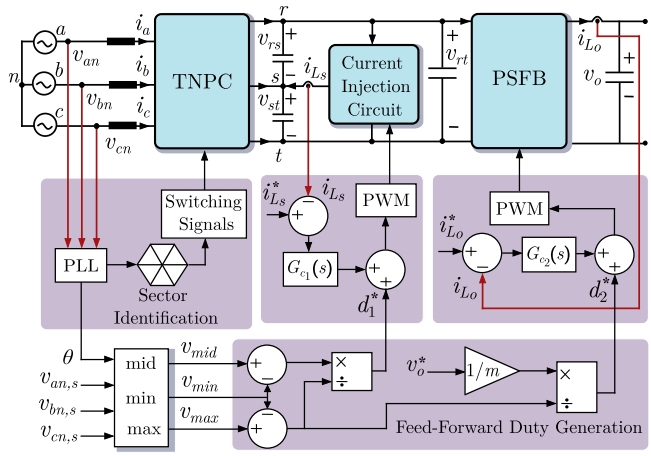

Fig. 5. Closed-loop control of the system.

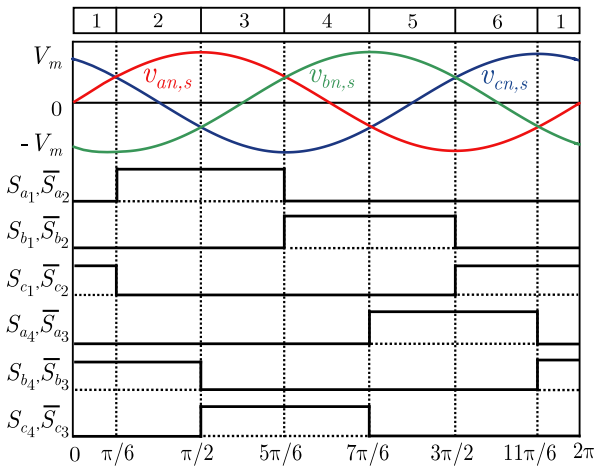

Fig. 6. Six sectors in a line cycle and the switching pulses of TNPC.

the input current of the PSFB must have a phase shift of 180° with the six-pulse dc-link. Hence, the phase shift between the two primary legs of the PSFB should be varied accordingly. The generalized expression of the phase shift is

$$d_2 = v_o/m v_{rt} \tag{10}$$

where m is the turns' ratio of the transformer. From (10), it is evident that d_2 must have an inverse six-pulse shape to draw a constant power.

III. CONTROL STRATEGY OF THE SYSTEM

The closed-loop control strategy is illustrated in Fig. 5. The switching logic of the TNPC is decided according to the instantaneous values of the grid voltages. The phase-locked loop (PLL) is implemented to determine the phase angle $\theta(=\omega t)$, and based on this information, the sector is identified. In each sector, the three grid voltages are categorized as maximum, minimum, and median according to their instantaneous magnitudes. The high-side and low-side devices corresponding to the maximum and minimum phases are turned ON. The remaining phase is connected to the mid dc-bus by the two mid-leg devices connected in antiseries fashion. The switching pulses are depicted in Fig. 6. The pulses provided to the TNPC devices have a fixed width.

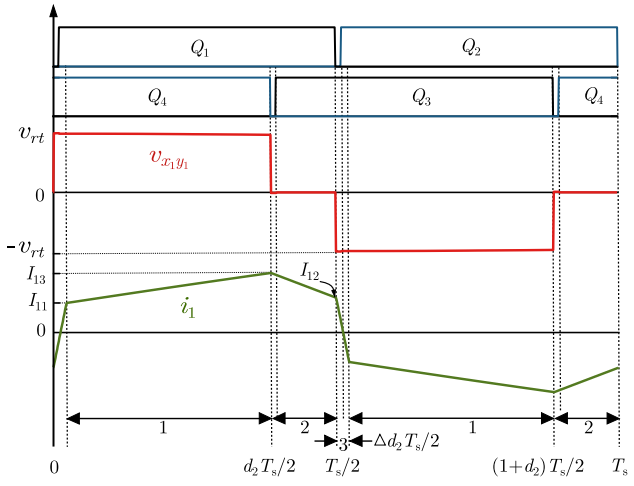

Fig. 7. Switching pulses of the PSFB H-bridge and transformer primary voltage and current indicating the three different modes of operation—power delivery mode (1), free-wheeling mode (2) and duty loss period (3).

Therefore, this converter cannot be used for the regulation of voltage or current.

The sensed grid voltages ($v_{an,s}, v_{bn,s}, v_{cn,s}$) are used to determine the maximum ($v_{\max}$), minimum ($v_{\min}$), and median (v_{mid}) voltages in a sector. The reference third-harmonic current is a function of v_{mid}, and its expression is given as

$$\bar{i}^*_{L_s} = -(2P/3V_m^2)v_{\text{mid}}. \tag{11}$$

A feed-forward duty is provided to reduce the controller burden. The feed-forward duty is the relative on-time of the high-side switch (S_1) of the current injection circuit and can be expressed as

$$d_1^* = (v_{\text{mid}} - v_{\min})/(v_{\max} - v_{\min}). \tag{12}$$

The devices of the primary H-bridge of the PSFB are operated at 50% duty in all operating conditions. For regulating the output voltage, the phase shift between the two half-bridges is varied. As mentioned earlier, the phase shift should have an inverse six-pulse shape to produce a constant output voltage. The output inductor current (i_{L_o}) is controlled to obtain the desired phase shift. The average current through the output inductor is the load current, and it is defined as

$$\bar{i}^*_{L_o} = P/v_o^*. \tag{13}$$

A feed-forward term is added with the controller output of PSFB as well for better closed-loop control. The feed-forward term is defined as

$$d_2^* = v_o^*/(m(v_{\max} - v_{\min})). \tag{14}$$

Small-signal models of the converters are developed to design the controllers. The third-harmonic current injection circuit is modeled as a buck converter. As the injected current has a dominant third-harmonic component, it is essential to design a high-bandwidth controller to track the current. However, the addition of the feed-forward term improves the controller performance significantly, allowing the use of a low bandwidth controller. The PSFB can be modeled as an isolated buck converter. The transfer function $\tilde{i}_{L_o}(s)/\tilde{d}_2(s))$ is used to implement the average current control. The controllers $G_{c_1}(s)$ and $G_{c_2}(s)$ are proportional-integral (PI) controllers.

IV. Design of the System

A. Voltage and Current Stresses on Semiconductor Devices

The analytical expressions of the voltage and current stresses on semiconductor devices and the design procedure of the passive components are discussed in this section.

The main leg switches of the TNPC, i.e., S_{j1} and S_{j4}, where $j \in \{a, b, c\}$, withstand a maximum voltage of $\sqrt{3}V_m$. The voltage stress on the mid-leg switches (S_{j2}, S_{j3}) is $(3/2)V_m$. Each device of the TNPC conducts for one-third duration of a grid cycle. The rms current expressions of the main leg and mid leg devices, assuming upf operation, can be written by the following equations:

$$\begin{aligned} I_{Sj1,\text{rms}} &= I_{Sj4,\text{rms}} = I_m\sqrt{1/6 + (\sqrt{3}/8\pi)} \\ I_{Sj2,\text{rms}} &= I_{Sj3,,\text{rms}} = I_m\sqrt{1/6 - (\sqrt{3}/4\pi)}. \end{aligned} \tag{15}$$

The voltage stress on the devices of the current injection circuit is $\sqrt{3}V_m$. The devices of the half-bridge carry third-harmonic current that contains switching frequency ripples. The peak-to-peak ripple over the low-frequency average is dependent on the variable dc-link voltages and can be written as

$$\Delta i_{L_s} = \frac{(v_{rt} - v_{st})d_1}{L_s f_s} = \frac{v_{rt}d_1(1-d_1)}{L_s f_s}. \tag{16}$$

The rms current of the current injection inductor in the ith switching cycle is given by

$$I_{L_s,\text{rms},i} = \sqrt{\left(\bar{i}^2_{L_s,i} + \Delta i^2_{L_s,i}/12\right)}. \tag{17}$$

Furthermore, the rms currents of the devices S_1 and S_2 can be expressed as

$$\begin{aligned} I_{S_1,\text{rms},i} &= \sqrt{d_1}I_{L_s,\text{rms},i} \\ I_{S_2,\text{rms},i} &= \sqrt{1-d_1}I_{L_s,\text{rms},i}. \end{aligned} \tag{18}$$

The overall rms current of the current injection inductor and the individual devices can be calculated by integrating all the switching cycle rms currents over one-third period of a grid fundamental cycle.

The H-bridge devices of PSFB need to block a maximum voltage of $\sqrt{3}V_m$, the peak line-to-line voltage. The maximum value of the reverse voltage that the secondary side diodes of the PSFB need to block is $\sqrt{3}mV_m$. Because of the finite slope of the transformer current, the effective phase shift ($d_{2,eff}$) between the two legs of PSFB is lower than the applied phase shift (d_2). The effective phase shift is given by

$$d_{2,eff} = d_2 - \Delta d_2 \tag{19}$$

where Δd_2 is the duty loss. The frequency of the output inductor current (Δi_{L_o}) is twice the switching frequency. The peak-to-peak current ripple in i_{Lo} can be calculated as

$$\Delta i_{L_o,i} = \frac{(mv_{rt} - v_o)d_{2,\text{eff}}}{2(L_o + m^2L_k)f_s} = \frac{mv_{rt}d_{2,\text{eff}}(1-d_{2,\text{eff}})}{2(L_o + m^2L_k)f_s} \tag{20}$$

where L_k is the leakage inductance of the transformer. The maximum and minimum values of i_{L_o} in the ith cycle are given by

$$I_{L_o,\max,i} = \bar{i}_{Lo} + \Delta i_{L_o,i}/2,$$
$$I_{L_o,\min,i} = \bar{i}_{Lo} - \Delta i_{L_o,i}/2. \quad (21)$$

The three points marked in the primary current waveform of the transformer in Fig. 7, I_{11}, I_{12}, and I_{13} are expressed as

$$I_{11,i} = mI_{L_o,\min,i}$$
$$I_{13,i} = mI_{L_o,\max,i}$$
$$I_{12,i} = I_{13,i} - [mv_o(1-d_2)/(2f_s(L_o + m^2L_k))]. \quad (22)$$

The rms value of the current flowing through the primary side devices can be expressed in terms of the transformer rms current $I_{1,i}$

$$I_{Q,i} = I_{1,i}/\sqrt{2}. \quad (23)$$

The transformer rms current can be derived as

$$I_{1,i} = \sqrt{2f_s(I_{x1}^2 + I_{x2}^2 + I_{x3}^2)} \quad (24)$$

where I_{x1}, I_{x2}, and I_{x3} are given by

$$I_{x1} = \sqrt{\frac{d_{2,\text{eff}}}{6f_s}(I_{11,i}^2 + I_{13,i}^2 + I_{11,i}I_{13,i})}$$
$$I_{x2} = \sqrt{\frac{(1-d_2)}{6f_s}(I_{12,i}^2 + I_{13,i}^2 + I_{12,i}I_{13,i})}$$
$$I_{x3} = \sqrt{\frac{\Delta d_2}{6f_s}(I_{11,i}^2 + I_{12,i}^2 - I_{11,i}I_{12,i})}. \quad (25)$$

The average and rms current of the diodes can be estimated by the following equations:

$$I_{D,\text{avg},i} = (0.25/m)[I_{13,i} + d_2I_{11,i} + (1-d_2)I_{12,i}] \quad (26)$$
$$I_{D,\text{rms},i} = I_{1,i}/\left(m\sqrt{2}\right). \quad (27)$$

B. Selection of Passive Components

The maximum peak-to-peak ripple of the current injection inductor is

$$\Delta i_{L_s} = \sqrt{3}V_m/(4L_sf_s). \quad (28)$$

The value of L_s is selected using the following equation:

$$L_s \geq \sqrt{3}V_m/(4f_s\Delta i_{L_s,\max}) \quad (29)$$

where $\Delta i_{L_s,\max}$ is the maximum allowable peak-to-peak current ripple. The current ripple through L_s is divided between the two capacitors C_{rs} and C_{st}. These capacitance values are selected using the following inequality:

$$C_{rs} = C_{st} \geq \sqrt{3}V_m/(64L_sf_s^2\Delta v_{rs,\max}). \quad (30)$$

Here, $\Delta v_{rs,\max}$ is the specified peak-to-peak voltage ripple in the two voltages v_{rs} and v_{st}. As the three capacitances C_{rs}, C_{st}, and C_{rt} form a delta configuration, the selected value of C_{rt} is equal to the other two capacitors to maintain symmetry.

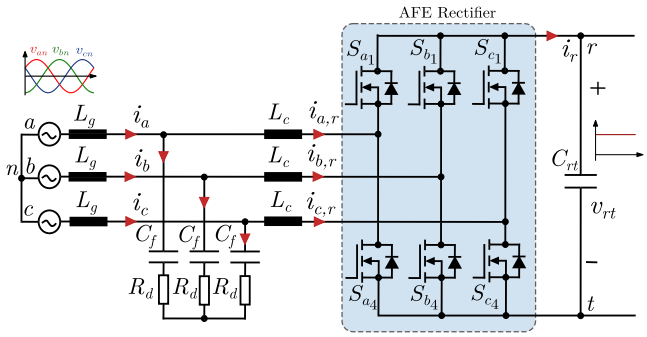

Fig. 8. Conventional two-level AFE with LCL filter for attenuation of switching frequency components.

The peak-to-peak ripple in i_{Lo} varies with the phase shift applied between the two primary half-bridges. The output inductance value is selected using

$$L_o \geq \left(1 - \frac{v_o}{\sqrt{3}mV_m}\right)\frac{v_o}{2f_s\Delta i_{L_o,\max}}. \quad (31)$$

The highest ripple is experienced when the dc-link voltage v_{rt} is equal to the peak line-to-line voltage. The output capacitance is selected to restrict the peak-to-peak voltage ripple within $\Delta v_{o,\max}$

$$C_o \geq \left(1 - \frac{v_o}{\sqrt{3}mV_m}\right)\frac{v_o}{32L_of_s^2\Delta v_{o,\max}}. \quad (32)$$

Further, the turns' ratio of the transformer is determined by

$$m = v_o/(d_2v_{rt}). \quad (33)$$

Here, the turns' ratio has been chosen to be unity to achieve high coupling between the two windings. The leakage inductance should be high enough to dissipate the stored energy in the device parasitic capacitances and the transformer winding capacitance to achieve ZVS of Q_1 and Q_2 as explained in [22]. On the basis of the above design equations, the semiconductor and passive component selection is done.

V. Comparison With Other Topologies

The topology described in the article has been compared with conventional AFE and other third-harmonic current injection-based topologies. The main difference from the conventional two-stage topology is in the passive size, whereas the difference with the Swiss rectifier-based topologies lies in the dc–dc stage. The detailed comparative analysis is presented in the following sections.

A. Comparison of the Input Filter With Three-Phase AFE

One of the advantages of the grid frequency operated TNPC is the reduction in the grid filter and dc-link capacitor size. In order to quantify the passive size difference between the conventional and proposed system, a comparison is presented between two-level AFE and the three-level TNPC. For fair comparison, the rated power is taken as 6.6 kW for both topologies. The switching frequency of AFE is 50 kHz. The system specifications are given in Table II. The AFE circuit with input filters is depicted in Fig. 8. Usually, an LCL filter is used on the

TABLE II
SYSTEM SPECIFICATIONS AND COMPARISON OF PASSIVE VALUES

Parameter	TNPC + CI	AFE
Specifications		
Grid line - line voltage (rms)	400 V	400 V
Rated output power (P_o)	6.6 kW	6.6 kW
Maximum dc-link voltage ($V_{dc,\max}$)	565 V	630 V
Output voltage (V_o)	250 - 400 V	250 - 400 V
AC-DC stage operating frequency	50 Hz	50 kHz
DC-DC stage switching frequency (f_s)	100 kHz	100 kHz
Passive Components		
Grid filter	L filter $L_g = 75\,\mu$H	LCL filter $L_g = 0.75$ mH $L_c = 1.5$ mH $C_f = 3.3\,\mu$F
DC-link capacitance	C_{rs}, C_{st}, C_{rt} = 0.47 µF	$C_{rt} = 100\,\mu$F
PSFB transformer	1:1, 20 turns	1:1, 20 turns
Current injection inductance (L_s)	430 µH	-
PSFB output inductance (L_o)	100 µH	100 µH
PSFB output capacitance (C_o)	16 µF	16 µF

input side to attenuate the switching frequency harmonics and other higher-order harmonics. For designing the LCL filter, the guidelines provided in [23] have been used.

1) The first step is to calculate the base impedance and the base capacitance. For the specified system parameters, the base impedance and base capacitance values are 24.24 Ω and 131 µF, respectively. There are certain restrictions that must be taken into account when choosing inductance and capacitance values. The total inductance value should not exceed 10% to avoid significant voltage drop. The capacitor value should be restricted within 5% to maintain the power factor close to unity.
2) The converter side impedance is considered 2% of the base impedance, resulting in a filter inductance (L_c) value of 1.5 mH. If the filter capacitance (C_f) is too low, the grid inductance value will be high. A 3.3 µF capacitor is chosen that is 2.5% of the base capacitance.
3) The grid side inductance (L_g) is related to converter side inductance by a factor r, and based on the ripple attenuation requirement in the grid side current compared to the ripple in the converter side current, the value of r is selected. The value of r is selected as 0.5, resulting in the grid side ripple to be 0.41% of the converter side ripple.
4) The consequent resonance frequency is calculated by

$$\omega_{res} = \sqrt{(L_g + L_c)/(L_g L_c C_f)}. \tag{34}$$

Substituting the selected inductance and capacitance values into (34), the resonant frequency is 3.86 kHz, which lies in the desired frequency range to avoid resonance issues due to the LCL filter. The frequency range is given by the following inequality:

$$10 f_g \leq f_{\text{res}} \leq 0.5 f_s. \tag{35}$$

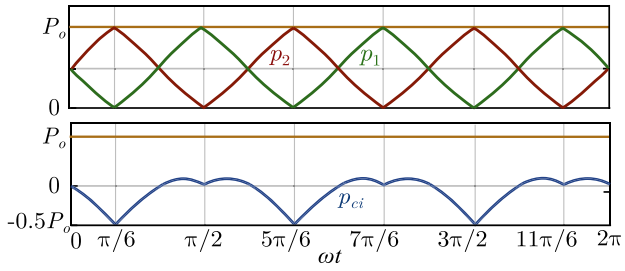

Fig. 9. Power processed by the two DC–DC converters (p_1, p_2) of Swiss rectifier and the current injection circuit (p_{ci}) where the total power is P_o.

Although the resonance frequency lies within the acceptable range, some passive damping should be provided for stable operation. The value of the resistance is chosen in a way to achieve sufficient damping without losing the effectiveness of the filter too much. The value of the damping resistance connected in series with the capacitive filter is: 15 Ω.

B. Line Filter Design of the Proposed System

The high-frequency components of the input currents to the current injection circuit and PSFB flow through the dc-link capacitors C_{rs}, C_{st}, and C_{rt}. The high-frequency currents through the capacitors lead to high-frequency ripples in the dc-link voltages. The high-frequency ripple in v_{rs} and v_{st} can be extracted with the help of the following equation:

$$\Delta v_{rs} = (1-s)\cdot v_{rt} + L_s \frac{di_{Ls}}{dt} - \bar{v}_{rs}$$
$$\Delta v_{st} = s \cdot v_{rt} - L_s \frac{di_{Ls}}{dt} - \bar{v}_{st} \tag{36}$$

where s denotes the switching function of the current injection circuit while $\bar{v}_{rs}$ and $\bar{v}_{st}$ are the low-frequency components of v_{rs} and v_{st}. Higher order harmonics are impressed upon the grid inductors because of the presence of high-frequency ripples in the dc-link voltages. From the Fourier analysis of the grid current, the most dominant harmonics are found at $h = 2m_f \pm 1$ where m_f is the ratio of the switching frequency to the line frequency. Here, the value of m_f is 2000. In order to achieve -40 dB attenuation for the dominant harmonic, the required filter inductance value is 75 µH at each phase.

C. Comparison With Swiss Rectifier-Based Topologies

A detailed comparison is presented with Swiss rectifier-derived isolated topologies [11], [13], [14], and [15]. The difference between the Swiss rectifier-based topologies and the presented topology lies in the dc–dc stage. The configuration proposed in [11] employs two PSFB converters connected to the two ports of the front-end converter, as shown in Fig. 1. Each of the PSFB devices needs to block a peak voltage of $(\sqrt{3}/2)V_{ml}$ where V_{ml} is the peak line-to-line voltage. The current stress on the active devices of the PSFB converters can be calculated as discussed in Section IV. The expressions of power processed by the two dc–dc converters are given below

$$p_1 = v_{rs} i_r, \qquad p_2 = -v_{st} i_t. \tag{37}$$

The instantaneous powers p_1 and p_2 vary from zero to full power as depicted in Fig. 9. Although each dc–dc converter has to

TABLE III
COMPARISON OF THE PROPOSED CONVERTER WITH SWISS RECTIFIER-BASED TOPOLOGIES

Topologies	[11]	[13]	[14]	[15]	Proposed
DC-DC stage	PSFB(×2)	Full-bridge + Clamper	Full-bridge + Clamper (HLHL modulation)	T-type converter with LCC resonant tank	CIHB + PSFB
Number of active switches	8	8	8	8	6
Number of diodes	4	4	4	4	4
Voltage stress (S.F. V_{ml})	0.866	1, 0.866	1, 0.866	1, 0.866	1, 1
Current stress (S.F. P/V_{ml})	0.988	0.946, 0.457	0.957, 0.534	0.885, 0.431	0.244, 0.988
NTASS	1.541	1.208	1.279	1.133	1
Details of Magnetic Components					
Specifications	380 V (l-l) 400 V o/p, 10 kW	380 V (l-l) 400 V o/p, 10 kW	380 V (l-l) 400 V o/p, 10 kW	480 V (l-l) 650-755 V o/p, 21 kW	400 V (l-l) 250-400 V o/p, 6.6 kW
Switching frequency (kHz)	90	90	40 - 60	85	100
Number of inductors in ac side	3	3	3	3	3
Values (each phase) (μH)	190	70	70	600	75
Inductor core	24 stacked cores NPS141125 146.11 cm^3, 904.8 g	3 stacked cores NPS141125 18.26 cm^3, 113.1 g	not specified	not specified	ETD5419 core 35.5 cm^3, 180 g
Number of inductors in dc side	1	1	0	1	2
Values (μH)	540	540	-	28.3	430, 100
Inductor core	96 stacked cores NPS090075 181.15 cm^3, 1113.6 g	96 stacked cores NPS090075 181.15 cm^3, 1113.6 g	-	not specified	EE6527, ETD5922 78.2 cm^3, 385 g 51.2 cm^3, 262 g
Number of HFTs	2	1	1	1	1
Transformer core	2×9 EI60 core 548.17 cm^3, 2502 g	9 EI60 core 274.08 cm^3, 1251 g	not specified	not specified	EE8020 core 72.3 cm^3, 340 g

process half of the rated power in an average sense, the components must be designed for full power. Two high-frequency transformers are required for isolated systems, resulting in a bulky system.

The topology presented in this article employs a simple half-bridge and an inductor to inject the third-harmonic current. The peak power handled by the current injection circuit is half of the total power. The peak current through devices S_1 and S_2 is only half of the peak line current. The power p_{ci} processed by the current injection circuit can be written as follows:

$$p_{ci} = v_{rt}\bar{i}_{S_1} = v_{rt}d_1\bar{i}_{L_s}. \tag{38}$$

The topology proposed in [13] uses a single full-bridge along with a "mid-point clamper" circuit for PFC and voltage regulation. Elimination of a full-bridge results in improved system efficiency and core utilization. Another variation of [13] is presented in [14], where a HLHL type modulation technique is adopted for realizing soft switching in the dc–dc stage. In addition, a new hybrid frequency control is implemented to achieve high power factor operation. Unlike [11], [13] and the proposed converter, the output filter inductor is not required in this converter. The current stress on the devices has been determined with the help of the time duration expressions and switching pulses provided in [14]. A MATLAB script is written to obtain the rms values of the currents of the main leg and mid leg devices. First, the rms current expression for one switching cycle is written in the form of an equation. Then, the rms value of each cycle is integrated over one-third of a power cycle to obtain the overall rms currents.

In [15], a T-type converter is used in conjunction with an LCC resonant tank circuit after the three-phase unfolder. The two duty ratios (d_p, d_n) of the T-type converter are modulated to achieve PFC and regulate the tank voltage. All third-harmonic current injection-based circuits usually employ a three-level converter, like an NPC or a TNPC, in the front-end. The difference lies in the dc–dc stage. Hence, the active device count, diode count, voltage and current stresses of the semiconductor devices and normalized total active switch stress (NTASS) in the dc–dc stages of the respective topologies are considered in the first part of the comparison presented in Table III. An input line-to-line rms of 400 V, output voltage of 400 V and 6.6-kW output power have been considered for the calculation of NTASS. The total active switch stress (S_j) is calculated using the following equation:

$$S_j = \sum_{j=1}^{k} V_j I_j \tag{39}$$

where V_j is the maximum voltage that the device must block, I_j is the rms current through the device, and k is the number of devices. Parameters V_j and I_j are normalized using the scaling factors V_{ml} and (P_o/V_{ml}), respectively. Here, P_o is the rated output power 6.6 kW and V_{ml} is the peak line-to-line voltage ($= 400\sqrt{2}$ V). The two different values of voltage and current stresses represent the stresses of the main-leg and mid-leg devices of the converters discussed in [13], [14], [15]. For the proposed converter, the device stresses are of the current injection half-bridge (CIHB) and the PSFB, respectively. After the computation of S_j of each topology, NTASS is calculated taking

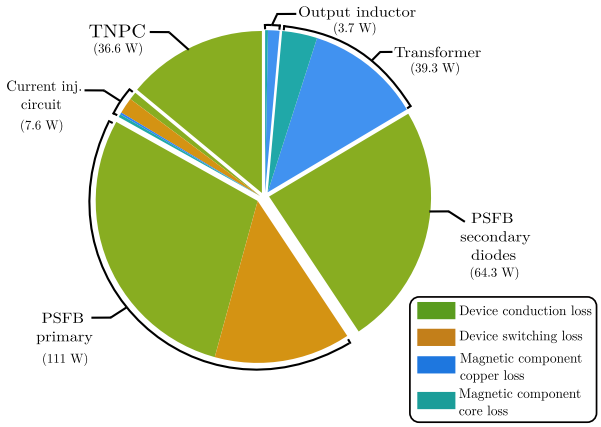

Fig. 10. Loss distribution of the system at 6.6 kW.

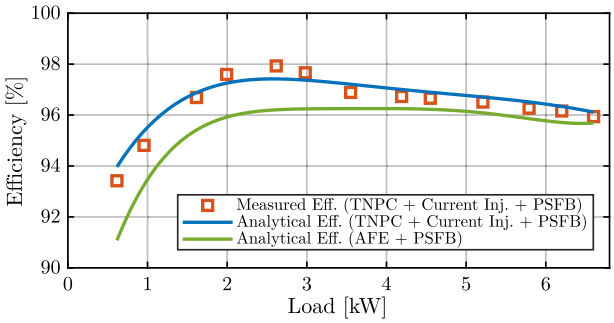

Fig. 11. Analytical efficiencies of the proposed system and the conventional system, along with measured efficiency indicated by the markers.

S_j of the proposed converter ($2 \times 0.244 + 4 \times 0.988 = 4.44$) as the base value. Although the NTASS of the dc–dc stage of the presented converter is the lowest compared to other topologies, it suffers from some disadvantages, like duty loss and secondary voltage oscillations because of PSFB. Due to the leakage inductance, the transformer current requires a finite time to change its direction. This duration is called the duty loss period. As the leakage inductance value increases, the duty loss period also increases, reducing the effective phase shift that is responsible for active power transfer. At the start of each power delivery mode of PSFB, oscillations are observed in the secondary voltage of the transformer because of the resonant circuit formed by the leakage inductance, transformer winding capacitance, and diode junction capacitances [24].

The second part of the comparison entails the description of the magnetic components used in the converters, along with the design specifications. The converter discussed in [11] employs two phase-shifted full-bridge converters and therefore requires two high-frequency transformers. The improved SR-based converters discussed in [13], [14] and [15] require only one transformer. In [11] and [13] and the presented converter, an output filter inductor is required, whereas it is eliminated in [14] and [15], further improving the power density of the converters. The proposed converter uses two inductors on the dc–dc side, the inductor in the third-harmonic current injection circuit and the output inductor of PSFB. The description of the inductor and transformer cores, including the volume and weight, are also provided in Table III.

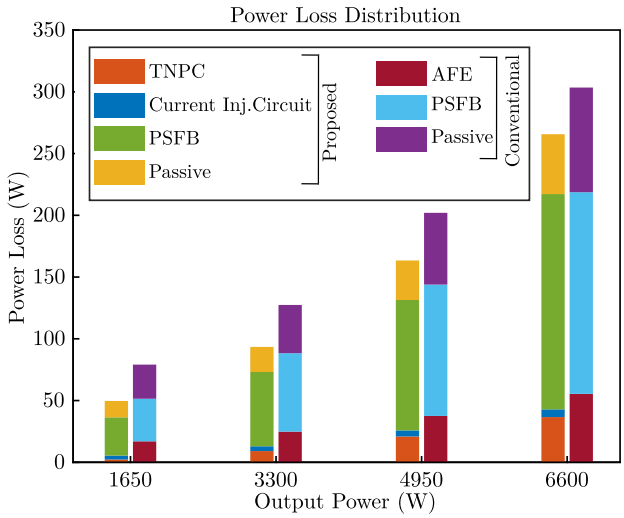

Fig. 12. Loss distribution of the proposed system and the conventional system.

VI. Loss Analysis and Efficiency Comparison

The efficiency of the system is theoretically estimated and compared with the efficiency of the conventional two-stage architecture. The isolated dc–dc stage is PSFB for both cases. For fair comparison, the same 1000 V Silicon Carbide (SiC) device C3M0120100 K listed in Table IV is considered for TNPC and AFE to calculate efficiency.

The semiconductor losses are calculated by curve-fitting the drain-source on resistance ($R_{DS,on}$) and switching energy plots available in the datasheet. The $R_{DS,on}$ is expressed as a function of the junction temperature (T_j) and is expressed as

$$R_{DS,on}(T_j) = aT_j^b + c. \tag{40}$$

The rms current expressions for the TNPC and the dc–dc stages are provided in Section IV. The conduction loss of the TNPC is given by

$$P_{c,TNPC} = 6(I_{Sj1,\text{rms}}^2 + I_{Sj2,\text{rms}}^2)R_{DS,\text{on}}(T_j). \tag{41}$$

As the voltages and currents of the current injection circuit and PSFB have 150 and 300 Hz envelopes, respectively, the energy loss is calculated for each switching cycle and integrated over one-third or one-sixth of the fundamental cycle. Finally, the average power loss is calculated by multiplying it by the appropriate frequency. The generalized expression of the conduction loss in the dc–dc stage devices is given by

$$P_{c,\text{dc-dc}} = f\sum_{i=1}^{n_s} 1/f_s(I_{\text{rms},i}^2 R_{DS,\text{on}}(T_j)) \tag{42}$$

where $I_{\text{rms},i}$ is the rms current of the device in the ith cycle and n_s is the number of switching cycles in one-third or one-sixth of the fundamental cycle. The frequency f is 150 Hz for the current injection circuit and 300 Hz for the PSFB.

For the proposed system, the TNPC is switched at 50 Hz. Hence, the switching loss is neglected. The devices of the dc–dc stage are switched at high frequency. As the current through the current injection inductor (L_s) is alternating in nature, the circuit works both in the buck and in the boost mode. In a switching half-bridge, one of the devices undergoes ZVS naturally during

turn ON. If the current ripple through L_s can be made sufficiently large, making the inductor current reverse its direction, both devices can be turned ON at zero voltage. However, a very small value of L_s can lead to deterioration in grid current quality.

The ZVS mechanism in the two legs of PSFB is different [22]. The ZVS of leg 2 (Q_3, Q_4) is aided by both the leakage inductance (L_k) and the output filter inductance (L_o). When leg 2 devices of the PSFB are turned ON, the current through the transformer primary winding is the reflected output inductor current. As the current through the transformer is at its peak during the turn ON, the devices Q_3 and Q_4 undergo ZVS throughout the entire load range. However, for leg 1 devices (Q_1, Q_2), ZVS depends on the leakage inductance and the load current. If the energy stored in the leakage inductance is not enough to charge/discharge the output capacitances of Q_1 and Q_2, partial soft switching occurs, or the devices may be hard switched. The condition for achieving ZVS in leg 1 is given by

$$E_{L_k} \geq (C_{oss} + 0.5C_{tr})V_{\text{in}}^2 \tag{43}$$

where E_{L_k} is the energy stored in the leakage inductance. C_{oss} and C_{tr} are device equivalent output capacitance and transformer winding capacitance, respectively. The critical current above which the ZVS of Q_1 and Q_2 is possible, can be calculated from

$$i_{\text{crit}} = \sqrt{\frac{2}{L_k}(C_{\text{oss}} + 0.5C_{\text{tr}})V_{\text{in}}^2}. \tag{44}$$

Here, the transformer is designed to have a small leakage inductance to reduce secondary voltage ringing. Hence, under light load conditions, ZVS of leg 1 devices cannot be achieved. The ZVS conditions are taken into account while calculating the switching losses of the semiconductor devices. The switching energy dependencies on the device current, junction temperature, and external gate resistance have been curve-fitted. Thereafter, utilizing the curve-fitted data, the turn-ON and turn-OFF switching losses have been calculated as described in [25].

The temperature rise in the inductors and the transformer is calculated using the same method as that used in the semiconductor devices. The copper loss expression is $I_M^2 R_M(T_M)$ where I_M is the rms current through the inductor/ transformer winding and R_M is the inductor/ transformer winding resistance. The core loss of the magnetic components is calculated using the improved generalized Steinmetz equation [26]. First, the total loss in a magnetic component is calculated at ambient temperature, then the temperature rise (ΔT_M) is iteratively updated for a specific surface area A_t

$$\Delta T_M = (P_{\text{loss}}/A_t)^{0.826}. \tag{45}$$

The loss distribution diagram at 6.6 kW is depicted in Fig. 10, indicating that the conduction loss is dominant. The efficiency curves for the proposed system and the conventional system are shown in Fig. 11. The loss in PSFB is almost the same for both systems. However, because of high-frequency switching in the AFE, the switching loss becomes substantial, resulting in lower efficiency than the proposed system. The loss distribution at different stages of the proposed system and the conventional system is shown at four different power levels in Fig. 12. The power loss incurred in the current injection circuit is negligible. The passive component loss includes the conduction loss and core loss of the inductors and transformer.

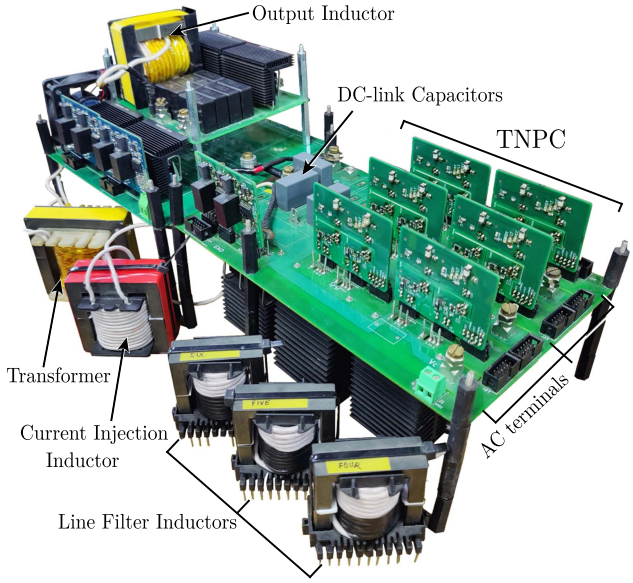

Fig. 13. 6.6-kW hardware prototype of the system.

TABLE IV
SELECTED COMPONENTS BASED ON DESIGNED VALUES

Component	Description
TNPC Devices (S_{j1} - S_{j4})	1000 V SiC MOSFET, C3M0120100 K, Wolfspeed.
Current Injection Half-Bridge Devices (S_1, S_2)	1000 V SiC MOSFET, C3M0120100 K, Wolfspeed.
PSFB Primary Devices (Q_1 - Q_4)	1000 V SiC MOSFET, C3M0120100 K, Wolfspeed.
PSFB Secondary Diodes (D_1 - D_4)	1200 V, 20 A SiC Schottky Diode, C4D20120D, Wolfspeed.
Line Filter Inductor (L_g)	75 µH, 22 turns-250 strands SWG40 Litz wire, ETD 54 core Cosmo Ferrites.
Current Injection Inductor (L_s)	430 µH, 42 turns-250 strands SWG40 Litz wire, EE6527 core Cosmo Ferrites.
Transformer	1:1, 250 strands SWG40 Litz wire, EE8020 core Cosmo Ferrites.
PSFB Output Inductor (L_o)	100 µH, 18 turns-380 strands SWG40 Litz wire, ETD 59 core Cosmo Ferrites.
DC-link Capacitors (C_{rs}, C_{st}, C_{rt})	0.47 µF, 1000 V, metallized polyester film, R60QR34704040K, KEMET.
PSFB Output Capacitor (C_o)	8 x 2 µF, 1100 V, metallized polypropylene film, ECWFG1B205J, Panasonic.
Digital Controller	TMS320F28379D, Texas Instruments.

VII. EXPERIMENTAL RESULTS

A 6.6-kW hardware prototype, as illustrated in Fig. 13, was developed and tested at a grid line-to-line voltage of 400 Vrms. The semiconductor devices and passive components used in the hardware are listed in Table IV. The prototype incorporates SiC

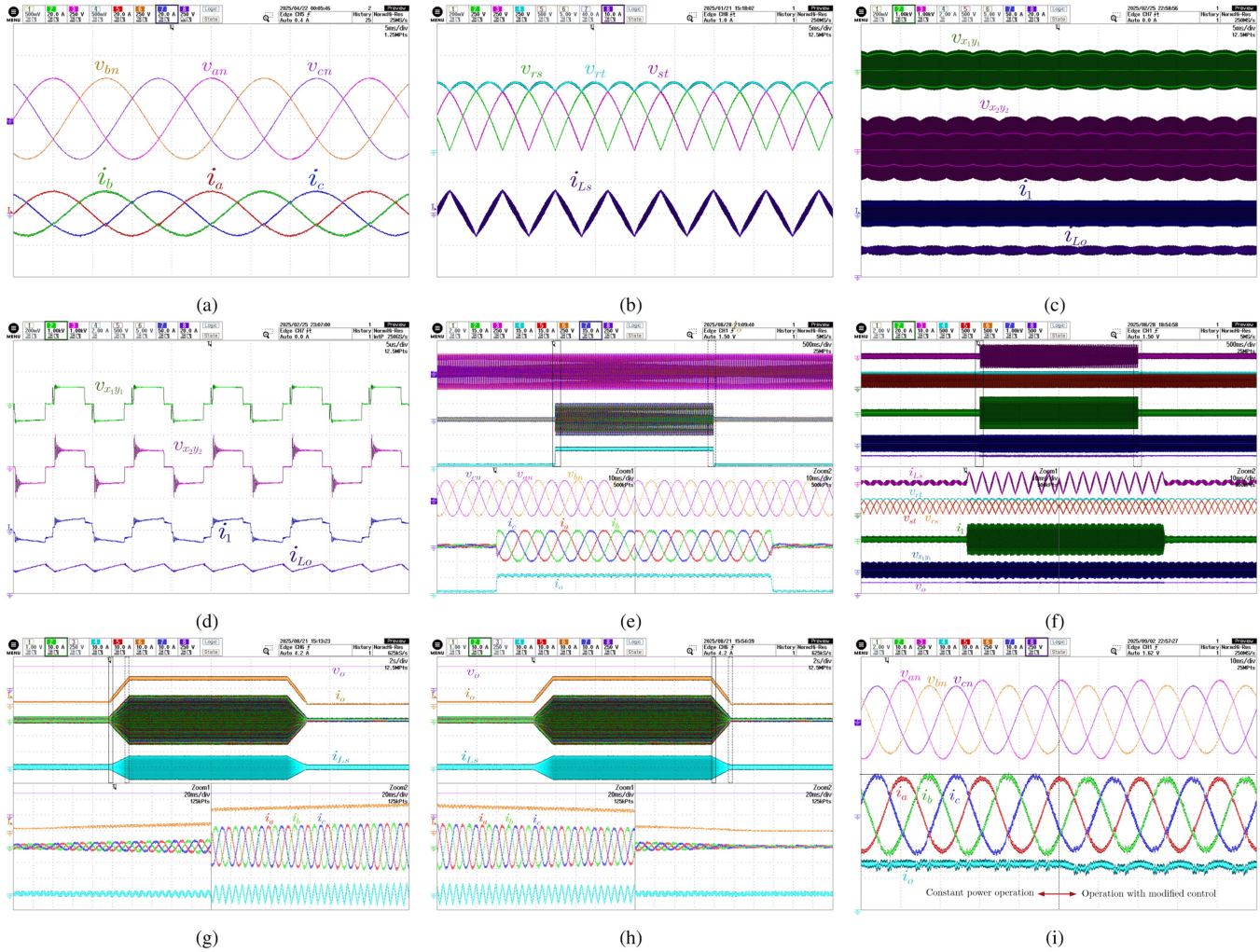

Fig. 14. Experimental results showing (a) line-to-neutral grid voltages (v_{an}, v_{bn}, v_{cn}) and the line currents (i_a, i_b, i_c) at 6.6-kW output power, (b) the variable dc-link voltages (v_{rs}, v_{st}, v_{rt}), and the injected third-harmonic current (i_{L_s}), (c) primary voltage ($v_{x_1y_1}$), secondary voltage ($v_{x_2y_2}$), primary current (i_1) of the transformer, and the output inductor current (i_{L_o}), (d) zoomed version of the waveforms shown in (c); (e), and (f) show a step change from 10% load to full-load, (g), (h) depict a linear load transition from 10% load to full-load in a duration of one second, and (i) demonstrates the operation of the system in an unbalanced grid condition before and after the control modification.

MOSFETs, Schottky diodes, film capacitors in the dc-link, and ferrite core filter inductors in the input side and dc–dc stage.

Fig. 14(a) demonstrates the line-to-neutral grid voltages (v_{an}, v_{bn}, v_{cn}) and the line currents (i_a, i_b, i_c) at 6.6-kW output power with the output voltage regulated at 400 V. The input current THD is 1.7%, and the currents are in phase with the corresponding voltages. The sinusoidal line currents are obtained by the closed-loop operation of the current injection circuit and the PSFB, as explained in Sections II and III.

Fig. 14(b) illustrates the three piecewise sinusoidal dc-link voltages (v_{rs}, v_{st}, and v_{rt}). The six-pulse voltage v_{rt} is the sum of the varying dc-link voltages v_{rs} and v_{st} phase shifted by 60°. The peak value of v_{rt} is 565 V, which is much lower compared to the constant dc-link voltage maintained at the output of the AFE rectifier. The lower peak value of the dc-link voltage reduces the voltage stress on the devices. Due to the variable nature of the voltages, bulky electrolytic capacitors are eliminated from the system, ensuring better reliability and power density. Fig. 14(b) also presents the third-harmonic current (i_{L_s}) injected by the current injection circuit. The peak value of the injected current is half of the peak of the grid current. Fig. 14(c) shows the waveforms of the PSFB converter depicting the transformer primary and secondary voltages ($v_{x_1y_1}, v_{x_2y_2}$), primary current (i_1), and the output inductor current (i_{L_o}). The zoomed waveforms are shown in Fig. 14(d). At the start of each power delivery mode of PSFB, voltage ringing is observed in the secondary voltage waveform. To reduce the ringing, the two windings of the transformer were interleaved, resulting in a leakage inductance of 1.77 μH. No external snubber circuit was employed to reduce the voltage oscillations.

Fig. 14(e)–(h) demonstrates the dynamic response of the system. The step response of the system when the load is changed from 10% to 100% is shown in Fig. 14(e) and (f). The load transition occurs within 1 ms. The system remains in full-load condition for two seconds, and then the load is changed from 100% to 10%. Line currents, third-harmonic currents, and output currents exhibit a smooth transition, as shown in the two zoomed-in windows. Fig. 14(g) and (h) illustrates the dynamic

response when the load is increased linearly over a duration of 1 s. The zoomed-in portions of the waveforms confirm that the line currents remain sinusoidal throughout the transition.

As the instantaneous power of a balanced three-phase ac source is constant, the output current i_o is also constant for a given output voltage. However, if the grid voltages are unbalanced and the output power is still maintained constant, the ac line currents no longer remain sinusoidal. During a voltage imbalance, balanced sinusoidal grid currents can be obtained by allowing the second-harmonic component power in the output. Hence, the third-harmonic current and the output inductor current are controlled in such a way that the output power contains a second-harmonic ripple superimposed on the average value. Fig. 14(i) shows the experimental results in an unbalanced condition when a fundamental negative sequence component of 10 V is present in the grid voltages. The instant at which the control is changed from constant power operation to equal input current control is marked in the diagrams. When the system operates in constant power mode, transferring 5 kW of power to the load, distortions occur in the line currents. The amplitudes of the line currents are also different in this operating mode. After the new control is enabled, the output current i_o contains a second-harmonic oscillation. In [27], a modulation strategy is presented in which the grid currents are proportional to the respective phase voltages during voltage imbalance. However, the control technique implemented for this topology ensures balanced sinusoidal currents in an unbalanced grid condition.

The efficiency of the system is measured using the Hioki PW6001 power analyzer. The experimental efficiency is shown in Fig. 11. The peak efficiency is 97.93%, achieved at 2.5 kW output power. The THD of the input currents is maintained below 5% in the load range from 25% to full load. The minimum THD of 1.7% is recorded at 6.6 kW output power. The power factor is unity throughout the operating region.

VIII. Conclusion

The article discusses an isolated ac–dc converter for EV charging application featuring a line frequency switched TNPC with a partial power processing third-harmonic current injection circuit for PFC. Line frequency switching helps to achieve better efficiency, along with a reduction in the grid filter and dc-link capacitance requirement. The proposed system requires a single isolated dc–dc converter for unity power factor operation using three-phase unfolding. The lower device count and negligible filter requirement make this converter a viable alternative to existing three-phase unfolding-based chargers. A simple closed-loop control strategy is adopted for modulation of the dc–dc stage, incorporating feed-forward duties. The line filter size and analytical efficiency of the system are compared with the conventional two-stage OBC. A detailed comparison is presented with the Swiss rectifier-based topologies, considering the device voltage and current stresses and the magnetic components. A 6.6-kW hardware prototype was developed and tested for experimental validation. The experimental results confirm sinusoidal controllability of the system in both balanced and unbalanced grid conditions while maintaining unity power factor in the entire operating range. The grid currents and the third-harmonic current exhibit a smooth transition when the system is subjected to a step change in load from 10% to 100%. An efficiency over 95% was measured for a load range of 15% to 100%, achieving a peak efficiency of 97.93%.

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