Computationally Efficient Model Predictive Control Based on Adaptive Switching States for Grid-Connected Three-Level ANPC Inverters

Euntaek Nam, *Student Member, IEEE*, and Suyong Chae, *Senior Member, IEEE*

***Abstract*—Finite control set model predictive control (FCS-MPC) is regarded as one of the most powerful controllers for multilevel inverter systems. However, the FCS-MPC still suffers from a heavy computational burden due to its iterative computational process in the control loop. This article proposes a computationally efficient model predictive control (CE-MPC) based on adaptive switching states for grid-connected three-level active neutral-point-clamped (3L-ANPC) inverters. The proposed CE-MPC method optimizes the switching states of the 3L-ANPC inverter by applying three-step constraints of adaptive candidate vector boundary, small voltage vector polarity, and zero switching states operation mode. Therefore, the adaptively selected switching states reduce MPC computation time by up to 84.08% compared to the traditional FCS-MPC algorithm, effectively minimizing the computational burden and freeing up processing resources for other tasks. The feasibility and effectiveness of the proposed CE-MPC method are experimentally validated using a 3 kW hardware prototype.**

***Index Terms*—Adaptive switching states, finite control set model predictive control (FCS-MPC), grid-connected application, multilevel inverters, three-level active neutral-point-clamped (3L-ANPC).**

I. Introduction

With the growing penetration of inverter-based resources (IBRs), the multilevel inverters are being increasingly adopted to improve power quality [1], [2]. For medium- and high-power systems, the voltage stress on semiconductor switches must be reduced and balanced to extend device lifetime and reduce operational costs [3]. Among various multilevel inverter topologies, such as T-Type [4], cascaded H-bridges [5], and neutral-point-clamped [6], [7], three-level neutral point clamped (3L-NPC) has attracted interest in the field of IBRs as it could use power semiconductor devices with low voltage stress. However, unbalanced voltage stress across the switch devices can lead to uneven power dissipation and thermal stress, which may indirectly limit the output current and power delivery range. The main drawbacks of the 3L-NPC inverter include unequal power dissipation and junction temperature imbalance, both of which accelerate aging of specific switches [8], [9].

The three-level active neutral-point-clamped (3L-ANPC) topology was introduced to overcome the drawbacks of the 3L-NPC and is a promising solution in three-level multilevel topology [10], [11]. The 3L-ANPC inverter features multiple redundant zero switching state operation modes, which result in varying voltage stress across the switching devices. This redundancy provides additional degrees of freedom, enabling the inverter to select appropriate switching states and achieve balanced voltage stress.

As the 3L-ANPC inverter emerges as a promising multilevel structure for medium-, and high-power applications, various advanced control strategies and modulation methods have been proposed to control its key parameters, such as power loss, output current and voltage, and dc-link capacitor voltages [12], [13]. However, various pulsewidth modulation techniques for 3L-ANPC inverters significantly increase the complexity of optimal controller design. In grid-connected inverter systems, multiobjective control plays a critical role in handling dc-link voltages, phase currents, voltage stress, and current limitation. As the number of control variables increases, conventional linear controllers, such as proportional-integral or proportional-resonant controllers [14], [15], become increasingly difficult to design, thereby making efficient and reliable operation more challenging.

Finite control set model predictive control (FCS-MPC) is one of the most popular model predictive control (MPC) methods in multilevel inverters and is widely studied in power electronics converters and drive applications [16], [17], [18], [19]. FCS-MPC has the advantages of fast dynamic response, effective incorporation of multiple constraints, and an intuitive design that exploits the discrete nature of power converters. One of its outstanding features is the multiobjective control by applying a well-designed cost function, making it suitable for grid-connected multilevel inverters. However, in a practical application, the main drawback of FCS-MPC is that it requires a large number of calculations within the control loop. For example, in the three-level inverter, the controller requires an iteration of $3^3 = 27$ candidate switching states to evaluate the

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The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea (e-mail: net1210@postech.ac.kr; sychae@postech.ac.kr).

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cost function, and at least 27 iterations are implemented in each control cycle.

To fully exploit the advantages of FCS-MPC, its calculation time must be minimized. To address this challenge, numerous studies have been presented to reduce the computational burden by optimizing the switching states. For instance, a two-stage MPC method for 3L-NPC inverter-fed permanent-magnet synchronous machine (PMSM) drive is proposed in [20]. This approach selects a small hexagon in the first stage and rearranges the voltage vector duty cycles at its center in the second stage. By decoupling the control into two stages, the number of cost function evaluations is reduced to 12, simplifying the computational burden. Similarly, in [21], a weighting-factor-less MPC method is proposed for a 3L-Hybrid ANPC inverter-fed PMSM drive. This method divides the control process into three steps, reducing the switching states from 27 to 8. In [22], an optimal MPC method is proposed to optimize the switching states of a five-level ANPC inverter. The rolling optimization is reduced from 125 to 15, with weighting factors adjusted based on the priorities of control objectives. A comparable method, as presented in [23], [24], and [25], reduces the set of candidate switching states to achieve multiobjective control in grid-connected 3L-ANPC inverters. Although [25] demonstrated the potential for effectively reducing the computation time, it lacks sufficient theoretical analysis and validation regarding the optimization of the candidate switching states and the selection of zero switching states. In [26], sequential layers are introduced to eliminate weighting factors and reduce the number of iterations required for cost function evaluations. The sequential MPC in [27] evaluates candidate voltage vectors twice to reduce the number of switching states and improve control performance.

In [28], the candidate regions are divided into hexagon and triangle sectors to further reduce the computational burden. The switching states of a 3L-NPC back-to-back converter with a wind turbine system are reduced to 12 for hexagon sectors and to a mean value of 4.6 when triangle sectors are used. In [29] and [30], divide large hexagon sectors in the space vector into small triangle sectors to reduce unnecessary candidate switching states based on the deadbeat concept. A similar subsector selection strategy was employed in [31] using optimal switching sequence MPC (OSS-MPC), reducing execution time by approximately 40% compared to prior OSS-MPC methods.

Extensive research has focused on mitigating the computational burden of FCS-MPC by reducing candidate switching states. However, high-complexity control schemes remain challenging to implement on digital controllers with limited processing capabilities, and computation time is often insufficient to add other control algorithms, such as state observers and protection, within the control loop. The control performance of FCS-MPC improves with higher sampling frequency, as switching is restricted to time instants that are integer multiples of the sampling period [32]. The competitiveness of FCS-MPC can be improved by utilizing predefined effective switching states, which significantly reduce the computational burden and avoid the implementation of complex algorithmic structures.

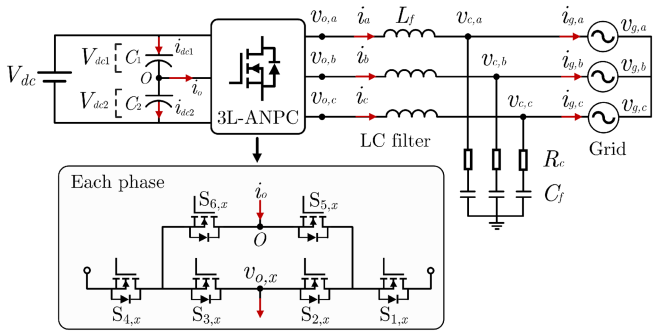

Fig. 1. Grid-connected 3L-ANPC inverter with an LC filter.

In this article, a computationally efficient model predictive control (CE-MPC) based on adaptive switching states is proposed for grid-connected 3L-ANPC inverters. The proposed method controls the grid-injected current and dc-link capacitor voltage of the 3L-ANPC inverter by adaptively selecting candidate switching states, thereby eliminating the need for weighting factors in the cost function. The main contribution of CE-MPC is a substantial reduction in computation time. This is achieved by analyzing a grid-connected inverter system in detail and optimizing the number of switching states used for the cost function evaluation. The three-step constraints are applied to guide the adaptive selection of the switching states.

1) Define the candidate vector boundary and limit the transitions of voltage vectors by considering the trajectory of the reference output voltage vector, effectively reducing the number of candidate voltage vectors evaluated during the iteration process.
2) Constrain the current path to the dc-link capacitors by classifying small voltage vectors between the positive and negative small voltage vectors.
3) Select essential zero switching states to distribute the voltage stress on the power switches, so only two zero switching states are enough to be used for the control.

The rest of this article is organized as follows. Section II describes the system modeling of the grid-connected 3L-ANPC inverter and prediction model for FCS-MPC. Section III introduces the proposed CE-MPC method. Section IV presents experimental results to demonstrate the effectiveness of the proposed method. Finally, Section V concludes this article.

II. System Modeling

A. Topology Description

The grid-connected 3L-ANPC inverter with an LC filter is shown in Fig. 1. $V_{\rm dc}$ is the dc input voltage, $V_{\rm dc1}$ and $V_{\rm dc2}$ are the dc-link voltages for capacitors C_1 and C_2, respectively. $i_{\rm dc1}$ and $i_{\rm dc2}$ are the dc-link capacitor currents and i_o is the neutral point current. L_f and C_f represent the filter inductor and capacitor, and the damping resistance R_c is connected in series at C_f. Each phase is composed of six switches $S_{1,x}$–$S_{6,x}$ $(x = a, b, c)$, and the inverter-side output voltage is $v_{o,abc}$. The inverter-side current is i_{abc}, and the filter capacitor voltage is $v_{c,abc}$. $i_{g,abc}$ and $v_{g,abc}$ represent the grid-injected current and voltage, respectively.

TABLE I
SWITCHING STATES OF THE 3L-ANPC INVERTER

States	$S_{1,x}$	$S_{2,x}$	$S_{3,x}$	$S_{4,x}$	$S_{5,x}$	$S_{6,x}$	S_x	$v_{o,x}$
[P]	1	1	0	0	0	1	1	$V_{dc}/2$
[ZU1]	0	1	0	0	1	0	0	0
[ZU2]	0	1	0	1	1	0	0	0
[ZU3]	0	1	0	0	1	1	0	0
[ZUL]	0	1	1	0	1	1	0	0
[ZL1]	0	0	1	0	0	1	0	0
[ZL2]	1	0	1	0	0	1	0	0
[ZL3]	0	0	1	0	1	1	0	0
[N]	0	0	1	1	1	0	-1	$-V_{dc}/2$

In Table I, the 3L-ANPC inverter has the following states: [P] state, [Z] state, and [N] state. [P] and [N] states represent the positive and negative switching states, [ZU] represents the upper-side zero switching state, and [ZL] represents the lower-side zero switching state. [ZUL] represents the both-side zero switching state, where neutral point current flows switch $S_{2,x}$, $S_{3,x}$, $S_{5,x}$, and $S_{6,x}$.

B. Mathematical Model of Grid-Connected 3L-ANPC Inverter

According to the states in Table I, $v_{o,x}$ is calculated by a linear combination of S_x ($x = a, b, c$) as

$$v_{o,x} = \left[\tfrac{1}{2}V_{\text{dc}} \quad 0 \quad -\tfrac{1}{2}V_{\text{dc}}\right]^T \tag{1}$$

where S_x takes values of 1, 0, or -1, enabling $v_{o,x}$ to produce a three-level output voltage.

The continuous-time state-space equation of the grid-connected 3L-ANPC inverter can be expressed as

$$\frac{d}{dt}\underbrace{\begin{bmatrix} i_{\alpha\beta}(t) \\ v_{c,\alpha\beta}(t) \end{bmatrix}}_{x_{\alpha\beta}(t)} = \underbrace{\begin{bmatrix} 0 & -1/L_f \\ 1/C_f & 0 \end{bmatrix}}_{A_c}\begin{bmatrix} i_{\alpha\beta}(t) \\ v_{c,\alpha\beta}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L_f \\ 0 \end{bmatrix}}_{B_c} v_{o,\alpha\beta}(t) + \underbrace{\begin{bmatrix} 0 \\ -1/C_f \end{bmatrix}}_{D_c} i_{g,\alpha\beta}(t) \tag{2}$$

where the system parameters $i_{\alpha\beta}$, $v_{c,\alpha\beta}$, $i_{g,\alpha\beta}$, and $v_{o,\alpha\beta}$ are obtained by using Clarke transformation from the abc frame to the stationary $\alpha\beta$ frame.

The continuous-time state-space equation in (2) is discretized using the zero-order hold method with a sampling period T_s as follows:

$$x_{\alpha\beta}(k+1) = A_d\, x_{\alpha\beta}(k) + B_d v_{o,\alpha\beta}(k) + D_d i_{g,\alpha\beta}(k) \tag{3}$$

where matrices A_d, B_d, and D_d are defined as

$$A_d = e^{A_c T_s} \quad B_d = \int_0^{T_s} e^{A_c\tau} B_c d\tau \quad D_d = \int_0^{T_s} e^{A_c\tau} D_c d\tau. \tag{4}$$

As shown in Fig. 1, the 3L-ANPC inverter consists of two dc-link capacitors and a neutral point, and the discrete-time prediction model for the dc-link capacitors can be derived using Euler's forward formula as follows:

$$\begin{bmatrix} V_{\text{dc1}}(k+1) \\ V_{\text{dc2}}(k+1) \end{bmatrix} = \begin{bmatrix} V_{\text{dc1}}(k) \\ V_{\text{dc2}}(k) \end{bmatrix} + \begin{bmatrix} T_s/C_1 & 0 \\ 0 & T_s/C_2 \end{bmatrix}\begin{bmatrix} i_{\text{dc1}}(k) \\ i_{\text{dc2}}(k) \end{bmatrix}. \tag{5}$$

The neutral-point current i_o can be calculated from the linear combination of the inverter-side current and the switching state, which can be expressed as

$$i_o(k) = (1-|S_a|)\, i_a(k) + (1-|S_b|)\, i_b(k) + (1-|S_c|)\, i_c(k) \tag{6}$$

or:

$$i_o(k) = i_{\text{dc1}}(k) - i_{\text{dc2}}(k). \tag{7}$$

Under the assumption of a balanced system, the three-phase output currents satisfy $i_a(k) + i_b(k) + i_c(k) = 0$. Then, (6) can be simplified as

$$i_o(k) = -|S_a|\, i_a(k) - |S_b|\, i_b(k) - |S_c|\, i_c(k). \tag{8}$$

Therefore, the discrete-time prediction model for the neutral-point potential can be formulated as

$$\Delta V_{\text{dc}}(k+1) = \Delta V_{\text{dc}}(k) + (T_s/C_{\text{dc}})\, i_o(k) \tag{9}$$

where C_{dc} represents the capacitance of C_1 and C_2, which are assumed to be identical. $\Delta V_{\text{dc}}(k+1)$ and $\Delta V_{\text{dc}}(k)$ are the difference between V_{dc1} and V_{dc2} at (k) and $(k+1)$, respectively.

The current reference is calculated from the point of common coupling voltage and active/reactive power reference

$$i^\star_{g,\alpha}(k) = \frac{2}{3}\,\frac{v_{c,\alpha}(k)\,\text{P}_{\text{ref}} + v_{c,\beta}(k)\,\text{Q}_{\text{ref}}}{v^2_{c,\alpha}(k) + v^2_{c,\beta}(k)} \tag{10}$$

$$i^\star_{g,\beta}(k) = \frac{2}{3}\,\frac{v_{c,\beta}(k)\,\text{P}_{\text{ref}} - v_{c,\alpha}(k)\,\text{Q}_{\text{ref}}}{v^2_{c,\alpha}(k) + v^2_{c,\beta}(k)} \tag{11}$$

where $i^\star_{g,\alpha}(k)$ and $i^\star_{g,\beta}(k)$ are the grid-side current reference, and P_{ref} and Q_{ref} are the active/reactive power reference, respectively.

In the Laplace domain, the inverter-side current reference $i^\star_{\alpha\beta} = i^\star_\alpha + j i^\star_\beta$ can be calculated in the stationary $\alpha\beta$ frame as

$$\begin{cases} i^\star_\alpha(k) = i^\star_{g,\alpha}(k) - \omega C_f v_{c,\beta}(k) \\ i^\star_\beta(k) = i^\star_{g,\beta}(k) + \omega C_f v_{c,\alpha}(k) \end{cases} \tag{12}$$

where ω represents the nominal angular frequency.

The second-order generalized integrator (SOGI) is applied to extract the fundamental components of the current reference [33]. The transfer functions are defined as

$$G_{i\alpha}(s) = \frac{k_s\omega_g s}{s^2 + k\omega_g s + \omega_g^2} \tag{13}$$

$$G_{i\beta}(s) = \frac{k_s\omega_g^2}{s^2 + k\omega_g s + \omega_g^2} \tag{14}$$

where k_s denotes the SOGI damping gain, which is set as 1.414 and ω_g is the grid angular frequency.

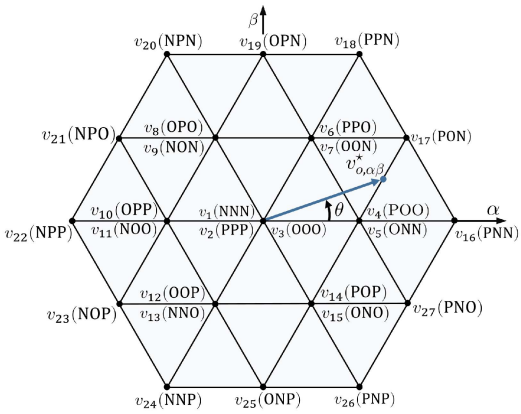

Fig. 2. Voltage vectors in the space vector diagram of the 3L-ANPC inverter. θ denotes the angle of the grid voltage and $v^{\star}_{o,\alpha\beta}$ denotes the magnitude of reference voltage vector.

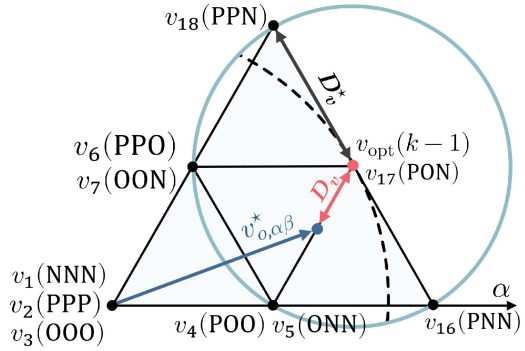

Fig. 3. Schematic diagram of effective boundary for candidate voltage vectors when $v_{opt}\ (k-1) = v_{17}$. The corresponding candidate set is $v_{o,\alpha\beta}(k) \triangleq [v_4, v_5, v_6, v_7, v_{16}, v_{17}, v_{18}]$.

Given that the current reference is obtained at grid frequency ($f_g = 50$ or 60 Hz), it changes slowly compared to the dynamics of the prediction model operating at the sampling period. Therefore, the current reference is predicted using the Lagrange extrapolation

$$i^{\star}_{\alpha\beta}\ (k+1) = 3i^{\star}_{\alpha\beta,f}\ (k) - 3i^{\star}_{\alpha\beta,f}\ (k-1) + i^{\star}_{\alpha\beta,f}\ (k-2) \tag{15}$$

$$i^{\star}_{\alpha\beta}\ (k+2) = 3i^{\star}_{\alpha\beta}\ (k+1) - 3i^{\star}_{\alpha\beta,f}\ (k) + i^{\star}_{\alpha\beta,f}\ (k-1) \tag{16}$$

where $i^{\star}_{\alpha\beta,f}(k)$ denotes the filtered current reference dervied from $i^{\star}_{\alpha\beta}(k)$ using (13) and (14).

III. Proposed CE-MPC Method

The proposed CE-MPC eliminates the requirements for all 27 switching states and weighting factors when calculating the minimum cost function by employing an adaptively reduced set of switching states. This significantly reduces the excessive computational burden and enables faster switching operations. The control algorithm involves three-step constraints: 1) adaptive candidate vector boundary; 2) small voltage vector polarity; and 3) the zero switching state operation mode.

A. Step 1 - Adaptive Candidate Vector Boundary

Fig. 2 illustrates the reference output voltage vector $v^{\star}_{o,\alpha\beta}\angle\theta$ rotating synchronously in the space vector plane with grid frequency, and it can be calculated as

$$v^{\star}_{o,\alpha\beta}\ (k) = v_{c,\alpha\beta}\ (k) + (L_f/T_s)\left(i^{\star}_{\alpha\beta}\ (k+1) - i_{\alpha\beta}\ (k)\right) \tag{17}$$

where $v^{\star}_{o,\alpha\beta}(k)$ denotes the discrete-time form of $v^{\star}_{o,\alpha\beta}\angle\theta$.

Since $v^{\star}_{o,\alpha\beta}(k)$ is derived from $i^{\star}_{\alpha\beta}(k+1)$, which rotates at the same angular frequency θ, minimizing the distance between candidate voltage vector $v_{o,\alpha\beta}(k)$ and $v^{\star}_{o,\alpha\beta}(k)$ leads to accurate current tracking. Therefore, among the candidates $v_{o,\alpha\beta}(k) \triangleq [v_1, \ldots, v_{27}]$, the optimal voltage vector $v_{\rm opt}(k)$ that minimizes the distance to $v^{\star}_{o,\alpha\beta}(k)$ should be selected. Minimizing the current tracking error inherently leads to selecting a voltage vector that closely approximates $v^{\star}_{o,\alpha\beta}(k)$, thereby achieving the same objective. Therefore, the cost function can be formulated solely based on $i_{\alpha\beta}(k+1)$ and $i^{\star}_{\alpha\beta}(k+1)$. Assuming balanced dc-link capacitor voltages, their influence on current tracking can be considered negligible at this step.

Fig. 3 illustrates the boundary of the candidate voltage vector region when v_{17} is selected as $v_{\rm opt}(k-1)$. The blue line boundary indicates the feasible region of $v^{\star}_{o,\alpha\beta}(k)$, whose radius $\boldsymbol{D^{\star}_v}$ corresponds to the one-level distance between adjacent voltage vectors. The radius $\boldsymbol{D^{\star}_v}$ is calculated as

$$\begin{aligned}\boldsymbol{D}^{\star}_{v}\ (v_x, v_y) = \frac{V_{\rm dc}}{3} \big|\big| &\left(S\left(v_{x,a}\right) - S\left(v_{y,a}\right)\right) \\ &+ \mathrm{a}\left(S\left(v_{x,b}\right) - S\left(v_{y,b}\right)\right) \\ &+ \mathrm{a}^2\left(S\left(v_{x,c}\right) - S\left(v_{y,c}\right)\right)\big|\big|_2 = \frac{V_{\rm dc}}{3}\end{aligned} \tag{18}$$

where $S(v_x)$ and $S(v_y)$ are the switching states corresponding to voltage vectors v_x and v_y, and $\mathrm{a} = e^{j2\pi/3}$.

Since $v^{\star}_{o,\alpha\beta}(k)$ does not vary dramatically between control cycles, $v_{\rm opt}(k)$ is selected within a circular region centered at the previously selected voltage vector $v_{\rm opt}(k-1)$. Therefore, the distance $\boldsymbol{D_v}$ between $v_{\rm opt}(k)$ and $v^{\star}_{o,\alpha\beta}(k)$ remains within one-level distance $\boldsymbol{D^{\star}_v}$. Accordingly, the distance between $v_{\rm opt}(k)$ and $v_{\rm opt}(k-1)$ is restricted within one-level distance, expressed as

$$\|v_{\rm opt}\ (k) - v_{\rm opt}\ (k-1)\| \le \boldsymbol{D^{\star}_v} \tag{19}$$

$$\|v^{\star}_{o,\alpha\beta}\ (k) - v_{\rm opt}\ (k-1)\| = \boldsymbol{D_v}\ \ \boldsymbol{D_v} \le \boldsymbol{D^{\star}_v}. \tag{20}$$

To reduce a computational effort while maintaining tracking performance, voltage vectors beyond the one-level boundary are excluded from the candidate set.

B. Step 2 - Small Voltage Vector Polarity

The 3L-ANPC inverter has 27 switching states, which produce 19 different voltage vectors, as shown in Fig. 2. These voltage vectors are categorized into zero, small, medium, and

TABLE II
VOLTAGE VECTOR CLASSIFICATION

Type	Voltage Vector Type	Symbol
I	Zero Voltage Vector	v_1, v_2, v_3
II	Positive Small Voltage Vector	v_4, v_6, v_8, v_{10}, v_{12}, v_{14}
III	Negative Small Voltage Vector	v_5, v_7, v_9, v_{11}, v_{13}, v_{15}
IV	Medium Voltage Vector	v_{17}, v_{19}, v_{21}, v_{23}, v_{25}, v_{27}
V	Large Voltage Vector	v_{16}, v_{18}, v_{20}, v_{22}, v_{24}, v_{26}

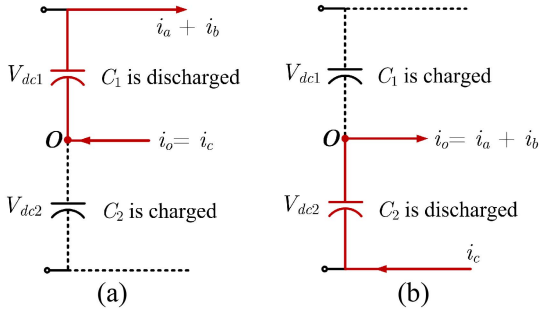

Fig. 4. Current path depending on small voltage vectors. (a) Positive voltage vector [PPO]. (b) Negative voltage vector [OON].

large voltage vectors based on their magnitudes. Among them, the small and medium voltage vectors listed in Table II include zero switching states that connect the current path to the neutral point, thus affecting the neutral-point current i_o.

DC-link capacitor voltages vary depending on the direction of the capacitor current, where positive and negative voltage vectors generate complementary current directions. While the medium voltage vector includes both positive and negative switching states, the direction of the neutral-point current cannot be directly influenced by these vectors. Therefore, the small voltage vectors are employed to regulate both the direction of capacitor current and the neutral-point current. By dividing these vectors into positive and negative groups and selecting between them based on a comparison between $V_{\rm dc1}$ and $V_{\rm dc2}$, dc-link capacitor voltage balancing can be achieved.

Fig. 4 illustrates an example of a current path depending on the polarity of small voltage vectors. When $V_{\rm dc1} \geq V_{\rm dc2}$, the positive small voltage vector group is selected. In the case of Fig. 4(a), i_o is calculated using (6) as follows:

$$i_o = i_c \tag{21}$$

where i_o flows into C_1, and the dc-link capacitor voltage variation is predicted from (9). As C_1 is discharged, $V_{\rm dc1}$ decreases. To maintain the total dc-link voltage $V_{\rm dc}$, the dc source supplies a compensating current that charges C_2, resulting in an increase in $V_{\rm dc2}$. This complementary behavior preserves voltage balance in the dc-link capacitors.

Conversely, when $V_{\rm dc1} < V_{\rm dc2}$, the negative small voltage vector group is selected. In the case of Fig. 4(b), i_o can be written as

$$i_o = i_a + i_b \tag{22}$$

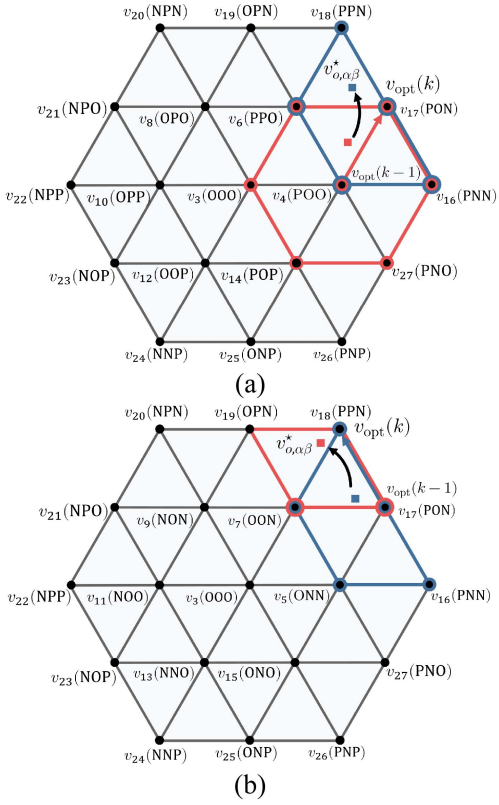

Fig. 5. Schematic diagram of the candidate vector boundary transition. (a) v_4 to v_{17} transition when $V_{\rm dc1} \geq V_{\rm dc2}$. (b) v_{17} to v_{18} case when $V_{\rm dc1} < V_{\rm dc2}$.

where i_o flows into C_2, resulting in a decrease in $V_{\rm dc2}$, which in turn leads to an increase in $V_{\rm dc1}$. Therefore, dc-link capacitor voltage balancing can be solved without adding a control objective term (9) in the cost function.

In the case of the zero voltage vectors in Table II, v_1 and v_2 are excluded from Type I since both produce the same voltage magnitude as v_3 and do not affect neutral-point potential balancing.

Fig. 5 illustrates examples of candidate vector boundary transitions by applying the Step-1 and Step-2 constraints. According to the Step-1 constraint, voltage vectors located within a one-level boundary from $v_{\rm opt}(k-1)$ are grouped together. Thus, the number of candidate voltage vectors is adaptively reduced to a range of 4 to 7.

C. Step 3 - Zero Switching States Operation Mode

In a 3L-ANPC inverter, the output voltage $v_{o,abc}$ is generated by switching between the [P] and [Z] switching states during the positive half-cycle, and between the [N] and [Z] switching states during the negative half-cycle. The selection of zero switching states [Z] directly influences the voltage stress on the switches.

As summarized in Table I, the 3L-ANPC inverter topology typically provides seven types of zero switching state modes [34], [35], [36], each resulting in a different voltage stress across individual switches ranging from 0 to $V_{\rm dc}/2$. Fig. 6 describes the commutation behavior for the three cases, [Z1], [Z2], and [Z3],

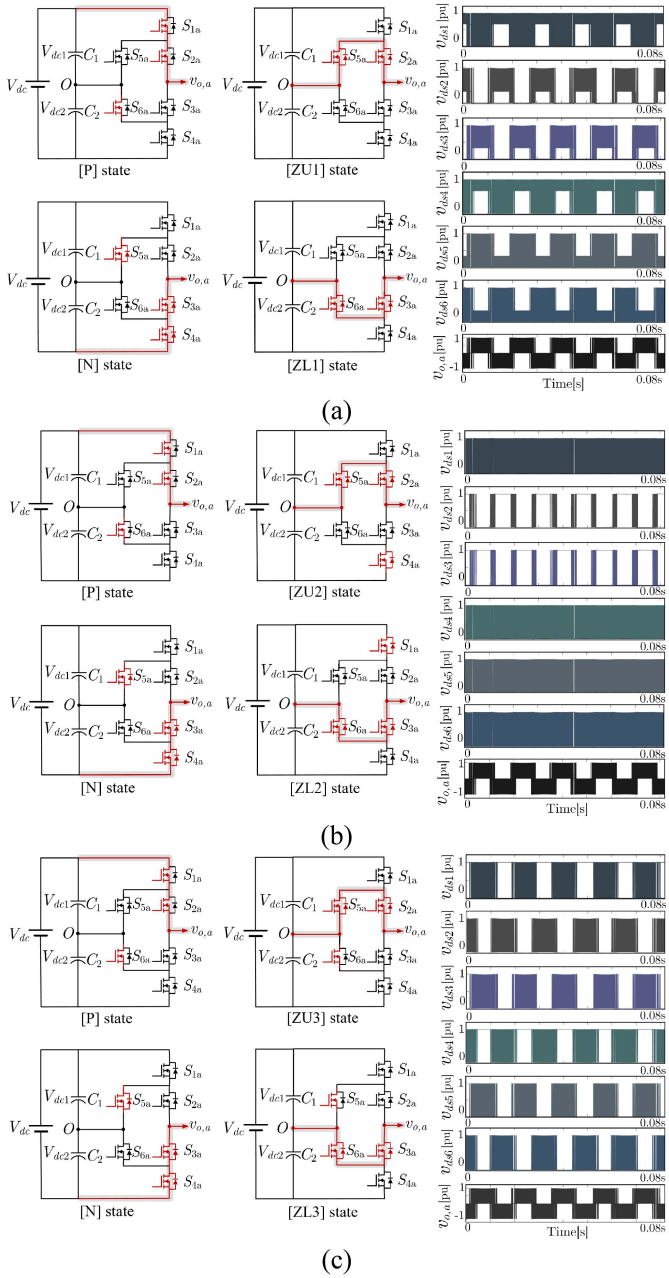

Fig. 6. Switching transitions and the corresponding voltage stress across the switches under $i_a > 0$. (a) [ZU1] and [ZL1]. (b) [ZU2] and [ZL2]. (c) [ZU3] and [ZL3].

along with their corresponding drain-source voltage v_{ds} and output voltage $v_{o,a}$. [Z1] represents the pair of [ZU1] and [ZL1], and [Z2] and [Z3] are defined similarly for their corresponding upper and lower zero switching states. In the commutation loop from [P] to [ZU1] and from [N] to [ZL1] in Fig. 6(a), excessive switching transitions occur on S_5 and S_6, leading to unbalanced voltage stress among the switches within the commutation loop. In the case of [P] to [ZU2] and [N] to [ZL2] in Fig. 6(b), S_2 and S_3 operate at the lower switching frequency, while excessive switching still occurs on S_1, S_4, S_5, and S_6. In [ZUL] state, S_2, S_3, S_5, and S_6 are simultaneously turned ON during

Algorithm 1: Cost Function Evaluation for CE-MPC.

Input: $i(k)$, $v_c(k)$, $i_g(k)$, $v_g(k)$, $V_{dc1}(k)$, and $V_{dc2}(k)$
Initialize: $g_{\text{prop,opt}} \leftarrow \inf$, $\mathrm{S}_{x,\text{opt}} \leftarrow 0$, $x_{\text{opt}} \leftarrow 0$
Clarke transformation of sampling values
Calculate the reference by (10)-(16)
Read the previous optimal voltage vector $v_{\text{opt}}(k-1)$
if $V_{dc1}(k) \geq V_{dc2}(k)$ **then**
  Select the positive small voltage vector group
else
  Select the negative small voltage vector group
end if
Determine the optimal iteration length
for $j = 1 : \mathrm{S}_{\text{adap}}(v_{\text{opt}})$ **do**
  Calculate $v_{o,\alpha\beta}(k)$ and $v_{o,\alpha\beta}(k+1)$ from S_x
  Predict $i_{\alpha\beta}(k+2)$, $i_{\alpha\beta}(k+1)$, $v_{c,\alpha\beta}(k+1)$
  Calculate g_{opt} based on (25)
  if $g_{\text{prop},j} < g_{\text{prop,opt}}$ **then**
    $g_{\text{prop},opt} \leftarrow g_{\text{prop},j}$
    $S_{x,\text{opt}} \leftarrow S_x$
  end if
end for
Update $v_{\text{opt}}(k-1)$ from $v_{\text{opt}}(k)$
if $v_{c,x}(k) \geq 0$ & $S_x == 0$ **then**
  $[\mathrm{Z}]_{1\times 6} = [\mathrm{ZU3}]$
end if
if $v_{c,x}(k) < 0$ & $S_x == 0$ **then**
  $[\mathrm{Z}]_{1\times 6} = [\mathrm{ZL3}]$
end if
Output: $(S_{a,\text{opt}}, S_{b,\text{opt}}, S_{c,\text{opt}})$

commutation, which violates the complementary operation of switch pairs and increases the risk of short circuit [36].

In contrast, the commutation paths from [P] to [ZU3] and from [N] to [ZL3], as shown in Fig. 6(c) ensure a more balanced voltage stress distribution across all switches and prevent excessive switching transitions on specific devices, which can lead to uniform thermal distribution and reliable long-term operation. Leveraging the characteristics of FCS-MPC, the appropriate selection of zero switching state operation mode can mitigate these imbalances through a simple algorithm without additional layers in the control loop.

The proposed CE-MPC selects the [P] to [ZU3] transition during the positive half-cycle and the [N] to [ZL3] transition during the negative half-cycle of $v_{c,x}(x = a, b, c)$, as shown in Fig. 6(c), and the switching condition is formulated as follows:

$$[\mathrm{Z}]_{1\times 6} = \begin{cases} [\mathrm{ZU3}], & v_{c,x} \geq 0 \;\&\; S_x = 0 \\ [\mathrm{ZL3}], & v_{c,x} < 0 \;\&\; S_x = 0 \end{cases} \tag{23}$$

where $[\mathrm{Z}]_{1\times 6}$ denotes the selected zero switching states.

D. Implementation Procedure

In practical implementations, the turn-ON or turn-OFF signal is updated at time step $(k+1)$ due to the control latency of the digital controller. To compensate for this control delay, the

TABLE III
COMPARATIVE ANALYSIS WITH OTHER MPC SCHEMES

Description	FCS-MPC [16],[39]	MO^2-MPC [23],[24]	Sequential MPC [27]	Sequential MPC [26]	FCS-MFPC [40]	Sequential MPC [21]	FSS-MPC [29],[30]	**Proposed CE-MPC**
Topology / Application	3L-NPC/ Grid	3L-ANPC/ Grid	3L-T-type/ RL Load	3L-T-type/ Grid	3L-NPC/ RL Load	3L-HANPC/ PMSM	3L-T-type/ Grid	**3L-ANPC/ Grid**
Multi-objective optim.	Weighting factor	Weighting factor	Sequential lexicographic	Multi-layer Sequential	Online NNA/ Priority-based	Multi-stage Sequential	Small sector identification	**Three-step Constraints**
Use of weighting factors	Yes	Yes	No	No	No	No	No	**No**
Number of candidate switching states	27	5 to 15	10	8	27	8	3	**4 to 7**
Number of iterative loops	27	27 + α	26 + α	19 + α	19 + α	8	3 + 10	**4 to 7**
Computation burden	High	High	High	High	Relatively High	Moderate	Moderate	**Low**
Steady-state performance	Moderate	Moderate	Moderate	Good	Good	Good	Good	**Good**
Dynamic response	Fast	Fast	Very fast	Fast	Fast	Fast	Fast	**Fast**
Robustness under grid distortion	Not considered	Not considered	Not considered	Not considered	Not considered	Not considered	Not considered	**Robust**

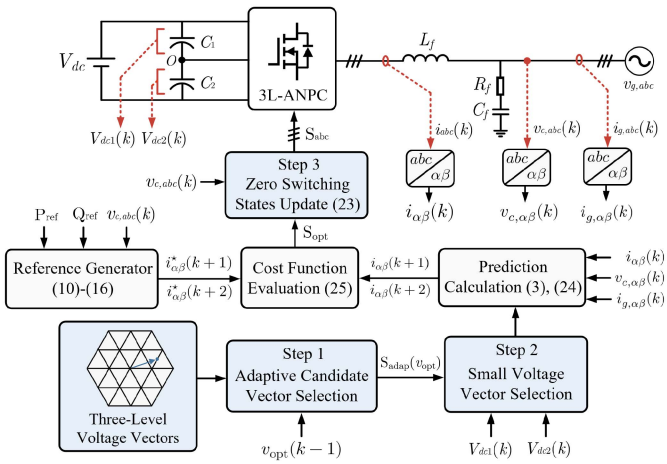

Fig. 7. Control block diagram of the proposed CE-MPC.

prediction model is shifted forward by one period and can be formulated as

$$i_{\alpha\beta}\ (k+2) = i_{\alpha\beta}\ (k+1) + (T_s/L_f)\,(v_{o,\alpha\beta}\,(k+1) - v_{c,\alpha\beta}\,(k+1))\,. \tag{24}$$

Therefore, the cost function of CE-MPC can be expressed as

$$g_{\text{prop},j} = \sum_{N_p=1}^{2} \left(i^{\star}_{\alpha\beta}\,(k+N_p) - i_{\alpha\beta,j}\,(k+N_p)\right)^2 \tag{25}$$

where $j = 1, \ldots, S_{\text{adap}}(v_{\text{opt}})$ is the index of the iterative process and N_p represents the prediction horizon.

Algorithm 1 summarizes the procedure for evaluating the cost function in CE-MPC. The process relies exclusively on sampled data and the previously selected voltage vector. This mechanism avoids the need for complex decision-making and remains uniformly bounded within a finite set, while maintaining stability [30], [37], [38]. Fig. 7 illustrates the block diagram of the proposed CE-MPC.

E. Comparative Analysis With Other MPC Schemes

The main objective of the grid-connected three-level inverter system is to track the current reference while maintaining constant dc-link capacitor voltages. The effectiveness of the proposed CE-MPC is validated through comparison with other MPC schemes presented in Table III that either optimize switching states or eliminate weighting factors.

The conventional multiobjective model predictive control (MO-MPC) scheme presented in literature [16], [22], [23], [24], [39] prioritizes control objectives based on their importance in control. This approach evaluates all 27 switching states and employs weighting factors to control the multiobjectives. Among them, [22], [23], [24] filter out switching states that degrade control performance prior to cost function evaluation. It limits the excessive phase voltage variation and prohibits direct transitions between $S_x = 1$ and $S_x = -1$.

Although MO-MPC solves switching state optimization, the weighting factor design and filtering process still require considerable effort and computation time. As a result, higher sampling frequency and freeing up computational resources for other tasks become challenging.

The sequential MPC method in [26] eliminates the need for weighting factors by dividing the control layers according to the priority of control objectives. However, its performance is highly sensitive to layer configuration, and multiple iterative steps are required to filter candidate switching states and reconstruct feasible input vectors. Similarly, the tolerant-sequential MPC in [27] presents a lexicographic optimization framework to avoid weighting factor tuning and improve control performance, but requires at least 26 iterations to construct the candidate set at every sampling period.

The FCS model-free predictive control scheme in [40] follows the MO-MPC approach, but separates the objective terms in the cost function according to the neutral-point voltage. The sequential MPC approach in [21] eliminates weighting factors by employing multistage optimization and sector identification. Although both approaches decouple the objective terms,

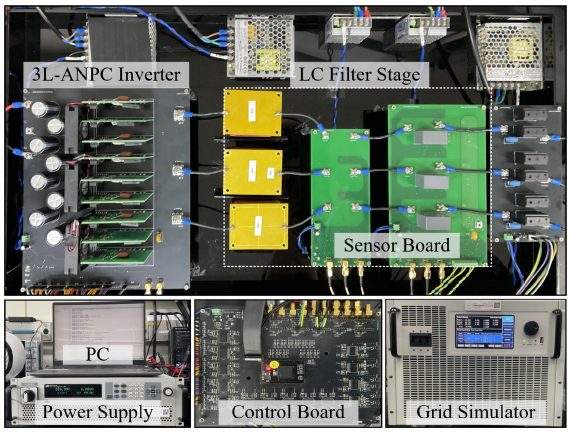

Fig. 8. Experimental setup.

their effectiveness has not been validated in grid-connected applications.

The fast finite switching-state MPC in [29] and [30] reduces the number of candidate switching states for the iterative loop by identifying the small triangular sector in which the reference voltage vector is located, effectively limiting the candidate set to three. However, this approach restricts the degrees of freedom required for multiobjective control and requires an exhaustive search algorithm to identify the reference voltage vector.

The proposed CE-MPC significantly reduces computational burden by adaptively selecting the candidate set through predefined switching states. Since CE-MPC is based on the conventional MO-MPC framework, MO-MPC is employed to compare computational burden and control performance.

The basic cost function of the MO-MPC can be written as

$$g_j = \lambda_i \left(i^{\star}_{\alpha\beta}(k+1) - i_{\alpha\beta,j}(k+1)\right)^2 + \lambda_{\mathrm{dc}}(\Delta V_{\mathrm{dc}}(k) + (T_s/C_f) i_{o,j}(k))^2 + I_{lim} \quad (26)$$

where λ_i and λ_{dc} are the weighting factors for the control objectives, affecting the overall control error across all $j = 0, \ldots, 27$ switching states. I_{lim} denotes the limit value of the predicted inverter-side current, defined as

$$I_{lim} = \begin{cases} \infty, & |i_{\alpha\beta}(k+1)| \geq I_{\max} \\ 0, & |i_{\alpha\beta}(k+1)| < I_{\max} \end{cases} \quad (27)$$

where $I_{\max}$ is set to 1.2 p.u. of the maximum phase current.

IV. Experimental Results

The proposed CE-MPC was experimentally validated and compared with the conventional MO-MPC to demonstrate its control performance, using a hardware prototype of a grid-connected three-phase 3L-ANPC inverter. The experimental setup, shown in Fig. 8 consists of a 3L-ANPC inverter, an LC filter, an ITECH bi-directional power supply, and a three-phase bidirectional grid-simulator. The 3L-ANPC inverter is built using 18 CREE C3M0045065D SiC MOSFETS (650 V/49 A). A 32-bit digital signal processor, TMS320F28386D by Texas Instruments, was used to implement the control algorithms. The system parameters are listed in Table IV. A 3 kW prototype was built to verify the feasibility and effectiveness of the proposed CE-MPC.

TABLE IV
System Parameters

Parameter	Symbol	Value
Input voltage	V_{dc}	400V
Grid voltage (RMS)	V_g	110V
Fundamental frequency	f_g	60Hz
Filter inductance	L_f	2.95mH
Filter capacitance	C_f	4.7μF
DC-link capacitor	C_1, C_2	600μF
Sampling period	T_s	15μs, 30μs, 60μs

A. Steady State Response

To validate the feasibility and effectiveness of the proposed CE-MPC, both steady-state and dynamic responses were experimentally measured. Fig. 9 shows the steady-state experimental waveforms of grid-injected current and filter capacitor voltage. The conventional MO-MPC was compared with the proposed CE-MPC with three different sampling periods. In MO-MPC, the weighting factor ratio between λ_i and λ_{dc} in (26) is set to 0.5. The active power reference $\mathrm{P_{ref}}$ was set to 3 kW and the reactive power reference $\mathrm{Q_{ref}}$ to zero, resulting in a unit power factor.

Fig. 10 presents the fast Fourier transform spectrum of the phase-A current ($i_{g,a}$). The proposed CE-MPC achieves a lower total harmonic distortion (THD) of 2.45%, compared to 5.17% in MO-MPC under the same sampling period of 60μs. Furthermore, the THD is reduced to 1.21% at 30μs sampling period and to 0.88% at 15μs sampling period, without incurring execution delays. These results demonstrate the effectiveness of the proposed CE-MPC in improving steady-state control performance. The THD values are calculated using harmonic components up to the 50th order.

B. Dynamic Response

Fig. 11 presents the experimental waveforms of grid-injected current and filter capacitor voltage under the active power reference changes. Fig. 11(a) shows the startup process as the active power reference $\mathrm{P_{ref}}$ steps from 0 kW to 3 kW. The proposed CE-MPC operates at a sampling period of 30μs, which results in a similar average switching frequency to that of MO-MPC operating at 60μs. During the startup process, MO-MPC exhibits a slight overshoot due to the coupling of the dc-link voltage control objective and current control objectives in its cost function. In contrast, the proposed CE-MPC achieves a smoother transition by decoupling these control objectives and adaptively limiting the candidate voltage vectors. Fig. 11(b) and (c) shows the experimental results for the grid-injected currents, filter capacitor voltages, and dc-link voltages

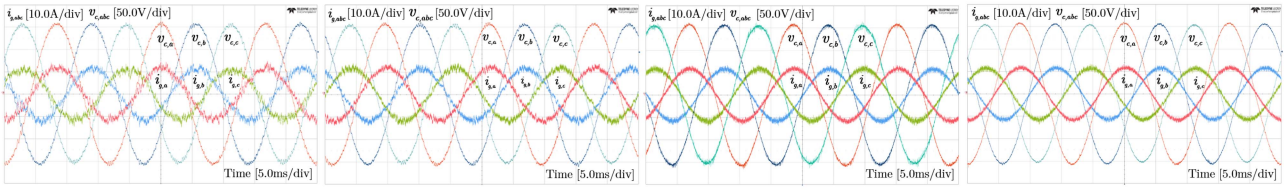

Fig. 9. Steady-state response of grid-injected currents ($i_{g,abc}$), filter capacitor voltage ($v_{c,abc}$). (a) MO-MPC [60μs]. (b) CE-MPC [60μs]. (c) CE-MPC [30μs]. (d) CE-MPC [15μs].

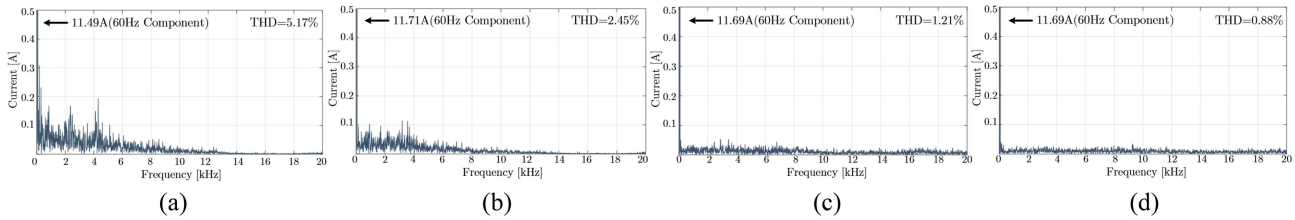

Fig. 10. Harmonic distribution of the phase-A current ($i_{g,a}$). (a) MO-MPC [60μs]. (b) CE-MPC [60μs]. (c) CE-MPC [30μs]. (d) CE-MPC [15μs].

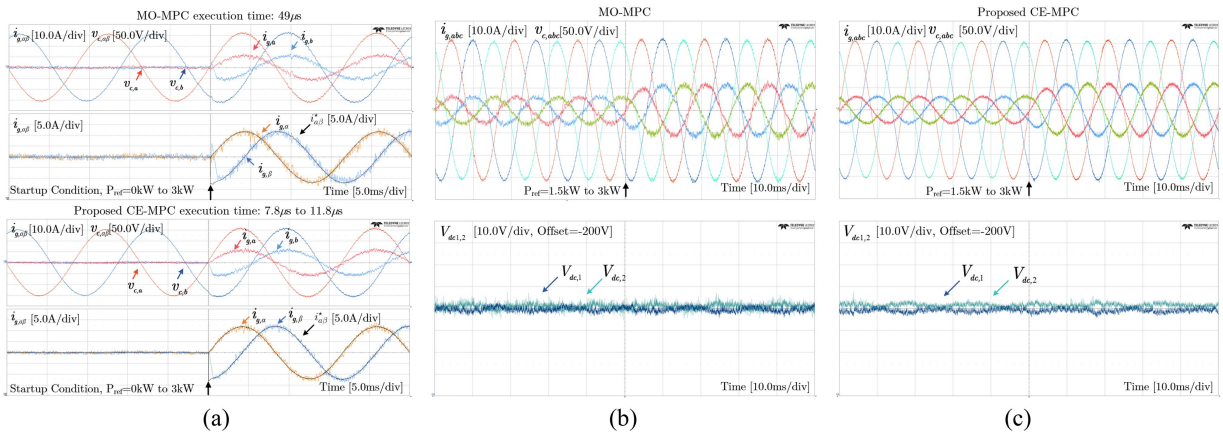

Fig. 11. Dynamic response of grid-injected current ($i_{g,ab}$, $i_{g,\alpha\beta}$, and $i^{\star}_{g,\alpha\beta}$), filter capacitor voltage ($v_{c,abc}$), and DC-link voltage ($V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$). (a) Startup process. (b) MO-MPC with $\mathrm{P_{ref}}$=1.5 kW to 3 kW. (c) CE-MPC with $\mathrm{P_{ref}}$=1.5 kW to 3 kW.

when $\mathrm{P_{ref}}$ changes from 1.5 kW to 3 kW. It is observed that both controllers well track the reference with low dc-link voltage ripple, maintaining ΔV_{dc} within 8 V.

Fig. 12 shows the distance $\boldsymbol{D_v}$ in (20) between the previous selected optimal voltage vector $v_{\mathrm{opt}}(k-1)$ and the reference voltage vector $v^{\star}_{o,\alpha\beta}$ (as described in Fig. 3), along with the optimal cost function $g_{,\mathrm{opt}}$ and $g_{\mathrm{prop,opt}}$ under a step change in $\mathrm{P_{ref}}$. The one-level boundary radius $\boldsymbol{D^{\star}_v}$ is calculated as 133.33 V from (18). In Fig. 12(a), the MO-MPC evaluates all switching states at every control cycle, resulting in unbounded $\boldsymbol{D_v}$ when $\mathrm{P_{ref}}$ changes. In contrast, as constrained by Step-1 in CE-MPC, $\boldsymbol{D_v}$ in Fig. 12(b) remains bounded within $\boldsymbol{D^{\star}_v}$= 133.33 V regardless of $\mathrm{P_{ref}}$, leading to a consistently lower $g_{\mathrm{prop,opt}}$ compared to MO-MPC.

Fig. 13 demonstrates the experimental results under the input voltage and grid voltage disturbance. Fig. 13(a) shows experimental waveforms of dc-link voltages (V_{dc1} and V_{dc2}), grid-injected current ($i_{g,a}$), and filter capacitor voltage ($v_{c,a}$). Under an input voltage variation from 400 V to 430 V with a slope of 300 V/s, the proposed CE-MPC accurately tracks the input voltage change, ensuring robust control performance without including the dc-link voltage control objective term in the cost function. As shown in Fig. 13(b), when a 30% grid voltage sag occurs in phase B, the proposed CE-MPC maintains robust and accurate current control without causing overcurrent.

Fig. 14 shows the experimental waveforms of grid-injected currents and filter capacitor voltages under both unbalanced and distorted grid conditions. Fig. 14(a) shows unbalanced voltage (30% voltage sag in phase B) with distorted grid voltage by 3rd, 5th, 7th, 9th, and 11th harmonics, with respective magnitudes of 1.1%, 2.8%, 1.4%, 2.3%, and 1.5% relative to the grid fundamental voltage. Fig. 14(b) shows distorted grid voltage

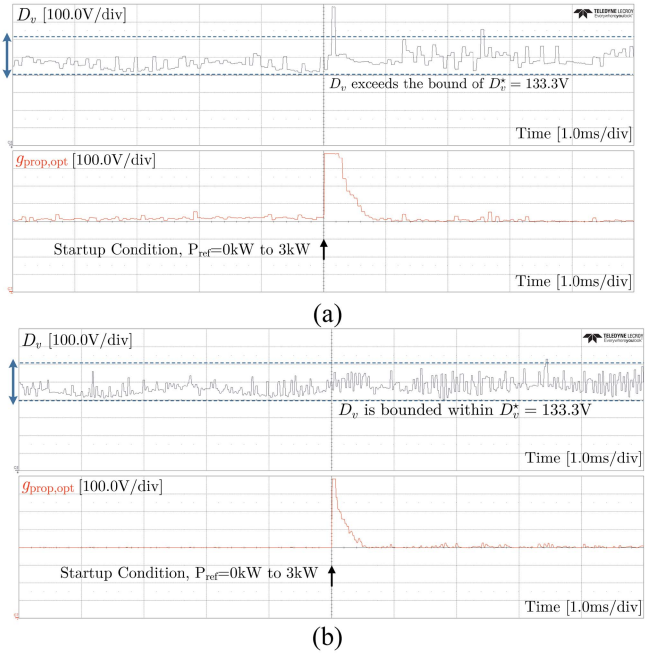

Fig. 12. Experimental results of distance $\boldsymbol{D_v}$ and optimal cost function $g_{\text{prop,opt}}$. (a) MO-MPC. (b) Proposed CE-MPC.

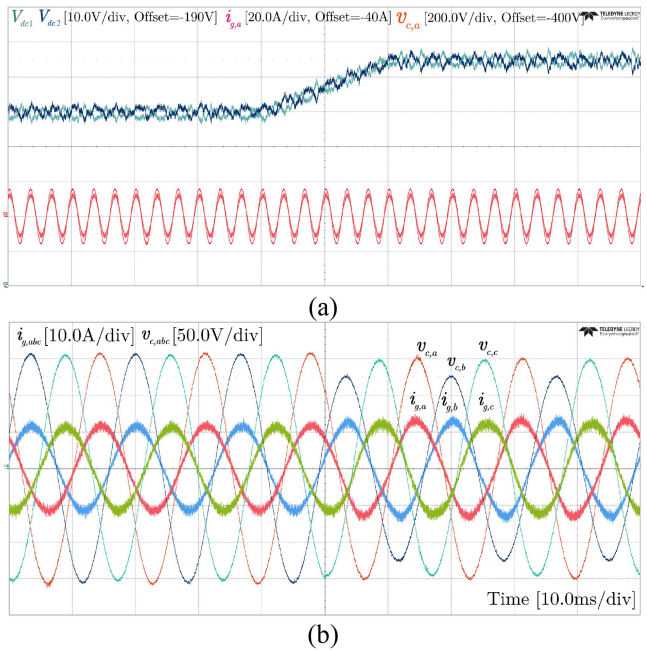

Fig. 13. Experimental results of input voltage variation and grid voltage sag. (a) V_{dc} varies from 400 V to 430 V with a slope of 300 V/s. (b) 30% grid voltage sag in phase B grid voltage.

by 2nd, 5th, and 7th harmonics, with increased magnitudes of 2.7%, 9.8%, and 15.8%, respectively. The experimental results demonstrate that the proposed CE-MPC has excellent control performance and robustness even in unbalanced and distorted grid voltage conditions.

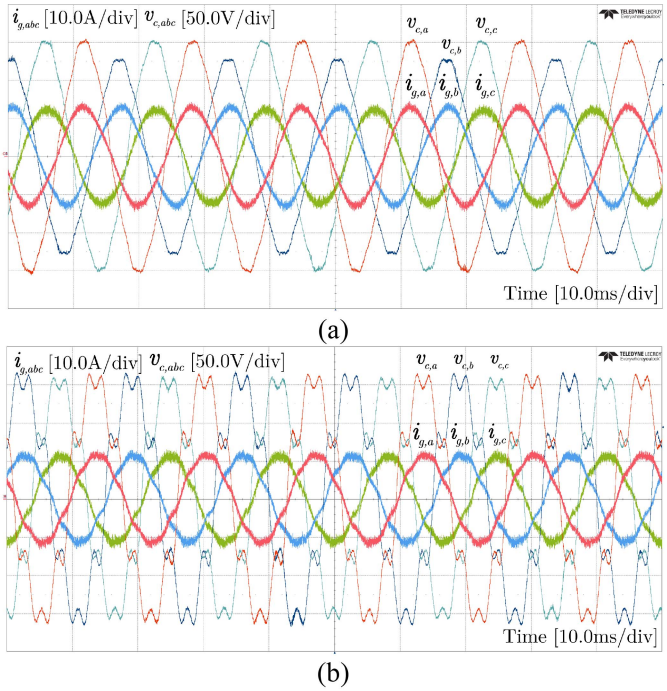

Fig. 14. Experimental results of grid-injected currents ($i_{g,abc}$) and filter capacitor voltages ($v_{c,abc}$) under unbalanced and distorted grid conditions. (a) Unbalanced and distorted grid voltages. (b) Distorted grid voltages with a high magnitude of harmonic components.

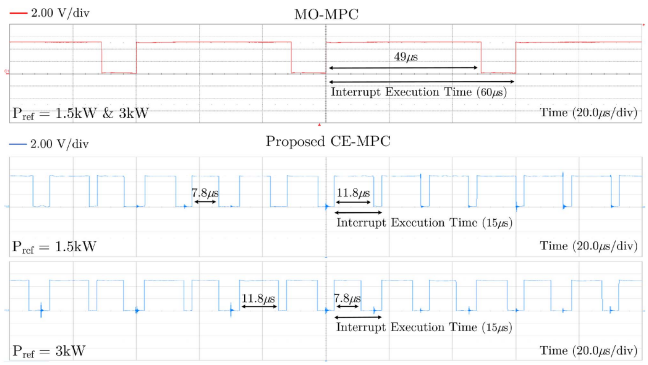

Fig. 15. Execution time comparison (sampling period).

C. Computational Burden

Fig. 15 compares the execution times of the conventional MO-MPC and the proposed CE-MPC. In the case of CE-MPC, different P_{ref} conditions were used to evaluate the execution time under both small and large voltage vector synthesis scenarios. The execution time was measured by toggling a GPIO pin within the control loop. The control loop includes A/D conversion, MPC computation, and auxiliary tasks. The sampling period, T_s, for the MPC algorithm, is set equal to the interrupt execution time. In the case of MO-MPC, a sampling period of 60μs is required to ensure sufficient computation time and to prevent system delays.

The MO-MPC requires 27 iterations to evaluate the cost function, resulting in an MPC computation time of 49μs. In

TABLE V
COMPUTATIONAL DETAILS OF CE-MPC

Operation	Value
Sampling period	15μs
A/D sampling process	1.3μs
MPC computation	7.8μs – 11.8μs
Auxiliary tasks	1.09μs
Number of iterations	4 – 7
Computation time reduction	75.92% – 84.08%

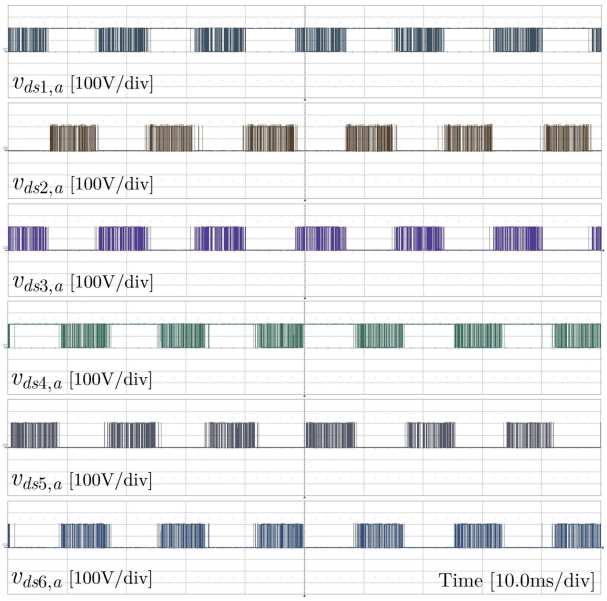

Fig. 16. Experimental results of $v_{ds1-6,a}$ under zero switching states of [Z3].

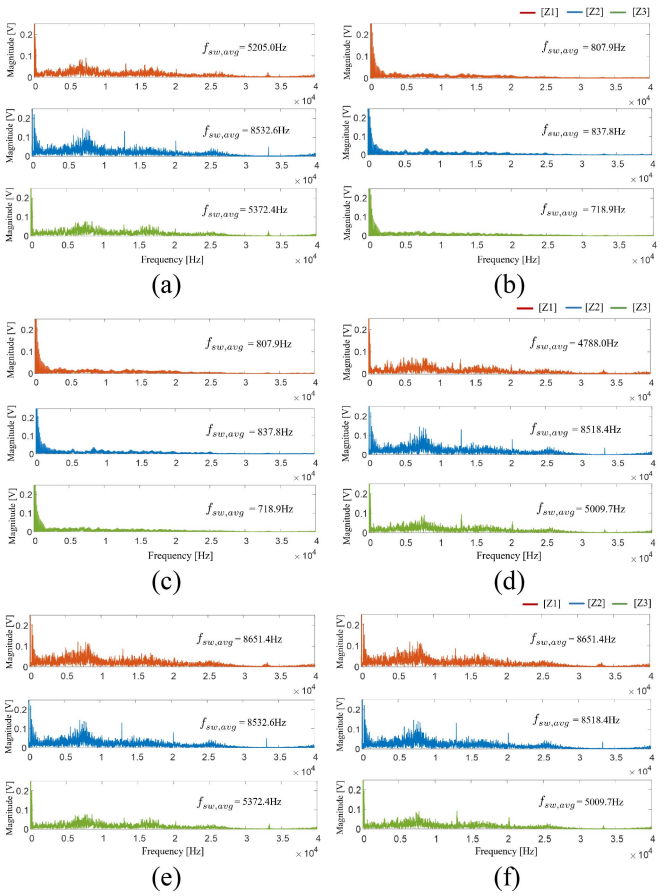

Fig. 17. Frequency spectrum comparison of phase-A switching signals under 3 different zero switching states ($P_{ref} = 3$ kW). (a) $S_{1,a}$. (b) $S_{2,a}$. (c) $S_{3,a}$. (d) $S_{4,a}$. (e) $S_{5,a}$. (f) $S_{6,a}$.

contrast, the proposed CE-MPC achieves significantly shorter computation times, operating within 7.8μs to 11.8μs. Therefore, the sampling period of the CE-MPC can be reduced to 15μs, as shown in Fig. 15.

When $P_{ref} = 1.5$ kW, CE-MPC tends to select small voltage vectors, with computation time typically around 11.8μs. Conversely, for $P_{ref} = 3$ kW, large voltage vectors are frequently selected, and computation times of 7.8μs are more commonly observed.

The ratio of the computation time of the proposed CE-MPC to that of MO-MPC can be calculated as

$$\begin{cases} (7.8\mu s/49\mu s) \times 100 \cong 15.92\% \\ (11.8\mu s/49\mu s) \times 100 \cong 24.08\% \end{cases}. \tag{28}$$

The computation time of the CE-MPC ranges from 15.92% to 24.08% of the MO-MPC algorithm, representing a reduction of 75.92% to 84.08%. Table V summarizes the computational details of the CE-MPC.

D. Analysis of Voltage Stress and Switching Frequency

Fig. 16 shows the experimental waveforms of drain-source voltage v_{ds} for the phase-A leg switches. As defined by the Step-3 constraint, employing the zero switching states [Z3] clamps the voltage stress to either $V_{dc}/2$ or 0, enabling a more even distribution of voltage stress across all switches, as illustrated in Fig. 6(c).

Fig. 17 presents the switching frequency spectrum components of the CE-MPC for the three different zero switching states [Z1], [Z2], and [Z3]. The average switching frequency, $f_{sw,avg}$, denotes the mean frequency calculated from the power spectrum of these components. Among the zero switching states, [Z3] exhibits a lower overall spectral magnitude and average switching frequency compared to the other states.

The power losses and thermal distribution under different zero switching states are presented in Fig. 18. The power losses were estimated using the CREE SiC MOSFET thermal model in PLECS and compared with the experimental results. In Fig. 18(a), [Z2] exhibits the highest switching loss of 25.80 W among the zero switching states, due to higher switching frequencies. In contrast, [Z3] results in the lowest switching loss, indicating lower thermal stress. In Fig. 18(b), the temperatures of all the switches were measured using an infrared camera. The initial switch temperature was around 27°C (below 30°C), and the active power reference P_{ref} was fixed at 3 kW. Each thermal distribution was observed for 180s under a given zero switching state. Under [Z1] and [Z2], the temperatures of specific switches rise to 48.6°C and 55.1°C, respectively. In contrast, a more

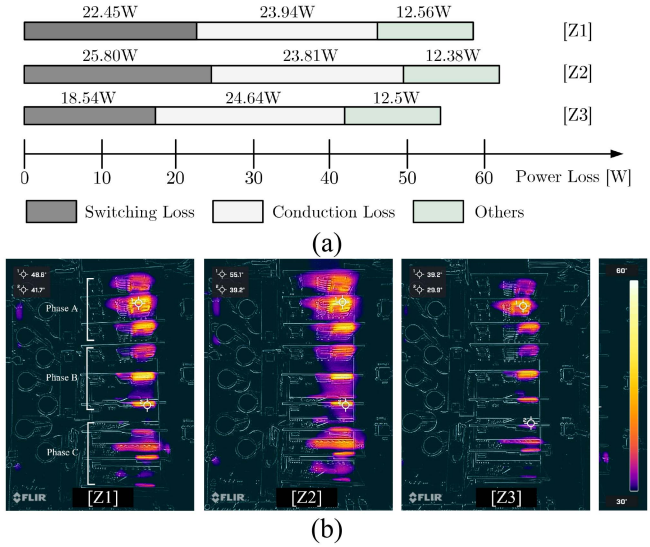

Fig. 18. Thermal distribution and loss analysis of SiC MOSFETS under different zero switching states. (P_{ref} = 3 kW, T_s= 30μs). (a) Loss comparison. (b) Temperature comparison.

TABLE VI
PERFORMANCE COMPARISON

Control Scheme	MO-MPC	Proposed CE-MPC		
T_s	60μs	60μs	30μs	15μs
P_{ref}	3kW			
$f_{sw,avg}(S_{1,a})$	3759.0Hz	3247.1Hz	5372.4Hz	8080.7Hz
$f_{sw,avg}(S_{2,a})$	3709.9Hz	398.2Hz	718.9Hz	1114.0Hz
$f_{sw,avg}(S_{3,a})$	3709.9Hz	398.2Hz	718.9Hz	1114.0Hz
$f_{sw,avg}(S_{4,a})$	3805.2Hz	3109.9Hz	5009.7Hz	7983.7Hz
$f_{sw,avg}(S_{5,a})$	3759.0Hz	3247.1Hz	5372.4Hz	8080.7Hz
$f_{sw,avg}(S_{6,a})$	3805.2Hz	3109.9Hz	5009.7Hz	7983.7Hz
$f_{sw,avg}(S_{1-6,a})$	3758.0Hz	2251.7Hz	3700.3Hz	5726.1Hz
η_s	98.16%	98.53%	98.24%	97.58%
η_e	97.72%	98.20%	97.82%	97.31%
THD	5.17%	2.45%	1.21%	0.89%

uniform temperature distribution was achieved under [Z3], with all switches operating within a range of 29.9°C to 39.2°C.

Table VI summarizes the control performance comparison between the conventional MO-MPC and the proposed CE-MPC under different sampling periods. The proposed CE-MPC uses the zero switching states of [Z3]. The average switching frequency $f_{sw,avg}$ and THD are evaluated using the phase-A leg switching signals and phase-A grid-injected current, respectively. The simulated efficiency η_s obtained from PLECS simulation, while the experimental efficiency η_e is calculated as the ratio of the output active power to the input power in steady-state conditions. Under the same sampling period of 60μs, the proposed CE-MPC achieves a lower mean switching frequency $f_{sw,avg}(S_{1-6,a})$ than MO-MPC, and highest overall efficiency (η_s= 98.53%, η_e= 98.20%). Under the sampling period of 30μs, the proposed CE-MPC shows a similar $f_{sw,avg}(S_{1-6,a})$ to that of MO-MPC with 60μs, but with improved THD and slightly higher efficiency. When the sampling period is reduced to 15μs, CE-MPC further enhances the current THD due to its reduced sampling period, while minimizing efficiency degradation.

V. CONCLUSION

This article proposes the CE-MPC method for a grid-connected 3L-ANPC inverter. The proposed method adaptively reduces the switching states using three-step constraints and evaluates the cost function by considering a previously stored optimal voltage vector. The candidate switching states are selected around the previous voltage vector location, and this strategy reduces the number of possible switching states from 27 to a range of 4 to 7, thereby significantly reducing the number of iterations of the control algorithm. The reduced switching states allow a higher sampling frequency, and control performance is improved without any complicated controller design. The computation time of CE-MPC is reduced by up to 84.08% compared to MO-MPC, significantly alleviating the computational burden. Experimental results in steady-state and dynamic conditions validate that the proposed control method ensures the high-performance operation of a grid-connected 3L-ANPC inverter.

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Euntaek Nam (Student Member, IEEE) received the B.S. degree from Handong Global University, Pohang, South Korea, in 2023, and the M.S. degree from the Pohang University of Science and Technology, Pohang, South Korea, in 2025, where he is currently working toward the Ph.D. degree.

His research interests include multilevel inverters and the control of grid-connected converters.

Suyong Chae (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from the Seoul National University, Seoul, South Korea, in 2009.

From 2000 to 2010, he was a Research Engineer with Samsung SDI. From 2010 to 2022, he was a Principal Researcher with the Korea Institute of Energy Research, Daejeon, South Korea. Since 2022, he has been a Faculty Member with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea, where he is working as an Associate Professor. His research interests include power electronics, modeling, and control of distributed power systems.