Body Diode Induced Negative-Bias V_{th} Instability of Synchronous SiC MOSFET in Bridge-Leg Circuit

Peixuan Wang, Yunhong Lao, Youyi Yin, Meng Zhang, Michael Lee, Jack Chen, Tony Chau, and Jin Wei

***Abstract*—This article reports a body diode induced negative-bias V_{th} instability of synchronous SiC MOSFET in a bridge-leg circuit. During reverse recovery phase, the holes injected from body diode are swept towards the source/gate side. A portion of holes bombard at the gate oxide, which results in the generation of defects/traps at the gate oxide and the consequent V_{th} shift. The shift is strongly influenced by the $V_{\mathrm{GS\text{-}OFF}}$ on the synchronous MOSFET: a more negative $V_{\mathrm{GS\text{-}OFF}}$ leads to a larger portion of holes moving towards the gate oxide and thus a more appreciable V_{th} shift. The shift is also heavily dependent on the gate structure of the MOSFET: it is more obvious in planar-gate MOSFET and double-trench MOSFET than the asymmetric-trench MOSFET. The technology computer-aided design simulation reveals that the p-shield under trench of AT-MOS provides a strong protection for the gate oxide. Furthermore, an external antiparallel Schottky barrier diode is found to significantly weaken the V_{th} instability, since it mutes the body diode conduction. In summary, this article identifies a new reliability mechanism in SiC MOSFET (body diode induced V_{th} instability) and provides an insight to engineer out the instability via circuit design and/or device structure design.**

***Index Terms*—Body diode, double pulses test, gate oxide instability, half-bridge circuit, negative V_{th} shift, silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET), trench gate.**

I. Introduction

SILICON carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) are increasingly adopted in high-efficiency and high-power-density applications, due to the low conduction loss and fast switching speed [1], [2], [3], [4], [5], [6], [7], [8]. In these applications, the SiC MOSFETs usually work under high-voltage and fast-switching conditions. Considering the high *dV/dt*, the SiC MOSFETs are very prone to false turn ON [9], [10], [11]. To avoid false turn-ON, multiple solutions have been proposed, such as integrating an active Miller clamping circuit in the gate driver, increasing the V_{th} of the device, and applying negative gate bias, etc [12], [13], [14], [15], [16], [17], [18], [19], [20]. Among them, applying a negative $V_{\mathrm{GS\text{-}OFF}}$ is one of the most common approaches, creating a wider margin below V_{th} to accommodate the gate voltage spikes induced by crosstalk [10], [21]. However, previous studies have reported the negative gate bias may lead to V_{th} shift due to charge trapping near the SiC/SiO_2 interface [22], [23]. For instance, researchers have demonstrated the effects of negative bias temperature instability (NBTI) in SiC MOSFETs under a wide range of oxide electric field stresses [24]. Additionally, a prior study analyzed the V_{th} shift of a commercial SiC MOSFETs to understand charge trapping and oxide-trap activation mechanisms under high-temperature negative bias stress [25]. These studies provide valuable insights into how negative gate bias affects V_{th} instability. However, most of these investigations are conducted under static conditions [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38]. There is still a lack of research focusing on the V_{th} instability of SiC MOSFETs under practical switching conditions.

In this article, we report a body diode induced negative-bias V_{th} instability of synchronous SiC MOSFET in a bridge-leg circuit. When the body diode is turned ON, holes are injected from p-base into the drift region. During reverse recovery, the holes are driven upwards; a negative $V_{\mathrm{GS\text{-}OFF}}$ leads to more holes bombarding at the gate oxide. Three commercial SiC MOSFETs are investigated, including a planar-gate MOSFET (P-MOS), a double-trench MOSFET (DT-MOS), and a symmetric-trench MOSFET (AT-MOS). The AT-MOS is found to exhibit least V_{th} shift since the oxide is better shielded by the p-well region. Furthermore, an antiparallel Schottky barrier diode (SBD) is also effective to suppress the above-mentioned V_{th} instability, which further verifies the proposed mechanism.

The rest of this article is organized as follows. Section II discusses the half-bridge test circuit design and presents the design details about this circuit. Section III presents the degradation phenomena of the DUTs working in test circuit under different $V_{\mathrm{GS\text{-}OFF}}$ conditions. Section IV, the degradation mechanism is discussed. Meanwhile, technology computer-aided design (TCAD) simulations are conducted to investigate the gate oxide

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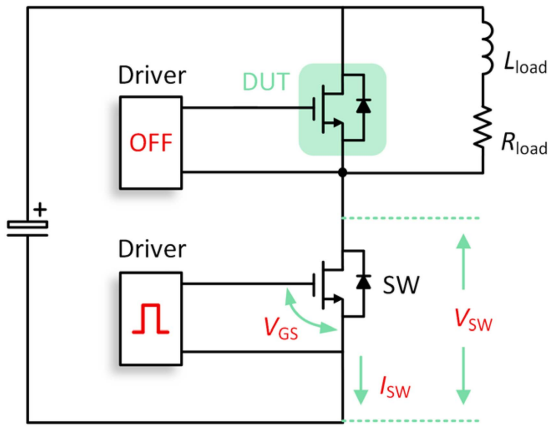

Fig. 1. Schematic diagram of the half-bridge test circuit. The high side transistor (DUT) is in OFF state with a fixed negative $V_{GS\text{-}OFF}$, and the low side device is switching (SW). A power resistor load (R_{load}) maintains steady-state current, and the inductive load current freewheels through the DUT body diode during OFF state of SW.

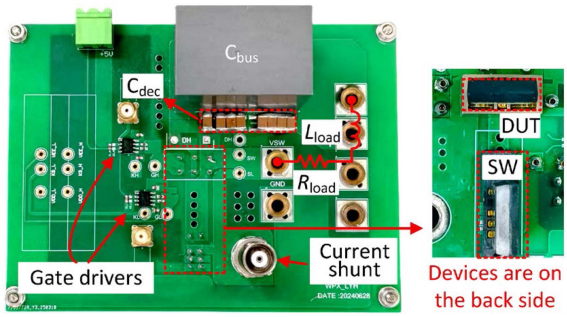

Fig. 2. Photograph of the test bench. The isolated gate drivers are used to control the transistors.

degradation mechanism. Section V investigates the V_{th} instability for synchronous SiC MOSFET with an antiparallel SBD. Finally, Section VI concludes this article.

II. Half-Bridge Circuit Test Setup

Fig. 1 shows the schematic of the half-bridge test circuit. The DUT serves as a synchronous MOSFET, and is paralleled with the L/R load consisting of a 400 μH inductor and a 10 Ω power resistor. The transistors are driven by isolated gate drivers (SI8271GB-IS). A Keysight 81150 A function generator provides the gate drive signal to the low-side transistor (SW). When the SW is turned ON, the DUT operates in the OFF-state and blocks high voltage. when the SW is turned OFF, the load current flows through the body diode of DUT. To ensure test safety, high-bandwidth passive voltage probes and a current shunt are applied to monitor the voltage and current waveforms of the SW.

Fig. 2 shows the photograph of the test bench. The power loop and gate driver loop are carefully designed to minimize crosstalk and oscillations during testing. To reduce voltage noise and minimize parasitic inductance in the power loop, a 10 μF bulk bus capacitor (C_{bus}, C4AEHBU5100A11J) and eight 0.1 μF multilayer ceramic decoupling capacitors (C_{dec}, C1812X104-K102T) are connected in parallel and placed as close as possible to the DUT. A 0.1 Ω coaxial shunt (SSDN-10) measures current

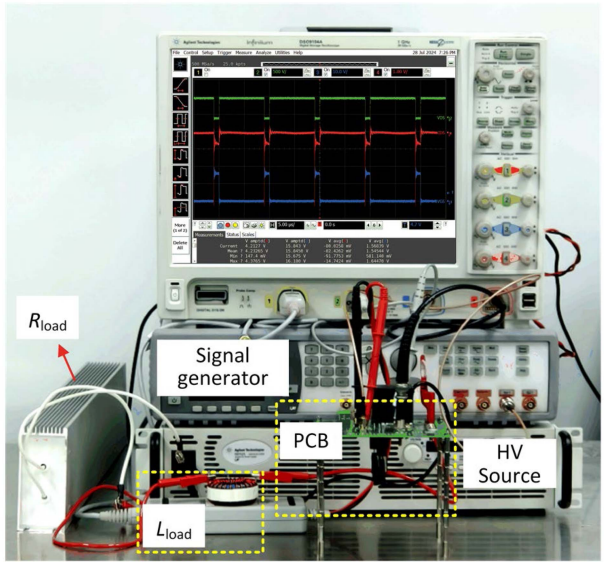

Fig. 3. Photograph of test system.

via voltage drops with minimal circuit disturbance. Additionally, the Kelvin source of the DUT (P-MOS and AT-MOS) is adopted to suppress the interference between the power loop and gate loop. The gate drivers are mounted near the DUT and SW. The output voltage of the gate driver for SW is set to 0 V/20 V. As this article focuses on the V_{th} shift mechanism during the body diode reverse recovery transient, to simplifies the test circuit, the DUT was always applied with a negative $V_{GS\text{-}OFF}$ bias during the test. Each DUT corresponds to a negative $V_{GS\text{-}OFF}$, and the range of negative $V_{GS\text{-}OFF}$ is from 0 to -10 V. The gate resistors of SW are set to 50 Ω to minimize DUT's gate voltage oscillation, which is caused by the fast switch of SW.

Fig. 3 shows a photograph of the test system. The dc power supply (Agilent N8762A) with a maximum voltage of 600 V and a maximum current of 8.5 A is utilized as the HV source. The pulse signals with adjustable pulse widths are generated from an arbitrary function generator Keysight 81150 A. The switching frequency was set to 50 kHz, which is a commonly adopted operating frequency for SiC MOSFETs [39], [40]. The switching waveforms is monitored by a four-channel digital storage oscilloscope (Keysight Infiniium DSO9104A) with 1 GHz bandwidth. A power resistor (4 kW, 10 Ω) is connected in series with the inductor to ensure stable current in the half-bridge circuit. The differential probe featuring a 100 MHz bandwidth (N2790A) is used to monitor the V_{GS} of the SW. The V_{DS} is monitored by a high voltage passive probe Keysight 10076C with bandwidth of 500 MHz. The 0.1 Ω coaxial current shunt (SSDN-10) with small insertion impedance is used to monitor the drain current of the SW.

Fig. 4 shows the test waveforms of the half-bridge circuit, including the voltage of the switching node (V_{SW}), the V_{GS} and the current (I_{SW}) of the low-side transistor (SW). When the SW is turned ON (the pulsewidth is set to be 2 μs), the inductive load is charged. the I_{sw} increases to 7.5 A and flows through the external inductor and resistor. At the same time, the DUT works in off-state to block the high voltage. Then, the SW is turned OFF, and the current flows through the body diode of the

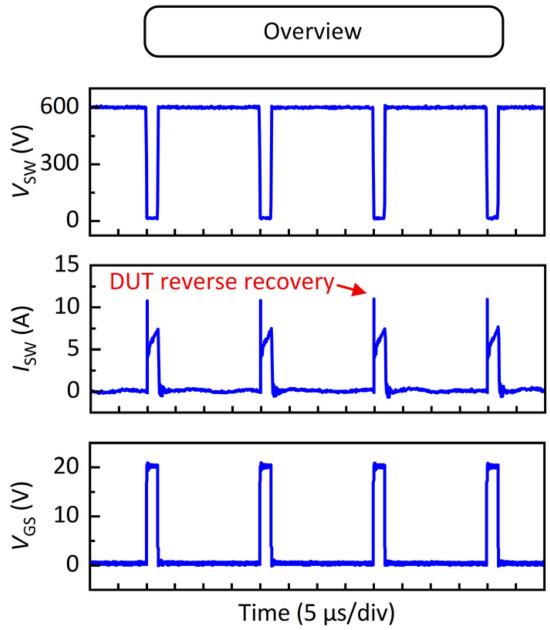

Fig. 4. Test waveforms, including the V_{GS}, the V_{SW}, and the I_{SW} of the SW. The frequency is 50 kHz.

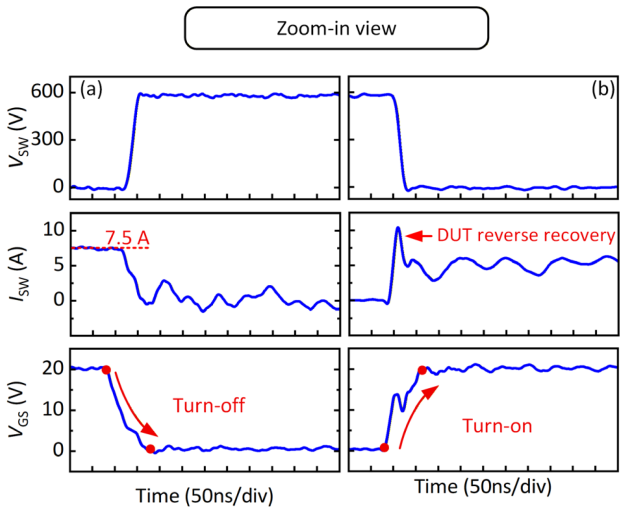

Fig. 5. (a) Turn OFF transient of the SW. (b) Turn ON transient of the SW.

DUT. During this transition, the body diode works in reverse conduction, and the I_{SW} gradually decreases due to the power dissipation of the resistor load, ensuring a stable load current during the test. After 18 μs, the SW is turned ON again, the V_{DS} of the DUT to rise from approximately -4 V to 600 V. During this transition, the body diode undergoes reverse recovery. The DUT repeats this process in the half-bridge test circuit.

Fig. 5(a) shows the turn-OFF waveforms of the SW. At this moment, the body diode of the DUT acts as a freewheeling diode, and the I_{SW} flowing through the body diode is initially 7.5 A. Fig. 5(b) shows the waveforms at the subsequent turn-ON transient of the SW. The I_{SW} increase to 10.4 A, this peak current comprises both the inductor current and DUT reverse recovery current. At the same time, the DUT is in the OFF-state, and its body diode undergoes reverse recovery. Holes injected from p-base into n-drift are swept to source and gate side.

TABLE I
COMPARISON OF THE DEVICES: P-MOS, DT-MOS, AND AT-MOS

Device technology	Part #	BV (V)	R_{ON} (mΩ)	V_{th} (V)	V_{SD} (V)
P-MOS	E3M0160120K	>1200	159	2.8	4.8
DT- MOS	SCT3160KLHR	>1200	160	4.2	4.1
AT-MOS	IMZ120R140M1H	>1200	140	4.5	4.8

* V_{th} of all devices was extracted at I_D = 2.5 mA, while V_{SD} was extracted at 4.25 A, 7 A, and 6 A for planar (P-) MOSFET, double trench (DT-) MOSFET, and asymmetrical trench (AT-) MOSFET, respectively. (The data were obtained from the device datasheets)

III. DEVICE CAPABILITY AND V_{TH} INSTABILITY UNDER PRACTICAL TESTS

Since the first commercial SiC MOSFET was produced in 2012, many manufacturers have launched different kinds of products to make better use of the SiC material. In this article, we select three SiC MOSFET as the devices under test (DUTs), including planar-gate MOSFET, double-trench MOSFET, and asymmetric-trench MOSFET (designated as P-MOS, DT-MOS, and AT-MOS, respectively) from Wolfspeed, Rohm, and Infineon, with identical voltage ratings (1200 V) and comparable current ratings (18, 17, and 19 A, respectively) [41], [42], [43]

Table I presents a comparison of key parameters among P-MOS, DT-MOS, and AT-MOS devices. The three kinds of DUTs have the same BV and similar R_{ON} for a fair comparison. The V_{th} is 2.8, 4.2, and 4.5 V (defined at $V_{DS} = V_{GS}$ and $I_D = 2.5$ mA), respectively. The turn-ON voltage (V_{SD}) of the body diode for three devices is similar since all devices are fabricated on silicon carbide. It is important to note that the P-MOS and AT-MOS are in TO-247-4 packages (which have a Kelvin source to minimize parasitic inductance), whereas the DT-MOS is in a TO-247-3 package. This difference has little influence on the study due to the moderate switching frequency of 50 kHz.

Fig. 6(a) illustrates the measure-stress-measure sequences used in this article. First, the transfer curve is measured using the Keysight B1505A semiconductor analyzer to extract the initial V_{th}. Subsequently, the device is put into the half-bridge circuit to operate under switching conditions. Then, the V_{th} is measured after the switching operation. Repeat the above steps until the cumulative working time reaches the target time. Fig. 6(b)–(d) shows the transfer curves of three DUTs after different cumulative working time in the half-bridge circuit, measured by the Keysight B1505 semiconductor analyzer. To avoid overheating-induced device failure, a pulse-mode I–V measurement is applied to the DUTs. Furthermore, the current compliance is set to 100 mA to further protect the DUTs. When the DUT works in the half-bridge circuit, the $V_{GS\text{-}OFF}$ is set to -10 V. For the P-MOS case, the transfer curves significantly shift leftward as the cumulative working time increases, clearly demonstrating the negative V_{th} shift. The V_{th} shifts significantly from 2.75 to 1.88 V and only partial recovery is observed after

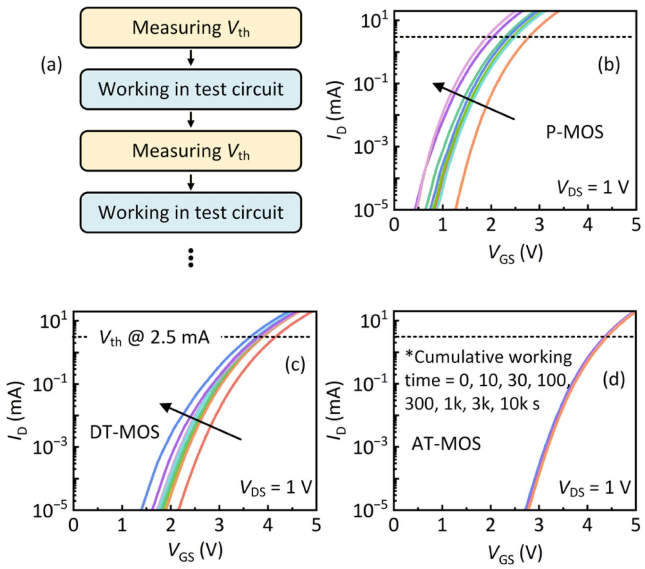

Fig. 6. (a) Measure-stress-measure sequences used in this article. The transfer curves of (b) the P-MOS, (c) the DT-MOS. (d) AT-MOS after cumulative switching time of 0, 10, ..., and 10 000 seconds in a half-bridge circuit with $V_{\text{GS-OFF}} = -10$ V applied to DUTs.

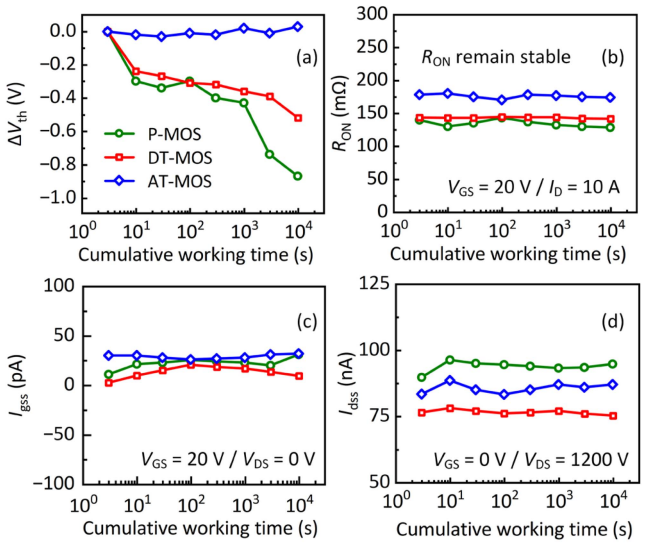

Fig. 7. (a) ΔV_{th} (V_{th} defined at $I_D = 2.5$ mA). (b) R_{ON} ($V_{\text{GS}} = 20$ V / $I_D = 10$ A). (c) I_{gss} ($V_{\text{GS}} = 20$ V / $V_{\text{DS}} = 0$ V). (d) I_{dss} ($V_{\text{DS}} = 1200$ V / $V_{\text{GS}} = 0$ V) as functions of cumulative working time in the half-bridge circuit with $V_{\text{GS-OFF}} = -10$ V.

30 days of rest at room temperature. Similarly, for the DT-MOS, it also presents a significantly negative V_{th} shift from 4.10 to 3.58 V. However, for the AT-MOS, the transfer curves show no marked change, and its V_{th} remains stable.

Fig. 7(a) shows the ΔV_{th} shift as a function of the cumulative working time for the three DUTs [extracted from Fig. 6(a)–(c)]. The V_{th} is defined at $V_{\text{DS}} = 1$ V and $I_D = 2.5$ mA. For the P-MOS and DT-MOS case, the negative V_{th} shift is similar after 1000-s switching operation in the half-bridge circuit (and also observable in Fig. 6). However, after 10000 s of switching operation, the P-MOS exhibits a more severe negative V_{th}

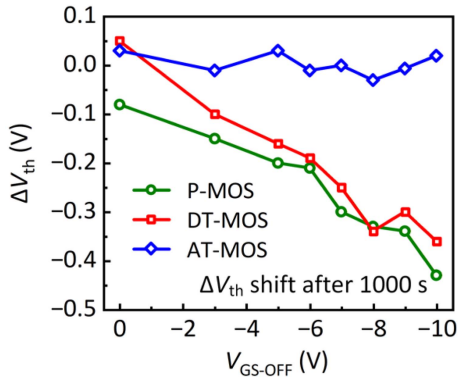

Fig. 8. ΔV_{th} of the DUTs as a function of $V_{\text{GS-OFF}}$ after 1000-s cumulative switching operation in a half-bridge circuit each testing point corresponds to a distinct device. (V_{th} extracted at $I_{\text{D}} = 2.5$ mA).

shift (−0.87 V) than the DT-MOS (−0.52 V). This indicates more severe gate degradation in P-MOS than in DT-MOS in long-term switching operations. These results demonstrate that the double-trench structure shows better V_{th} stability than the planar-gate structure in long-term switching operations when utilizing the body diode. At the same cumulative working time in the half-bridge circuit, AT-MOS demonstrates stable V_{th} characteristics, indicating superior V_{th} stability for long-term applications. For the P-MOS and DT-MOS, the degradation phenomenon was preliminarily validated at a switching frequency of 50 kHz. At higher frequencies (such as above 100 kHz), the hole injection rate increases in these devices, which may lead to more pronounced V_{th} degradation.

Fig. 7(b) shows the ON-resistance (R_{ON}) variation as a function of cumulative working time under $V_{\text{GS-OFF}} = -10$ V condition. The R_{ON} of the devices was characterized via *I-V* curve measurements under conditions of $V_{\text{gs}} = 20$ V and $I_d = 10$ A. For all devices, R_{ON} shows minor fluctuations with increasing cumulative working time, which may result from the competition between different physical mechanisms. On one hand, holes impacting the SiC/SiO_2 interface increase interface trap density, causing strong Coulomb scattering at interface charges and significantly reducing channel mobility. On the other hand, holes accumulating in oxide traps induce an additional electric field across the gate oxide, leading to a noticeable V_{th} reduction and consequent decrease R_{ON}.

As shown in Fig. 7(c) and (d), the gate leakage current (I_{gss}) and drain leakage current (I_{dss}) of the DUTs were also measured, and no changes were observed after the dynamic test. This indicates that no conductive path formed in the gate oxide, and the body diode remained intact after switching operation.

Fig. 8 shows the ΔV_{th} shift as a function of $V_{\text{GS-OFF}}$, measured after 1000 s of continuous operation in a half-bridge circuit. For each type of DUTs, to obtain the ΔV_{th} of a specified $V_{\text{GS-OFF}}$, one device was first measured to obtain the fresh V_{th}; after 1000 s of operation in the half-bridge circuit under specified $V_{\text{GS-OFF}}$, the same device's V_{th} was measured again to calculate the ΔV_{th} for this specified $V_{\text{GS-OFF}}$. Then, for another specified $V_{\text{GS-OFF}}$ value, a new device was tested following the same procedure. The V_{th} is defined at $V_{\text{DS}} = 1$ V and $I_{\text{D}} = 2.5$ mA.

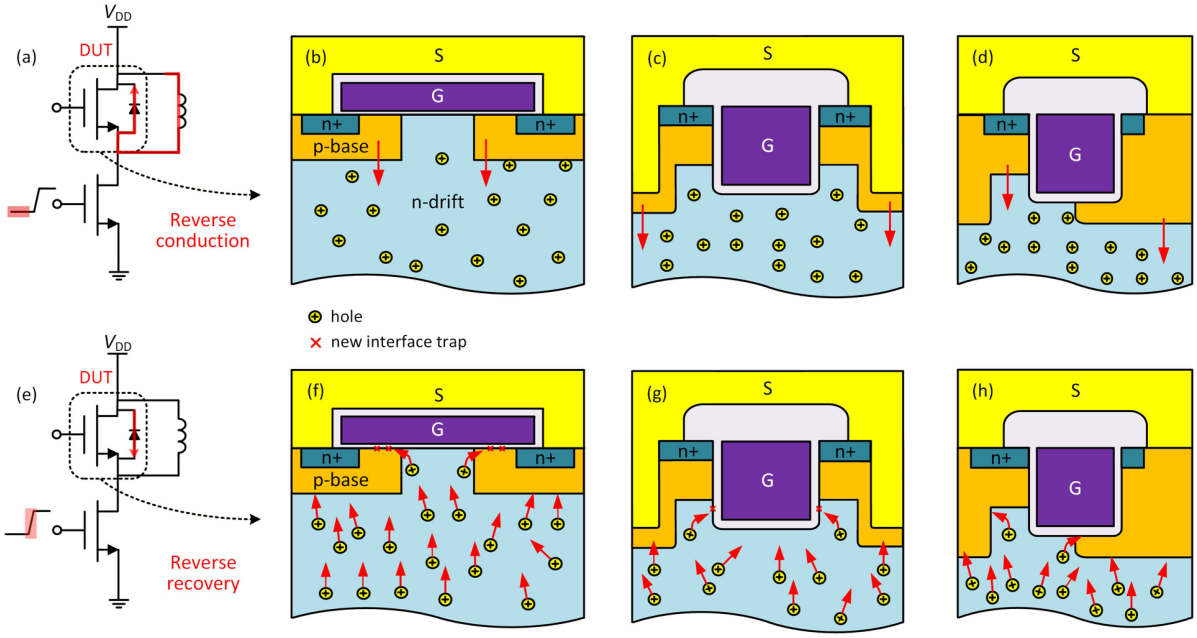

Fig. 9. (a) Schematic of the reverse conduction path in the circuit. (b)–(d) Internal carrier transport mechanisms in: (b) P-MOS; (c) DT-MOS; and (d) AT-MOS structures, showing hole injection from the P-base into the N-drift region. (e) Schematic of the reverse recovery current path in the circuit. (f)–(h) Internal carrier transport mechanisms in: (f) P-MOS; (g) DT-MOS; and (h) AT-MOS structures, showing hole injection from the P-base into the N-drift region followed by hole return to the P-base, with partial holes being attracted by negative $V_{\mathrm{GS\text{-}OFF}}$ and impacting the oxide interface.

Both P-MOS and DT-MOS devices show that as $V_{\mathrm{GS\text{-}OFF}}$ becomes more negative, the V_{th} shifts further in the negative direction due to increased hole injection into the oxide layer. For the P-MOS under $V_{\mathrm{GS\text{-}OFF}} = -10$ V, the V_{th} shifts from 2.75 to 2.32 V, the device presents an appreciable negative V_{th} shift ($\Delta V_{\mathrm{th}} = -0.43$ V). For the DT-MOS under $V_{\mathrm{GS\text{-}OFF}} = -10$ V, same as P-MOS, the V_{th} shifts from 4.10 V to 3.74 V ($\Delta V_{\mathrm{th}} = -0.36$ V), the transfer curves significantly shift leftward, indicating the negative V_{th} shift. In contrast, the AT-MOS always maintains stable V_{th} under various $V_{\mathrm{GS\text{-}OFF}}$. It should be noted that multiple devices (not merely a single device) were evaluated in this article, as shown in Fig. 8, where each testing point corresponds to a distinct device. Furthermore, the negative V_{th} shift intensifies with increasingly negative $V_{\mathrm{GS\text{-}OFF}}$, which clearly demonstrates the repeatability of the observed behavior.

IV. Mechanism Analysis and TCAD Simulation

Fig. 9 illustrates the physical mechanism behind the above-mentioned phenomenon. This phenomenon is that the body diode acts as a freewheeling diode under a negative $V_{\mathrm{GS\text{-}OFF}}$ during switching operations, leading to the observed negative V_{th} shift. Fig. 9(a) shows the working state of the DUT during the reverse conduction when the low-side transistor (SW) is turned OFF and the load inductor is energized, causing the body diode to conduct as a freewheeling diode. Fig. 9(b)–(d) shows the physical mechanism of the device under reverse conduction. For all DUTs, when the body diode is turned ON, the holes are injected from the p-base into the n-drift region. Fig. 9(e) shows the working state of the DUT during the reverse recovery. This condition is triggered when the low side transistor is turned ON. At this point, the body diode blocks high V_{DS} stress. Due to the high electric field, the holes are accelerated to become hot carriers and are swept back into the p-base region. Fig. 9(f) illustrates the physical mechanism of the P-MOS under reverse recovery. During the reverse recovery transient, most holes return to the p-base region, while some are drawn toward the interface by the negative $V_{\mathrm{GS\text{-}OFF}}$ to bombard the gate oxide. These hot holes induce positive charge trapping and interface defect generation at the MOS interface, resulting in significant negative V_{th} shift. Fig. 9(g) illustrates the physical mechanism of the DT-MOS operating in reverse conduction. Owing to its unique double-trench structure and deeper p-base region compared to the P-MOS, more holes return to the p-base in DT-MOS than in P-MOS. This explains why P-MOS exhibits more severe gate degradation than DT-MOS over extended periods. Fig. 9(h) shows the physical mechanism of the AT-MOS operating in reverse conduction. Since the deep p-shield partially surrounds the gate, holes have difficulty approaching the channel, the V_{th} keeping stable under this condition.

To investigate the negative V_{th} shift in SiC MOSFETs during body diode conduction under negative $V_{\mathrm{GS\text{-}OFF}}$, TCAD simulations are performed to analyze the physical mechanism.

The device structure employed in this article was calibrated against fabricated conventional SiC MOSFETs. All three simulated devices are based on 4H-SiC technology. The drift region has a thickness of 12 μm with a doping concentration of 8×10^{15} cm^{-3} and an electron mobility of $\sim$840 cm^2/V·s. The p-body and p-shield regions are doped to 2×10^{17} cm^{-3} and 2×10^{18} cm^{-3}, respectively. A 50 nm gate oxide was used in all devices. The channel length is 0.5 μm, with a channel electron mobility of 20 cm^2/V·s for the P-MOS and 60 cm^2/V·s

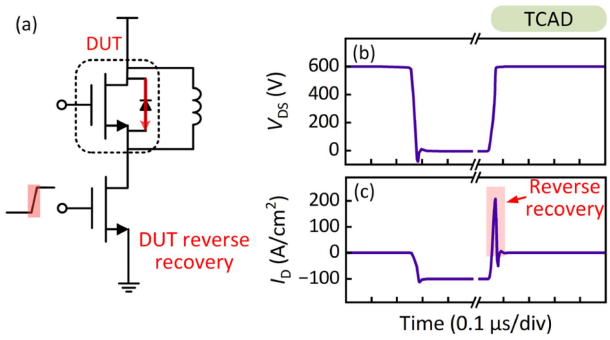

Fig. 10. (a) Double-pulses test circuit used in the simulation. (b) V_{DS} waveform of the DUT. (c) I_D waveform of the DUT.

for both the DT-MOS and AT-MOS. The cell pitch is 4 μm for the P-MOS, 3.5 μm for the DT-MOS, and 2.2 μm for the AT-MOS, where the gate trench accounts for 1 μm of the AT-MOS and DT-MOS cell pitch. All structural and doping parameters are consistent across the simulations to ensure a fair comparison. Fig. 10(a) displays the implemented double pulse test circuit. When the low-side switch turns ON and the inductance has been charged, the high-side transistor (DUT) undergoes reverse recovery. Fig. 10(b) and (c) shows the test waveforms of the double pulse circuit, including V_{DS} and I_{D} of the DUT during the reverse recovery phase. The inductor is charged to a current density of 100 A/cm^2 before the low-side transistor is turned ON. When the low-side transistor is turned ON for the second time, the DUT enters reverse recovery, generating a peak current through the device.

Fig. 11(a)–(c) shows the hole current path distribution and hole current density distribution for three DUTs with $V_{\mathrm{GS\text{-}OFF}} = 0$ V and -10 V at the reverse recovery transient. When $V_{\mathrm{GS\text{-}OFF}} = 0$ V, only a small amount of hole current flows along the SiC/SiO$_2$ interface, thereby the V_{th} remains almost unchanged. When $V_{\mathrm{GS\text{-}OFF}} = -10$ V, for the P-MOS, more holes are attracted by the negative $V_{\mathrm{GS\text{-}OFF}}$, passing through the JFET region and reaching the gate oxide layer. These holes flow along the interface between SiC and SiO$_2$. Due to the high drain voltage, holes are accelerated and gain high energy (becoming hot holes). The hot holes induce positive charge trapping and/or defect generation at the MOS interface, leading to a significant negative V_{th} shift; for the DT-MOS, due to its special double-trench structure and deeper p-base region compared to P-MOS, DT-MOS redirects more holes back to the p-base. However, since the p-base is not adjacent to the channel, hole current still flows along the SiC/SiO$_2$ interface. Under prolonged stress conditions, DT-MOS exhibits superior performance to P-MOS; For the AT-MOS, which adopts an asymmetric trench gate structure by sacrificing one channel, this design effectively protects the gate oxide. During reverse recovery, the structure directs most hole current toward the p-base instead of the channel region. Moreover, it reliably avoids degradation induced by negative gate voltage during body diode conduction. These simulation results indicate that a deeper p-shield can offer strong protection for the gate oxide and provide an insight into engineering out the instability via device structure design.

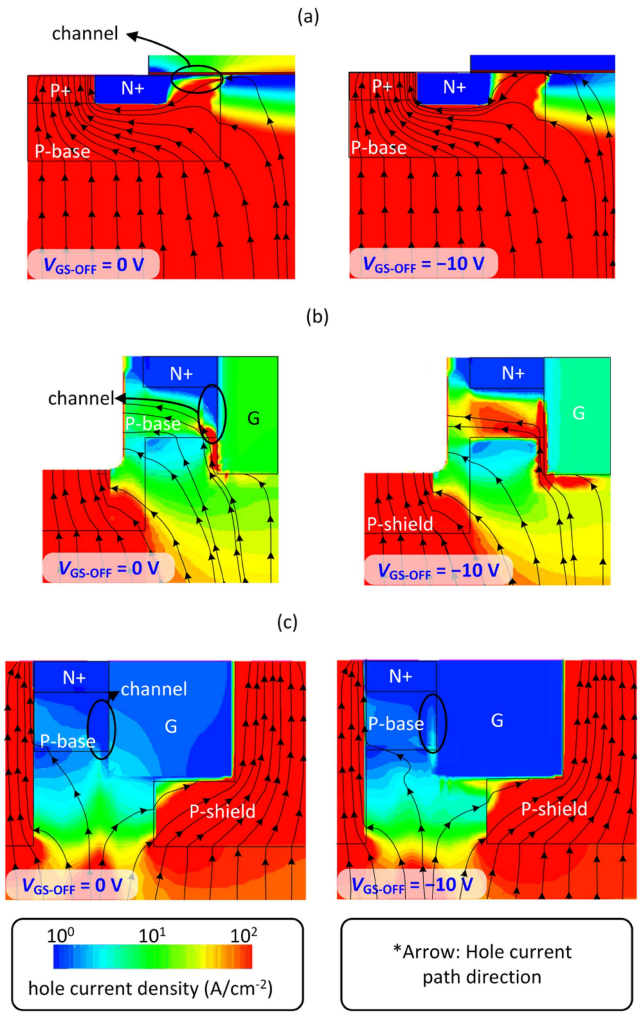

Fig. 11. Hole current path distribution and hole current density distribution during reverse recovery transient in (a) P-MOS, (b) DT-MOS, and (c) AT-MOS structures, comparing $V_{\mathrm{GS\text{-}OFF}} = 0$ V and -10 V conditions.

According to these results, for the P-MOS which remains a very popular solution in current applications, adopting a deeper p-base through channeling implantation represents a viable approach to address the proposed reliability issue [44], [45], [46]. A deeper p-base facilitates more efficient collection of hot holes during reverse recovery, operating in a manner similar to that in an asymmetric trench MOSFET.

V. SBD Impact on V_{TH} Instability

To further prove the impact of the negative V_{th} shift caused by the conduction of the body diode, the DUT is connected in parallel with a 1200 V SiC SBD (STPSC20G12) for comparison. The body diode can be bypassed during switching operations since the SBD has a smaller turn-ON voltage, effectively mitigating V_{th} drift. Unlike the previously mentioned DUT, which consists solely of a MOSFET, the device under test here is a MOSFET /SBD pair. For all types of MOSFET (including P-MOS, DT-MOS, and AT-MOS), the body diode turn-ON voltage is at least approximately 3 V. In the MOS/SBD configuration, the

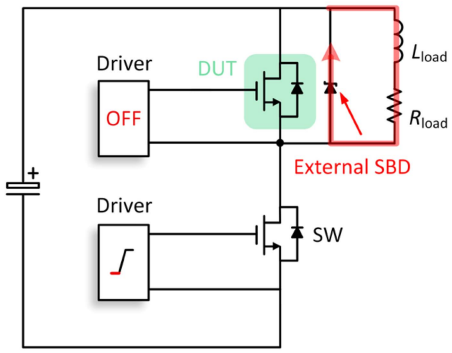

Fig. 12. SBD-paralleled DUT in a half-bridge configuration. During switching operation, the current flows through the Schottky barrier diode (SBD) rather than the body diode.

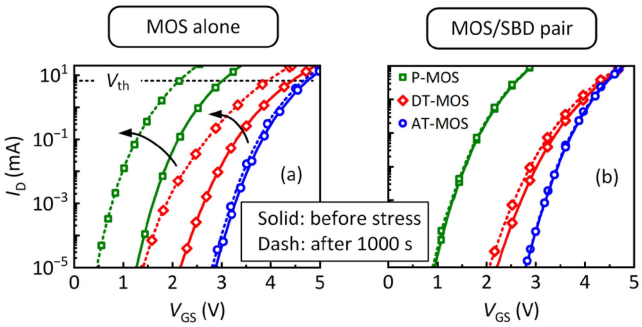

Fig. 13. Comparison of the transfer curves for (a) the MOS alone and (b) the MOS/SBD pair in a half-bridge circuit with $V_{\text{GS-OFF}} = -10$ V, comparing the initial state with the state after a cumulative switching time of 1000 seconds. Solid lines: initial state; dashed lines: after 1000-s operation.

SBD exhibits a turn-ON voltage of about 0.8 V, ensuring that the SBD successfully bypasses the body diode during switching operations.

Fig. 12 shows a half bridge circuit in which a SiC MOSFET serves as the synchronous switch. Compared to the circuit in Fig. 1, an external antiparallel SBD is connected across the synchronous SiC MOSFET. This SBD provides an alternative current path during reverse conduction, bypassing the body diode. As a result, there is no holes injection in n-drift of SiC MOSFET.

Fig. 13(a) and (b) shows the transfer curves of an individual MOSFET (MOS alone) and a MOS/SBD pair, respectively. These curves represent the initial state and the state after the devices underwent cumulative 1000-s switching time in a half-bridge test, where the solid lines denote the initial state and the dashed lines represent the state after 1000-s operation. The test results show that the addition of the SBD effectively prevents the V_{th} shift after this cumulative switching period. When characterized under identical $V_{\text{GS-OFF}}$ conditions, the MOSFET/SBD pair showed no significant negative V_{th} shift, while notable negative V_{th} shift was observed in the MOSFET alone. This comparison confirms that the V_{th} instability originates from body diode operation rather than conventional NBTI mechanisms. According to this phenomenon, two effective design pathways are suggested to mitigate performance degradation. From a circuit design perspective, this can be achieved by using a less negative $V_{\text{GS-OFF}}$ or by connecting an external antiparallel SBD. From a device design perspective, effective solutions include employing an SBD-integrated or channel-diode-integrated MOSFET [47], [48]. The integrated diode inactivates the turn-ON of the body diode due to its lower forward voltage drop, thereby avoiding hole injection from the p-base into the n-drift region. These approaches help enhance device robustness under repetitive body-diode operation.

VI. Conclusion

This article investigates the impact of body diode to V_{th} instability of synchronous SiC MOSFET under switching conditions in bridge-leg circuit. During reverse recovery, holes injected from p-base into n-drift are swept to source and gate region by high drain voltage. Some holes are attracted by the negative gate bias, bombarding the gate oxide and leading to a V_{th} shift. Three commercial SiC MOSFETs are studied, including P-MOS, a DT-MOS, and an AT-MOS. A half-bridge test system is constructed for switching tests, where the DUT operates in the off-state as a freewheeling diode. The test results indicate that the AT-MOS presents the least V_{th} shift due to its deeper p-shield region, which offers strong protection to the gate oxide. Furthermore, when an external anti-parallel SBD is used with synchronous SiC MOSFET in bridge-leg circuit, the abovementioned V_{th} instability of SiC MOSFET can be weakened. This test result further verifies the proposed mechanism. In summary, body diode conduction is proven to induce the gate bias V_{th} instability. Therefore, special care should be taken in the design of power switching circuits that utilize the SiC MOSFET's body diode.

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