Analysis and Mitigation Method of Inrush Current for Quasi-Two-Level Series-Connected SiC MOSFETs

Yangjian Li, Jun Zeng, *Member, IEEE*, Yue Li, Jinghao Zheng, Qing Zhang, Zhuokai Wang, Renjun Hu, Junfeng Liu, *Member, IEEE*, and Zhixing Yan

***Abstract*—Series-connected SiC MOSFETs is considered a promising approach for medium-voltage (MV) dc applications, providing an effective balance between cost and performance. In particular, based on quasi-two-level (Q2L) modulation strategy, the hybrid-clamping structure with indirect series connection is attractive due to its inherent voltage self-balancing capability, eliminating the need for additional voltage control loop. However, the issue that the switched-capacitor loop introduced for self-balancing can cause inrush current and additional turn-ON switching loss in certain device has not been analyzed, which limits the potential of this topology. In this article, the switching process of the device within the switched-capacitor loop is first analyzed, clarifying the mechanisms behind the inrush current and additional losses. Then, an improved hybrid-clamping topology is proposed, which maintains the self-balancing capability while reducing inrush current and turn-ON switching loss. In the end, 2000 V double pulse tests demonstrate effective mitigation of inrush current to the level of the load current, along with an average 23% reduction in turn-ON switching loss. Furthermore, continuous experiment validated the effectiveness of the proposed method.**

***Index Terms*—Hybrid-clamping structure, inrush current, quasi-two-level (Q2L), series-connected, SiC MOSFETs, switched-capacitor, switching loss.**

I. Introduction

With the development of wide bandgap semiconductors, SiC MOSFETs offer advantages such as higher switching speed, lower switching loss, and better thermal stability compared to silicon (Si)-based IGBTs. In medium-voltag (MV) dc applications, such as photovoltaic power generation, energy storage systems, and electric vehicle charging, the adoption of SiC devices enables converters to achieve higher efficiency and power density [1], [2]. However, the high manufacturing cost of higher-voltage SiC MOSFETs has limited their use, making 1.2 and 1.7 kV devices more widely adopted in the market [3]. To balance the cost and performance requirements in MV converter applications, the use of series SiC technology has become the most applicable solution [4]. This technique connects multiple low-voltage SiC MOSFETs in series to withstand higher voltages than a single device, and the main challenge is to ensure dynamic voltage balancing across all devices to prevent localized overvoltage and breakdown [5]. Among existing solutions, three main methods can be identified.

1) Passive snubber-based balancing: This strategy primarily involves parallel snubber circuits to reduce the dv/dt of each device, helping to maintain a lower voltage difference between them [6]. However, reducing the switching speed increases switching loss, which limits the switching frequency of SiC devices [7].

2) Gate-drive-based balancing: This strategy mainly relies on adapting the gate drive to regulate voltage balance. One approach adjusts the gate voltage or driving resistance based on source-drain voltage feedback [8], [9], [10], but this requires high-speed sampling and fast response, posing implementation challenges for fast-switching SiC devices. Another approach uses a single gate driver with coupling circuits to synchronize devices [11], [12], [13], [14], but variations in parasitics lead to inconsistent switching behavior, making voltage balancing difficult.

3) Topology-based balancing: This strategy achieves voltage balancing by constructing power half-bridge structures and indirectly connecting SiC devices in series using clamping circuits [15]. Unlike conventional multilevel modulation methods, a quasi-two-level (Q2L) modulation strategy is introduced, characterized by an extremely short duration of the intermediate voltage level [16]. The clamping circuit is solely responsible for voltage balancing and scarcely participate in the main power transmission path, which greatly reduces both the size and power stress of the devices within the clamping circuit [17].

In MV dc–dc applications, Q2L PWM is applied in a modular multilevel converter (MMC) MV dc–dc converter, which helps mitigate the issue of large energy storage capacitors in traditional MMC [18], [19], [20]. But the large number of MMC

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submodules and frequent switching limit the overall power density and efficiency. To simplify the structure, Q2L-based flying capacitor (FC) and neutral-point clamped (NPC) topologies are considered more attractive [21], [22], [23], as it only the integration of compact clamping circuits implemented with FCs or diodes. However, achieving voltage balancing among devices typically needs additional closed-loop control, which increases system complexity. Based on Q2L PWM, Liu et al. [15] presented a hybrid clamping topology applicable to continuous conduction nonisolated dc–dc structures. It incorporates two switched-capacitor loops, thereby achieving voltage self-balancing. Nevertheless, The analysis does not consider the impact of the switched-capacitor loop under high-voltage and high-current conditions. where a considerable voltage difference may exist between the FC and the dc bus capacitor. If a device in this loop turns on under such conditions, an inrush current will occur, leading to substantial turn-ON switching loss and localized current stress. To address the issues caused by the switched-capacitor loop, a snubber inductor can be introduced to suppress inrush current or enable soft charging. However, its impact on device switching loss has not been addressed [24], [25]. Furthermore, for the hybrid clamping structure, whether the inclusion of the snubber inductor affects the inherent voltage self-balancing capability remains unexplored.

Therefore, to address the issues of the indirectly series-connected hybrid clamping structure, this article presents the first analyzes of the mechanism of inrush current and trun-ON switching loss caused by the switched-capacitor loop, On this basis, an improved method is proposed, in which a snubber inductor is introduced between the dc bus capacitor and the clamping diode midpoint. This method mitigates the inrush current caused by the formation of the switching capacitor loop and reduces the turn-ON switching loss of the devices involved, and the analysis of the device turn-ON process reveals the mechanism. In addition, the operating process of the hybrid clamping structure with the snubber inductor is analyzed, demonstrating that the inclusion of the snubber inductor does not compromise the inherent voltage self-balancing capability of the topology. In conclusion, this article offers the following contributions.

1) The switching process of devices in the switched-capacitor loop of the indirectly series-connected hybrid clamping structure has been first analyzed, further revealing the mechanism of additional losses introduced by the switching capacitors.
2) A snubber inductor is introduced into the switched-capacitor loop to effectively mitigates the inrush currents and reduce switching loss. In addition, design considerations for the inductor are provided.

II. Switching Process Under the Switched-Capacitor Loop

During the operation of the hybrid clamping topology, the introduction of the switched-capacitor loops is critical for maintaining voltage balance across the devices. However, this loop also introduces several challenges.

a) Hybrid clamping topology: As shown in Fig. 1(a), four SiC MOSFETs (S_1, S_2, S_3, S_4) are connected in series, and the clamping circuit of the hybrid clamping topology consists of two diodes (D_1, D_2) and a capacitor C_3. The clamping circuit is designed to maintain voltage balance among devices and only conducts power when the converter leg output voltage V_{M} reaches its intermediate states ($V_{\mathrm{M}} = V_{\mathrm{i}}/2$). Under Q2L modulation strategy (introduced in Section III-B), the duration of the intermediate states is extremely short. Therefore, the clamping circuit can be designed with a low power rating. By employing a small capacitance C_3 and low power diodes D_1 and D_2, voltage self-balancing capability of the topology can be achieved, while also offering the advantage of compact size.

b) Topology operation process: With the employment of a small capacitance C_3, voltage fluctuations of V_{C3} inevitably occur during topology operation process. As shown in Fig. 1(b), V_{C3} oscillates between V_{C1} and V_{C2} (The principle of topology operation process is presented in [15]). When V_{C1} is higher than V_{C3}, the turn-on of S_1 forms a switched-capacitor loop, initiating the switched-capacitor process.

c) Switched-capacitor loop: As shown in Fig. 1(c), once the switched-capacitor process is formed, C_1 begins charge C_3 through the switched-capacitor loop, and the loop parasitic inductance L_{p} provides minimal snubbering during the charging process, resulting in a significant inrush current during the switching of S_1.

d) Turn-ON switching process of S_1: As shown in Fig. 1(d), during the interval from t_1 to t_2, I_{D} is the sum of the load current and the inrush current. Unlike a conventional switching transition, after V_{DS} drops by ΔV (the voltage difference between V_{C1} and V_{C3}) at t_1, it enters a slowly decreasing phase from t_1 to t_2. This leads to a considerable overlap between V_{DS} and I_{D}, resulting in large additional losses. These losses are attributed to the switched-capacitor process and will be analyzed in detail in Section IV-B.

In conclusion, the incorporation of the switched-capacitor loop has a detrimental impact on both the current stress and the turn-ON switching loss of the device.

1) The inrush current significantly increases the current stress on S_1, potentially limiting the operation of the device or even the entire converter under rated current conditions.
2) The added turn-ON switching loss caused by the capacitor loop results in higher power dissipation in S_1, deteriorating its switching performance.

III. Circuit Topology and Operation Principles

In this section, an improved hybrid clamping method is proposed to address the issues discussed in Section II. The voltage balancing principle and the topology operation process of the improved method are also presented.

A. Improvement of the Hybrid Clamping Topology

a) Improved hybrid clamping topology: As shown in Fig. 2(a), different form hybrid clamping topology, the improved hybrid clamping topology introduces a snubber inductor L (much

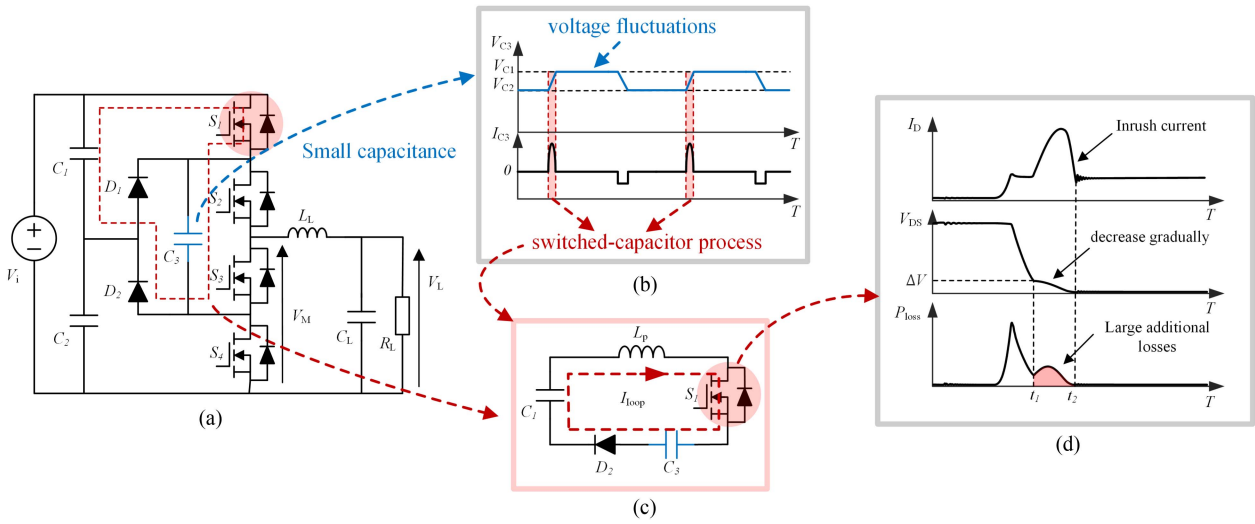

Fig. 1. Switching process under the switched-capacitor loop of hybrid clamping topology. (a) Hybrid clamping topology. (b) Topology operation process. (c) Switched-capacitor loop. (d) Turn-ON switching process of S_1.

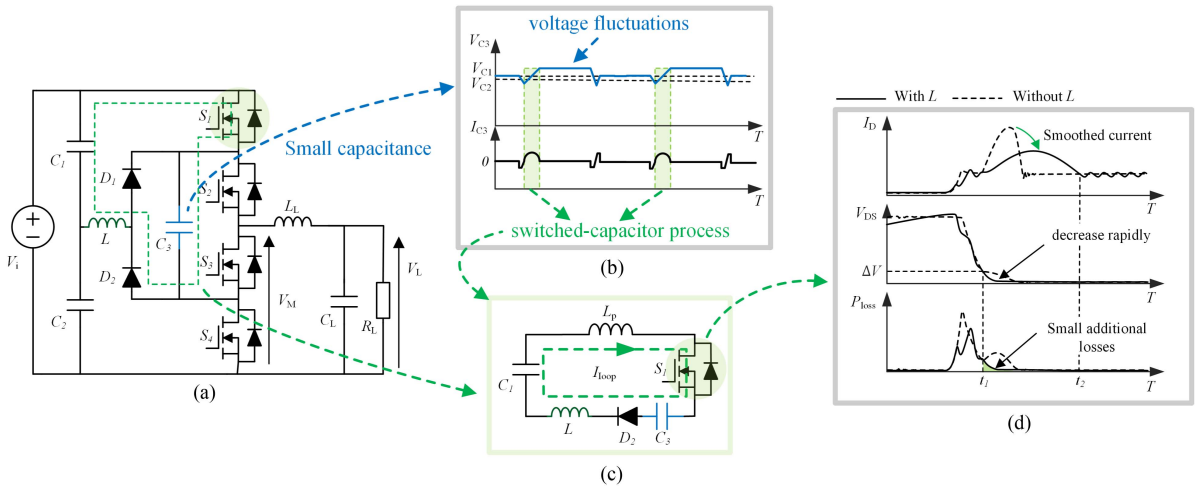

Fig. 2. Switching process under the switched-capacitor loop of the improved hybrid clamping topology. (a) Improved hybrid clamping topology. (b) Topology operations process. (c) Switched-capacitor loop. (d) Turn-ON switching process of S_1.

greater than L_p), which is inserted between the midpoint of the dc bus and the clamping circuit.

b) Topology operation process: As shown in Fig. 2(b), similar to previous cases, the use of a small value capacitance C_3 causes voltage fluctuations in V_{C3}. When V_{C1} is higher than V_{C3}, the turn-ON of S_1 forms a switched-capacitor loop, initiating the switched-capacitor process.

c) Switched-capacitor loop: As shown in Fig. 2(c), a snubber inductor L is introduced into the switched-capacitor loop to mitigate the inrush current.

d) Turn-ON switching process of S_1: As shown in Fig. 2(d), the introduction of L converts the original inrush current into smoothed current, and accelerates the voltage drop of V_{DS} during the phase from t_1 to t_2. This effectively reduces the additional losses caused by the switched-capacitor process.

The introduction of the snubber inductor L effectively reduces the inrush current and trun-ON switching loss of S_1. Moreover, the added inductance does not compromise the voltage balancing, as will be further demonstrated in the following analysis.

B. Q2L Modulation Strategy

The Q2L modulation strategy is illustrated in Fig. 3, which shows the gate-source voltages V_{GS} of devices S_1, S_2, S_3, and S_4, as well as the converter leg output voltage V_M. When S_1 and S_2 are turned ON, $V_M = V_i$; When S_1 is turned OFFand S_2 is turned ON, $V_M = V_i/2$; When S_1 and S_2 are turned OFF, $V_M = 0$. Unlike three-level modulation strategies, the duration (ΔT) of its intermediate states ($V_M = V_i/2$) is relatively short, typically in the range of several hundred nanoseconds, and T_{dead} represents the dead time. The duty cycle D can be calculated as

$$D = \frac{T_{S1} + T_{S2}}{2T} \tag{1}$$

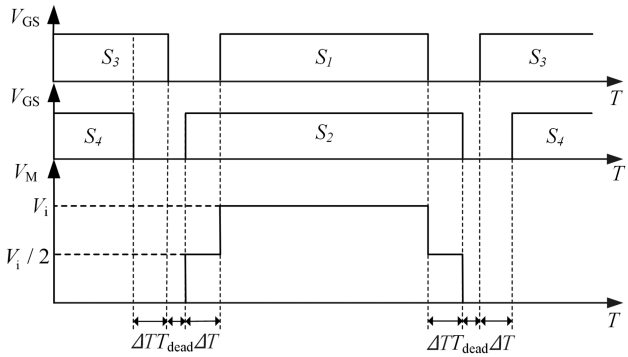

Fig. 3. Q2L modulation strategy.

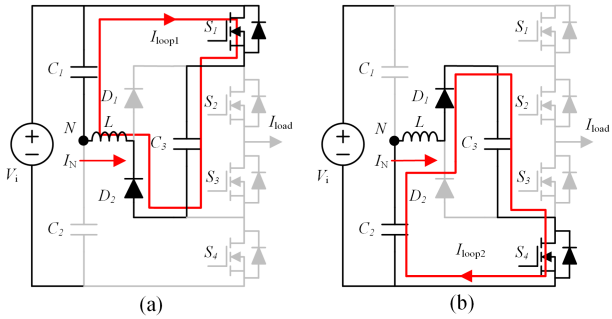

Fig. 4. Switched-capacitor loops. (a) When S_1 is on. (b) When S_4 is on.

where T_{S1} and T_{S2} represent the switching times of S_1 and S_2, respectively, and T denotes the switching cycle.

C. Voltage Balancing Mechanism of the Devices

Voltage balancing during device operation is the most fundamental requirement for series-connected topologies. The proposed topology inherently achieves voltage self-balancing, which is primarily governed by two key factors.

1) The proposed topology introduce two switched-capacitor loops, as shown in Fig. 4. When either S_1 or S_4 is turned ON, the bus capacitor C_1 or C_2 charges the FC C_3, ensuring that V_{C3} does not fall below V_{C1} and V_{C2}.
2) Under continuous conduction mode (CCM), the load current is unipolar. For the Q2L modulation strategy shown in Fig. 3, when S_1 is turned OFFand S_2 is turned ON, C_3 discharges during two intermediate states through the path which is shown in Fig. 5 ⓐ, ensuring that V_{C3} does not remain higher than V_{C1} and V_{C2}.

Therefore, if $V_{C1} \approx V_{C2} \approx V_i/2$ and remain stable, the presence of the switched-capacitor loop prevents V_{C3} from dropping to zero, while the continuous discharging during the intermediate states prevents V_{C3} from rising to V_i, and the combined effect of these two mechanisms leads to the existence of a steady state where $V_{C1} \approx V_{C2} \approx V_{C3} \approx V_i/2$, ensuring voltage balancing across the devices. To ensure bus voltage V_{C1} and V_{C2} remain stable, the net charge Q_N flowing through the point N over one switching cycle must be zero, which leads to the following condition:

$$Q_N = \int_0^T I_N dt = 0. \tag{2}$$

To satisfy this condition, $V_{C1} > V_{C2}$ must exist. It can be assumed that $V_{C1} = V_{C2}$, under which condition $Q_N > 0$. When $V_{C1} < V_{C2}$, Q_N becomes even larger, causing C_1 to charge and C_2 to discharge until $V_{C1} - V_{C2} = \Delta V$. To calculate the bus capacitor voltage difference ΔV and the voltage variation of the FC C_3, a detailed analysis of the topological operation process will be carried out.

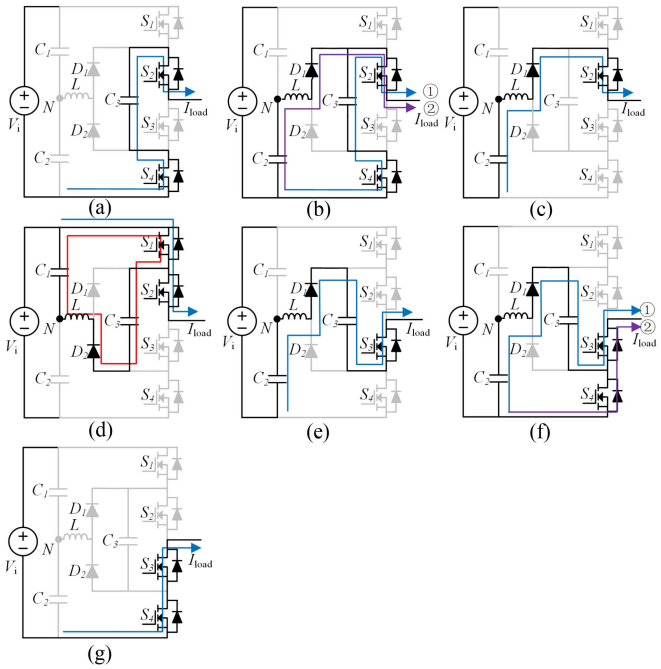

Fig. 5. Commutation paths of improved hybrid clamping topology. (a) Mode ⓐ. (b) Mode ⓑ. (c) Mode ⓒ. (d) Mode ⓓ. (e) Mode ⓔ. (f) Mode ⓕ. (g) Mode ⓖ.

D. Topology Operation Process

Before analyzing the topology operation process, the following assumptions are made: 1) C_1 and C_2 are large enough, and are considered as a voltage source in the resonant loop; 2) the commutation process is extremely short, and the load current I_{load} is considered constant during commutation; 3) the commutation calculation process neglects the parasitic inductance L_p and parasitic resistance R_{loop1} and R_{loop2}; and 4) all switches are ideal.

Under CCM, three possible operating cases exist depending on the commutation process. the possible commutation paths for each case are illustrated in the Fig. 5.

Case 1: ⓖ-ⓐ-ⓑ-ⓒ-ⓓ-ⓐ-ⓑ-ⓔ-ⓕ-ⓖ

As shown in Fig. 6. After t_1, the topology operates in ⓐ, C_3 is discharged by I_{load}, and its voltage drops to V_{C2} at time t_2. After t_2, the topology operates in ⓑ, where I_{load} commutates from ① to path ②. During the commutation, C_2 acts as a voltage source, while L, C_3 resonate in the loop shown in Fig. 4(b), with

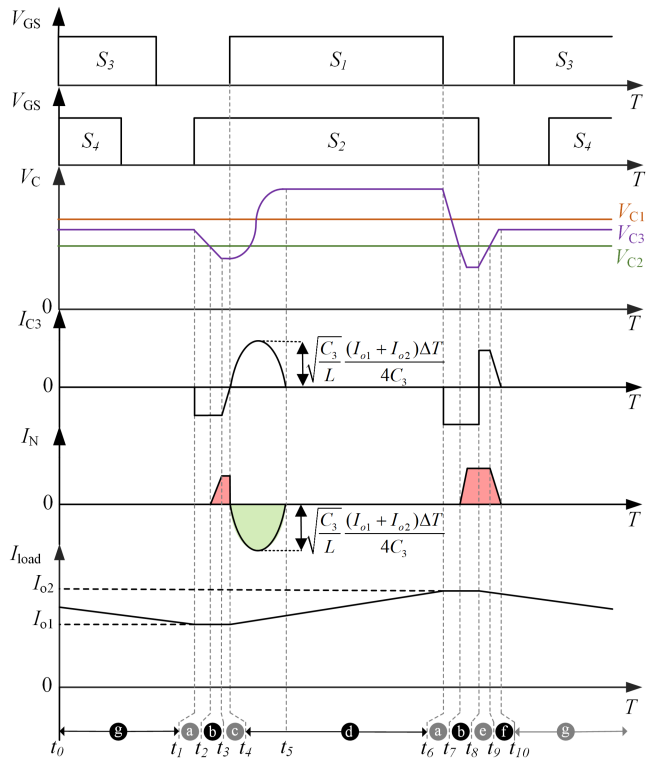

Fig. 6. Topology operation process (Case 1).

C_3 having an initial current of I_{01} and an initial voltage of V_{C2}. The voltage across V_{C3} can be derived from the second-order differential equation

$$\begin{cases} V_{C3}(t) = -\frac{I_{o1}}{C_3\omega_0}\sin\left(\omega_0(t-t_2)\right) + V_{C2}. \\ \omega_0 = \frac{1}{\sqrt{LC_3}} \end{cases} \tag{3}$$

At time t_3, the commutation is completed, I_{C3} drops to zero, when $t - t_2 = \frac{\pi}{2}$ and V_{C3} settles at

$$V_{C3}(t_3) = V_{C2} - \frac{I_{o1}}{C_3\omega_0}. \tag{4}$$

After t_3, the topology operates in ⓒ until the end of the interval at t_4. As $V_{C3}(t_1) = V_K$, From t_1 to t_4, the net charge Q_N is

$$Q_{N1} = I_{01}\Delta T - C_3\left(V_K - V_{C2} + \frac{I_{o1}}{C_3\omega_0}\right). \tag{5}$$

After t_4, The topology operates in ⓓ, and switched-capacitor loop is formed, during which C_3 is charged. C_1 acts as a voltage source, while L, C_3 resonate in the loop shown in Fig. 4(a), with C_3 having an initial voltage of $V_{C3}(t_3)$. The expression of V_{C3} and I_{C3} can be derived

$$\begin{cases} V_{C3}(t-t_4) &= A\cos(\omega_0(t-t_4)) + V_{C1} \\ I_{C3}(t-t_4) &= -C_3\omega_0 A\sin\omega_0(t-t_4) \end{cases} \tag{6}$$

$$A = V_{C2} - \frac{I_{o1}}{C_3\omega_0} - V_{C1}. \tag{7}$$

When I_{C3} reaches zero after half a resonant cycle ($t - t_4 = \pi$), the charging of C_3 ends due to the turn-OFFof the diode in the switched-capacitor loop. At this moment, V_{C3} is

$$V_{C3}(t_5) = 2V_{C1} - V_{C2} + \frac{I_{o1}}{C_3\omega_0}. \tag{8}$$

From t_4 to t_5, the net charge Q_N is

$$Q_{N2} = -2C_3\left(V_{C1} - V_{C2} + \frac{I_{o1}}{C_3\omega_0}\right). \tag{9}$$

From t_6 to t_8, the topology operates in ⓐ and ⓑ. Similar to the previous analysis, V_{C3} at t_8 can be obtained as

$$V_{C3}(t_8) = V_{C2} - \frac{I_{o2}}{C_3\omega_0}. \tag{10}$$

From t_6 to t_8, the net charge Q_N is

$$Q_{N3} = I_{o2}\Delta T - C_3\left[2(V_{C1} - V_{C2}) + \frac{I_{o1}}{C_3\omega_0} + \frac{I_{o2}}{C_3\omega_0}\right]. \tag{11}$$

After t_8, S_2 turns OFFand the topology operates in ⓔ, during which C_3 is charged until V_{C3} equals V_{C2}.

After t_9, the topology operates in ⓕ. The load current begins to commutate from path ① to path ②, and fully transfers to path ② at t_{10}. During this interval, L, C_3 resonate in the loop shown in Fig. 4(b), with C_3 having an initial current of I_{o2} and an initial voltage of V_{C2}. The commutation ends at t_{10} when I_{C3} becomes zero, and V_{C3} is equal to V_K.

$$V_{C3}(t_{10}) = V_{C2} + \frac{I_{o2}}{C_3\omega_0} = V_K. \tag{12}$$

From t_8 to t_{10}, the net charge Q_N is

$$Q_{N4} = 2C_3\frac{I_{o2}}{C_3\omega_0}. \tag{13}$$

Combining (5), (9), (11), (13), Q_N over one switching cycle can be derived

$$\begin{aligned} Q_N = (I_{o1} + I_{o2})\Delta T - 4C_3\frac{I_{o1}}{C_3\omega_0} \\ - 4C_3(V_{C1} - V_{C2}). \end{aligned} \tag{14}$$

According to the condition in (2), $V_{C1} - V_{C2}$ can be obtained

$$\begin{aligned} V_{C1} - V_{C2} &= \frac{(I_{o1} + I_{o2})\Delta T}{4C_3} - \frac{I_{o1}}{C_3\omega_0} \\ &= \frac{(I_{o1} + I_{o2})\Delta T}{4C_3} - I_{o1}\sqrt{\frac{L}{C_3}}. \end{aligned} \tag{15}$$

Meanwhile, the peak value of the inrush current in the switched-capacitor loop can be obtained from (6), (7)

$$\begin{aligned} I_{inrush} &= C_3\omega_0(V_{C1} + \frac{I_{o1}}{C_3\omega_0} - V_{C2}) \\ &= \sqrt{\frac{C_3}{L}}\frac{(I_{o1} + I_{o2})\Delta T}{4C_3} = \sqrt{\frac{C_3}{L}}\Delta V. \end{aligned} \tag{16}$$

In Case 1, seven operating modes are identified. However, with the increase of the inductance L, Modes ⓒ and ⓔ may disappear. This is because a larger L prevents the inductor

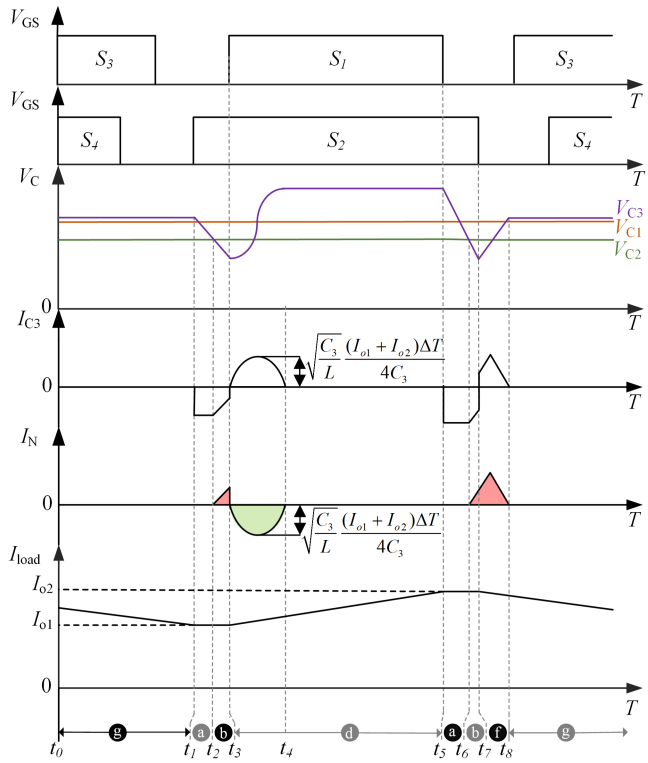

Fig. 7. Topology operation process (Case 2).

current at t_3 and t_8 from reaching I_{o1} and I_{o2}, Therefore, based on the two boundary conditions $I(t_3) = I_{o1}$ and $I(t_8) = I_{o2}$, it can be determined as

$$\begin{cases} \frac{(I_{o1}+I_{o2})\sqrt{LC_3}}{I_{o1}} = \Delta T \\ 2\sqrt{LC_3} = \Delta T. \end{cases} \tag{17}$$

Based on the condition $I_{o1} < I_{o2}$, the boundary conditions of the three possible operating Cases can be derived as follows:

Case 1: $2\sqrt{LC_3} = \Delta T$

Case 2: $\frac{(I_{o1}+I_{o2})\sqrt{LC_3}}{I_{o1}} > \Delta T$

Case 3: $\frac{(I_{o1}+I_{o2})\sqrt{LC_3}}{I_{o1}} < \Delta T < 2\sqrt{LC_3}$.

Case 2: ⓖ-ⓐ-ⓑ-ⓓ-ⓐ-ⓑ-ⓕ-ⓖ

As shown in Fig. 7, compared with Case 1, Case 2 does not include ⓒ and ⓔ. Following the same analytical approach as in Case 1, $V_{C1} - V_{C2}$ and I_{inrush} can be obtained:

$$\begin{cases} V_{C1} - V_{C2} = \frac{(I_{o1}+I_{o2})\Delta T}{4C_3} - I_{o1}\sqrt{\frac{L}{C_3}}\sin\omega_0\Delta t_1 \\ \Delta T - \Delta t_1 = \frac{I_{o1}}{I_{o2}}\sqrt{LC_3}\sin(\omega_0\Delta t_1) + \frac{(I_{o2}-I_{o1})\Delta T}{2I_{o2}} \end{cases} \tag{18}$$

$$\begin{aligned} I_{inrush} &= \sqrt{\frac{C_3}{L}}(V_{C1} - V_{C2} + I_{o1}\sqrt{\frac{L}{C_3}}\sin\omega_0\Delta t_1) \\ &= \sqrt{\frac{C_3}{L}}\frac{(I_{o1}+I_{o2})\Delta T}{4C_3} = \sqrt{\frac{C_3}{L}}\Delta V. \end{aligned} \tag{19}$$

Case 3: ⓖ-ⓐ-ⓑ-ⓓ-ⓐ-ⓑ-ⓔ-ⓕ-ⓖ

Case 3 can be regarded as a combination of Case 1 and Case 2. During one switching cycle, the first half of the commutation process is identical to that shown in Fig. 7, while the second half corresponds to Fig. 6. Following the same derivation as before, the expressions for the voltage difference $V_{C1} - V_{C2}$ and I_{inrush} remain the same as those in (18) and (19).

To sum up, as the L increases, the system operating mode changes when ΔT remains constant. In the case of small inductance (Case 1), increasing the inductance significantly reduces $V_{C1} - V_{C2}$, as indicated by (15), which is beneficial for balancing the bus capacitor voltages. When the inductance becomes larger (Case 2 and Case 3), further increases in inductance do not cause $V_{C1} - V_{C2}$ to become negative. This is because the $\sin(\omega_0\Delta t_1)$ in (18) limits the continuous decrease of $V_{C1} - V_{C2}$, which is consistent with the analysis in Section III-C. Furthermore, based on (16) and (19), the magnitude of the inrush current is directly affected by the inductance L. A larger value of L significantly reduces the inrush current.

IV. Design Considerations and Turn-On Switching Loss Modeling Analysis

A. Design Consideration

The design mainly considers three aspects: the selection of inductance L, the clamping capacitance C_3, and the ΔT.

1) Adding an snubber inductor helps mitigate the inrush current and turn-ON switching loss of S_1 during switching process, while also helping to reduce the voltage difference between the dc-link capacitors. Therefore, The snubber inductor design mainly considers two aspects.

First, the inrush current (the switching process of S_1) should be limited such that the peak current during the switching process is approximately 1.5∼2 times I_{o1}. This design helps constrain the impact of the inrush current on device current stress. Moreover, the reduced inrush current effectively minimizes additional switching losses, keeping them at a low level. This mechanism is further discussed in Sections IV-B and IV-C. Therefore, according to the inrush current equation (19) under Case 2 conditions, the snubber inductor should satisfy

$$L = C_3\left(\frac{(I_{o1}+I_{o2})\Delta T}{4kC_3I_{o1}}\right)^2, k = 0.5 \sim 1. \tag{20}$$

Second, the voltage difference between V_{C1} and V_{C2} should be maintained at a low level. In this case, the converter will operate in Case 2. According to the conditions of Case 2, the snubber inductor should satisfy

$$L > \frac{I_{o1}^2\Delta T^2}{C_3(I_{o1}+I_{o2})^2}. \tag{21}$$

By satisfying the above two conditions, on one hand, the insertion of the snubber inductor helps reduce the inrush current, switching losses, and the voltage difference between the dc-link capacitors. On the other hand, the inductance is kept from being excessively large, preventing an increase in the overall system size and avoiding unnecessary additional losses.

In terms of inductor packaging, an integrated molded power inductor can be selected due to its advantages of low parasitic parameters, high current-carrying capability, high power density, and strong mechanical robustness. According to the topology operation process analysis, the current flowing through

the snubber inductor only exhibits several short spikes within one switching cycle and does not participate in the main power loop, resulting in a relatively small power rating. Therefore, by using an integrated molded inductor, the additional inductive loss can be considered negligible, while the high power density helps maintain the compact size advantage of the Q2L clamping circuit.

2) The design of the FC primarily considers its rated voltage, rated current, and capacitance value. For the rated voltage, its value should exceed $V_{\rm i}/2$ with a sufficient safety margin. For the rated current, after selecting the snubber inductor, according to the capacitor waveform in Case 2 of Fig. 7 and the selection criterion of the snubber inductor, the inrush current caused by the switched-capacitor loop has been limited below the load current. Therefore, its current stress only needs to meet the load current requirement. In addition, the capacitance should be selected based on the acceptable voltage ripple.

3) The selection of ΔT should be as small as possible to reduce the power loss in the clamping circuit. At the same time, the switching time of the MOSFETs needs to be considered to avoid interference with the switching process.

B. Switching Loss Modeling

To analyze in detail the turn-ON switching transient of the switched-capacitor loop in the hybrid clamping topology under Q2L modulation, an LTspice simulation is carried out, the circuit is shown in Fig. 1(a). The SiC MOSFETs uses the SPICE model C3M0032120J1, and the diode uses C4D20120A. The FC C_3 was set to 50 nF, and the dc-link capacitors C_1 and C_2 were both set to 10 μF. No additional inductance was included in the circuit. The load consists of an inductor of 1 mH, a capacitor of 100 μF, and a resistor of 40 Ω. The dc bus voltage was 2000 V. ΔT and $T_{\rm dead}$ was set to 400 ns, the duty cycle and the switching frequency were set to 50%, and 50 kHz. The turn-ON switching process of S_1 is shown in Fig. 8.

1) $t_1 - t_2$: The gate driver voltage rises from $-5\,V$ to $20\,V$, and $V_{\rm GS}$ increases until it reaches the MOSFET threshold voltage $V_{\rm GS,th}$ at t_2. In this period, the drain current $I_{\rm D}$ remains zero, and no switching loss occurs.

2) $t_2 - t_3$: As $V_{\rm GS}$ exceeds the threshold voltage $V_{\rm GS,th}$, the drain current I_D begins to increase and reaches the load current $I_{\rm load}$ at t_3. Since the diode of D_1 has turned ON, as shown in Fig. 5 ⓒ, $V_{\rm DS}$ remains clamped by $V_{\rm C1}$, resulting in switching loss $E_{\rm on1}$

$$E_{\rm on1} = \int_{t_2}^{t_3} I_{\rm D} \cdot V_{\rm DS} dt. \tag{22}$$

3) $t_3 - t_4$: The device enters the Miller plateau. The gate-to-source capacitance is charged, and $V_{\rm DS}$ begins to drop. The diode of D_1 turns OFF, causing reverse recovery current and loss $E_{\rm D}$, while $I_{\rm load}$ contributes additional switching loss $E_{\rm on2}(t_3 - t_4)$

$$E_{\rm on2}(t_3 - t_4) = \int_{t_3}^{t_4} I_{\rm load} \cdot V_{\rm DS} dt. \tag{23}$$

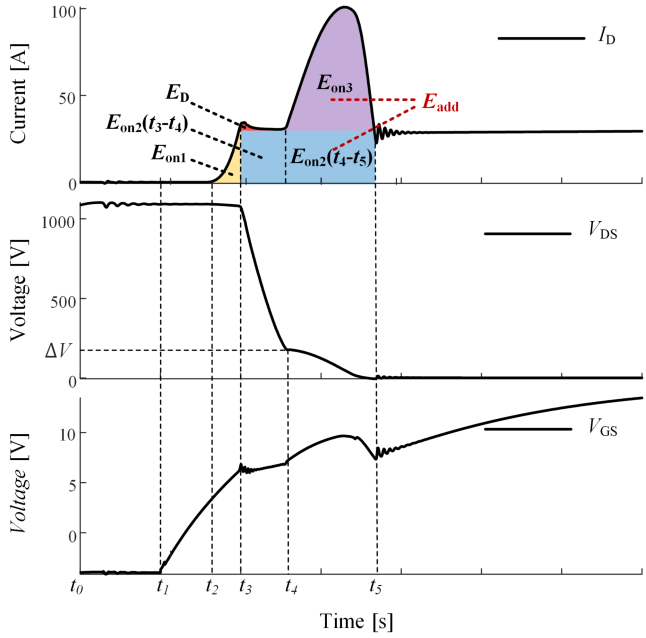

Fig. 8. Turn-ON switching loss modeling.

4) $t_4 - t_5$: $V_{\rm DS}$ drops to ΔV, and diode D_2 turns ON, forming the switched-capacitor loop. Capacitor C_1 starts charging C_3, with $V_{\rm C1} - V_{\rm C3} = \Delta V$ and $V_{\rm S1} - V_{\rm D2} = \Delta V$. According to (16), the inrush current primarily depends on ΔV and loop inductance L. In the absence of snubber inductor, the loop inductance is mainly composed of small parasitic inductance $L_{\rm p}$, resulting in a large inrush current. Due to the small voltage drop across $L_{\rm p}$, most of the ΔV appears across S_1, causing a slow decline in $V_{\rm DS}$, which reaches zero at t_5. During this stage, $I_{\rm D}$ consists of two components: the loop current $I_{\rm loop1}$ and the load current $I_{\rm load}$. Therefore, a significant overlap between the drain current $I_{\rm D}$ and the drain-source voltage $V_{\rm DS}$ occurs during turn-ON switching, resulting in turn-ON switching loss that can be divided into two components: $E_{\rm on2}(t_4 - t_5)$ and $E_{\rm on3}$. At this stage, the switch remains in the Miller plateau, and the introduction of the switched capacitor causes the Miller duration to be prolonged

$$E_{\rm on2}(t_4 - t_5) = \int_{t_4}^{t_5} I_{\rm load} \cdot V_{\rm DS} dt \tag{24}$$

$$E_{\rm on3} = \int_{t_5}^{t_6} I_{\rm loop1} \cdot V_{\rm DS} dt. \tag{25}$$

These two components of loss do not exist in conventional hard-switching. Their presence is mainly caused by the existence of the switched-capacitor loop. These additional losses are defined as $E_{\rm add}$.

$$E_{\rm add} = E_{\rm on2}(t_4 - t_5) + E_{\rm on3}. \tag{26}$$

5) t_5˜: Diode D_2 becomes reverse-biased, blocking reverse current, and the gate-drain capacitance is charged until the switch is fully turned ON.

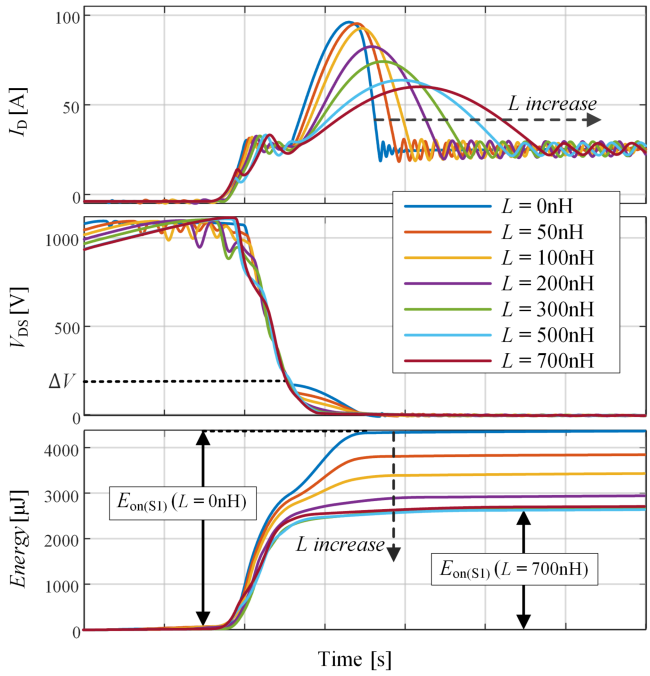

Fig. 9. Simulation switching waveforms for the turn-on switching transient at $V_i = 2000$ V and $I_D = 25$ A, and snubber inductor L of 0-700 nH.

Consequently, the total turn-ON switching loss of S_1 can be expressed as the sum of the individual loss components

$$E_{on(S1)} = E_{on1} + E_{on2}(t_3 - t_4) + E_{on2}(t_4 - t_5) + E_{on3} + E_D = E_{on1} + E_{on2} + E_{on3} + E_D. \quad (27)$$

C. Switching Performance

To evaluate the effectiveness of introducing an snubber inductor L in mitigating inrush current and reducing turn-ON switching loss, a set of comparative simulation experiments is conducted. The experimental circuit is shown in Fig. 2(a). Based on the parameters given in Section IV-B, inductors of 50, 100, 200, 300, 500, and 700 nH are added as L.

As shown in Fig. 9, the inrush current during the turn-ON switching process decreases as the inductance increases. Meanwhile, once V_{DS} drops to ΔV, a larger inductance accelerates the voltage drop of V_{DS}. This occurs because the added inductance helps absorb the voltage difference ΔV between C_1 and C_2 after the diode turns ON, allowing V_{DS} to fall more rapidly. As a result, the overlap between voltage and current during switching process is reduced, contributing to lower switching loss.

From the energy curves, as the inductance L increases, the turn-ON loss $E_{on(S1)}$ decreases. However, when the inductance exceeds 300nH, its impact on turn-ON switching loss becomes less pronounced. This is because the primary function of adding L is to suppress the losses E_{add} caused by the switched-capacitor loop. Once L increases beyond a certain point, the falling rate of V_{DS} becomes sufficiently fast to nearly eliminate the overlap region. At this stage, further increasing L no longer contributes to switching loss reduction.

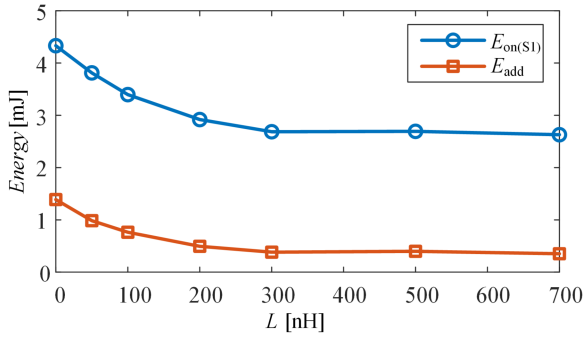

Fig. 10. Turn-ON switching energy of $E_{on(S1)}$ and E_{add}.

As shown in Fig. 10, the switching loss of S_1 ($E_{on(S1)}$) and the additional losses caused by the switching capacitor (E_{add}) vary with the increase of the snubber inductor L. $E_{on(S1)}$ and E_{add} are calculated according to (26) and (27). As L increases, both $E_{on(S1)}$ and E_{add} gradually decrease. When L exceeds 300 ṅH, the two losses reach a balance and no longer decrease. At this point, E_{add} remains at a low level and is mainly composed of conduction loss. Since S_2 is not affected by the switched-capacitor loop, its switching behavior follows conventional hard switching. Therefore, When the influence of the switched-capacitor loop on S_1 is eliminated by the introduction of L, the switching behavior of S_1 approaches that of conventional hard switching, and the switching loss of S_1 and S_2 become comparable.

V. Experimental Verification

To verify the experimental effectiveness of the snubber inductor on the turn-ON switching loss of devices in the switched-capacitor circuit, turn-ON switching loss was evaluated using 2000 V DPTs under various current levels. In addition, a 1000 V/20 A continuous test was conducted to examine the influence of the snubber inductor on bus voltage balance and FC voltage balance. Furthermore, a comparison between the hybrid-clamping topology and the improved hybrid-clamping topology was carried out.

A. Double Pulse Test (DPT) Results

The 2000 V DPT circuit and modulation scheme are shown in Fig. 11. and the Experimental prototype of DPT test is built as shown in Fig. 12. The experimental setup is built using two AST Technology 1700 V SiC MOSFET modules (ASC800N1700MED). In the modulation strategy, S_1 and S_2 are controlled using the Q2L scheme described in Section III-B, while S_3 and S_4 are kept OFF with negative gate bias. Capacitors C_1 and C_2 serve as the dc-link capacitors, C_3 is the FC, and C_4 functions as the decoupling capacitor. To ensure that the voltage imbalance $\Delta V = V_{C1} - V_{C3}$ remains consistent in the comparative DPT experiments, voltage divider resistors are employed to divide the voltage across the two bus capacitors C_1 and C_2, thereby indirectly controlling $\Delta V = V_{C1} - V_{C3}$, and the voltage difference $V_{C1} - V_{C2}$ is calculated based on (15) and (18) to emulate continuous operation, I_{o1} refers to the current at the end

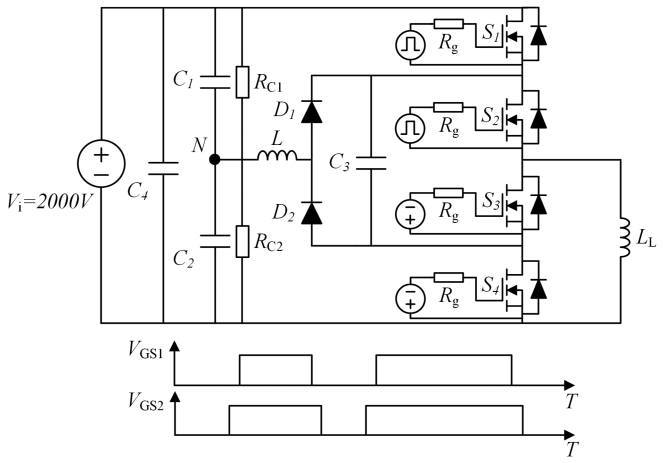

Fig. 11. DPT circuit and modulation scheme.

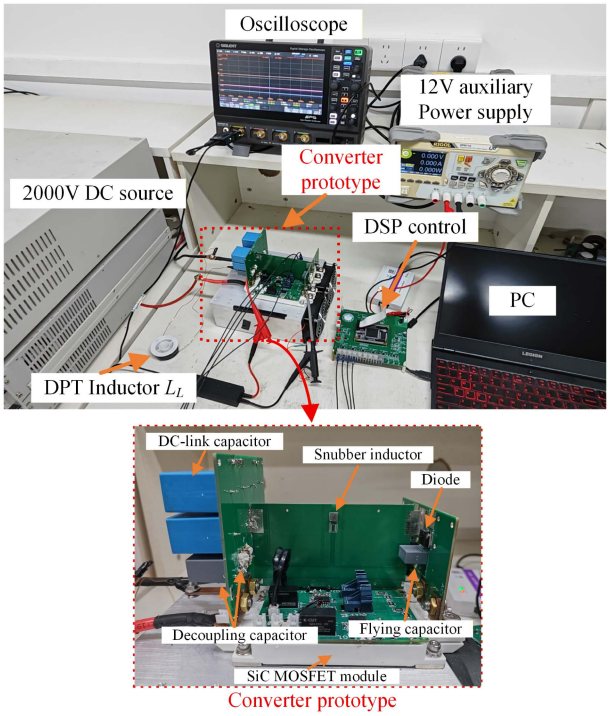

Fig. 12. Experimental prototype of DPT test.

of the first pulse in the DPT. In this study, a comparative experiment was made between two cases: $L = 0$ nH and $L = 800$ nH [satisfies the range specified in (20) and (21)], and the snubber inductor L adopts the YSPIT0520A-R80M integrated molded power inductor from YJYCOIN. The key parameters of the devices and components used in the setup are summarized in Table I.

Fig. 13 shows the DPT waveforms and the switching turn-ON process of the second pulse S_1 under $L = 0$ nH and $L = 800$ nH. The first pulse is set to 10 μs, and the load current reaches $I_D = 50$A after the first pulse. Under this condition, After the snubber inductor L is added, the inrush current of S_1 is reduced from 129.5 to 80.7 A, a decrease of 37.7 %, effectively alleviating the current stress on the device. The voltage imbalance $\Delta V = V_{C1} - V_{C3}$ under the two conditions is 168.08 and 165.53 V, respectively. The difference between them is small, and its influence on the switching loss can be considered negligible.

TABLE I
PARAMETERS OF THE CONVERTER PROTOTYPE OF DPT

Parameter	Description
SiC MOSFET module	1700V(ASC800N-1700MED)
Diode D_1 and D_2	1700V(NTBG028N-170M1)
DC-link capacitors C_1 and C_2	10 μF
Flying capacitor C_3	100 nF
decoupling capacitor C_4	1.665 μF
DPT inductor L_L	800 μH
Snubber inductor L	800 nH(YSPIT0520A-R80M)
Intermediate states time ΔT	400 ns

TABLE II
PARAMETERS OF THE CONVERTER PROTOTYPE OF CONTINUOUS EXPERIMENT

Parameter	Description
DC-link capacitors C_1 and C_2	10 μF
Flying capacitor C_3	100 nF
decoupling capacitor C_4	1.665 μF
Load inductor L_L	3 mH
Load capacitor C_L	100 μF
Load resistor R_L	20 Ω
Snubber inductor L	800 nH
Intermediate states time ΔT	400 ns
Duty cycle D	0.4
frequency f	25 kHz

From the loss calculation results, the turn-ON switching loss of S_1 decreases from 9.12 to 6.94 mJ, a reduction of 23.9 %. it can be seen that due to the reduction of inrush current and the disappearance of the slow drop in V_{DS}, the overlapping area of voltage and current is reduced. This loss reduction is primarily attributed to the suppression of additional losses caused by the switching capacitor loop.

Figs. 14 and 15, respectively, show the turn-ON switching loss calculations and the inrush current magnitude during the turn-ON process of S_1 under different load currents I_{load}. It can be observed that both the turn-ON switching loss and inrush current increase as I_{load} increases. With the added snubber inductor L, the turn-ON switching loss is reduced, with an overall decrease of approximately 23%, and the inrush current is mitigated, keeping it close to the load current I_{load} during the turn-ON process.

B. Continuous Experiment Results

In the continuous experimental verification, two comparative groups were set up: the hybrid-clamped topology (without snubber inductor, $L = 0$, operating in Case 1) and the improved hybrid-clamped topology (with a snubber inductor inserted, $L = 800$ nH, operating in Case 2). All experiments were conducted under an input voltage of $V_i = 1000V$ and a load current of $I_{load} = 20A$. The experimental circuit is shown in Fig. 2(a), and the key parameters of the devices and components used in the experimental setup are summarized in Table II.

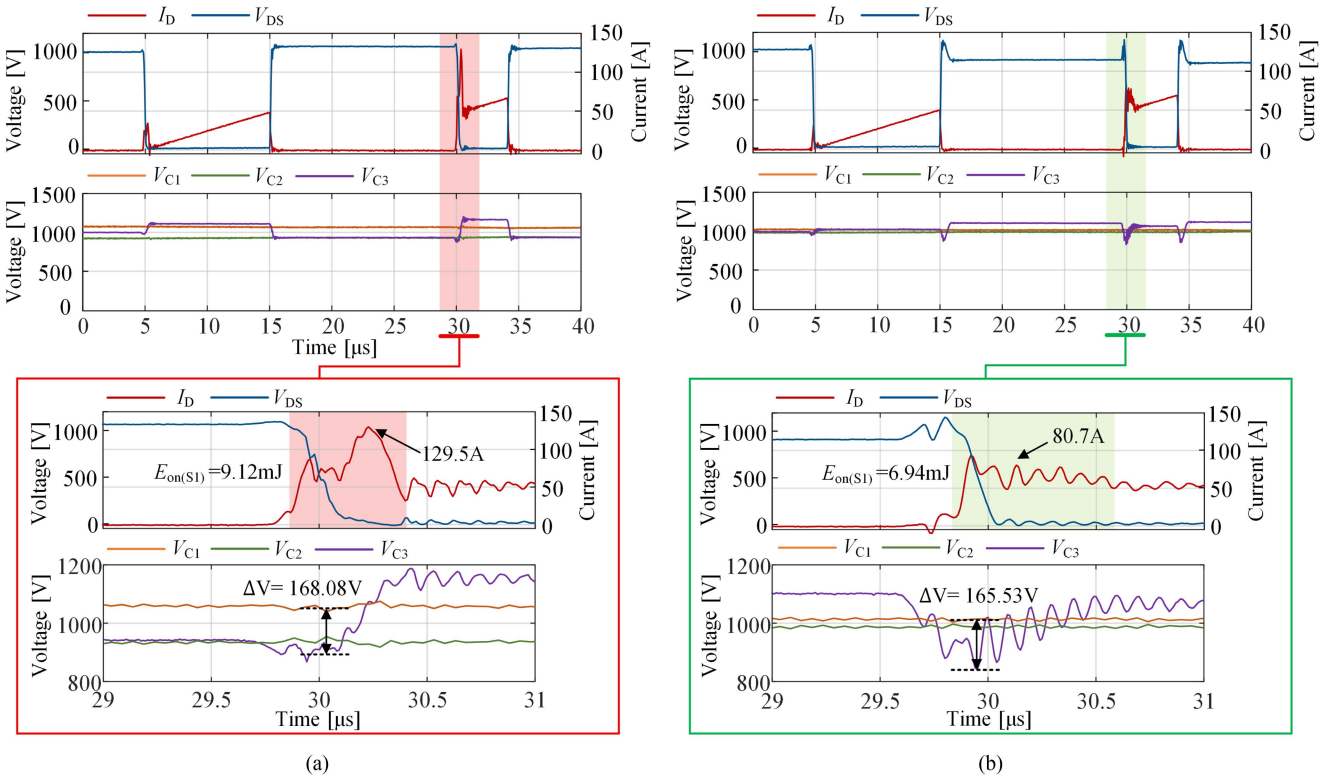

Fig. 13. Experimental switching waveforms for the turn-ON switching transient at $V_i = 2000$ V and $I_D = 50$ A. (a) $L = 0$ nH. (b) $L = 800$ nH.

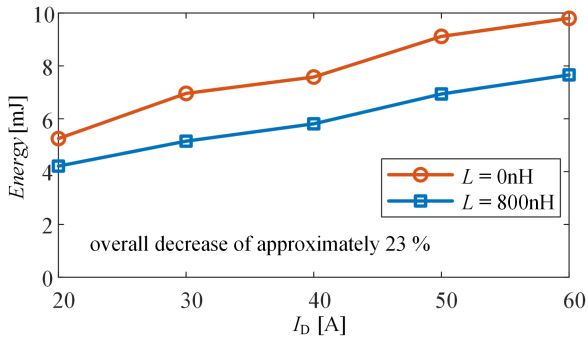

Fig. 14. Turn-ON switching loss at $V_i = 2000$ V and I_D of 20–60 A.

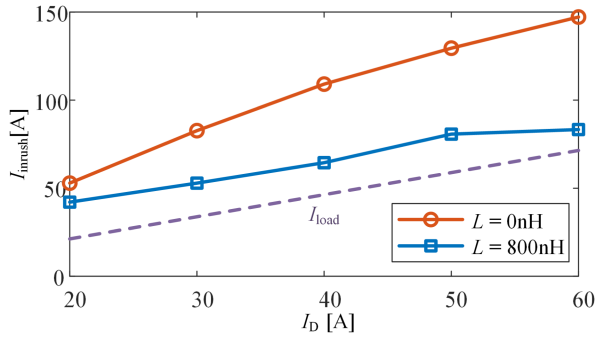

Fig. 15. Inrush current at $V_i = 2000$ V and I_D of 20–60 A.

Figs. 16 and 17 illustrate the operating processes of the hybrid-clamped topology and the improved hybrid-clamped topology, respectively. The waveforms of the dc-link capacitor voltages (V_{C1} and V_{C2}) and the FC voltage (V_{C3}) are presented, along with the current waveform of the snubber inductor L. It can be observed that, by introducing the snubber inductor, the improved hybrid-clamped topology reduces the dc-link voltage difference ($V_{C1} - V_{C2}$) from 66.5 to 18.5 V. Meanwhile, the inrush current of the snubber inductor L decreases from 38.7 to 19.7 A.

In terms of converter-stage efficiency, under the given experimental conditions, the efficiency of the hybrid-clamped topology is 97.55%, with a loss power of 180.88 W. For the improved hybrid-clamped topology, the efficiency increases to 98.05%, with a loss power of 143.59 W. This represents an efficiency improvement of 0.5% and a reduction in loss power of 37.29 W. The reduction in loss mainly results from the decreased turn-ON loss of S_1 after introducing the snubber inductor. Although the overall efficiency improvement is relatively small, it makes a significant contribution to reducing the switching loss of S_1. Since the total loss reduction is concentrated in the mitigation of S_1's turn-ON loss, the inductor effectively alleviates the stress on the most heavily loaded device in the converter.

C. Comparative Study

The study focuses on addressing the issues existing in the hybrid-clamping topology for continuous-conduction nonisolated dc–dc converters and analyzing their underlying causes. Accordingly, a comparative study is conducted between the

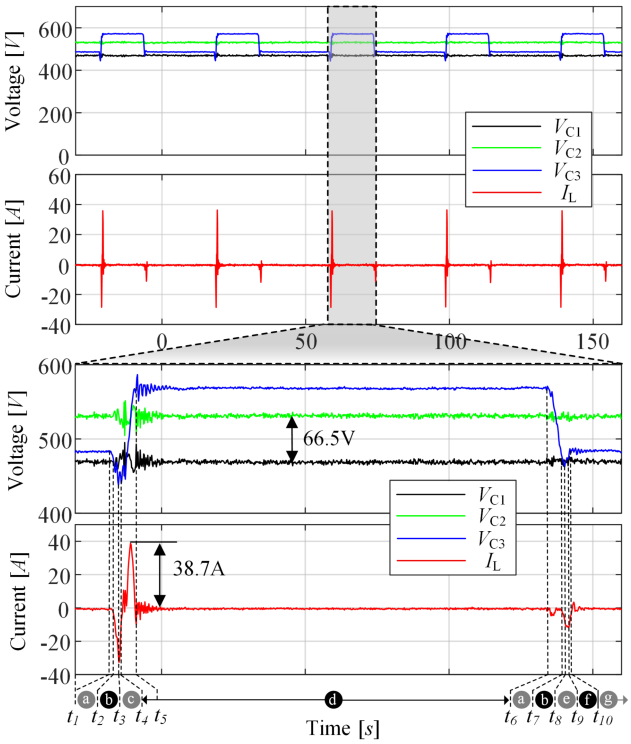

Fig. 16. Experimental topology operation process under V_i = 1000V (Case 1).

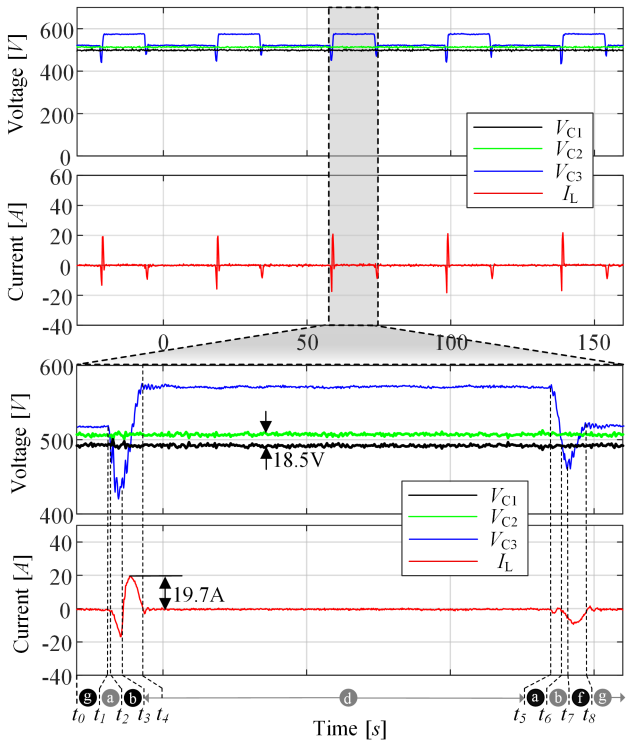

Fig. 17. Experimental topology operation process under V_i = 1000V (Case 2).

TABLE III
PERFORMANCE COMPARISON

Topology	Hybrid-Clamping	Improved Hybrid-Clamping
Clamping circuit	One capacitor, and two diodes.	One capacitor, one inductor, and two diodes.
Switching current stress of S_1	High	Low
Flying capacitor current stress	High	Low
Diode current stress	High	Low
Bus capacitor voltage imbalance	Large	Small
Voltage self-balancing capability	Yes	Yes
Switching loss of S_1	High	Low
Overall efficiency	High	Slightly higher than hybrid-clamping

hybrid-clamping topology and the improved hybrid-clamping topology incorporating a snubber inductor. As shown in Table III, although the improved hybrid-clamping topology introduces an additional snubber inductor compared with the conventional hybrid-clamping topology, it effectively reduces the switching current stress of S_1, the current stress of the FC and diodes, and the voltage imbalance of the dc-link capacitors. Consequently, it exhibits lower switching losses, slightly higher overall efficiency, and better operating performance.

VI. CONCLUSION

Based on the indirect series-connected SiC MOSFETs, this article analyzes the switching behavior of devices in the switched-capacitor loop of the hybrid clamping structure, clarifying the mechanisms behind the inrush current and increased turn-ON loss. Based on this, an improved hybrid clamping method to mitigate the inrush current and additional turn-ON switching loss is proposed in this article. Theoretical analysis further confirms that the added snubber inductor in the improved method preserves the voltage self-balancing capability. In experiments, 2000 V DPTs were conducted to evaluate the inrush current and the turn-ON switching loss of S_1 under I_D of 20–60 A. The results demonstrate effective mitigation of inrush current to a level close to I_D, along with an average 23% reduction in turn-ON switching loss. Subsequently, 1000 V continuous experiment was conducted to analyze topology operation process, verifying the self-balancing of the dc bus capacitor voltage and the FC voltage, thereby ensuring voltage sharing among the devices. Therefore, the improved hybrid clamping method provides enhanced application potential for the indirect series-connected SiC MOSFETs.

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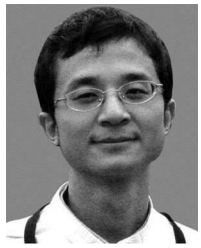

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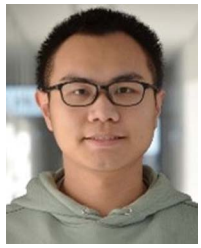

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