An Overview of Current Source Converters: State-of-the-Art and Future Trends

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***Abstract*—The current-source converter (CSC) has gained wide research interest in the last decade because it complements voltage-source converters and enjoys advantages such as direct control of the output current, inherent short-circuit protection, high reliability, voltage boosting as an inverter, voltage bucking as a rectifier, etc. With the anticipated commercialization of CSC, many key technical problems have arisen with respect to industrial applications, which have drawn increasing attention in the existing literature. The purpose of this article is to group and review these latest contributions, underscore the current status, and project possible future research trends. In this overview, the research and applications of CSC across various fields are outlined. Then, various two-level and multilevel CSCs are thoroughly discussed. The concepts of ac-link multilevel and dc-link multilevel are first coined for CSC research domain and some are further generalized through the duality and graph isomorphism. Furthermore, typical modulation and control strategies of CSC are reviewed, elucidating four pivotal issues encountered in practical CSC applications. The latest research and methods to solve or optimize these problems are summarized and discussed. Finally, future trends and challenges within the field of CSC are discussed, aiming to inspire subsequent contributions and novel possibilities.**

***Index Terms*—Control strategy, current-source converter (CSC), modulation strategy, topology.**

I. Introduction

CONTEMPORARY environmental degradation is intensifying alongside economic development. In response to the urgent need for enhancing ecological conditions and air quality, electric energy has garnered significant attention [1]. Fig. 1 offers a brief overview of the intricate dynamics governing electricity generation and consumption systems, highlighting the critical role of power converters in the advancement and utilization of electric energy [2]. Generally, a power converter can be categorized based on whether the dc-side has a relatively stable voltage or current: naming voltage-source converter (VSC) or the current-source converter (CSC).

A. Challenges Faced by VSC

Fig. 2(a) illustrates the conventional circuit topology of a VSC, specifically a three-phase voltage-source rectifier. This configuration is widely researched due to its advantages, such as adjustable input power factor and controllable output voltage, among others [3]. However, it shares some common bottlenecks with other VSC topologies.

1) A sufficiently large capacitor bank is normally needed as the energy storage component on the dc side, where electrolytic capacitors are utilized, potentially threatening the converter service life and increasing the maintenance cost.
2) Deadtime is commonly used as safety insurance since short circuits in bridge arms is normally not allowed given the unique commutation requirement. In practice, the power quality, system resilience, and fault-tolerance could face great challenges.
3) VSC (rectifier) can be considered as a generalization of a dc/dc boost converter. Hence, the output is higher than the input voltage, which normally requires an additional voltage bucking stage when the output dc voltage is lower than the grid voltage.

B. Challenges Faced by CSC

As a complement to VSCs, various CSC topologies have been proposed. Fig. 2(b) illustrates a typical three-phase current-source rectifier (CSR). However, CSCs have several inherent disadvantages compared with VSCs, including the following.

1) *Device requirements:* The commutation requirements of CSC are uniquely defined as compared to VSC counterparts: a reverse voltage blocking capability of its switching devices is normally necessary. This leads designers to either choose to utilize a configuration where IGBTs or MOSFETs are serially connected with diodes, or devices with a four-quadrant operation range, such as monolithic bidirectional switches [4].
2) *Safety requirements:* When a load or arm undergoes an open circuit fault, it results in a significant voltage surge on the dc-side of the CSC. As a preventive measure, CSC typically includes a freewheeling diode in reverse

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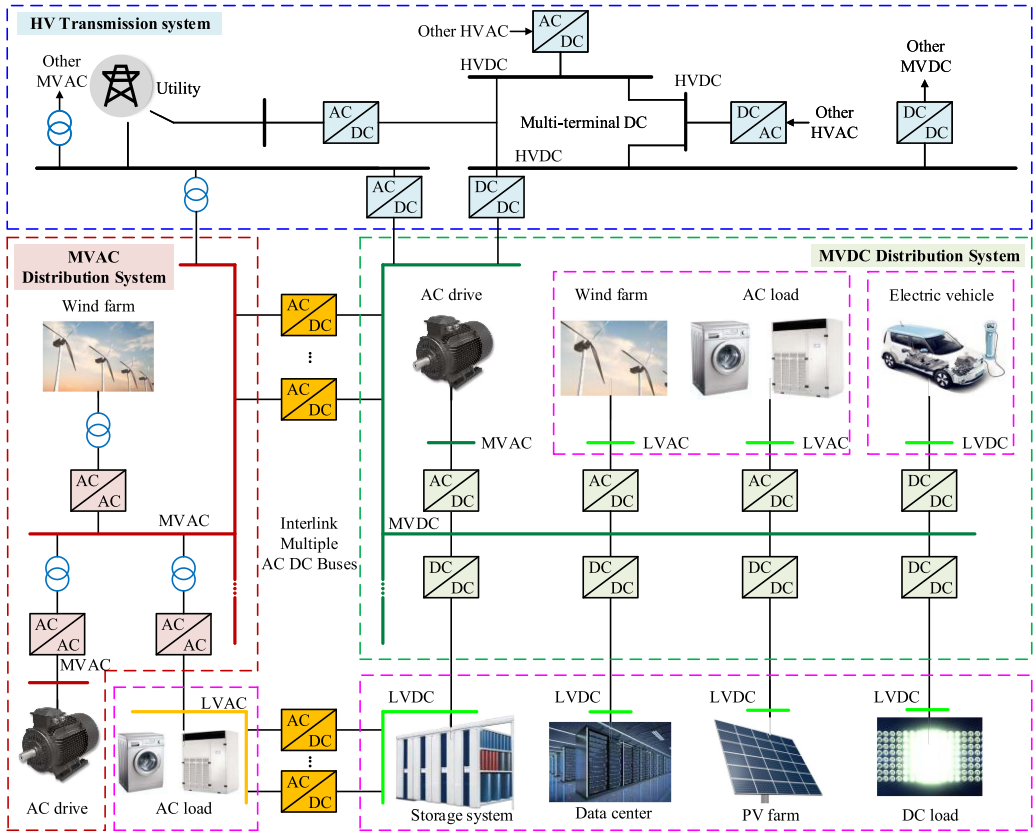

Fig. 1. General overview of electricity generation/consumption system [2].

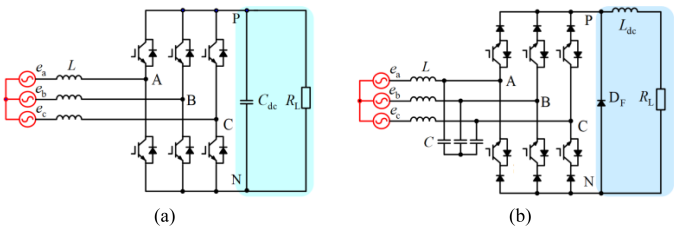

Fig. 2. Typical power converters. (a) Voltage-source rectifier. (b) CSR.

parallel on the dc-side. This arrangement facilitates the formation of a circuit for the inductor current through the freewheeling diode, effectively mitigating overvoltage occurrences.

3) *DC Inductor:* When comparing the VSC and CSC, the need for a large dc inductor in CSC is normally considered to be another unfavored factor [5]. Unlike the ac inductors used as filters in VSCs, the dc inductor in CSCs functions similarly to the capacitor bank in a VSC and must be placed in series with the dc bus, leading to higher cost and conduction losses. However, in scenarios requiring voltage boosting, VSC systems also need a series inductor in the boost dc–dc stage and thus face similar drawbacks.

Despite the above-mentioned aspects, there are more subtle differences in the status of research between VSC and CSC underlining the social and historical interplay. Though the predecessor of CSC, i.e., load-commutated inverter (LCI) or line-commutated converter (LCC) converters has been dominant in the transmission system, however, in terms of research depth, breadth, and practical applications, modern CSC development still lags behind VSC in the field of modern electrical engineering. As compared to VSC, the manufacture, packaging, circuit development, safety, device maturity of CSC have not yet fully addressed. This is partially due to the commercialization of CSC (especially PWM CSC) having been quite limited and gained much less research attention across the history of power electronics. Another reason is that current common power sources, such as grid voltages and batteries, are inherently voltage sources. Introducing a CSC-based system into such an electrical grid may require extra efforts and infrastructure cost.

C. Unique Advantages of CSC

However, as shown in Fig. 2(b), CSC possesses some unique advantages, which are summarized as follows.

1) The inductor is used as the energy storage component on the dc-side. Therefore, electrolytic capacitor is not needed, which means a longer service life than VSC.
2) Short circuit of the bridge arm is an ordinary operation mode in a conventional CSC as it provides zero current level in PWM waveform. From a circuit theory point of view, the short circuit is allowed as the rate of current change is limited due to the existence of dc-link inductor.
3) CSC (rectifier) can be considered as a generalization of dc/dc buck converter. The output voltage is lower than input voltage, which can be regulated from zero. Therefore,

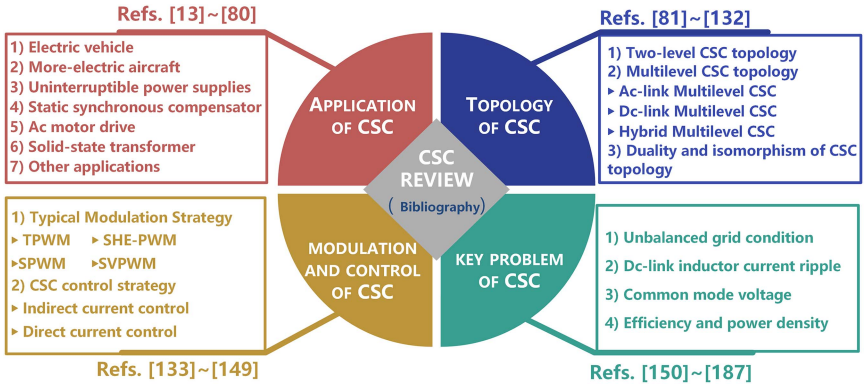

Fig. 3. Proposed approach and bibliography of the CSC.

flexible voltage regulation of CSC can be achieved without extra dc/dc stage, which can reduce the cost and volume of system.

Owing to the features outlined above, CSCs have undergone extensive research, demonstrating substantial potential across a wide span of applications. This engagement underscores its established industrial relevance and a notable level of technological maturity. However, with the anticipated commercialization of CSC, many key technical problems arise in some industrial applications. For these key problems, great research efforts have been dedicated and many papers have been published, while a systematic research especially covering recent progress is still absent. Therefore, this paper presents a technology review to fill this gap. Compared to existing recent overview papers on CSC (e.g., modulation for CSC-based drives [6], CSC topology derivations [7], operation of CSC in high power electric machine systems [8], current-fed multilevel converters [9], current-fed-isolated-bidirectional converter [10], etc.), the holistic research progress of CSC, especially in the current decade, covering applications, conventional and new promising topologies, modulations, controls, and operational issues, was the focus of our work. In addition, this article outlines developing applications, difficulties, approaches, and possible future directions in CSC development, aiming at stimulating more research efforts in this area. In particular, four key issues are highlighted with detailed discussions.

1) Unbalanced grid voltage condition.
2) DC-link inductor current ripple suppression.
3) Common-mode voltage (CMV) suppression.
4) Efficiency and power density improvement.

Fig. 3 shows a summarizing diagram of the comprehensive review of CSC.

The rest of this article is organized as follows. Section II presents the main applications of the CSC and commercial products. In Section III, a comprehensive review of the topologies currently existing in CSC is given. In Section IV, the current modulation and control schemes of CSC are summarized. In Section V, some key technical problems in practical application of CSC are revealed, and their recent advances are discussed. Section VI concludes with the challenges and trends of CSC in the future. Finally, Section VII concludes this article.

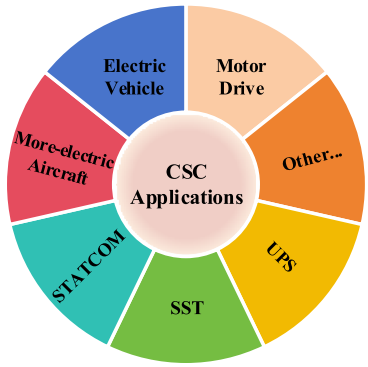

Fig. 4. Some typical applications under the influence of CSC techniques.

II. Overview of CSC Applications

The early adoption of current-source (CS)-based static power conversion can be traced back to 1939, when L.W. Parker obtained one of the first patents related to current-source inverter (CSI) systems [11]. Entering the semiconductor era, one of the classical CS-based topologies, thyristor-based LCC has been employed since the 1960s for enabling the high-voltage direct current (HVdc) transmission [12]. At present, numerous LCC-based HVdc lines are still in operation, and the approach remains a viable and competitive choice.

With advances in semiconductor devices and converter design, CSC losses have been further reduced, facilitating their wider industrial adoption. This section summarizes and analyzes the main potentials and industrial applications of CSCs. Fig. 4 illustrates representative applications that have been implemented or hold significant potential for benefiting from CSC technology, with detailed analyses provided below.

A. Electric Vehicle

With the growing trend of adopting electric vehicles (EVs) into transportation systems, considerable research has delved into the application of CSC as their core power conversion equipment. In [13], CSC- and VSC-based EV chargers were modeled in PSIM using Nissan LEAF battery parameters. Results show that, in the 15–50 kW power range, CSCs can achieve higher efficiency because VSCs require an additional

dc/dc stage to match the battery charging voltage. However, as power increases, output losses rise in both CSC and VSC systems. Typically, inductor losses account for 2%–4% of output power, while capacitor losses in VSC are approximately 0.5% [5]. A bidirectional vehicle charging system based on soft-switching CSR is proposed in [14]. The system leverages the advantages of the CSR, including a high-quality input voltage waveform, improved short-circuit current tolerance, and extended dc-choke lifetime. Experimental results confirm that the system achieves high efficiency and stable operation, making it suitable for charging EVs with multiple battery packs. On the other hand, in the EV drive system, three configuration schemes for heavy-duty EV powertrain based on CSI and asymmetric six-phase motor were proposed in [15]. In [16], a charging–driving integrated topology based on a CSC is proposed, where the motor windings are utilized as the dc inductor, thereby eliminating the need for a bulky external inductor.

Therefore, the structural simplification and inherent short-circuit tolerance provided by the CSC topology enable it to show promising application potential in EV applications.

B. More-Electric Aircraft

In the aviation field, more-electric aircraft represent an intermediate stage in the transition from conventional aircraft to all-electric aircraft [17] offering advantages such as an optimized overall structure, simplified power systems, and improved performance and efficiency [18], [19].

Reflecting on these advancements, there has been a noticeable increase in the adoption of more-electric aircraft in recent years. The typical representatives are Boeing 787 and Airbus A380 [20]. In [11], the application prospects of voltage-source inverter (VSI) and CSI in the aerospace field are discussed. Although VSI has been widely used in the field of electric drive, with the development of semiconductor technology, CSI has gradually been rerecognized and has potential application value. In [21], an energy control strategy based on CSC is proposed, which uses the double closed-loop structure of the outer power loop and the inner dc current loop. When the load fluctuates greatly, the output voltage and current of the converter still remain constant, extending the service life of the generator in the aircraft. In [22], a comparison is made between medium-voltage CSC and VSC in electric aircraft propulsion systems. It shows that CSC provides higher quality output current with very low total harmonic distortion (0.88%), but at the expense of lower efficiency. However, in low-temperature environments, the CSI is considered more suitable for fully electric aircraft. The application of superconducting coils in [23] changed the volume characteristics of CSC, and the total volume of its passive components was reduced by 32% compared with VSC. When designing and building power converters for aircraft applications, the two primary performance goals are high reliability and weight reduction. The advantages of using 1.2-kV Silicon Carbide (SiC) MOSFETs compared with IGBTs in CSC for practical applications in aircraft power systems were investigated in [24]. Furthermore, a hybrid predictive control method for CSC in aircraft dc microgrid is proposed in [25]. In addition, many of ECU's products use CSC combined with boost topology [26]. These products are used in the aviation industry and can achieve 85–140Vac input and 270Vdc output, as shown in Table I.

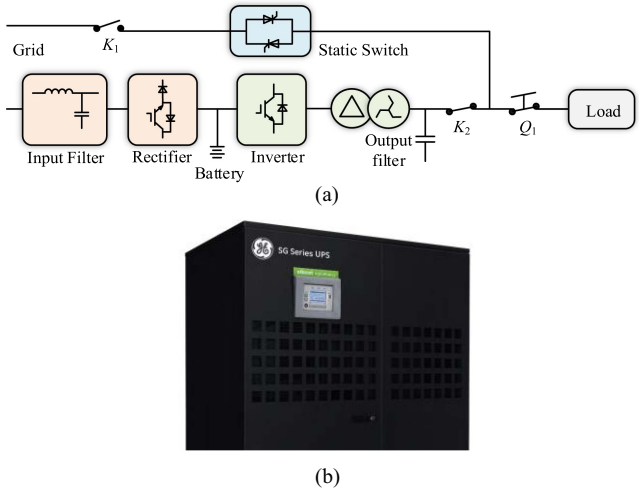

Fig. 5. UPS with CSC. (a) UPS system. (b) SG series UPS [27].

These developments signify a growing recognition of the potential benefits associated with the integration of electric systems (especially CSC-based solutions) in aircraft design and operation. However, it is imperative to approach these benefits with a balanced perspective, recognizing the complexity of aviation systems and the myriad factors that influence the design, performance, and efficiency of aircraft. Future research and empirical studies will continue to elucidate the full scope of advantages, limitations, and practical implications of transitioning to more-electric aircraft systems.

C. Uninterruptible Power Supplies

The expansion of power grids and the growth of nonlinear loads have worsened power quality, posing challenges to sectors with high reliability demands such as healthcare, banking, telecommunications, and semiconductor manufacturing. Uninterruptible power supply (UPS) systems have thus become essential for providing uninterrupted power during grid disturbances.

A typical UPS structure comprises a rectifier, a storage battery, and an inverter, as shown in Fig. 5(a). Currently, VSCs are widely used in many UPS systems. However, when the grid voltage is 220 V, the boost characteristic of VSCs results in a minimum dc bus voltage of 540 V, which is higher than the traditional battery charging voltage of 400 V. Thus, a dc/dc converter is required to reduce the voltage for battery charging. In contrast, CSCs enable flexible adjustment of the output voltage, ranging from 0 to 466 V. Therefore, the application of CSCs in UPS systems can simplify the structure and reduce system complexity.

UPS products employing CSCs are listed in Table I, including GE's SG series [27] and SG-CE series UPS [28]. As shown in Fig. 5(b), GE's UPS adopts a CSC as the rectifier. Owing to the characteristics of the CSC topology, the input current total harmonic distortion (THD) of the UPS is less than 2%

TABLE I
SELECTED COMMERCIALIZED APPLICATIONS BASED ON CSC

Product model	Country	Company	Converter type	Power range	Output voltage	Application areas
SG Series UPS [27]	America	GE	PWM-CSR	0.01–0.6 MVA	0.38–0.415 kV	Uninterruptible Power Supplies
SG-CE Series UPS [28]	America	GE	PWM-CSR	0.06–0.5 MVA	0.38–0.415 kV	Uninterruptible Power Supplies
MPFC-115-3PH-270P-FP [57]	America	SynQor	PWM-CSR	1.5 kW	270 Vdc	Aerospace
EPFC-3PAW-1k5-270-F-V1 [26]	China	ECU	PWM-CSR	1.5 kW	270 Vdc	Aerospace
MEGADRIVE-LCI [58]	Switzerland	ABB	LCI	2–150 MW	2–20 kV	Medium voltage drive
Bulletin 1557 [59]	America	Rockwell	PWM-CSI	0–10 MW	2.3–6.9 kV	Medium voltage drive
PowerFlex 7000 [60]	America	Rockwell	PWM-CSI	0.15–6 MW	2.4–6.6 kV	Medium voltage drive
2000/4000 Series [61]	Japan	TEMIC	LCI	0–13 MW	2.3–4.16 kV	Medium voltage drive
Silcovert S-LCI [62]	Japan	Nidec	LCI	0–65 MW	4.5–10 kV	Medium voltage drive
SINAMICS GL150 [63]	Germany	SIEMENS	LCI	1.4–85 MVA	3–12 kV	Medium voltage drive

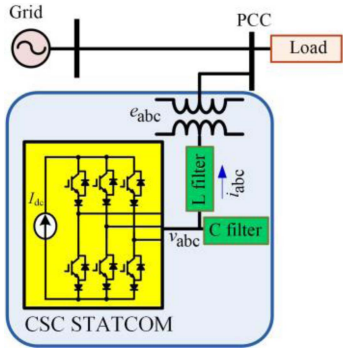

Fig. 6. STATCOM with CSC.

without requiring additional harmonic filters. The UPS input power factor can reach 0.99, and maintaining constant behavior at all loads. Meanwhile, this UPS series exhibits good current-sharing capability, and CSCs are easier to parallel compared with VSCs. Therefore, in high-power applications, up to six UPS modules can be paralleled. In addition, relevant research was conducted on utilizing CSC in UPS systems, as detailed in [29], aimed at improving reliability.

D. Static Synchronous Compensator

Static synchronous compensator (STATCOM) is an ac transmission device based on power electronic converters that achieves rapid reactive power compensation by adjusting the output voltage/current amplitude and phase, thereby improving the power factor of the power grid and suppressing flicker and harmonics.

Although VSCs are currently predominant in STATCOM applications [30], the use of CSCs in STATCOMs still offers several unique advantages. As illustrated in Fig. 6, a CSC-STATCOM demonstrates lower reactive current distortion and possesses inherent short-circuit protection capability [31]. In detail, the advantages of the CSC-STATCOM are as follows.

1) *Controlled AC Current Output*: CSC-STATCOM can directly produce controllable ac current, whereas VSC-STATCOM generates controllable ac voltage.
2) *Low Current Harmonics*: Under normal operation, the current injected by STATCOM via CSC constitutes only a small fraction of the line current, resulting in minimal current harmonics. In contrast, VSC, despite injecting a small current, produces larger output voltage close to the system voltage, leading to larger current harmonics and higher filtering costs [32].
3) *Lower DC-Side Energy Storage Requirements*: For CSC-STATCOM, the dc-side current only needs to marginally exceed the peak of the injected current, representing just a small portion of the line current. In contrast, VSC-STATCOM demands a dc voltage above the peak line-to-line voltage to transfer reactive power. This means that the dc energy storage requirement of CSC is lower than that of VSC when used to realize a STATCOM [32].

The design method of CSC-STATCOM is given in [33], and the impact of dc-side inductor on system loss and waveform quality is pointed out. The research results show that integrated gate-commutated thyristor (IGCT)-based CSC can be applied to STATCOM industrial systems. In addition, the feasibility of multilevel current-source converters (MCSC) as STATCOM applications was discussed in [34], pointing out that MCSC can be considered as a potential candidate for flexible ac transmission system applications. In response to the current imbalance problem caused by MCSC applied to STATCOM, a current balancing algorithm was proposed in [35] to ensure that the inductor current remains balanced and promotes the application of CSC in STATCOM.

It can be seen that the application of CSC in STATCOM has been deeply studied. When the control objective of the system shifts from regulating reactive power to real-time tracking and cancellation of harmonic currents, its name changes from STATCOM to active power filter, which is divided into voltage-source active filter (VSAF) and current-source active filter (CSAF). Under the same operating conditions, the THD improvement achieved by the CSAF is approximately 4.6 percentage points higher than that of the VSAF [36]. However, a key challenge facing the application of CSC-STATCOM technology is the loss associated with the dc-side inductor. The use of superconducting materials is a promising solution to reduce these losses and improve efficiency [37]. However, challenges such as high operational and maintenance costs, complex cryogenic cooling requirements, and the brittleness of superconductors cannot be overlooked. Even so, the potential gains in efficiency and performance continue to drive sustained research and development efforts in this area.

E. AC Motor Drive

AC motor drive systems are one of the primary application areas of CSCs, and they have been intensively studied in recent

years [38]. Examples include permanent-magnet synchronous motor [39], [40], doubly-fed induction generator [41], [42], [43], and multiphase motor drives [44], [45], [46]. The main advantages of using a CSC-based motor drive are that the fundamental harmonics of the stator current and voltage are nearly sinusoidal, the stator voltage dv/dt imposes no stress, and long cables can be connected to the motor without causing stator overvoltage [47].

When a CSI is used to drive low-power induction motors, the distortion of motor voltage and current waveforms is small, and the motor itself operates with high efficiency. However, due to the inclusion of dc-link inductors in the CSI configuration, the losses in the dc-link are greater than those in VSI. Although, under such conditions, the insulation stress on the induction motor remains relatively low [48].

In addition, CSC is suitable for industrial medium-voltage (MV) high-power drives [6], [49], [50], [51], [52], [53], [54]. Among them, the CSI can generally be divided into pulsewidth modulation (PWM) CSI and LCI. PWM-CSI usually uses symmetrical gate turn-off (GTO) or IGCT as switching devices. LCI usually uses silicon controlled rectifier devices [49]. Currently, MV drives based on CSC have been applied to products by many companies, as shown in Table I. It is noteworthy that, in MV drive systems, the CSC drive system using an 18-pulse thyristor rectifier exhibits higher dc-link losses (0.27%) compared with the three-level VSC drive system employing a 12-pulse diode rectifier, whose losses are only 0.04%. However, the VSC incurs 0.41% sinusoidal-filter losses on the inverter side, making the overall efficiency of the CSC comparable to that of the VSC [55].

F. Solid-State Transformer

Solid-state transformers (SSTs), also known as power electronic transformers (PETs), are a type of MV isolated power converter. As an emerging area, SSTs or PETs can achieve high efficiency, lightweight construction, and superior controllability compared to traditional line-frequency transformers [56]. The voltage-source SST topology typically includes three-stage power conversion: hard-switching inverter, isolated bidirectional dc/dc converter (such as dual-active bridge converter), and hard-switching cascaded multilevel converter. This approach has been widely researched and adopted.

In addition, current-fed power electronic converters are boost-type topology structures suitable for low-voltage high-current SST applications. Based on this, a bidirectional current shaping modular multilevel converter (MMC) topology with zero-current switching (ZCS) is proposed in [64], suitable for connecting MVdc and low-voltage dc (LVdc) distribution networks. In [65], a novel current-fed series resonant converter is introduced to address the challenges of achieving zero-voltage switching (ZVS) for MV MOSFETs and minimizing system capacitance over a wide voltage and load range. Compared to traditional three-level voltage-source SSTs, single-stage CS SSTs offer potential advantages of higher efficiency, higher density, and fewer components. In recent years, several CS-SST topology structures have been proposed [66], [67], [68], [69]. In addition, CS-SSTs have advantages of no electrolytic capacitors, high reliability, and high-temperature operation [70]. Therefore, the application of CSCs in SSTs has great potential.

G. Other Applications

With the continued advancement of power electronics technology, the application of CSCs is expected to expand into a wider range of fields. Examples include superconducting magnetic energy storage systems [71], [72], renewable energy generation systems [73], [74], HVdc transmission systems [75], [76], fuel cell power systems [77], [78], power spring systems [79], and variable-speed drive systems for subsea applications [80], among others.

In summary, the current application scope of CSCs remains confined to specific fields such as uninterruptible power supplies, aerospace, and MV drives, primarily due to the dual constraints imposed by power devices and the large dc-side inductor. On the one hand, the semiconductor industry has long focused on devices designed for VSC applications, leaving CSCs with limited mature power device options (e.g., devices with reverse-blocking capability), thereby requiring additional components and increasing system cost and complexity. Moreover, in applications that demand bidirectional energy flow, such as EV charging, CSC topologies must incorporate additional devices to achieve this functionality, further exacerbating their cost disadvantage. On the other hand, the large dc-side inductor not only restricts CSC efficiency but also limits the response speed of the dc current.

Nevertheless, these application-level challenges do not overshadow the inherent technical merits of CSCs. Their high-quality output voltage waveforms (with low harmonic distortion) and excellent dv/dt performance still provide value in specific scenarios. With advancements in semiconductor devices, such as the commercialization of monolithic bidirectional switches, the fundamental strengths of CSCs are receiving renewed attention, and CSCs are expected to overcome existing industrial bottlenecks and achieve broader application in the future.

III. Overview of CSC Topologies

In this section, typical and promising topologies are grouped and reviewed. In recent years, many CSC topologies have been designed for different applications. These power converters can be classified in many ways, such as by output level or the number of bridge arms. In this section, they are classified according to output levels, which are divided into two-level topologies and multilevel topologies (including three-level topologies), as shown in Fig. 7.

The output level of a CSC is determined by how large the phase current is and its magnitude with respect to the dc source. The most common CSC, as shown in Fig. 2(b), can produce three different levels in phase current, i.e., $+I_{\mathrm{dc}}$, 0, $-I_{\mathrm{dc}}$. Therefore, in contrast to the conventional VSC, which is classified as a two-level topology, the conventional CSC is actually classified as a three-level topology.

The two-level topology can be formed by a boost dc–ac inverter or a half-bridge-based CSC. In general, the multilevel

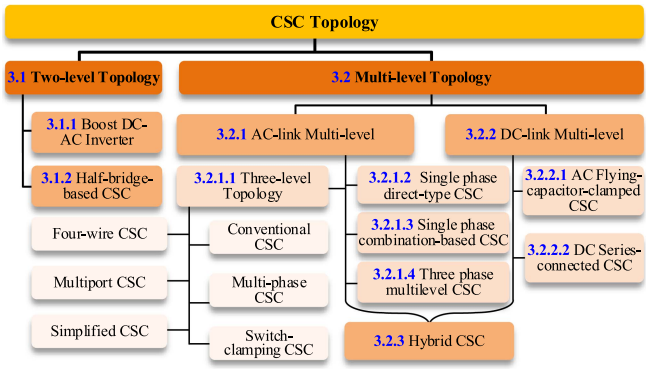

Fig. 7. Classification of CSC topology.

topology is divided into two categories: one is the ac-link multilevel type, covering combination mode multilevel CSC, direct-type multilevel CSC, and the more common three-level CSC. Among them, the three-level CSC topology mainly includes the traditional full-bridge CSC, multiple-phase CSC, switch-clamping CSC, four-wire CSC, multiport CSC, and simplified CSC. The other category is the dc-link multilevel CSC, which includes the recently emerged ac flying capacitor-clamped CSC and series-connected CSC. Hybrid multilevel CSC can also be found by combining ac-link and dc-link multilevel techniques.

A. Two-Level CSC Topology

Fundamentally speaking, a typical CSC (VSC) refers to a dc–ac converter that utilizes a constant dc current source (voltage source) or a large enough inductor (capacitor) on its dc-link, which can sustain a stable current (voltage). For a CSR (inverter), this means that power needs to be processed from ac (dc) to dc (ac), and its dc-link is (actively) maintained at a relatively constant value so that the rectifier (inverter) can modulate dc currents into PWM waveforms.

Fig. 8(a) illustrates the general structure of the power converter cell (per phase leg configuration), consisting of an input port, switching network, and output port. For dc–ac converters, the input port can be defined as voltage type (or current type) as shown in Fig. 8(b), and can be represented by various forms, including ideal voltage source (or ideal current source), voltage source in parallel with capacitor (or current source in series with inductor), and current source in parallel with capacitor (or voltage source in series with inductor). To provide the PWM waveform, a typical switching network features two switches as shown in the theoretical bridge cells of Fig. 8(c). To provide concrete examples, Fig. 8(d) and (e) also demonstrates the half-bridge-based converter cell. Notably, voltage-source buck-type converter cell is commonly implemented in conventional VSCs as well as some multilevel VSCs, e.g., active neutral-point-clamped (ANPC) converters, while CS boost-type converter cell can be found as a unique submodule in CSC-based MMC topology [34].

More broadly speaking, according to Fig. 8(b), a current-fed converter can also be considered current source-based since the input port is current-type, but normally considered to be

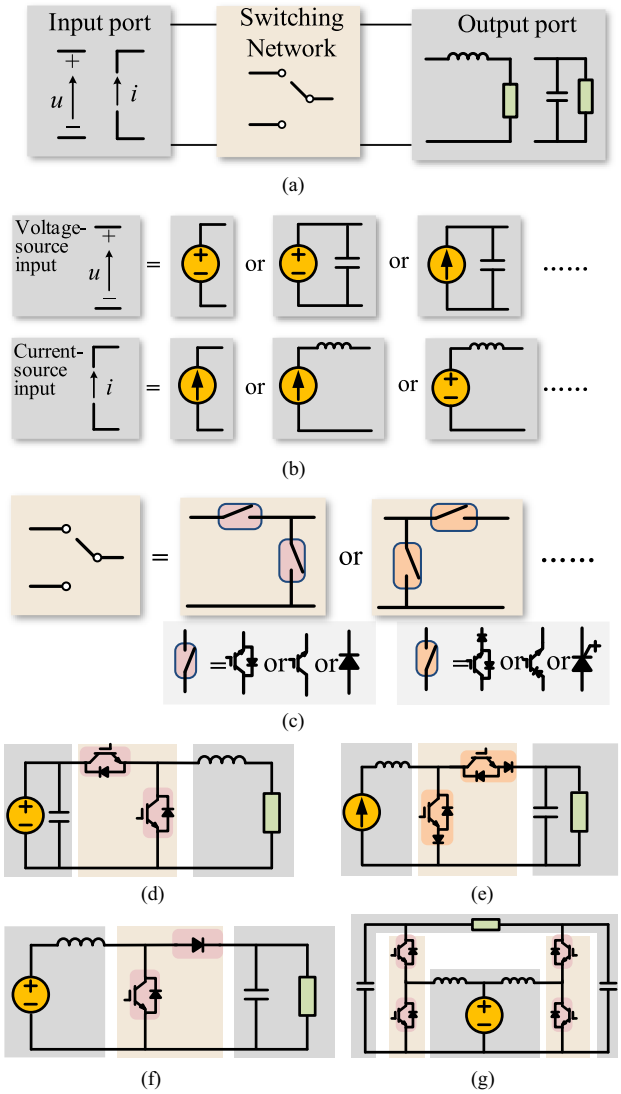

Fig. 8. Fundamental bridge cells of power converter. (a) General structure of the power converter cell (per phase leg configuration). (b) Different realizations of CS input and voltage-source input. (c) Different basic switching network configurations and suitable switches. (d) Half-bridge-based voltage-source buck-type converter cell. (e) Half-bridge-based CS boost-type converter cell. (f) Typical boost converter. (g) Boost DC–AC inverter [81].

classified into boost-type dc/dc converters as shown in Fig. 8(f). Integrating two boost converters can form into a unique type of boost dc–ac converter as shown in Fig. 8(g) [81]. Its current-fed nature enables the boost of output voltage per phase, which demonstrates a similar boosting capability as conventional CSC but only produces two-level current per phase. Another example can be found in [82], which presented a different half-bridge based CSC as shown in Fig. 9. The PWM waveform consists of positive and negative dc current, and thus, this topology is classified into two-level CSC.

B. Multilevel CSC Topology

The multilevel concept can be traced back to the early days of power electronics, when the first thyristor was far from being invented [83]. The motivations, however, have not changed

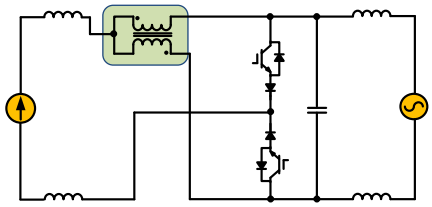

Fig. 9. Half-bridge CSC [82].

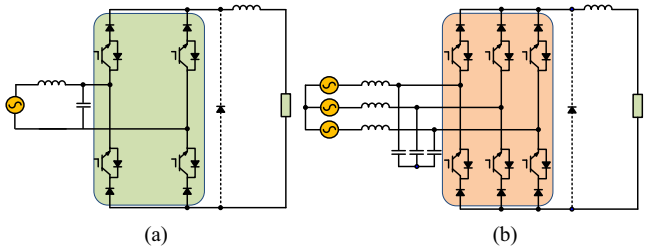

Fig. 10. Conventional CSCs: (a) single-phase CSC and (b) three-phase CSC.

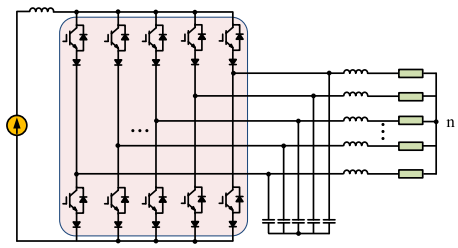

Fig. 11. Multiphase CSC.

much: to improve the output waveform quality, to enable higher voltage/power handling capability, to improve efficiency, etc.

As for CSC topologies, due to the limitations of power electronic devices, in some high-voltage and high-power applications, multilevel topologies or multiple module systems combined in a series-parallel configuration are needed to achieve high power output. When the voltage stress and switching frequency of the switch are determined, as the number of levels increases, the capacity of the CSC increases. Meanwhile, the current waveform becomes more sinusoidal due to the higher equivalent switching frequency, and the harmonic content is also reduced. In addition, multilevel converters have the advantages of large power capacity, fast dynamic response, low output harmonics, and good electromagnetic compatibility [84]. Therefore, they are widely researched [85], [86].

In detail, two different techniques can be found in multilevel CSC research: 1) ac-link multilevel CSC is featured by ac-side multilevel current generation, which has been extensively studied in the recent literature and 2) dc-link multilevel CSC is emerging and focuses more on dc-side challenges (e.g., dc ripples) and seeks solutions through dc-link multilevel generation.

1) AC-Link Multilevel CSC: The existing construction methods for ac-link multilevel CS topologies mainly include the multiple-module combination method and the direct method. Such classification is mainly based on how the converter is constructed to form multilevel current outputs. To further classify them, we categorize the ac-link multilevel CSCs as follows: single-phase direct multilevel CSC, single-phase combination multilevel CSC, and three-phase multilevel CSC. In addition, as mentioned before, conventional CSCs actually produce three different levels of current in their phase-current PWM waveforms. Following the same methodology from the VSC domain, we therefore consider the conventional CSC a three-level topology instead of a two-level one. Similarly, various other CSCs can also be classified as three-level. Therefore, we classify the three-level CSC as an ac-link multilevel CSC within the multilevel CSC category, which will also be covered in the following section.

a) Three-level CSC topology: i) Conventional CSC: An H-bridge single-phase CSC is considered as the typical example of conventional CSC [87], as shown in Fig. 10(a). The three-phase version [see Fig. 10(b)] is more commonly seen in the literature as the counterpart of a three-phase two-level VSC [88]. Adding a freewheeling diode is often recommended in practice as well.

ii) Multiphase CSC: By further increasing the number of phase arms, the CSC can be generalized into a multiphase topology, as shown in Fig. 11. Usually, the greater the number of bridge arms, the stronger the fault tolerance. For example, the multiphase CSC is usually used to drive multiphase motors in applications including ship propulsion systems, rail transit, and more-electric aircraft. The main advantages are summarized as follows [89], [90].

1) Fault tolerance is strong. In a multiphase CSC motor control system, even if one bridge arm fails, the remaining arms can continue to supply power to the motor, thereby improving system reliability.
2) The performance of driveline is improved. Compared with a single-phase system, the multiphase configuration reduces torque ripple, enhances dynamic response, and increases both power density and efficiency.
3) The reliability of the system is increased. Distributing the load across multiple bridge arms reduces the current and power stress per phase. As a result, device lifetime is extended and overall system cost is lowered.

iii) Switch-Clamping CSC: Beyond conventional topologies, specialized CSC configurations have been proposed to meet application-specific requirements. Nonisolated CSCs are widely used in motor drives for their compact size, higher efficiency, and lower cost compared with isolated CSCs. However, the absence of a transformer introduces CMV, leading to leakage currents that can damage motors and compromise safety. To overcome this, improved CSC designs have been developed to suppress CMV and reduce leakage currents.

Fig. 12 shows an improved single-phase CSC designed to solve the problems of CMV and leakage current. An additional auxiliary circuit is added to the dc side, as shown in Fig. 12(a), which was proposed in [91].

Similarly, another way to improve the single-phase CSC is by adding an additional auxiliary circuit on the ac side, as shown in Fig. 12(b) and (c) [92], [93]. Similar to the single-phase topology shown in [91], a nonisolated three-phase seven switch CSC is

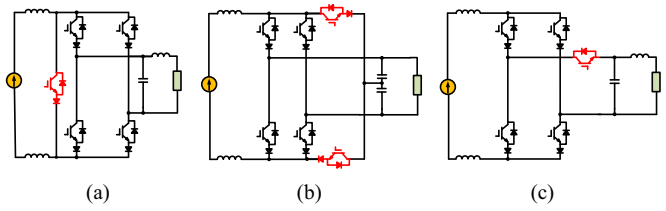

Fig. 12. Special functions single-phase CSC topology. (a) CSC with DC-side clamping [91]. (b) CSC with AC-side clamping I [92]. (c) CSC with AC-side clamping II [93].

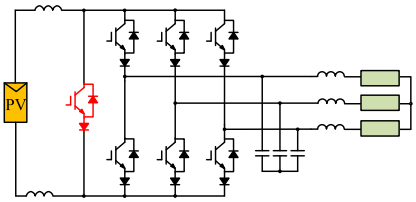

Fig. 13 Three-phase H7 CSC [94].

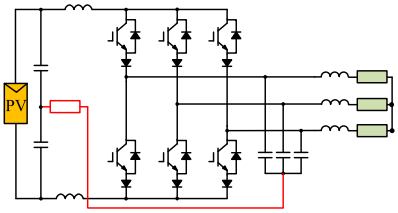

Fig. 14. Four-wire CSC [95].

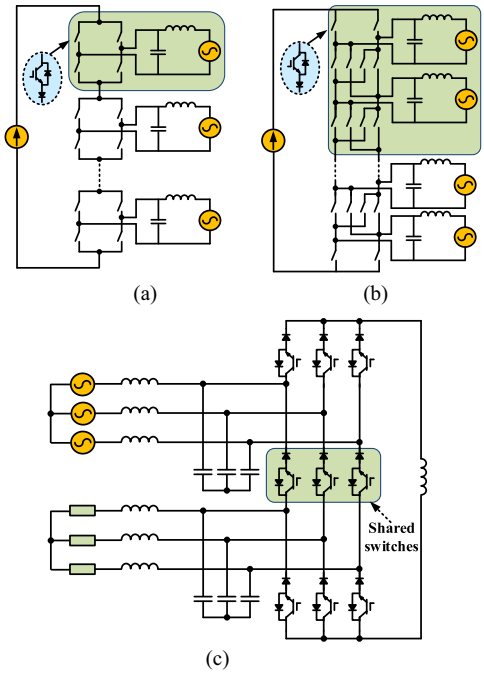

Fig. 15. Multiport converter. (a) Generalized of *n*-port single-phase CSC [97]. (b) Generalized X-type single-phase CSC [98]. (c) Three-phase nine-switch CSC [99].

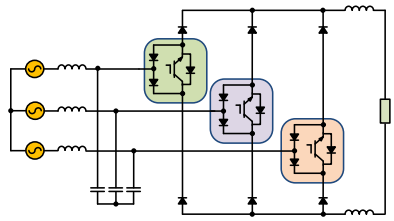

Fig. 16. Three-switch CSC [100].

proposed in [94], as shown in Fig. 13. Only one power device is added to the traditional three-phase CSC, so the cost and losses are low. Besides, the differential-mode characteristics are improved, which can suppress leakage current and CMV. By adding an auxiliary circuit to improve the circuit structure, the CMV and leakage current can be effectively suppressed.

iv) Four-Wire CSC: In [95], a four-wire split-capacitor-based CSC, shown in Fig. 14, is presented. In this topology, the leakage current and CMV can be suppressed by connecting the neutral point of the three-phase load to the midpoint of the dc side, which is an interesting approach. In fact, similar techniques can be found in VSC-based solutions, and this work can be considered the duality of the work presented in [96] (the main circuit as CSC versus VSC). In the following Section III-C, more details on the duality between CSCs and VSCs will be introduced.

v) Multiport CSC: Multiport CSCs are considered those with multiple power ports (ac-type or dc-type). The single-phase multiport CSC can be found in [97], and its topology is Fig. 15(a). A derivation can be found in [98] as shown in Fig. 15(b), which optimizes dc utilization, has fewer conduction losses compared with a conventional one, and more importantly, independent control of multiple ports. A further extension of Fig. 15(a) into a three-phase version can be found in [99]. Just like its counterpart of nine-switch VSC, this topology can provide dual three-phase ac ports. This enables applications like two motors, which require two ac power handling ports or a direct ac–ac conversion.

vi) Simplified CSC: Fig. 16 shows an interesting three-phase three switch CSC, which is analyzed in [100]. Compared with the traditional three-phase three-level CSC, the number of switches in this topology is reduced and the control is relatively simple. The modulation and control methods for this topology are studied in [101] and [102]. Furthermore, in [103], the hardware for this topology is designed, with the rated output power and output voltage set to 5 kW and 400 V, respectively. In addition, this topology can achieve sinusoidal grid current and unity power factor operation. At present, it can be applied to more-electric aircraft [24] and active power filters [104] due to the above-mentioned advantages.

b) Single-phase direct multilevel CSC: The characteristic of direct type multiple level CSC is that the multilevel structure is directly constructed by some power switches and inductors (or current sources), and there is no parallel connection of multiple modules on ac or dc-side.

In Fig. 17(a) [105], only one inductor and two switching devices are added for each additional level. With an increase

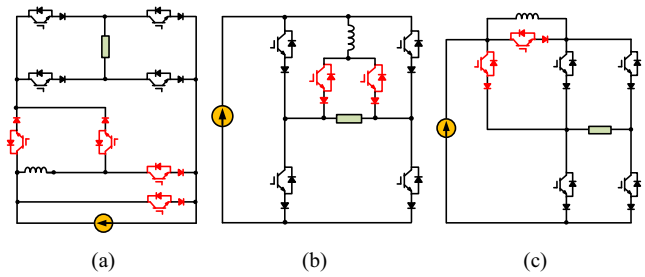

Fig. 17. Direct single-phase multilevel CSC topology I. (a) Topology 2 (5 level) [105]. (b) Topology 3 (5 level) [106]. (c) Topology 4 (5 level) [107].

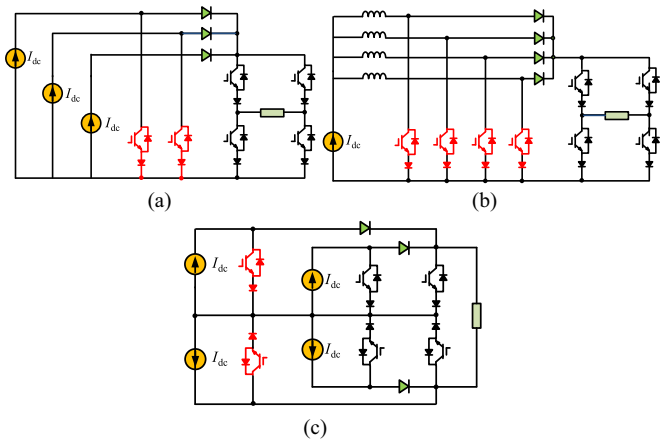

Fig. 18. Direct type single-phase multilevel CSC topology II. (a) Topology 1 [108]. (b) Topology 2 [109]. (c) Topology 3 [110].

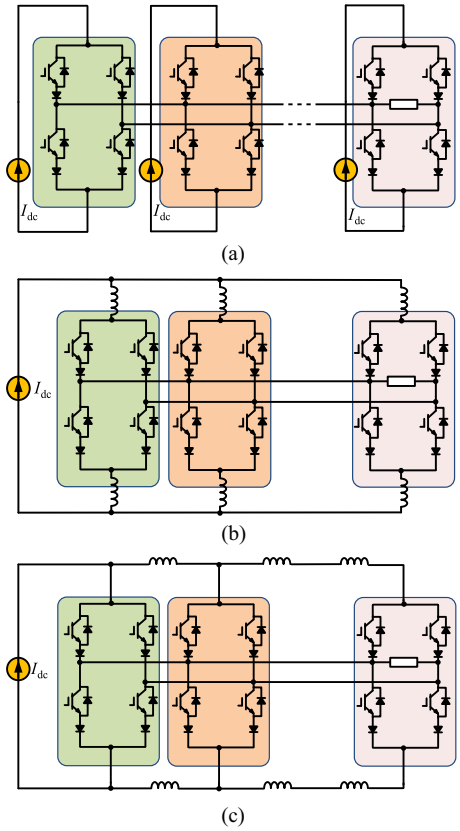

Fig. 19 Combination type single-phase multilevel CSC topology [114]. (a) General configuration of topology 1. (b) General configuration of topology 2. (c) General configuration of topology 3.

in the output level, more inductors are saved compared with other topologies, as shown in Fig. 17(a). Besides, Fig. 17(a) is a two-stage topology. The first stage uses inductors and switches to realize multilevel output, while the second stage uses an H-bridge structure to realize current commutation and pulsewidth control. As shown in Fig. 17(b) [106] and (c) [107], the number of devices is further reduced. For output levels higher than five, only one inductor and two switching devices are required for each additional level.

To further reduce the number of switching devices, a single-phase multilevel CSC topology composed of several independent current sources and switches is proposed in [108] and [111], as shown in Fig. 18(a). In this topology, only one current source and one switch are needed for each additional level. Therefore, the number of switching devices is reduced. Its disadvantage is that multiple dc current sources with the same characteristics are required. To avoid the use of multiple dc current sources, a topology similar to that shown in Fig. 18(a) is proposed in [109] and [112], as shown in Fig. 18(b), which is called a boost multilevel current-source converter (BMCSC). In Fig. 18(b), multiple inductors are used instead of dc sources. Then, the current in each inductor is I_{dc}/n to achieve multilevel output. This topology is also a two-stage topology: the first stage is a boost circuit, and the second stage is an H-bridge circuit to perform current commutation. The advantage of the BMCSC is that it requires only one dc source, which has attracted wide attention from many scholars [109], [112], [113].

When the switches are not connected in a common-emitter configuration, independent driving power supplies are needed due to inconsistent reference point potentials. With an increase in the number of output levels, the design of the driving power supplies becomes more complex. To reduce this complexity, a common-emitter single-phase multilevel CSC topology is proposed in [110], as shown in Fig. 18(c). The advantage of this topology is that the emitters of all switches are connected together, so only one driving power supply is required, which simplifies the design. The disadvantage of this topology is that it requires multiple dc sources.

c) Single-phase combination multilevel CSC: Different from single-phase direct multilevel CSC topology, single-phase combination multilevel CSC topology is characterized by multiple H-bridge cells in parallel at the ac-side to achieve the multilevel output. Therefore, only one dc source is needed. Three typical single-phase combination multilevel CSC topologies are shown in Fig. 19 [114].

The topology shown in Fig. 19(a) is composed of three independent single-phase two-level CSCs in parallel. The dc-side of each cell is an independent current source and there is no coupling. In Fig. 19(b) and (c), the single current source and shunt inductor are used. By a reasonable modulation method, the current flowing through each cell is I_{dc}/N in steady state to realize multilevel output. The difference between Fig. 19(b) and (c) is that the position of the inductor connection is different. In

TABLE II
DETAILED SUMMARY OF THE SINGLE-PHASE CSC TOPOLOGIES

Topology	Number of switches	Number of inductors	Required for each additional level	Level	Number of DC sources	Common emitter
Fig. 17(a)	eight switches	one inductor	one inductor; two switches	Five level	One	No
Fig. 17(b)	six switches	one inductor	one inductor; two switches	Five level	One	No
Fig. 17(c)	six switches	one inductor	one inductor; two switches	Five level	One	No
Fig. 18(a)	six switches	zero inductor	one source; one switch	Five level	Three	No
Fig. 18(b)	seven switches	three inductors	one source; one switch	Five level	One	No
Fig. 18(c)	six switches	zero inductor	two sources; two switches	Five level	Four	Yes
Fig. 19(a)	twelve switches	zero inductor	one source; four switches	Seven level	Three	No
Fig. 19(b)	twelve switches	six inductors	two inductors; four switches	Seven level	One	No
Fig. 19(c)	twelve switches	four inductors	one inductor; four switches	Seven level	One	No
Fig. 20	twelve switches	two inductors	one inductor; four switches	Nine level	One	No

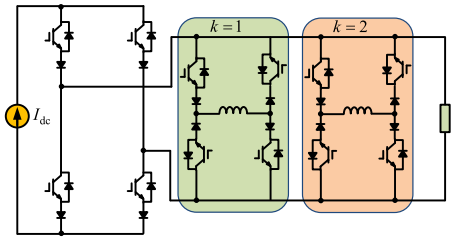

Fig. 20. H-bridge + inductor cell multilevel topology (9-level) [115].

Fig. 19(b), the inductors are connected to the H-bridge, and the current flowing through each inductor is equal, which is I_{dc}/N. But, in Fig. 19(c), the current flowing through each inductor is not equal, the closer to the dc source the inductor is, the greater the current flowing through the inductor. The advantage of combination multilevel CSC is that it can flexibly expand the number of output levels and power.

On the other hand, in multilevel CSC topologies with multiple shunt inductors, it is expected that the inductor currents can be evenly divided to achieve multilevel output. In most topologies, balanced inductor currents depend on symmetrical switching states. Since the inductor currents cannot be directly controlled, they may become unbalanced, which will reduce the output waveform quality of the converter and affect system stability. In order to realize the direct control of inductor current, a multilevel CSC topology based on H-bridge + inductor units is proposed in [115], as shown in Fig. 20.

The topology in Fig. 20 is also a two-stage topology. The first stage is a single-phase H bridge structure, which realizes pulse width control and current commutation; the second stage is an inductor cell, which realizes multilevel output by controlling the current of the inductor cell. The magnitude of the current flowing through each inductor unit is $I_{dc}/2^k$, and k is the number of the inductor cell. There are three operation modes of each inductor cell, including circulating current mode, charging mode, and discharging mode, respectively. The inductor current can be directly controlled by controlling the time of charging mode and discharging mode.

In order to present the above analysis more clearly, Table II presents a detailed summary and comparison of the single-phase CSC topologies.

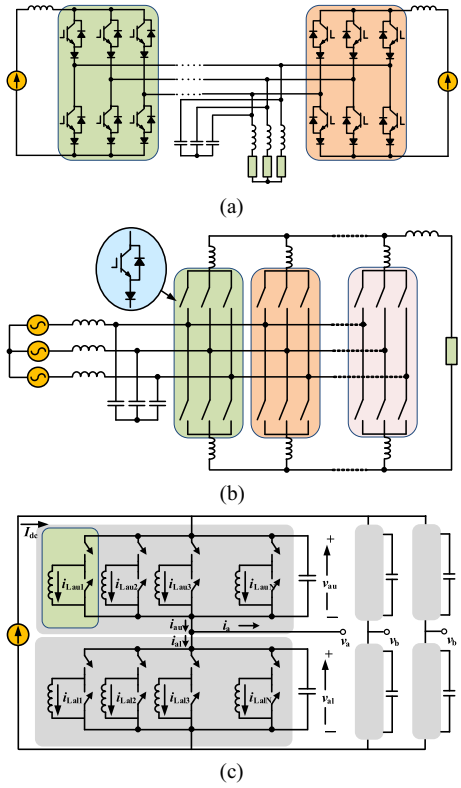

Fig. 21. Three-phase CSC. (a) Combination mode multilevel CSC [116]. (b) Direct-type multilevel CSC [117]. (c) Modular multilevel CSC [34].

d) Three-phase multilevel CSC: Fig. 21(a) shows a combination mode three-phase multilevel CSC [116], in which several CSCs are connected in parallel on the ac side and several independent current sources are used on the dc side. In this structure, many independent units are controlled separately, so the problem of inductor current equalization does not arise. However, several independent dc current sources are required for the combination-mode multilevel converter, which increases the cost and volume of the system. Therefore, a direct-type multilevel three-phase CSC is used [117], as shown in Fig. 21(b). Compared with the combination-mode three-phase multilevel CSC, it does not require multiple dc sources and needs only one current loop. Therefore, the circuit structure and control method are simpler.

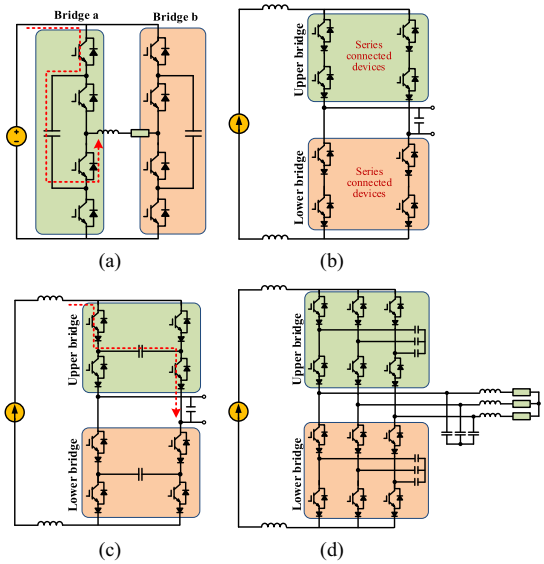

Fig. 22. Flying-capacitor-clamped (FCC) multilevel converter. (a) Single-phase flying-capacitor-clamped multilevel VSC [118], [119]. (b) Single-phase CSC with device series connections. (c) Single-phase flying-capacitor-clamped CSC with three-level AC currents. (d) Three-phase flying-capacitor-clamped CSC with three-level AC currents.

Fig. 21(c), on the other hand, uses a different configuration that forms an MMC [34], in which each submodule is a half-bridge CSC, just like the one shown in Fig. 8(d). Its working principle follows exactly the dual of the voltage-source-based MMC and can be derived through duality theory.

2) DC-Link Multilevel CSC: Different from ac-link multilevel CSCs, which generate multilevel PWM waveforms through different levels of constant dc currents, dc-link multilevel CSCs basically convert the ac-side voltages into the dc-side of the CSC and form multiple levels of dc-side voltages bounded by the ac-side line-voltage envelopes. Currently, there are two major ways to achieve dc-link multilevel CSCs: 1) using dc-side series connection and 2) using the ac-type flying-capacitor technique. If the ac line voltages feature multiple different magnitudes, stacking them together on the dc link would result in different levels. Similar results can also be realized by utilizing internal capacitors to subtract from or add to the line voltage.

a) Flying-capacitor-clamped CSC: The flying-capacitor-clamped CSC differs from the voltage-source flying-capacitor-clamped converter [see Fig. 22(a)] but shares some similarities in terms of how it enables the converter to sustain higher voltages. Based on the operation principle of a single-phase CSC, its dc-link voltage consists of pulsed ripples bounded by the ac-side line voltages. Traditionally, to accommodate a higher ac voltage range when converter operation exceeds the device voltage ratings, device series connection is adopted, as shown in Fig. 22(b). Such an arrangement is not a major issue when using IGCTs but can be quite challenging with IGBT + diode configurations, especially for recent wide-bandgap (WBG) devices.

The ac-type flying-capacitor-clamped technique can be considered as a unique generalization of the dc-type flying-capacitor-clamped technique, both of which utilize the embedded capacitors to provide extra levels of voltage across

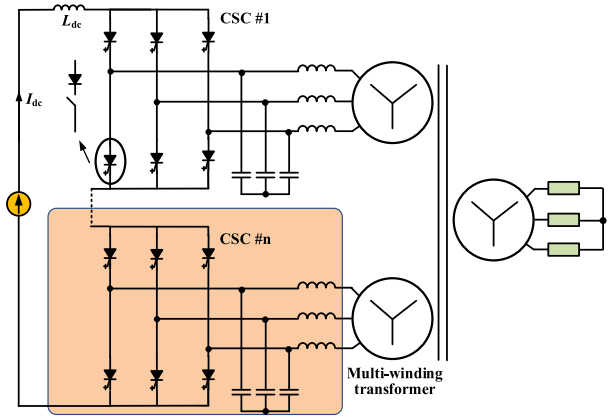

Fig. 23. Typical DC-series-connected CSC system.

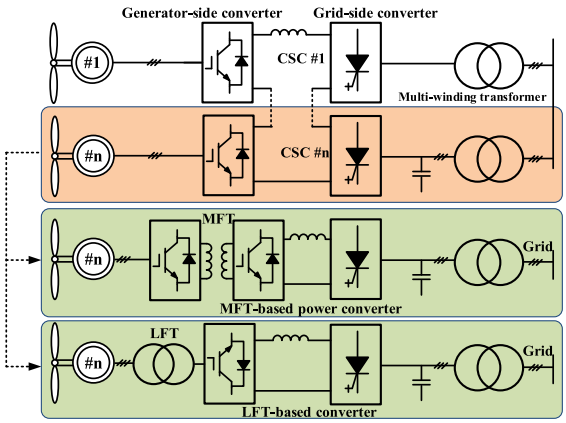

Fig. 24. Typical DC-series-connected CSC system [74].

the converter bridge [118]. The major difference is which type of the power form the capacitor needs to handle. In the flying-capacitor-clamped CSC [see Fig. 22(c)], the dc-link voltage potential is linked to phase voltages through the switching network and the capacitor (as indicated by the red dotted line), thus, by actively controlling the current conducting path of capacitor, one can maintain a relatively stable and divide the voltage cross upper/lower bridge into smaller magnitude. Such an idea can be further extended into three-phase version as shown in Fig. 22(d), where Y-connected flying capacitors can be used [119].

b) DC-series-connected CSC: Dc-series connection of CSCs can be traced back to 1990s [120], motivated mainly by the urgency for high voltage applications. With a 120° degree phase shift, the dc-link dv/dt can be reduced. A general configuration of dc-series- connected CSC is demonstrated in Fig. 23, where ac-side independent source can be achieved by multi-winding transformer [121], [122]. A well-studied application scenario is the wind energy generation, as shown in Fig. 24 [74]. The generator-side converter can be a VSC with either a line-frequency transformer or a medium-frequency transformer, while the grid-side converter consists of multiple conventional CSC modules connected in series.

In [123], a transformerless topology is proposed to provide all benefits of series-connected CSCs but without bulky and

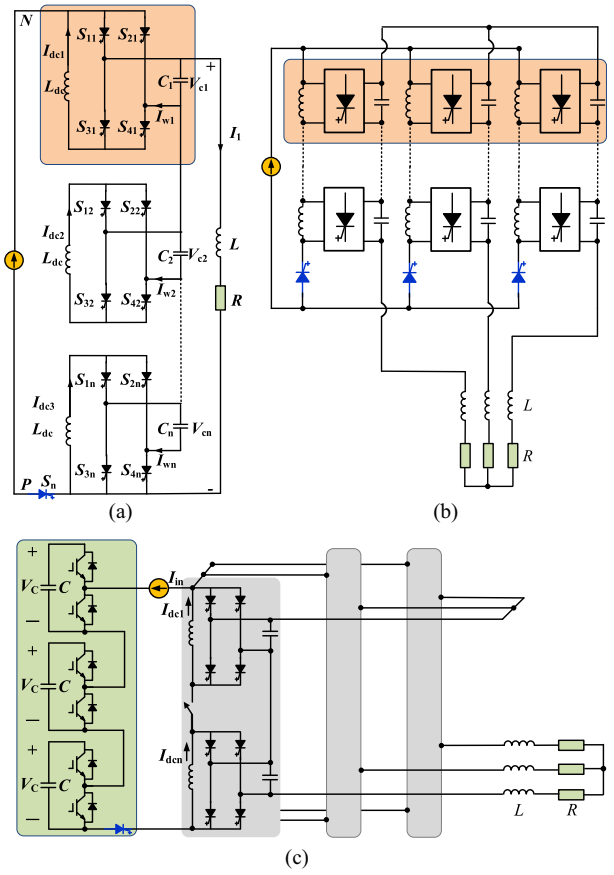

Fig. 25. Transformerless series connected CSC [123]. (a) Single-phase configuration. (b) Three-phase configuration. (c) A further derivation of the transformerless series connected CSC.

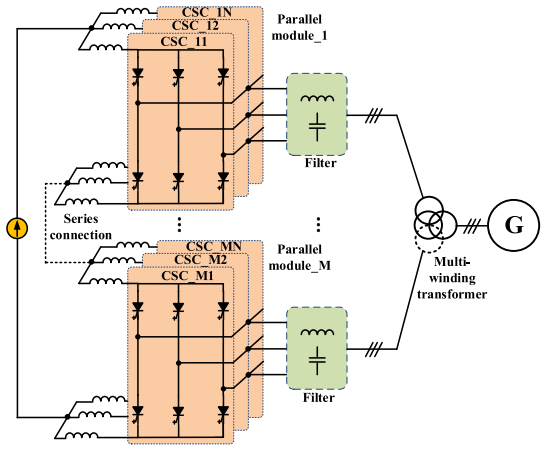

Fig. 26. Hybrid AC-parallel DC-series-connected CSC system [121].

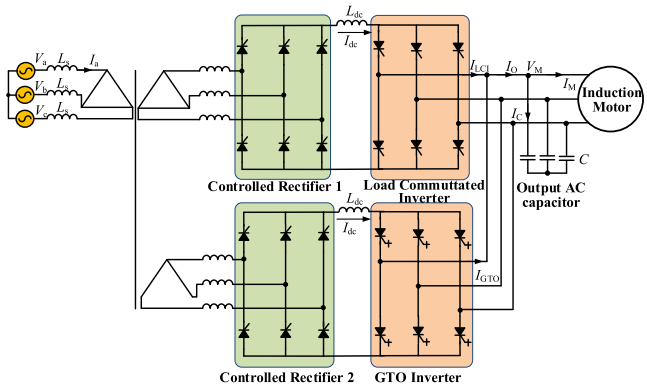

Fig. 27. Multilevel CSC system integrating LCI and GTO-based Inverters [116].

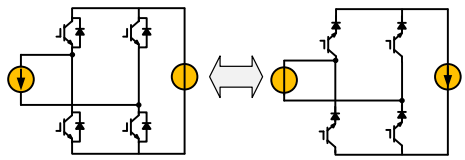

Fig. 28. Duality of H-bridge VSC is an H-bridge CSC.

costly transformers. The topology is shown in Fig. 25, where its ac line voltage is divided into n pieces, and thus, reduction of bearing voltage can be modularly achieved. To reduce the blocking voltage of the dc-link switch and provide active control of dc voltage, the derivative topology of Fig. 25(a) is shown in Fig. 25(c), where several MMC-like half-bridge modules are series-connected.

3) Hybrid Multilevel CSC: One way to further generalize the multilevel CSC topologies is to combine both the ac-link and dc-link multilevel techniques, resulting in hybrid multilevel CSCs.

One typical example is the series-parallel CSC introduced in [121], as shown in Fig. 26. The uniqueness of this hybrid topology lies in the fact that it features both ac-link multilevel waveforms and dc-link multilevel waveforms. Therefore, both the ac and dc sides enjoy improved power quality and thus provide composite benefits from both types of topologies.

Another unique example is the construction of three-phase multilevel CSCs through the combination of different types, e.g., a GTO-based inverter and a thyristor-based LCI, as shown in Fig. 27 [116]. Such a combination enjoys benefits similar to those in the VSC domain (e.g., IGBT + SiC in ANPC converters [124]), including high efficiency, low cost, uncompromised power quality, etc.

C. Duality and Isomorphism of CSC Topology

In recent years, interesting applications of graph theory in power electronics have emerged [125], such as the duality between VSCs and CSCs, and isomorphism between VSCs and CSCs, as shown in Fig. 28. These general relationships among different power converters not only bring the research on CSCs and VSCs closer together, but also open up great potential for further innovations on both sides. For example, one can derive a CSC topology from an existing or new VSC topology through duality (and vice versa through isomorphism) [126]. After the derivation, one can also build the link of their operation principles and models through duality and isomorphism. This gives researchers a universal tool for more systematic CSC research covering topology, modeling, modulation, and control of power electronics.

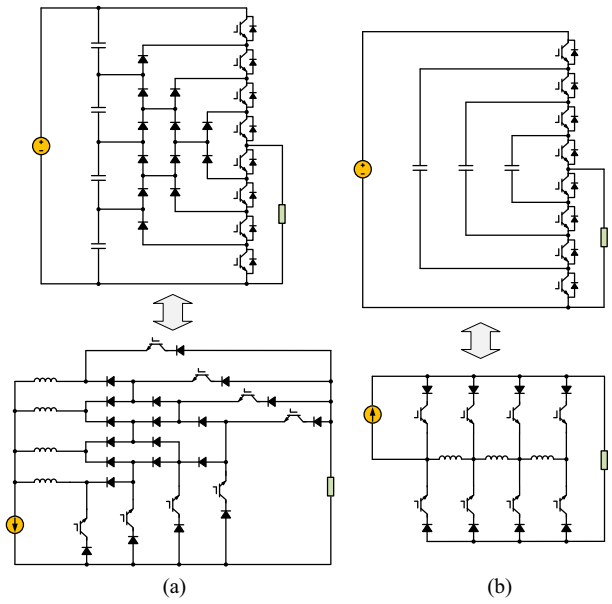

Fig. 29. Duality of multilevel VSCs and CSCs [114]. (a) Duality of diode-clamped multilevel VSC bridge is an ac-link multilevel direct-type CSC bridge with diode-clamping. (b) Duality of flying-capacitor-clamped multilevel VSC bridge is a half-bridge based ac-link multilevel direct-type CSC bridge.

1) Duality of CSC: The duality phenomenon is not new but lingers around through the history of science, and one can establish a simple yet profound relationship between CSC and VSC [114], [127], [128], [129]. Take the H-bridge VSC and CSC as an example [130]. It is easy to observe the following corresponding relations: for each part of the original converter, there is an associated dual component in a dual converter including the active switches; for the circuit connections, where VSC is series (parallel), CSC is parallel (series); the switching state is also dual; the deadtime in VSC becomes overlap time in CSC.

We can further extend the duality into multilevel CSC and VSC topologies as investigated in [114], e.g., general multilevel CSCs based on the duality of diode-clamped VSCs [see Fig. 29(a)], or flying-capacitor-clamped VSCs [see Fig. 29(b)]. More generally, the self-balanced multilevel VSC also has its CSC version as shown in Fig. 30 [131]. Following the same features of its counterpart, the self-balanced multilevel CSC can serve as the general topology to derive various other ac-link multilevel CSCs, covering most of the reviewed topologies in Section III-C.

2) Isomorphism of CSC: In addition to duality, another interesting universal tool for CSC topology research that has emerged in recent years is isomorphism. It originates from graph isomorphism, which is defined as the equivalence between two graphs that appear different but feature the same node connections [132]. Generally speaking, every VSC has its isomorphic CSC. One typical example is that the conventional three-phase CSC and the single-phase three-level T-type VSC can be modeled with the same graph and thus can be defined as an isomorphic converter pair, as shown in Fig. 31(a). Going beyond topology, it can also be observed that these two converters have the same number of switching states in the space vector domain, with

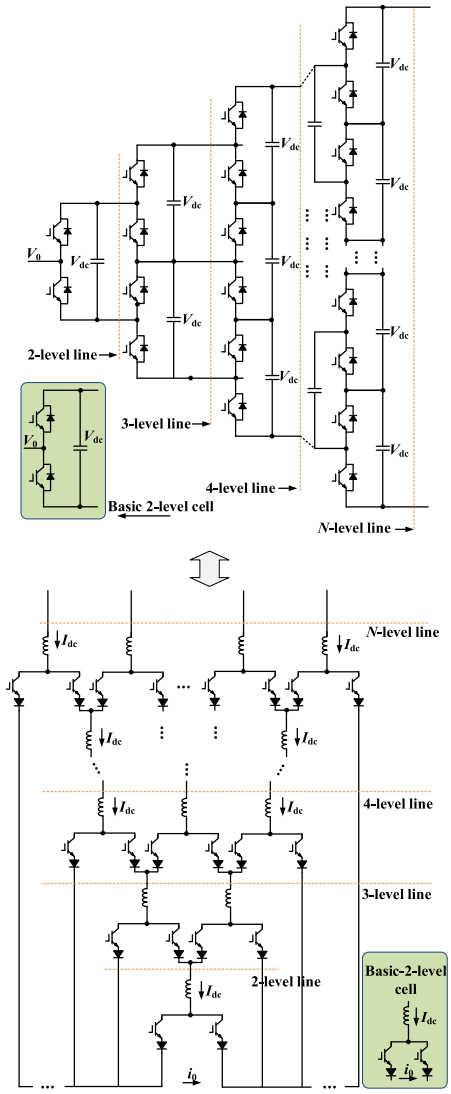

Fig. 30. Duality of self-balanced multilevel VSC and the duality CSC version [131].

identical physical meanings [see Fig. 31(b)]. This relationship can be further generalized to the isomorphism between a single-phase multilevel T-type VSC and a multiphase CSC, as shown in Fig. 31(c).

The deployment of isomorphism does not end here, but can be further extended to multilevel CSCs. For example, the five-level topology in Fig. 17(b) is isomorphic to a two-level three-phase VSC, and the five-level version of combination type single-phase multilevel CSC topology in Fig. 19(c) is isomorphic to two-level four-phase VSC. The dc-link multilevel CSC, e.g., ac-type flying-capacitor-clamped CSC is isomorphic to flying-capacitor-clamped VSC [see Fig. 32(c)], dc-series CSC is isomorphic to cascaded H-bridge VSC [see Fig. 32(d)]. The isomorphic relationships provide a different insight and explain well on how the dc-link multilevel CSCs work. Take series-connected CSC and VSC as examples, they share some interesting features.

1) The dc-link capacitor in the VSC is mapped into ac-link capacitors in the CSC.

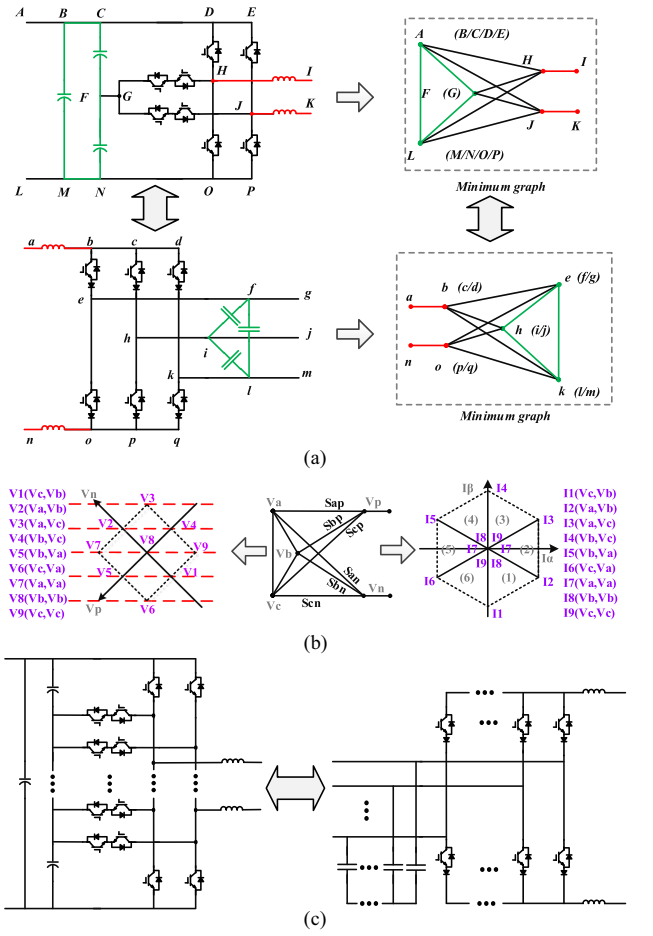

Fig. 31. Isomorphic of VSCs and CSCs. (a) Isomorphic relationship between a single-phase three-level T-type VSC and a conventional three-phase CSC. (b) Switching state corresponding relations between the isomorphic converter pair. (c) Isomorphic relationship between a single-phase multilevel T-type VSC and a multiphase CSC.

2) They have a one-to-one mapping among their vectors, that is, same number of active vectors, and same number of zero vectors.
3) They have multilevel waveforms enabled by cascaded connection, which means electromagnetic interference (EMI) reduction on their ac or dc side.

By utilizing the same idea, more innovative CSCs are expected to be derived based on the isomorphic VSCs. In [126], one can even combine both the duality and isomorphism, to link not only a pair, but up to four converters, through one-to-one mapping relations, and all major features within the four converters can be shared and provide systematic understanding of them.

IV. Overview of CSC Modulations and Controls

A. CSC Typical Modulation Strategy Overview

In this section, typical CSC modulation strategies are compared and their limitations are revealed. Currently, the modulation strategies for three-phase CSCs mainly include

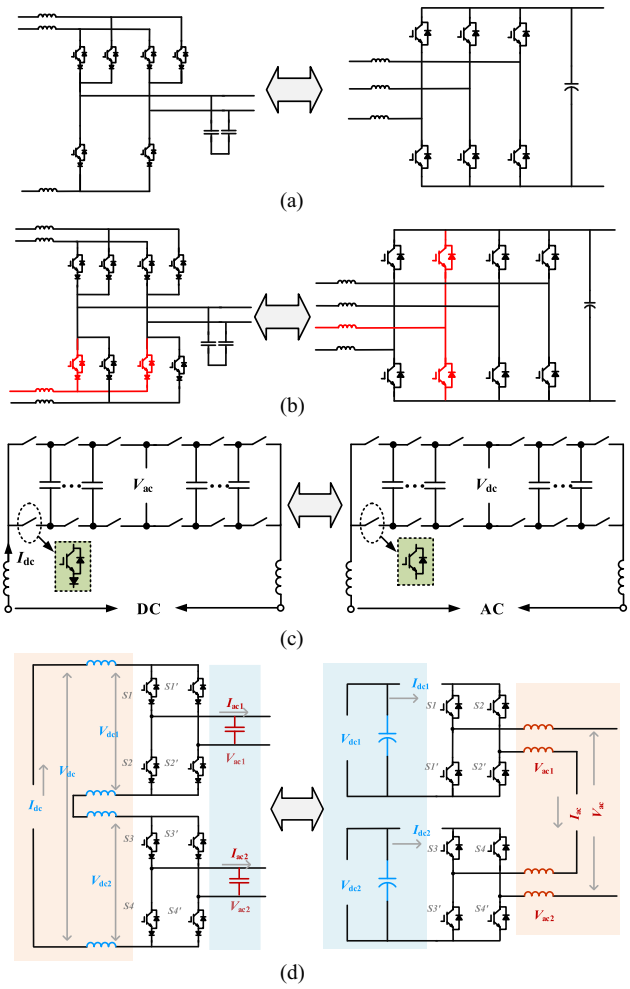

Fig. 32. Isomorphic relationship between (a) five-level topology 3 [direct single-phase multilevel CSC topology in Fig. 17(b)] and two-level three-phase VSC, (b) five-level (combination single-phase multilevel CSC topology) and two-level four-phase VSC, (c) Dc-link multilevel AC-type flying-capacitor-clamped CSC [generalized version of Fig. 22(c)] and flying-capacitor-clamped VSC, and (d) Dc-series H-bridge CSCs and Ac-series H-bridge VSCs.

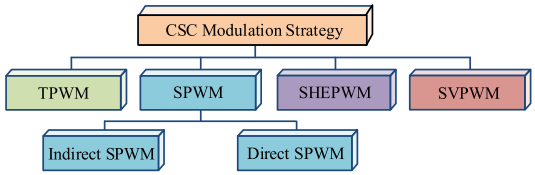

Fig. 33. Basic modulation strategy of three-phase CSC.

trapezoidal pulsewidth modulation (TPWM), selective harmonic elimination pulsewidth modulation (SHE-PWM), sinusoidal pulsewidth modulation (SPWM), and space vector pulsewidth modulation (SVPWM), which are illustrated in Fig. 33. The specific implementation processes are shown in Fig. 34.

TPWM [6], [133], [134], [135] is widely used in high power CSCs, where the trapezoid wave is used as a modulation wave and the triangle wave is used as a carrier wave in TPWM, which is shown in Fig. 34(a). The amplitudes of two waves are equal. Due to the equal amplitude, the fundamental component of

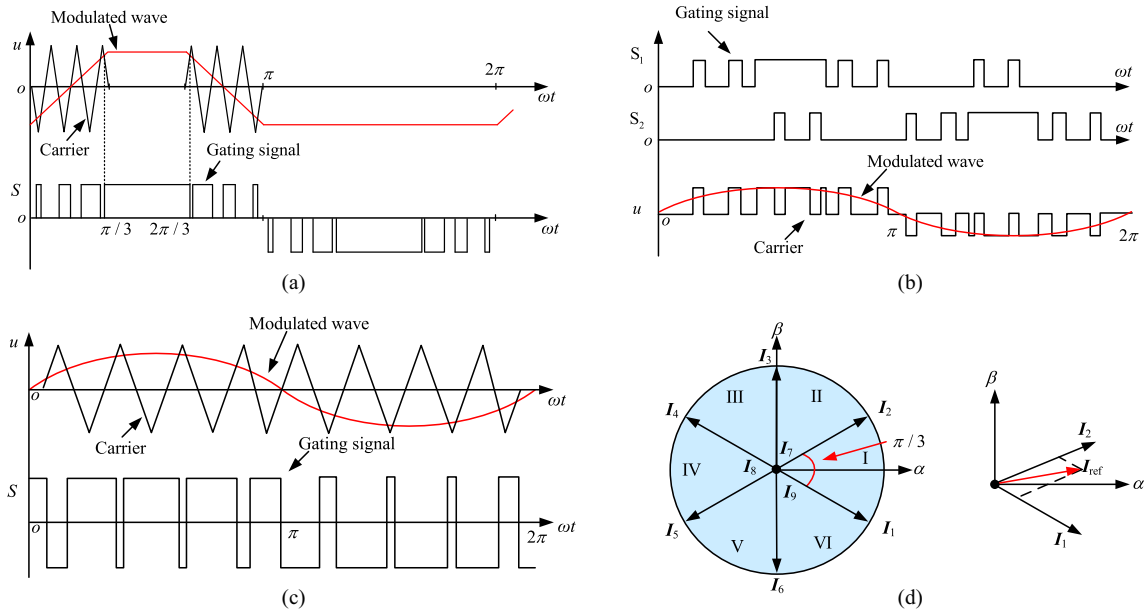

Fig. 34. Specific implementation for basic modulation strategy. (a) TPWM. (b) SHE-PWPM. (c) SPWM. (d) SVPWM.

modulation wave exceeds that of carrier wave. Therefore, the dc utilization ratio can effectively be improved, which is one of its main advantages. However, on the other hand, because the trapezoidal wave contains low order harmonics, the output waveform may contain the 5th, 7th, and other low order harmonics, which makes the design of filter difficult.

The SHE-PWM [136], [137] shown in Fig. 34(b) is usually used to reduce these low order harmonics in CSCs, where the switch angle of the harmonic to be eliminated is needed to calculate, and it is stored in the digital controller. It should be noted that although the method can eliminate the specified low order harmonics, the amplitude of the remaining harmonics may be increased. Besides, the frequencies of harmonics eliminated by the SHE-PWM are mainly focused on the low-order harmonics, which cannot eliminate high-order harmonics. What is worse, the calculation and storage of switch angle will occupy a large amount of controller memory, which increases the cost of the hardware. Therefore, this method is mainly used in high-power applications with low switching frequency, but it is not suitable for applications with the requirement of good dynamic response.

To simplify computational complexity, SPWM shown in Fig. 34(c) is used, which is a mature and widely used modulation strategy, where the gating signals are generated by only comparing sinusoidal modulation wave and triangular carrier wave. The output for the converter can be directly adjusted by changing the frequency and amplitude of the modulation wave, which is easy to implement. Furthermore, SPWM is divided into indirect SPWM [138], [139] and direct SPWM [140], [141], [142]. In [138], the advantages and disadvantages of the indirect SPWM applied to three-phase CSC are researched in detail. It is pointed out that the CSC is dual with VSC. Therefore, with this feature, in [139], the SPWM for CSCs can be obtained by mapping the switching states of VSC to the CSC. According to the specific implementation process of the indirect SPWM, it can be observed that there is a two/three logic conversion in the scheme, and the modulation signal makes the bridge arm current 30° ahead of the voltage. Therefore, the phase calibration is needed before the generation of gating signals.

According to the above-mentioned analyses, it can be concluded that the indirect SPWM for CSCs has the characteristics that the switching frequency is equal to the carrier frequency, phase calibration and two/three logic conversion are needed, which means that this modulation strategy still has the disadvantages of high switching loss, low dc current utilization and low efficiency of system. In order to solve the above-mentioned shortcomings of the indirect carrier modulation strategy, discontinuous PWM can be implemented as presented in [143].

Another way to tackle the above issue is through direct carrier modulation strategy for CSCs, e.g., a method is presented in [140], where the phase calibration and two/three logic conversion are no longer needed, which simplifies the algorithm. Besides, the switching frequency of this method is reduced by about 1/3. Therefore, the switching loss can also be reduced, and the efficiency of system is improved. In addition, the inductor current ripple and CMV are optimized respectively in [141] and [142].

The SVPWM for CSCs is shown in Fig. 34(d). The principle of SVPWM for CSCs is briefly explained as follows. Unlike VSCs, which use voltage vectors, CSCs employ current vectors. There are six active vectors ($\boldsymbol{I}_1$–$\boldsymbol{I}_6$) and three zero vectors ($\boldsymbol{I}_7$–$\boldsymbol{I}_9$), which divides the space into six sectors. The reference vector $\boldsymbol{I}_{\mathrm{ref}}$ is synthesized by two adjacent active vectors $\boldsymbol{I}_\alpha, \boldsymbol{I}_\beta$ and one zero vector $\boldsymbol{I}_0$. For example, in sector I, $\boldsymbol{I}_{\mathrm{ref}}$ is synthesized by vectors $\boldsymbol{I}_1$, $\boldsymbol{I}_2$ and zero vector $\boldsymbol{I}_7$. This is the traditional and commonly used vector selection method. Of course, optimized vectors can also be selected according to different needs [144]. Then, for the vector sequence arrangement, in the traditional SVPWM, taking the five-segment type as an example, at this time, in sector I, the

TABLE III
SUMMARY AND COMPARISON OF DIFFERENT CONVENTIONAL MODULATION

Modulation Strategy	TPWM	SHE-PWM	SPWM	SVPWM
DC utilization (within linear range)	0.74	0.73	0.612	0.707
Complexity	Complex	Complex	Simple	Complex
Low order harmonic	Poor	Better	Poor	Good
Flexibility	Inflexible	Inflexible	Inflexible	flexible
Dynamic characteristics	Medium	Low	High	High
Online implementation	Yes	NO	Yes	Yes
Application	High-power	High-power	Medium power	Medium power

vector sequence arrangement is $\boldsymbol{I}_0, \boldsymbol{I}_1, \boldsymbol{I}_2, \boldsymbol{I}_1, \boldsymbol{I}_0$. Then, the dwell times T_1, T_2, and T_0 for the vectors $\boldsymbol{I}_1, \boldsymbol{I}_2, \boldsymbol{I}_0$ can be calculated by the principle of "ampere-second balance", which is shown in the following equation:

$$\boldsymbol{I}_{\text{ref}} T_s = \boldsymbol{I}_1 T_1 + \boldsymbol{I}_2 T_2 + \boldsymbol{I}_0 T_0 \ . \tag{1}$$

From (1), the dwell times T_1, T_2, and T_0 can be obtained as (2), where T_s is the switching period, m is the modulation index, and θ is the reference vector angle

$$\begin{cases} T_1 = mT_s \sin(\pi/6 - \theta) \\ T_2 = mT_s \sin(\pi/6 + \theta) \\ T_0 = T_s - T_1 - T_2 \end{cases} . \tag{2}$$

Then, combined the vector sequence arrangement and the dwell time, the gating signals of CSC can be generated.

The most significant difference between SVPWM and SPWM is dc utilization ratio. Compared with SPWM, the dc utilization of SVPWM is increased. Besides, the vector sequence of SVPWM can be changed flexibly, which means that the SVPWM is flexible to control the output voltage and grid current. On the other hand, the digital realization for SVPWM is convenient. Therefore, it is widely used in different fields. The summary and comparison of the above-mentioned modulation strategies are shown in Table III [6].

B. CSC Control Strategy Overview

The primary control objectives of a CSC, taking the rectifier as an example, are to ensure sinusoidal grid current compliant with national THD standards, regulate the output voltage, and minimize ripple in the dc-link inductor current. In addition, unity power factor operation should be achieved. Accordingly, this section introduces and discusses the typical control strategies for CSCs.

There are two main control strategies for CSCs shown in Fig. 35, which are indirect current control and direct current control. The indirect current control is divided into static indirect current control [145] and dynamic indirect current control (DICC) [146]. In [145], an indirect current control strategy is proposed, where the phase-shift angle of the modulation wave is adjusted by the feed-forward control, which can realize the unit

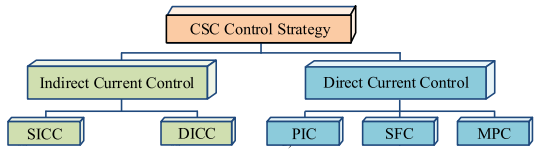

Fig. 35. Basic control strategies for three-phase CSC.

power factor operation of the system. However, it is sensitive with the change of system parameters and slow in dynamic response. Therefore, the DICC [146] is presented, where the grid current is indirectly controlled by using the dynamic model of grid voltage and grid current. Therefore, the disadvantage that is sensitive with the change of system parameters is solved by the dc current feedback, but the weak damping of *LC* filter may cause oscillation of the system.

Therefore, direct current control has been proposed to address the problems associated with indirect current control, such as current oscillations and slow dynamic response. The key difference between direct and indirect current control lies in the presence of a closed-loop grid current control in the former, whereas the latter lacks this feature. The direct current control strategies for CSCs include PI control (PIC), model predictive control (MPC), and state feedback control (SFC). PIC [147] is simple and robust but remains sensitive to parameter variations and exhibits slow dynamic response. In [148] and [149], MPC is employed to optimize the converter, thereby enhancing system robustness. MPC is particularly suitable for multiple-input multiple-output systems. Since CSCs typically involve multiple control variables—such as grid current and capacitor voltage—MPC enables effective collaborative optimization of these variables, which contributes to improved system performance and stability. Another interesting strategy is SFC. In this approach, the control variables can be directly measured, which is advantageous for system optimization as it allows the use of linear controllers. In [30], a method based on the zero set concept is proposed to solve the state feedback design problem for STATCOM applications, thereby improving controller stability. However, under strong constraints, tight design objectives, and significant uncertainties, the feasible set of SFCler gains may become empty. In this case, more complex control strategies must be used.

V. KEY PROBLEMS AND SOLUTIONS FOR PRACTICAL OPERATION OF CSCS

In Section IV, the operation methods for CSCs are reviewed, but only the fundamentals are covered. Based on the above-mentioned analysis, CSCs exhibit attractive application prospects in EVs, uninterruptible power supplies, more-electric aircraft, motor drives, and other fields. In these applications, CSCs offer significant potential for achieving high power density and high reliability. In practice, however, numerous operational challenges may arise during the deployment of CSCs, necessitating dedicated optimization and improvement to address specific issues related to modulation, control, topology, and more. Therefore, this section reviews and discusses the key problems

encountered in the practical application of CSCs along with their latest solutions.

A. Unbalanced Grid Voltage Condition

Typically, an EV charging station rectifies the grid voltage into dc voltage to charge the vehicle. Due to the nonlinear, intermittent, and power-imbalance characteristics of various loads in the power grid, grid faults may occur in practical systems. Simultaneously, adverse weather conditions such as lightning can also introduce grid disturbances. When the grid voltage becomes unbalanced, the dc-side output voltage of the CSC exhibits double-frequency pulsations, leading to severe distortion in the grid current and degradation of power quality. Therefore, in CSC-based EV chargers, the impact of grid voltage imbalance on the output waveform must be carefully addressed. Existing research tackles this issue through two primary approaches: 1) topological enhancements, such as adopting four-leg CSC structures, and 2) control-loop optimization techniques, including negative-sequence current control and instantaneous power control.

In [150], a single-stage bidirectional CSC is analyzed in detail, with particular focus on the adverse effects of unbalanced grid voltage. A PI-based control strategy is then proposed to independently regulate the *dq*-components of the negative-sequence current to zero, thereby eliminating the quadrature second-harmonic oscillation in the modulation index. This approach effectively suppresses the negative-sequence current and improves system stability.

In [151], mathematical models for both single and parallel three-phase CSCs are developed using instantaneous power theory. An improved control strategy is then proposed, which injects optimized negative-sequence currents and employs a hybrid current controller consisting of a high-bandwidth closed-loop harmonic current controller and a closed-loop fundamental grid current controller. This strategy reduces dc-link ripple under unbalanced grid conditions, suppresses *LC* resonance, ensures sinusoidal grid current, and achieves THD levels compliant with national standards.

Most improved control strategies require positive- and negative-sequence separation for CSCs under unbalanced grid voltage conditions, which is complex and difficult to implement. In [152], a zero-crossing detection method for CSCs is proposed to simplify the control strategy. This approach eliminates low-frequency fluctuations in the output voltage without requiring positive–negative sequence separation under unbalanced grid conditions. In [153], an input-voltage feedforward control strategy is proposed to suppress the odd harmonics in the ac input current and the even harmonics in the dc output voltage under unbalanced ac voltage conditions. Similar to other simplified approaches, this method does not require positive–negative sequence separation. In [154], a conductance-emulating control strategy is proposed for CSCs to regulate instantaneous power under unbalanced input phase voltages. This method eliminates the need for a PLL and sequence extraction, thereby simplifying computation. It simultaneously controls instantaneous active and reactive power to achieve balanced input currents or suppress output current ripple. However, the notch filter employed to attenuate the double-line-frequency ripple in the output current introduces implementation challenges in systems operating over a wide ac input frequency range. In [155], a CSC power tracking control strategy based on phase voltage reconstruction is proposed, which is suitable for unbalanced input phase voltage under wide-frequency ac input conditions. The input current imbalance is mitigated by controlling the input current to be proportional to the reconstructed phase voltage.

In addition to solving the problems caused by unbalanced ac voltage through control, four-leg CSCs can be another natural choice for such application [156]. The fourth leg can provide a path for zero-sequence current and solve the imbalance problem in the power grid.

B. DC-Link Inductor Current Ripple Suppression

For CSCs used in more-electric aircraft, converter size must be minimized due to space constraints. Although a large dc-link inductor ensures nearly constant current, it occupies significant space and increases losses. Reducing the inductor size leads to higher current ripple, which raises losses, causes EMI, and distorts the output waveform. Hence, effective dc-link current ripple suppression is a key technical challenge in aircraft CSC applications.

The inductor current ripple can be derived from the basic definition of the inductor current shown as (3), where Δi_L is the dc-link inductor current ripple, Δt is the time interval of each vector, v_{o} is the output voltage, L_{dc} is the dc-link inductor, and u_{dc} is the bridge arm voltage

$$\Delta i_L = \frac{u_{\mathrm{dc}} - v_{\mathrm{o}}}{L_{\mathrm{dc}}} \Delta t. \tag{3}$$

It can be observed that to reduce the inductor current ripple, improvements can be made across three dimensions. First, optimizing the design of the dc inductor. Second, increasing the switching frequency. Thirdly, reducing voltage differences across the inductor by optimizing modulation.

The design process of dc inductors and filter capacitors is introduced in [157], and the design constraints are considered to optimize them. The size of the dc inductor and capacitor is reduced, and the power density of the device is improved.

On the other hand, the modulation strategy can be optimized. In [158], an improved VSC modulation method reduces dc ripple by comparing three-phase current references with triangular carriers toggling between I_{dc} and 0 or 0 and $-I_{\mathrm{dc}}$. Mapping VSC switching states to CSC enables dc-link current ripple suppression, but the required logic transformation is complex.

In [159], a novel method is proposed for three-phase direct-parallel CSCs to reduce dc-link inductor current ripple. The approach employs steady-state current-balancing control by appropriately selecting redundant switching states and vector sequences. The key principle of this modulation strategy is to minimize both the voltage variation across the dc-link inductor and the duration of the applied switching states, thereby suppressing current ripple.

Similarly, Guo et al. [160] highlight that improper SVM pulse pattern design in three-phase back-to-back CSCs can result in

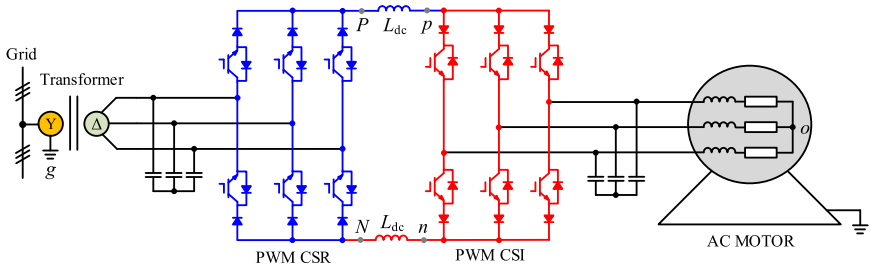

Fig. 36. Typical CSC medium-voltage drive system with transformer.

significant current ripple. Coordinating the gate signals of the CSR and inverter effectively reduces the ripple. However, this solution is topology-specific and cannot be generalized to other CSC configurations.

Furthermore, [161] introduces a 12-sector space vector modulation (SVM) method that synthesizes reference vectors using three active vectors per sector without employing zero vectors, reducing the voltage difference across the inductor and consequently lowering dc-link current ripple without increasing switching frequency or inductor size. Nevertheless, its modulation index range is limited to ($\sqrt{3}/3$, 1]. In order to solve this problem, within the modulation index range of [0, $\sqrt{3}/3$], the synthesis reference vector of adjacent active vectors and zero vector was proposed in [141]. This method can reduce the inductor current ripple within the full modulation range.

On the other hand, in [162], a virtual vector modulation method is proposed to further reduce current ripple, though its applicable modulation index range is limited to [0, $\sqrt{3}/2$]. In [163], the sector is divided into 24 sectors for optimization within the range of modulation index ($\sqrt{3}/3$, 1]. And use different vector sequences in the [0, $\sqrt{3}/6$] and ($\sqrt{3}/6$, $\sqrt{3}/3$] ranges to minimize the current ripple.

Based on the above-mentioned analyses, it can be found that the current ripple can be suppressed from two aspects, one is to optimize the voltage drop across the dc-link inductor, which can be reduced by proper selection of the switching states and vector sequences to avoid the large voltage drop. The other is to optimize the time interval of the switching states. It should be noted that there may be a problem of limited modulation index during the inductor current ripple optimization process.

C. CMV Suppression

In CSC-based ac motor drive systems, CMV is a critical issue, typically generated by the converter's switching actions. For nonisolated CSCs, failure to suppress CMV subjects the motor drive to voltage stress, leading to premature insulation aging or failure and reducing motor lifetime. CMV can also induce leakage currents through parasitic capacitances, potentially damaging motor bearings. Using an isolation transformer blocks the CMV path, as the transformer withstands the system CMV and prevents its transmission to the motor. A typical transformer-based CSC MV drive system is shown in Fig. 36. However, the bulky power-frequency transformer increases system volume, weight, and cost, while reducing efficiency. Thus, CMV suppression represents the fourth key technical challenge in the practical application of CSCs.

For the CMV suppression in CSCs, it can be divided into two categories: hardware improvement and software optimization. Hardware improvement methods include adding isolation transformers, passive common-mode filters [164], active common-mode filters [165], [166], improving the structure of the topology [167], etc. This type of method has the advantage of being simple and effective but increases volume and cost. The following mainly explains the methods of software optimization. For example, the optimization methods for SVM.

The SVM method for CMV suppression can be divided into two types: reducing the amplitude and average value of CMV. In Fig. 36, if no isolation transformer is used, the CMV will be superimposed on the phase voltage of the motor. For this series-connected CSC topology, the CMV $V_{\rm cm}$ is defined as the difference between the rectifier-side CMV $V_{\rm cm\_R}$ and the inverter-side CMV $V_{\rm cm\_I}$, and can be expressed as [50]

$$V_{\rm cm} = V_{\rm cm\_R} - V_{\rm cm\_I} = \frac{v_{\rm Pg} + v_{\rm Ng}}{2} - \frac{v_{\rm po} + v_{\rm no}}{2}. \tag{4}$$

In terms of reducing the CMV amplitude, in [50], based on the influence of switching states on CMV, it is pointed out that due to the use of zero vector, the peak value of the CMV generated by the CSC with SVM is twice as much as that of the TPWM and SHE without the use of zero vectors. For this reason, in [50], the modulation strategy without zero vector is introduced into CSC to reduce the high CMV peak. In this strategy, the zero vector is replaced by two active vectors in opposite directions. Therefore, the reference vector can be synthesized by three active vectors, which can reduce the peak value of CMV by nearly half. However, this method increases the computational complexity and the switching loss. Besides, the modulation index is limited, which can only be adjusted from 2/3 to 1. In [168], according to the different influence of the redundant switching state of zero vector on the CMV, the minimum CMV value can be obtained by selecting optimal redundant state of zero vector. Thus, the CMV generated by zero vector can be reduced. However, this method also increases the computational complexity and switching loss, meanwhile, the quality of grid current waveform will also be affected.

On the other hand, it is to reduce the average value of CMV ($\rm CMV_{ave}$), which is defined as [168]

$$\rm CMV_{ave} = \frac{1}{T_s} \sum_x (V_{cm\_x} \times T_x) \tag{5}$$

where T_s is the switching period, $V_{\mathrm{cm}\cdot x}$ represents the CMV of the vector $\boldsymbol{I}_x$, and T_x is the dwell time of the vector $\boldsymbol{I}_x$. It mainly solves the problem of large CM filter caused by low-order harmonics in CMV. In [168] and [169], the zero-state vector selection methods are employed to minimize the average value of the CMV. By using the $\mathrm{CMV}_{\mathrm{ave}}$ calculation formula, the zero-state vector with the smallest $\mathrm{CMV}_{\mathrm{ave}}$ is selected from the three zero-state vectors in each sector. This approach effectively reduces the low-order harmonic components, particularly the third order, in the CMV. However, it may lead to an increase in the switching frequency under different operating conditions. In addition, the impact of this method becomes less apparent when the modulation index is low, such as during light load operation of the motor.

To address this limitation, Lian et al. [170] introduce two methods, namely, the four-segment AVR SVRΔ and the three-segment AVR SVRΔ. These methods aim to suppress the third-order component of the CMV to zero by adjusting the dwell times of the two zero vectors. The effectiveness of these two methods becomes prominent when the modulation index is lower than 0.67. Furthermore, a method of using virtual vectors to reduce CMV to zero was proposed in [171], which can significantly reduce the third harmonic component in the CMV within the modulation index [0, 0.67]. In addition, this method reduces the CMV amplitude.

It can be observed that, although the existing literature can suppress the CMV, the output waveform quality may be affected, and the modulation index is limited. Also, the complexity of calculation is increased.

D. Improvement of Efficiency and Power Density

With the growing demand for compactness, high efficiency, and high power density in applications such as integrated motor drives, aerospace power systems, and data centers, conventional CSCs face the challenges of high switching losses and bulky passive components, which have become bottlenecks limiting their further deployment. To address these challenges, WBG semiconductor devices (e.g., SiC and GaN), featuring high breakdown voltage, high switching frequency, low conduction loss, and superior thermal conductivity, provide a solid device foundation for CSCs operating at higher frequencies and power densities. Moreover, soft-switching techniques, by enabling zero-voltage or zero-current transitions, effectively reduce switching losses and EMI while enhancing system efficiency and reliability. Consequently, the integration of soft-switching strategies with WBG devices represents a key pathway for advancing CSCs toward higher performance.

1) WBG Semiconductor Application Technologies: Silicon (Si) remains the dominant semiconductor material for power electronic converters, and Si-based power devices are well established. However, Si technology faces intrinsic limitations in blocking voltage, operating temperature, and switching frequency. These include relatively low voltage-withstand capability, considerable heat generation during operation—limiting switching frequency—and a junction temperature typically restricted to 150 °C [172]. In CSCs, the six controlled unidirectional switches must withstand bipolar voltage stress; due to the limited reverse-blocking capability of Si IGBTs, additional series diodes are required. This increases conduction losses, reduces efficiency, and enlarges the converter footprint, thereby restricting the broader adoption of CSCs [173].

To overcome these limitations, a new generation of power devices based on WBG semiconductor materials—such as SiC and GaN—is increasingly adopted in CSC applications. WBG devices offer higher breakdown voltage, lower conduction loss, faster switching speed, and higher allowable junction temperature [174]. Compared with Si devices of equivalent on-resistance, WBG devices enable operation at higher switching frequencies, leading to smaller converter volume, lower losses, and improved power density. For example, [175] reports that a full-SiC system comprising a buck dc chopper and a CSI achieves a 20.4% reduction in total power loss compared with a hybrid-SiC dc/dc converter combined with a VSI. Similarly, Tan et al. [176] demonstrate that a GaN-based CSI outperforms a VSI at 200 kHz switching frequency, achieving an efficiency of 98.24% and significantly reducing passive component size, including filters, thus further enhancing power density. According to [177], replacing Si switches with SiC devices can raise the power density of a CSI from 17 to 25 kW/L.

Beyond electrical performance, the high thermal conductivity and elevated junction temperature tolerance of WBG materials improve CSC thermal management. Lee et al. [178] show that combining high thermal conductivity with WBG characteristics allows for optimized thermal design, yielding a smaller and lighter cooling system. Moreover, the symmetrical lateral structure of WBG power devices enables highly integrated topologies. For instance, Torres et al. [179] report the use of dual-gate monolithic bidirectional GaN switches in CSI-based integrated motor drives, enabling a monolithic four-quadrant switch with reverse-current and reverse-voltage blocking capability. This design removes the need for series diodes in conventional CSIs, thereby reducing conduction losses and improving topological efficiency.

With continued advances in WBG materials, device technology, and integration, CSCs are expected to achieve higher efficiency, power density, and reliability. Although challenges related to cost and device reliability remain, WBG semiconductors are poised to play a critical role in enabling the next generation of CSCs, particularly for bidirectional power transfer applications. The commercialization of monolithic bidirectional GaN switches is anticipated to further accelerate the adoption of CSC technology.

2) Soft-Switching Strategies: Soft-switching techniques have been extensively investigated in power electronic converters [180]. However, compared with VSCs and dc–dc converters, systematic studies on CSCs soft-switching remain relatively limited. Nonetheless, the research community has actively explored the feasibility of CSC soft-switching through two main approaches: auxiliary circuit technology and the optimization of modulation strategies.

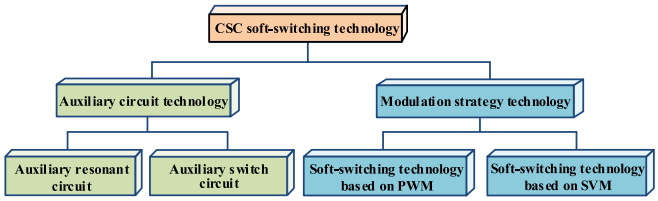

Fig. 37. CSC soft switching technology classification diagram.

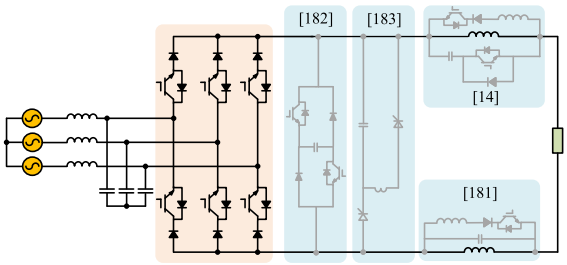

Fig. 38. Topology of auxiliary resonant circuit.

For CSCs, the core technique for achieving soft switching is to employ external auxiliary circuits or optimized modulation strategies to ensure that, at the critical switching instants (prior to turn-ON or turn-OFF), either the voltage across the power device or the current flowing through it is reduced to zero and maintained stably. By avoiding the overlap between voltage and current during device turn-ON and turn-OFF, switching loss can be effectively eliminated. As shown in Fig. 37, topology-based approaches to achieving soft switching in CSCs can be broadly divided into two categories: resonance-based circuits and switch-based circuits. Among them, auxiliary-circuit-based methods achieve soft switching by incorporating an auxiliary resonant network into the dc bus, as shown in Fig. 38. For instance, Xu et al. [14] propose inserting an auxiliary resonant circuit into the dc-link, where the auxiliary switch is turned ON at the end of each switching cycle to initiate resonance. This process resets the capacitor voltage according to a cosine profile, ensuring that the voltage across the CSC main switch falls to zero before the next conduction interval, thereby achieving ZVS. Similarly, Mauger et al. [181] realize ZVS with a resonant circuit comprising fewer components, further simplifying the implementation. Auxiliary circuits can also be configured as parallel branches. As reported in [182] and [183], a resonant branch is connected in parallel with the dc bus and coordinated with dedicated switching strategies. The resonance between the branch inductor and capacitor establishes ZVS conditions for the CSC main switches, thereby reducing switching losses and improving overall efficiency.

Soft-switching strategies based on switch topologies are predominantly implemented using the H7 CSC, as shown in Fig. 39. For example, Kumar and Yadav [184] propose an integrated soft-switching scheme for the H7 CSC, in which the seventh switch is used to insert a zero state during each switching transition, thereby achieving ZCS and reducing conduction losses during zero-state intervals. Although the H7 topology is effective, it requires a large number of gate signals and a relatively complex

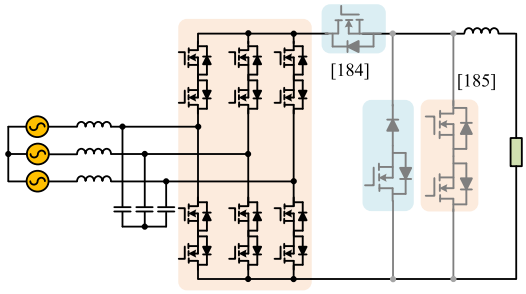

Fig. 39. Topology diagram of auxiliary switch circuit.

gate-drive circuit. To address this, Dai et al. [185] introduce the H8 topology, which reduces the gate-signal count by requiring only one gate signal and driver per bridge-arm switch, while maintaining the soft-switching capability and low gate-driver voltage overshoot of the H7 topology.

Auxiliary-circuit-based techniques, owing to their stable performance, are well suited for high-power applications. However, they add circuit complexity and cost, and the auxiliary branches themselves may introduce additional losses. In contrast, modulation-based soft-switching strategies require no extra resonant components, feature simpler structures, reduce switching losses, and are particularly suitable for high-frequency applications, thereby facilitating passive component downsizing [186], [187]. In [186], a pulsewidth modulation (PWM) scheme is proposed for soft commutation in three-phase CSCs, wherein the collector–emitter voltage of the input switch remains positive and that of the output switch remains negative during commutation, enabling natural soft commutation. Bai et al. [187] further present a SVM-based strategy that designs the switching vector sequence within a closed-loop control framework, achieving soft switching of all devices across the full power-factor range.

It can be observed that resonant networks, auxiliary switch circuits, and modulation strategies can effectively eliminate voltage–current overlap, thereby achieving zero-voltage or ZCS. Future research may focus on topology innovation and modulation optimization to realize full-range soft switching with minimal or no hardware modifications.

VI. Future Trends and Challenges

In Sections III–V, the various topologies, modulation schemes, and control strategies of CSCs are summarized, and their advantages and shortcomings are discussed. Then, for the key technical problems in the practical application of CSCs, the latest solutions are reviewed and analyzed, highlighting their industrial presence and recognized maturity. However, significant research gaps still remain for further development of CSCs. The trends and challenges are discussed in this section.

1) Further Development of Operations Under Unbalanced or Distorted Grids/Loads: In three-phase power systems, unbalances in input phase voltages are usually caused by single-phase loads or asymmetric line impedances. This results in input current distortion and a large amount of reactive input power in the three-phase rectifier. In addition, when the CSC operates under unbalanced grid conditions, to ensure the quality of the input

current waveform, the instantaneous power of the CSC will have twice the line-frequency pulsation. The current control scheme faces challenges such as complex control and a limited range of ac input frequencies. Therefore, further research is needed in the future on simplifying the control structure, achieving flexible adjustment of active and reactive power, and a wide range of input frequencies.

2) Further Development of CSC Topology With Small DC-Link Inductor: The CSC topology with a small dc-link inductor may represent a key direction for the future development of CSCs. The inductor is one of the most critical components. To achieve a constant current, the inductor value is usually large, which increases system volume, losses, and cost, while reducing efficiency and stability. Therefore, research on CSCs with small inductors may be a promising direction. The main issue caused by a small dc-link inductor is increased current ripple. Currently, for dc-link inductor current ripple suppression, the main objective is to reduce the voltage variation across the inductor. However, this approach is sensitive to the inductor value, which is typically assumed constant. Obviously, under varying operating conditions, such as different switching frequencies and temperatures, the inductor value may deviate from the nominal value, causing some existing ripple suppression methods to fail. Therefore, developing ripple suppression schemes that are insensitive to inductor variations may constitute an important research direction in the future.

3) Further Development of CSC Topology With Transformer-Less Configurations: In industrial applications, CSC with transformer is often used for motor systems. The functions of transformer are electrical isolation, CMV reduction, and leakage current suppression. The motor drive system with transformer has the disadvantages of large volume, cost and low efficiency. Therefore, the motor drive system without transformer may be a trend. However, due to the absence of transformer, the CMV may cause poor insulation of the motor system and shorten its service life. So, the CMV suppression is a key focus in the CSC without transformer. At present, to reduce the CMV, on one hand, only a part of the vector with constant CMV is used, which causes low dc utilization and narrow modulation index. On the other hand, the CMV can be suppressed by some special vector sequence. However, this method increases the computational complexity and switching loss. Therefore, in the future, the CMV amplitude and average suppression strategies with high dc utilization, wide modulation index and simple implementation process may be focused in the CSC.

4) Further Development of CSC Efficiency and Power Density Improvement: In fields such as aerospace power systems and integrated motor drives, high-frequency and compact CSCs based on WBG devices and soft-switching techniques are expected to become a key development direction. Conventional Si-based CSCs suffer from high switching losses, bulky passive components, and challenging thermal design at high frequencies, which limit further improvements in efficiency and power density. Therefore, for more compact and efficient applications, it is necessary to investigate high-frequency CSCs that leverage WBG device technology in coordination with soft-switching strategies. Currently, WBG semiconductors are rapidly advancing, offering higher breakdown voltages, higher switching frequencies, lower switching losses, and superior thermal stability. However, most existing soft-switching research on CSCs still relies on resonant circuits to assist in achieving ZCS or ZVS. Consequently, exploring how to fully exploit state-of-the-art WBG devices in CSCs and achieve full-range soft switching with little or no additional hardware may represent an important direction for future research.

VII. Conclusion

This article has presented an overview of recent advancements in CSCs. First, the industrial applications and advantages of CSC are summarized and analyzed, covering EVs, more-electric aircraft, uninterruptible power supplies, STATCOMs, ac motor drives, etc. In addition, the classical topologies, modulation, and control strategies of CSCs are reviewed, and their advantages and disadvantages are analyzed. Furthermore, four key technical problems in the practical application of CSCs—covering unbalanced grid voltage conditions, dc-link inductor current ripple suppression, CMV suppression, and efficiency and power density improvement—along with their latest solutions and related publications, are summarized and analyzed. Finally, future trends and challenges of CSCs are presented. In summary, we hope this article can serve as a handy resource and be helpful for the development of CSCs as a potential alternative to well-known VSC systems.

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