A Temperature-Compensated, Low-Power, Microsecond-Response Power Gating Circuit With Triple-Mode Overload Protection

Jingbin Feng, Qiuzhen Xu, Khalil Yousef, *Member, IEEE*, Pengda Qu, Yue Zhao, and Zhiming Xiao, *Member, IEEE*

***Abstract*—This article presents a power gating circuit with triple-mode overload protection, which can be integrated into low -ower charger or regulators for interface protection. It can respond in tens of microseconds while consuming 0.8 μA quiescent current under low-power mode conditions. A voltage-to-resistance converter is proposed to generate a resistance inversely proportional to the input supply voltage for setting the overload threshold. A temperature compensation mechanism is also integrated to maintain overload threshold deviations within ±2% over the −40 to 125 °C range. The mode control logic implements an auto-recovery function that automatically reconnects the power gating path after the overload condition clears. Fabricated in 0.18-μm Bipolar CMOS and DMOS (BCD) technology, the design operates over a 5–40 V range with an area of 0.35 mm^2, achieving an RDSON of 600 mΩ for the integrated power switches. For over-power protection (threshold: 1.2 W), the power conduction path is turned off with a response time of 17 μs under an abrupt 3 W power surge. For over-current protection (threshold: 106 mA), the path is shut down within 12 μs upon an abrupt 300 mA load current surge. For over-voltage protection (threshold: 24 V) for an abrupt voltage transition from 10 to 40 V, the conduction path is cut off within 1 μs via slope detection.**

***Index Terms*—Current limiting, power gating (PG), power limiting, temperature compensation, voltage limiting.**

I. Introduction

POWER conversion modules are susceptible to over-voltage, over-current, and over-power threats that may lead to severe damages such as dielectric breakdown, conduction fusing, or thermal runaway. Power-gating circuits play a pivotal role in power management systems through real-time overload detection and protection [1], [2], [3]. These circuits effectively safeguard various power management modules and electronic devices, such as low-dropout regulators [4], [5], [6], switching regulators [7], hot-swap controllers, servers, and battery energy storage systems [8], [9].

Power gating (PG) protection circuits have undergone continuous refinement to address the growing complexity of modern integrated circuit systems. Early PG protection relied on passive components such as fuses [10], metal-oxide varistors [11], and bimetallic thermal relays [12]. While effective against abrupt overvoltage transients such as surges, these solutions were limited by slow millisecond-scale response times, poor precision (with variations exceeding 10%), and nonrecoverable operation. With advancements in integrated circuits, integrated PG mechanisms have become the mainstream. Zener diodes, for instance, leverage picosecond-scale over-threshold responses to achieve voltage clamping [13], [14]. However, diodes exhibit thresholds with significant temperature and process variations. Resistive divider networks with high-speed comparators can attain <3% voltage detection accuracy but consume substantial power loss (>50 μA quiescent currents for microsecond-scale responses) [15]. Resistor-based [16], [17] and MOSFET on-resistance (R_{DS})-based [18] current-sensing circuits enable high-precision over-current detection. However, the former occupies a large PCB footprint, while the latter suffers from pronounced temperature drift (typically ±0.3% /°C). Digital solutions [19], [20] that employ analog to digital converters (ADCs) to convert voltage/current signals for digital analysis can provide timely PG protection. However, implementing power detection (I×V) requires multiplier units, which increases design complexity, cost, and area.

Despite continuous advancements in power-gating protection circuits, the aforementioned approaches present several persistent challenges. First, single-mode PG protection fails to address diverse catastrophic overload scenarios, whereas multimode architectures incur penalties in terms of increased area and power consumption. Second, balancing detection precision and power efficiency remains a critical challenge. Third, achieving both high-speed detection and low-power consumption constitutes an inherent tradeoff. To address these limitations, the proposed circuit detects over-current, over-power, and over-voltage conditions with a shared

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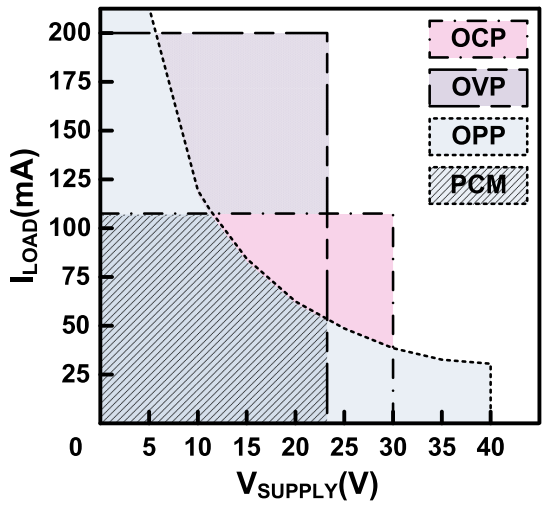

Fig. 1. Safe work areas for the proposed PG structure.

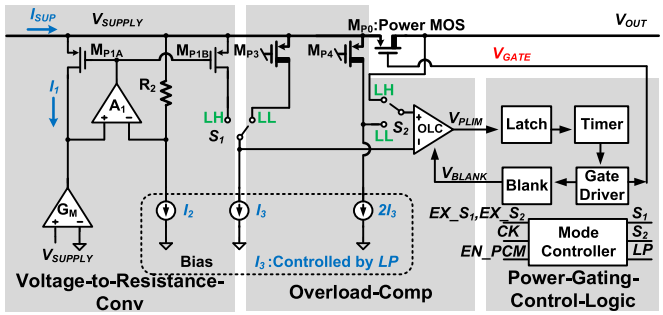

Fig. 2. Block diagram of the proposed PG circuit.

TABLE I
PG OPERATING MODE

Mode	S_1	S_2	LP
OPP	LH: Logic High	LH: Logic High	LL: Logic Low
OVP	LH: Logic High	LL: Logic Low	LL: Logic Low
OCP	LL: Logic Low	LH: Logic High	LL: Logic Low
LPM	LL: Logic Low	LH: Logic High	LH: Logic High

sense-and-comparison circuit with multioperation modes. In high-current sensing mode, the system operates in a cyclic protection sequence of OCP→OPP→OVP→OCP to prevent permanent device damage. In low-power mode (LPM, load current <22 mA), the protection circuit enters an ultra-low-power state (drawing only 0.8 μA), monitors basic current and rapid voltage transients, and instantly restores full detection capabilities upon detecting an anomaly. This hierarchical architecture cuts standby power consumption by over 95% via dynamic power management while balancing reliability and energy efficiency for modern low-power power electronics.

The proposed scheme is configurable and features four operational conditions: over-power protection (OPP), over-current protection (OCP), over-voltage protection (OVP), and a periodic cycling mode (PCM) that sequentially switches between states in the order LPM→OCP→OPP→OVP→LPM. The architecture is self-contained and requires no additional reference generation circuits or off-chip resistors. As illustrated in Fig. 1, each mode has clearly defined operational boundaries, where overlapping regions represent the safe operating area under normal conditions. This structure can be directly integrated into existing power delivery paths to provide either single-mode or triple-mode overload protection.

This article is organized as follows: Section II introduces the PG technique; Section III presents the transistor-level implementation of the proposed PG circuit; Section IV lists and discusses the design considerations; Section V provides and analyzes the measurement results; and Section VI concludes the article.

II. PROPOSED PG TECHNIQUE

The proposed PG protection circuit employs a detection architecture based on the MOSFET on-resistance ($R_{\mathrm{DS\cdot ON}}$). As shown in Fig. 2, the circuit is primarily composed of four components: a voltage-to-resistance converter (VRC), an overload comparator (OLC), a PG logic circuit, and a bias circuit. The VRC generates a reference for the overload threshold, which is the inverting input of the comparator. By combining this with the comparator's noninverting input, the circuit can implement over-power and over-voltage protection functions. Over-current protection is enabled by routing the OLC's inverting input to the drain of $\mathrm{M_{P3}}$ and connecting its noninverting input to V_{OUT}. Upon detecting an overload condition, the PG logic turns off the power transistor $\mathrm{M_{P0}}$ immediately. After a predefined interval, the circuit rechecks if the overload condition has been resolved. Throughout the entire operational process, the bias circuit provides the corresponding bias currents based on the selected mode.

Table I shows how different modes are set via the logic levels of S_1, S_2, and LP. PCM operation is enabled by the periodic toggling of input clock CK and a logic-high level on EN_PCM. The OLC, bias circuit, and PG logic circuit are multiplexed across all protection modes (OCP, OPP, OVP, and PCM). In over-power detection mode, the product of the power switch's current (I_{SUP}) and voltage (V_{SUPPLY}) is sensed and compared. When both S_1 and S_2 are at a logic-high level and LP is at a logic-low level, the noninverting input of the OLC is connected to the drain of power MOSFET $\mathrm{M_{P0}}$, and its inverting input is connected to the drain of $\mathrm{M_{P1B}}$. The source terminals of $\mathrm{M_{P0}}$ and $\mathrm{M_{P1B}}$ are both connected to V_{SUPPLY}. Thus, the comparator switches state when

$$R_{MP0} \cdot I_{\mathrm{SUP}} = V_{\mathrm{DS\_}MP1B} = R_{MP1B} \cdot I_3 \quad (1)$$

where R_{MP0} denotes the on-resistance of M_{P0}. Power comparison is achieved by configuring the voltage drop $V_{\mathrm{DS\cdot}MP1B}$ to be inversely proportional to the supply voltage V_{SUPPLY}. Therefore, $\mathrm{M_{P1B}}$ is a mirrored device of M_{P1A}. Operated in deep triode region via the negative feedback loop of amplifier A_1, it satisfies

$$R_{MP1A} = R_{MP1B} \quad (2)$$

$$I_1 \cdot R_{MP1A} = I_2 \cdot R_2 \quad (3)$$

$$I_1 = G_M \cdot V_{\mathrm{SUPPLY}}. \quad (4)$$

Based on (2), (3), and (4), R_{MP1B} exhibits an inversely proportional relationship with V_{SUPPLY}

$$R_{MP1A} = R_{MP1B} = I_2 \cdot R_2 / (G_M \cdot V_{\mathrm{SUPPLY}}). \quad (5)$$

By combining (1) and (5), the threshold for over-power mode is derived as

$$P_{\mathrm{TH}} = I_2 \cdot R_2 \cdot I_3 / (R_{MP0} \cdot G_M). \quad (6)$$

Thus, the over-power protection function for P_{TH} is achieved by leveraging R_{MP1B}, V_{SUPPLY}, and the on-voltage of M_{P0}.

For over-voltage detection, the circuit extracts the V_{SUPPLY} signal and compares it against a threshold. When S_1 is at a logic-high level and both S_2 and LP are at a logic-low level, the noninverting input of the OLC is connected to the drain of M_{P4}, and its inverting input is connected to the drain of M_{P1B}. The switching threshold here is given by

$$V_{\mathrm{DS\_}MP1B} = V_{\mathrm{DS\_}MP4} = 2 \cdot R_{MP4} \cdot I_3. \quad (7)$$

Based on the analysis above (5), $V_{\mathrm{DS}\cdot MP1B}$ is given by

$$V_{\mathrm{DS\_}MP1B} = I_2 \cdot R_2 \cdot I_3 / (V_{\mathrm{SUPPLY}} \cdot G_M). \quad (8)$$

Thus, the over-voltage threshold is given by

$$V_{\mathrm{TH\_SUP}} = I_2 \cdot R_2 / (2 \cdot R_{MP4} \cdot G_M). \quad (9)$$

Equation (9) demonstrates that the over-voltage protection threshold $V_{\mathrm{TH}\cdot\mathrm{SUP}}$ is achieved by leveraging the inverse relationship between $R_{\mathrm{DS}\cdot\mathrm{MP1B}}$ and V_{SUPPLY}. $V_{\mathrm{TH}\cdot\mathrm{SUP}}$ is set by a constant bias current.

In over-current detection mode, the circuit senses the current I_{SUP} through M_{P0} and compares it against a threshold. When both S_1 and LP are at a logic-low level, and S_2 is at a logic-high level, the noninverting input of the OLC is connected to the drain of M_{P0}, and its inverting input is connected to the drain of M_{P3}. Thus, the switching threshold is given by

$$I_{\mathrm{TH\_SUP}} = R_{MP3} \cdot I_3 / (R_{MP0}). \quad (10)$$

Both M_{P3} and M_{P0} operate in the deep triode region, with their on-resistance ratio remaining constant. Given that I_3 is a fixed value, the over-current threshold is achieved.

When S_1 is at a logic-low level, and both S_2 and LP are at a logic-high level, the proposed circuit operates in LPM. By reusing the OLC, precise protection thresholds across four operational modes are achieved.

The thresholds defined by (2)–(10) are susceptible to random device mismatches and temperature drift, which affect their threshold accuracy and chip-to-chip consistency. The proposal design incorporates a trimming scheme for chips process variations and device mismatch. Fine-tuning of these thresholds is accomplished by adjusting the dc level profiles of their respective bias currents (I_1, I_2, and I_3). Additionally, for large-scale proportional scaling of the thresholds without disturbing the dc operating point, the primary method involves adjusting the ratios of key resistors while maintaining a constant quiescent current. For example, if OPP thresholds are scaled to double, then resistance R_{MP0} for P_{TH} is halved, resulting in an approximate doubling of its V_{GS} parasitic capacitance. Thus, the gate driving capability must also be doubled to maintain the signal propagation delay at the submicrosecond level.

III. Transistor Level Implementation

The transistor-level design of the proposed PG circuit is shown in Figs. 3–6. Specifically, Fig. 3 depicts the voltage-to-resistance conversion circuit and the OLC. Fig. 4 demonstrates the low-power, high-speed level-shifting control circuit. Fig. 5 presents the PG control logic circuit, and Fig. 6 illustrates the bias circuit. In Fig. 3, MOS devices with thicker drain terminals are 45 V high-voltage FETs, while others are 5 V low-voltage devices.

A. VRC Circuit

Existing VRC implementations face certain limitations: for instance, the design in [21] requires multiple amplifiers, and the design in [22] adjusts the gate voltage through capacitor coupling, which raises concerns of leakage and noise; while [23] offers only limited input voltage ranges and adjustable resistance ranges. In contrast, the proposed VRC employs an architecture that consumes only tens of microamps of quiescent current, achieving an inverse relationship with the supply voltage over a wide input range of 5–40 V and a typical 550 kHz gain bandwidth (GBW).

As shown in Frame 2, by applying Kirchhoff's Current Law, the current through M_{P2} is I_2. As shown in Frame 3, by clamping the drain voltages of M_{P2} and M_{P1A} with M_{P6A} and M_{P6B}, respectively, the amplifier A_1 in Fig. 2 is realized. AC simulation analysis shows that amplifier A_1 exhibits a typical dc loop gain of 55 dB. The minimum dc loop gain is 49 dB under the FF process corner, -40 °C, and $V_{\mathrm{SUPPLY}} = 40$ V. Meanwhile, the minimum phase margin is 75° at the SS process corner, 125 °C, and $V_{\mathrm{SUPPLY}} = 5$ V. The V_{DS} voltages of M_{P2} and M_{P1A} are equal to the product of I_2 and R_{MP2}. After clamping the voltage across the active resistor of R_{MP1A}, its current is further regulated to be proportional to the supply voltage.

A negative feedback loop formed by M_{N0} and M_{N1} generates a current of V_{GSMN0}/R_{0A}, which is mirrored and flows into M_{NBN1}. With $R_0 = R_{0A} = R_{0B}$ and M_{N0} and M_{NBN1} having equal aspect ratios, their currents are nearly equal, approximating $\mathrm{V_{GSMN0}} = V_{GSMNBN1}$ and thus yielding a current proportional to V_{SUPPLY}

$$I_1 = V_{\mathrm{SUPPLY}} / R_0. \quad (11)$$

Thus, the resistance of R_{MP1A} is inversely proportional to the supply voltage.

M_{P1B} and M_{P1A} have identical dimensions and equal V_{GS} voltages, given that M_{P1A} operates in the deep triode region. Thus, if the current through M_{P1B} is ensured to be smaller than that through M_{P1A}, $V_{\mathrm{DS}\cdot MP1B}$ will be much smaller than $V_{DSAT\cdot MP1B}$, allowing M_{P1B} to be approximated as equivalent to M_{P1A}. Consequently, the resistance R_{MP1B} is inversely proportional to the supply voltage.

B. OLC Circuit

The OLC design circuit is shown on the right side of Fig. 3, with Frame 4 illustrating the input selection for the OLC circuit. The circuit operates in OPP mode when M_{P1B} and M_{P5} are gated, in OVP mode when M_{P1B} and M_{P4} are gated, and in OCP and LPM modes when M_{P3} and M_{P5} are gated.

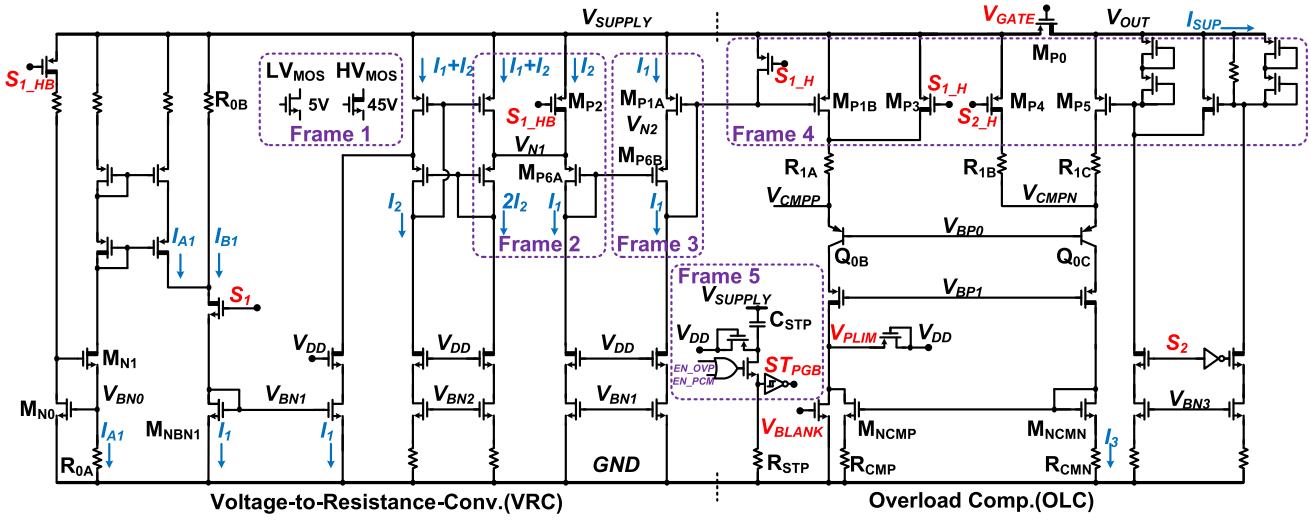

Fig. 3. Schematic of VRC and OLC.

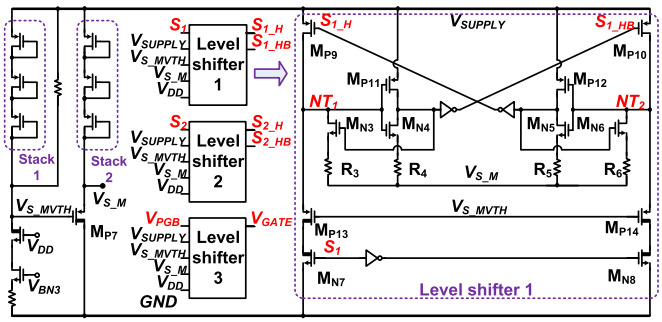

Fig. 4. Low-power and high-speed level-shifting control circuit.

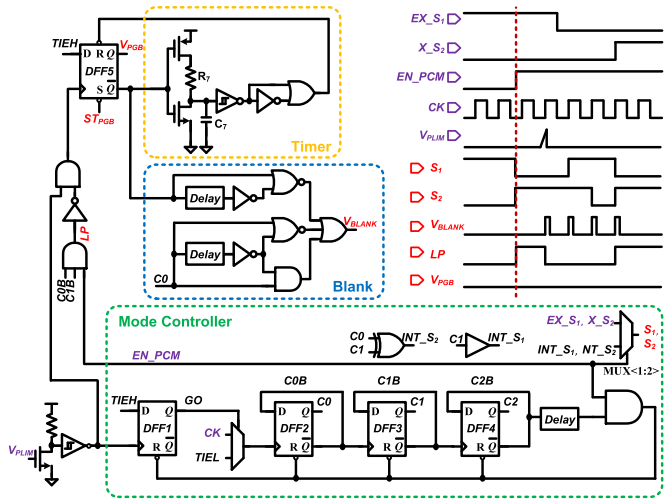

Fig. 5. PG control logic.

Subsequently, the input signal is routed to the emitter of the common-base PNP transistor via either R_{1A} and R_{1B} or R_{1C}. The resistance values of R_{1A}, R_{1B}, and R_{1C} follow the relationship of $R_{1A} = 2\times R_{1B} = 2\times R_{1C}$. In any of the three overload protection modes (OPP/OVP/OCP), these resistors

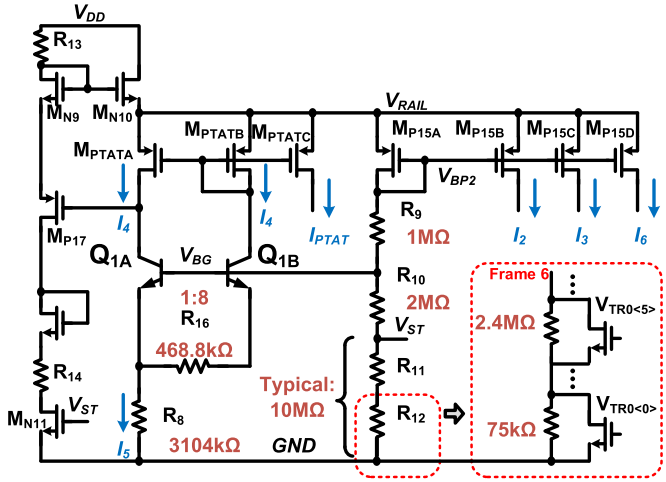

Fig. 6. High-precision, zero-temperature-coefficient trimmable bandgap reference.

function as current limiters. Additionally, R_{1A} ensures that the drain-source voltage (V_{DS}) of M_{P1B} remains within a safe range.

Common-base bipolar transistors are used as the input stage, offering a faster current response than MOSFETs structure. With an input current as low as the hundreds of nanoamperes, the comparator can achieve detection in the microsecond range. Under high-temperature and high-voltage conditions, the leakage current induced by the parasitic PNP structure in the common-base bipolar structure is within 5 nA. Compared with the 300 nA bias current, the impact of this leakage current is nearly negligible. The current-limiting resistor R_{1A}, clamp circuitry, and high-voltage cascode PMOS devices work together to ensure that the collector-emitter voltages (V_{CE}) of the PNP transistors never exceed 5 V under all operating conditions.

In the output stage, a resistor with higher matching precision is connected in series with the source of the load MOS to suppress random deviations in the transconductance (G_M) of the MOS. The output signal V_{PLIM} will be close to the threshold voltage

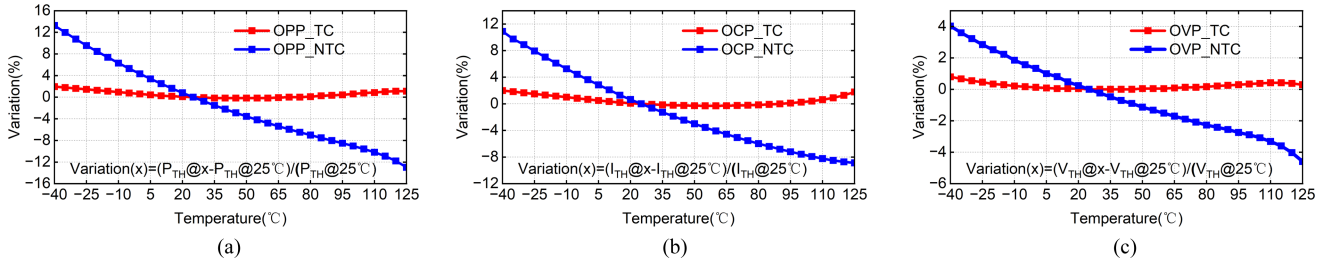

Fig. 7. Temperature coefficient of thresholds for the power gating circuit. (a) OPP mode at 40 V. (b) OCP mode at 40 V. (c) OVP mode.

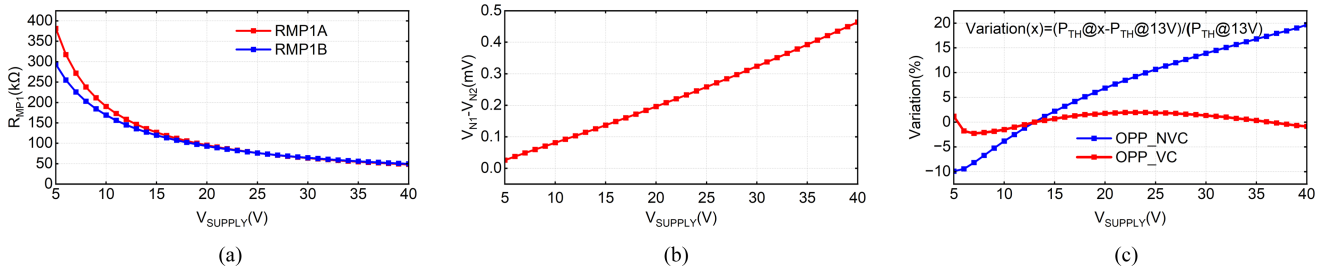

Fig. 8. Parameters of the VRC in OPP mode. (a) R_{MP1A} and R_{MP1B} are the resistor inversely proportional to the power supply. (b) V_{N1} and V_{N2} achieve virtual short-circuit through the $\mathrm{M_{P6A}}$ and $\mathrm{M_{P6B}}$ in Fig. 3. (c) The curves of OPP threshold varying with voltage with and without voltage compensation.

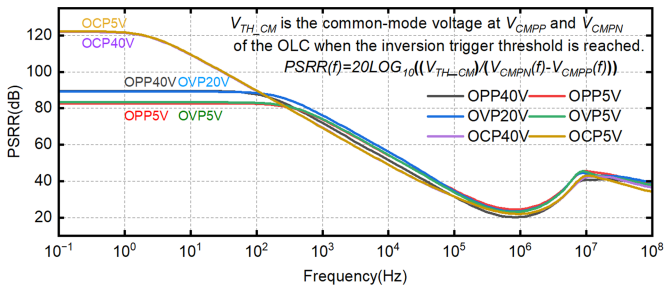

Fig. 9. PSRR at the comparator input.

(V_{TH}) of an NMOS. Therefore, the subsequent NMOS stage ensures the detection accuracy and speed. It should also be noted that a V_{SUPPLY} voltage slope detection circuit is added to the OLC and enabled in OVP or PCM, as shown in Frame 5. When the V_{SUPPLY} voltage surges high, it simultaneously pulls the $\mathrm{ST_{PGB}}$ voltage low to enable overload protection. To prevent the V_{PLIM} voltage from exceeding the safe range due to the rapid rise of V_{SUPPLY}, a diode-connected PMOS transistor is connected from V_{DD} to V_{PLIM} for voltage limiting.

The adoption of large-area devices (R_{1A}, R_{1B}, R_{1C}, R_{CMP}, R_{CMN}, Q_{0B}, and Q_{0C}), long-channel devices (M_{P1B}, M_{P3}, M_{P4}, M_{P5}, M_{PCMP}, M_{PCMN}), and precise layout matching can effectively reduce the inherent offset voltage of OLC.

C. High-Voltage Level-Shifting Circuit

Traditional zero-quiescent-current level-shifting circuits primarily include two typical types: the current-mirror level shifter and the direct-coupled level shifter [24]. However, when converting a 1 MHz clock signal from 3.3 to 40 V, their average current consumption exceeds 10 μA. Another structure proposed in [25] reduces power consumption in level-shifting circuits, but it may suffer potential transition failure under the FS process corner. So, this design added a biasing circuit based on [25] as shown in Fig. 4. A nanoampere-scale current is sunk from three diode-connected PMOS transistors in Stack 1 to generate a reference signal $V_{S\_MV\mathrm{TH}}$, which is 3 V_{TH} (with an average $V_{\mathrm{TH}} = 1.3$ V) below V_{SUPPLY}. Thus, the upper threshold of $V_{S\cdot M}$ is V_{SUPPLY} - 2 V_{TH}, whereas the lower threshold is V_{SUPPLY} - 3 V_{TH}. These voltage levels ensure sufficient voltage margin for all process corners and rapid transition.

When the PG circuit switches from OCP mode to OPP mode, the S_1 signal switches from a logic low level to a logic high level and is transmitted to the high-voltage domain through the high-voltage level-shifting circuit. First, when S_1 transitions from low to high, considering the previous $S_{1\cdot H}$ state of $V_{S\cdot M}$, the on-resistances of M_{P13} and M_{N7} are significantly lower than those of M_{P9}, enabling rapid discharge of NT_1 to $V_{S\cdot M}$. Second, the feedforward loop composed of M_{P11}, M_{N3}, and resistor R_4 accelerates the falling edge of NT_1, forcing $S_{1\cdot HB}$ to transition synchronously to $V_{S\cdot M}$. Third, the on-resistance of M_{P10} is much lower than the series impedance of M_{N6} and R_6, ensuring that NT_2 rapidly charges to V_{SUPPLY} and completes the level shifting. Upon completion of the conversion, the level shifter consumes nearly zero static power. Owing to the fully symmetric architecture, the reverse transition of switching from OPP mode to OCP mode (S_1 from logic high to low) mirrors the aforementioned process. Similarly, the logic for transmitting the levels of S_2 and V_{PGB} to the high-voltage domain is the same.

D. PG Control Logic Circuit

Fig. 5 illustrates the mode switching with reconnection trials. Mode selection and mode switching are primarily determined by the *EN_PCM* signal. When the *EN_PCM* is at a logic low

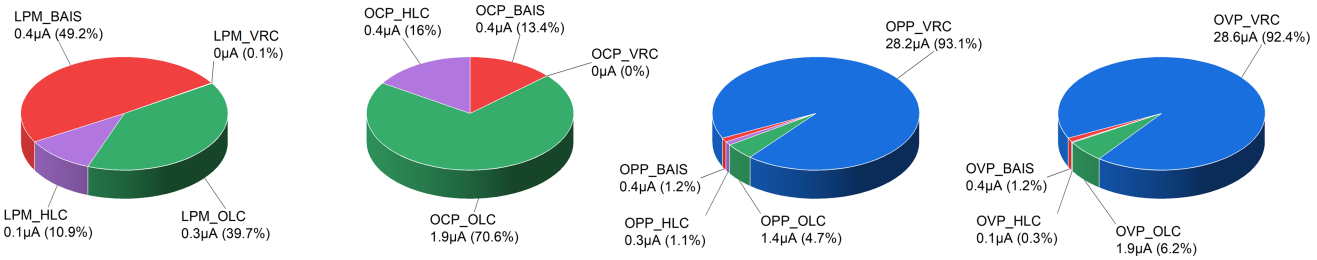

Fig. 10. Current contribution diagrams of Bais, VRC, OLC, and HLC under different modes with a 40 V power supply.

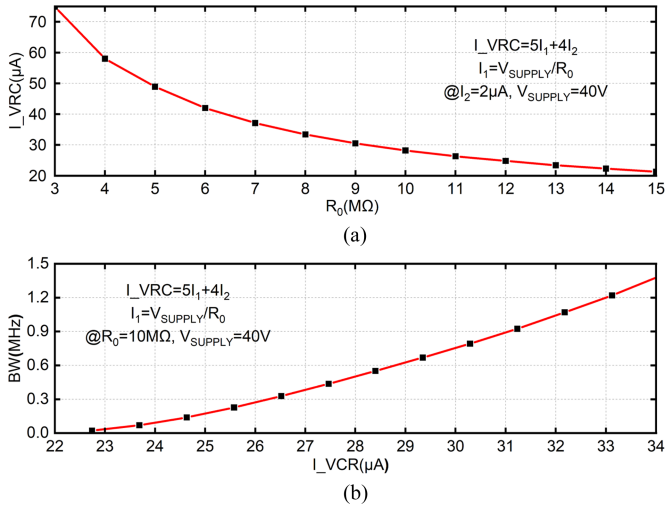

Fig. 11. Power consumption analysis of the VRC. (a) Current of the VRC versus the resistance of R_0. (b) Bandwidth of the VRC versus the current consumption.

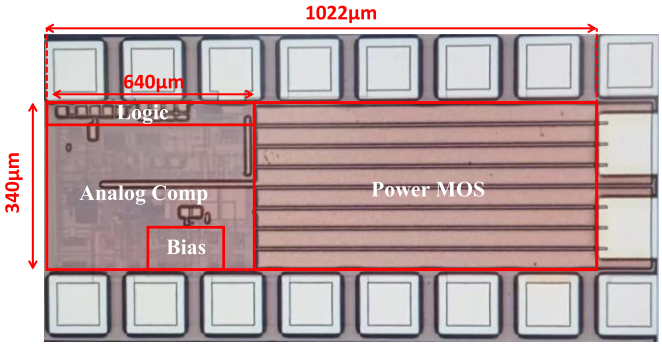

Fig. 12. Die micrograph.

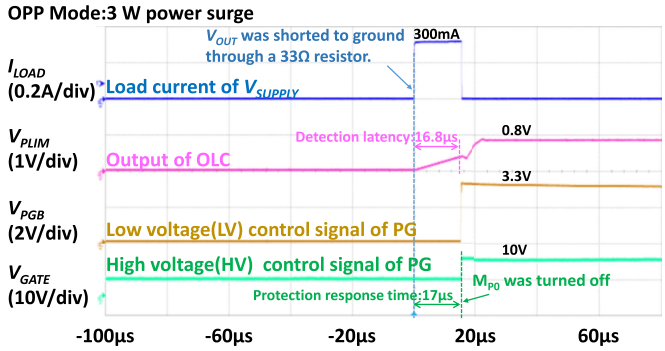

Fig. 13. Measured waveforms during over-power transient with a sudden 3 W power surge.

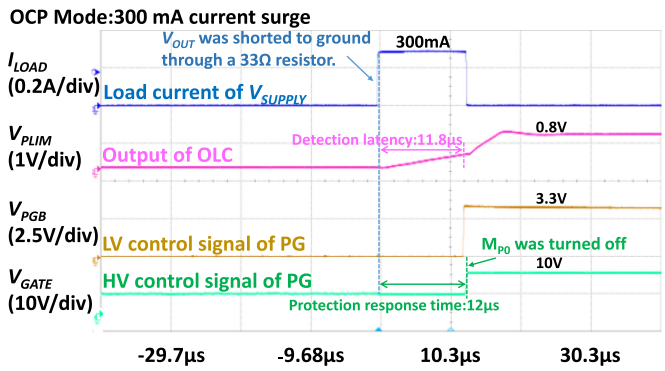

Fig. 14. Measured waveforms during over-current transient with a sudden 300 mA current surge.

level, the multiplexers (MUX<1:2>) gate the externally input EX_S_1 and EX_S_2 to control S_1 and S_2. The circuit can enter OCP, OPP, and OVP modes. When the *EN_PCM* is at a logic high level, the circuit enters PCM mode.

In PCM mode, when OLC is triggered, the mode controller determines the logic levels of signals S_1, S_2, and *LP*, enabling the circuit to switch sequentially among OCP, OPP, and OVP modes by the 32 kHz clock *CK*. To prevent mode-switching crosstalk and false triggering, a 5 μs blanking time resets the comparator's output (V_{PLIM} to GND) and inputs (V_{CMPP} / V_{CMPN} to V_{SUPPLY}), ensuring full readiness of the OLC and VRC. If the OLC does not trigger V_{PLIM} high, the circuit will remain in LPM mode.

In OCP, OPP, and OVP modes, triggering an over-threshold event initiates overload protection and trial reconnection. D flip-flop 5 (DFF5) assumes the function of the latch in Fig. 2 owing to its synchronous control capability and high reliability. The signal V_{PGB} of DFF5 is transmitted to the high-voltage domain via the high-voltage level-shifting circuit (HLC) circuit to turn off M_{P0}. A time-delay circuit with R_7 and C_7, and a Schmitt trigger enable M_{P0}'s reconnection function. This reclosing mechanism was selected for its straightforward behavior, aligning with the standard approach for protecting against overload conditions as documented in [26] and [27]. Specifically, the fixed-interval reclosing time is conservatively set based on

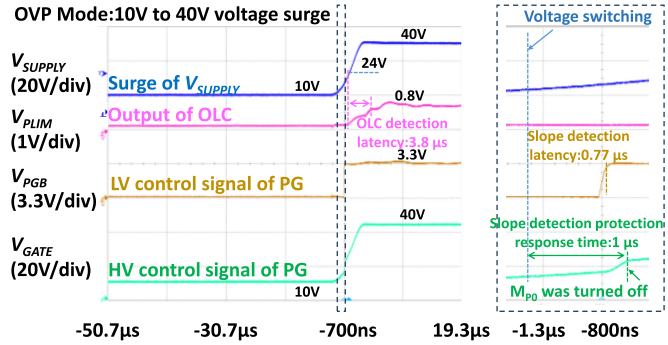

Fig. 15. Measured waveforms during over-voltage transient with a sudden 40 V voltage surge.

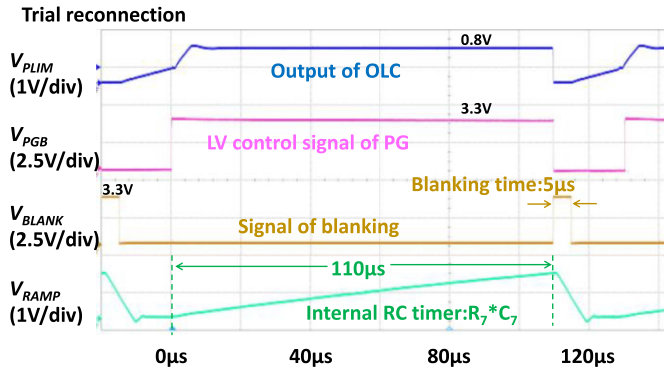

Fig. 16. Measured the details of trial reconnection.

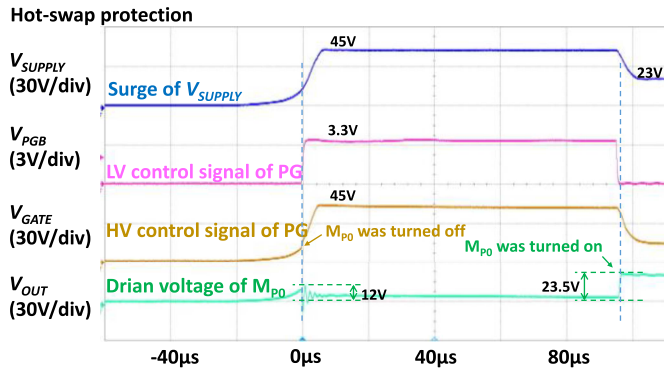

Fig. 17. Measured the hot-swap protection test.

worst-case thermal simulation results, ensuring that even under a high-power fault, the energy dissipated in the power switch during the fast-reclosing attempt remains within its absolute maximum ratings.

In PCM mode, the delay latency for triggering an OVP surge event is from 4 to 75.5 μs. The worst-case delay latency consists of a maximum time of approximately 4 μs for an over-threshold event occurring before the end of OVP mode without V_{PGB} signal reversal, 62.5 μs (time to complete the OCP and OPP monitoring phases), a 5 μs blanking period, and an intrinsic 4 μs OVP response delay. However, if the slew rate of V_{SUPPLY} exceeds 0.02 V/μs, the over slope detection (in Fig. 3, Frame 5) will be triggered, and M_{P0} will be turned off after a 1 μs delay. In summary, if slope detection is not triggered, the voltage may rise by approximately 1.5 V after an OVP event. The response delays for OPP and OCP are from 17 to 101.5 μs and from 12 to 91.5 μs, respectively.

E. Bandgap Reference Circuit

Fig. 6 shows a high-precision, zero-temperature-coefficient, trimmable bandgap reference with autonomous start-up, consuming 0.4 μA. During the power-on process from 0 to 3.3 V, when V_{DD} rises above V_{TH}, M_{N10} turns on, and V_{BG} and V_{ST} start to rise. As V_{DD} continues to increase, M_{N11} is activated. When V_{DD} exceeds V_{BG} + 2 V_{TH}, M_{P17} and M_{N9} turn on, establishing the global negative feedback loop. V_{BG} stabilizes at approximately 1.2 V, with no degeneration points encountered during this process. The start-up time of the bandgap reference is correlated with the power-on ramp speed (achieving microsecond-level performance) and maintains stability across all process corners. During this process, both internal current and voltages are under control within a safe-operating region.

Negative feedback combined with drift cancellation ensures that V_{BG} has a temperature coefficient of approximately 20 ppm/°C. The current through M_{P15A} is the bandgap voltage (V_{BG}) divided by the sum of the zero-temperature-coefficient resistors R_{10}, R_{11}, and R_{12}. Currents I_2, I_3, and I_6 are trimmed via R_{12} to compensate for resistor process variations and enable threshold adjustments across OPP, OCP, and OVP modes.

A proportional-to-absolute-temperature (PTAT) current I_{PTAT} derived from $\Delta V_{BE}/R_{16}$ is injected into either the M_{P15B} or M_{P15C} branch, depending on the selection of OVP mode or OPP and OCP modes.

IV. Design Considerations

A. Influence of R_0 on P_{TH} and $\mathrm{V}_{TH\cdot SUP}$

Building upon the preceding design analysis in (6), (9), and (11), the simplified threshold equations for OPP and OVP can be derived as follows:

$$P_{\mathrm{TH}} = I_2 \cdot R_{MP2} \cdot I_3 \cdot R_0 / R_{MP0} \tag{12}$$

$$V_{\mathrm{TH\_SUP}} = I_2 \cdot R_{MP2} \cdot R_0 / \left(R_{MP4} \cdot 2\right) . \tag{13}$$

Thus, the overload thresholds for OPP and OVP modes exhibit a linear relationship with the R_0 resistance value, where their absolute resistance and temperature coefficient directly influence both overload thresholds. Thus, 6-bit trim is employed to ensure that the absolute deviation within 1% for process corner variations and device mismatch. Its temperature compensation is realized through the series combination of resistors with positive and negative temperature coefficients. The composite temperature coefficient of the 10 MΩ resistor is 27.7 ppm/°C.

B. MOSFET On-Resistance ($\mathrm{R}_{\mathrm{MP}\,2}$, $\mathrm{R}_{\mathrm{MP}\,3}$, $\mathrm{R}_{\mathrm{MP}\,4}$, $\mathrm{R}_{\mathrm{MP}\,0}$)

These devices (M_{P2}, M_{P3}, M_{P4}, M_{P0}) operate in the deep triode region, while R_{MP2} and R_{MP4} are designed to have the same width and length. Their multiplier ratios are adjusted to set the OVP threshold according to (13), thereby preventing changes in the temperature coefficients of R_{MP2} and R_{MP4} caused by differences in channel length.

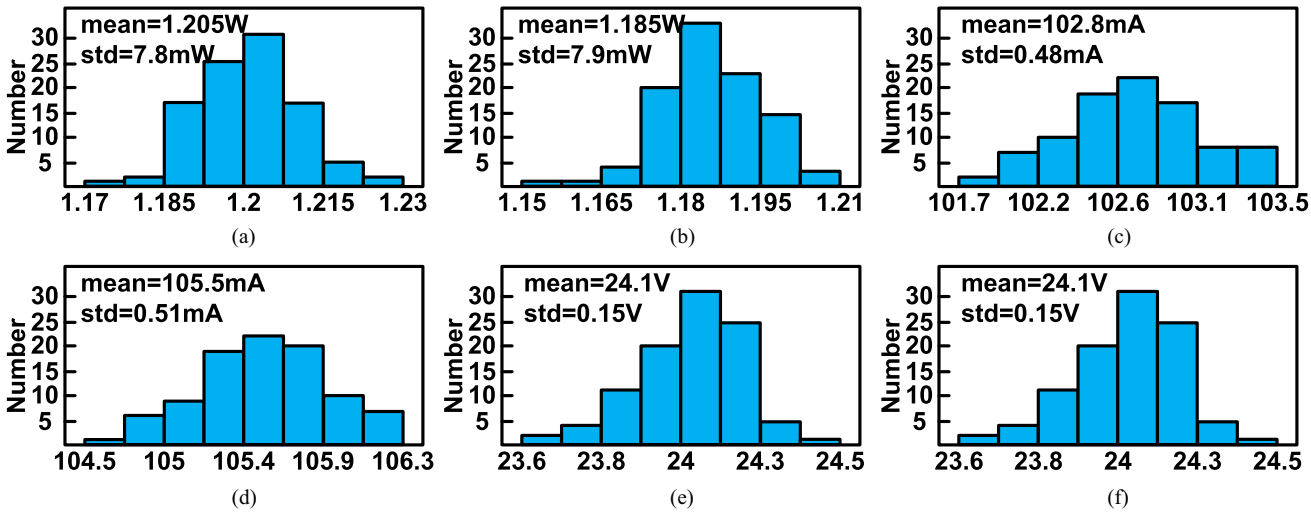

Fig. 18. Statistical results of overload threshold deviation test for 100 Chips. (a) OPP mode with a 5 V power supply. (b) OPP mode with a 40 V power supply. (c) OCP mode with a 5 V power supply. (d) OCP mode with a 40 V power supply. (e) OVP mode with a 1 mA load. (f) OVP mode with a 100 mA load. (a) $\mathrm{OPP_{TH}}$_5V(W). (b) $\mathrm{OPP_{TH}}$_40V(W). (c) $\mathrm{OPP_{TH}}$_5V(mA). (d) $\mathrm{OCP_{TH}}$_40V(mA). (e) $\mathrm{OVP_{TH}}$_1mA(V). (f) $\mathrm{OVP_{TH}}$_100mA(V).

TABLE II
MEASURED PERFORMANCE SUMMARY

Parameter	This Work	MAX17-527A [26]	TPS2595 [27]	TCASI [28]	TCASII [29]	TPEL [30]
Year	2025	2022	2018	2025	2023	2022
Tech. (nm)	180	not state	not state	180	180	GaN
Method	Rds_on	Res.	Res.	Res.	Res.	HEMT
V_{SUPLLY} (V)	5-40	5.5-60	2.7-18	5-90	3.3-40	200
I_Q (μA)	31	1460	175	65.1	49	2600
Standby I_Q (μA)	0.8	no	no	5.5	no	no
OCP Delay (μs)	12	3	250	not state	2	0.16
OVP Delay (μs)	4	3	5	no	no	no
OPP Delay (μs)	17	20000	no	no	no	no
PCM Delay (μs)	101.5	no	no	no	no	no
Accuracy (%)	≤2	≤7	≤7.5	≤6	≤5.2	≤2
TC*1	yes	yes	yes	yes	no	yes
Trimming	yes	yes	yes	yes	no	yes
Area*2 (mm^2)	0.15	not state	not state	0.3	0.286	16

*1: Temperature Compensation
*2: Area without power MOS

As shown in Fig. 7(a) and (b), a positive temperature coefficient current (I_{PTAT}) flows into I_3, while $\mathrm{OPP_{TC}}$ and $\mathrm{OPP_{NTC}}$ denote the temperature-compensated and uncompensated results, respectively, while $\mathrm{OCP_{TC}}$ and $\mathrm{OCP_{NTC}}$ represent the corresponding results for OCP. This approach effectively keeps temperature-induced threshold variations for both OCP and OPP within ±2% , which will exceed ±10% without I_{PTAT}. More specifically, in (10) and (12), the R_{MP3}/R_{MP0} and R_{MP2}/R_{MP0} ratios are sized large to reduce current consumption. Meanwhile, R_{MP0} is constrained to the minimum length to reduce chip area. So, M_{P2} and M_{P3} are both sized to be long-channel transistors, and M_{P0} is sized to be short-channel transistor for power conduction. Consequently, the OPP and OCP thresholds tend to decrease as temperature rises. To mitigate the approximate first-order temperature-dependent effects of the OPP and OCP threshold voltages, the design incorporates a PTAT current (I_{PTAT}) into I_3. When the I_{PTAT} of this current matches the absolute value of the negative temperature coefficient of the resistance ratio, the temperature dependence of the threshold voltages is much reduced.

Fig. 7(c) illustrates the threshold voltage deviation as a function of temperature in OVP mode. Without any temperature compensation, the OVP threshold exhibits a negative temperature coefficient. Since I_1 is an order of magnitude larger than I_3, and $V_{\mathrm{DS}\,MP1A}$ is approximately ten times larger than $V_{\mathrm{DS}\,MP1B}$ while R_{MP} and $V_{\mathrm{DS}\,MP}$ increase with temperature, the resistance ratio R_{MP1B}/R_{MP1A} consequently exhibits negative temperature dependence. With a positive temperature coefficient compensation current injected into I_2, the threshold deviation relative to the 25 °C baseline is constrained within ±1% .

C. Voltage-Dependent Deviation

The design employs cascode current mirrors and long-channel devices (length $> 5\ \mu$m) to minimize supply voltage-induced variation (across 5–40 V). However, according to (5), at low supply voltages, MOS transistor resistance values are large, making them more susceptible to current variations. Consequently, a mismatch between R_{MP1A} and R_{MP1B} is observed under such conditions, as shown in Fig. 8(a). Additionally, as shown in Fig. 8(b), the voltage difference between V_{N1} and V_{N2} increases with rising V_{SUPPLY}, leading to a higher threshold voltage at elevated supply voltages. To address this issue, a voltage compensation scheme has been introduced by incorporating a current that decreases with increasing V_{SUPPLY} into I_3. The compensation current is defined as $I_{\mathrm{CPS}} = (I_6 - 0.1 \times I_1)\ /\ 10$. To ensure accuracy under device mismatch conditions, the I_1 and I_6 can be trimmed accordingly to compensate for mismatches. As shown in Fig. 8(c), the P_{TH} deviation of the OPP mode with voltage compensation ($P_{\mathrm{TH}\cdot VC}$) is controlled within ±2% over the 5-40 V operating voltage range.

Fig. 9 presents the simulated ac power supply rejection ratio (PSRR) of the comparator's input differential voltage, defined

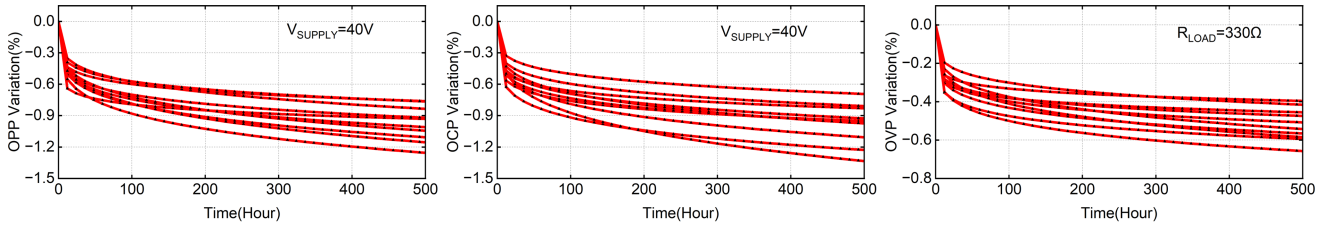

Fig. 19. Aging test: 10 chips, 40 V, 120 mA, 125 °C, 0–500 h. (a) OPP mode was tested at 12-h intervals. (b) OCP mode was tested at 12-h intervals. (c) OVP mode was tested at 12-h intervals.

as

$$\mathrm{PSRR}\,(f)=20\log_{10}\left(V_{\mathrm{TH\_}CM}/\left(V_{CMPN}\,(f)-V_{CMPP}\,(f)\right)\right) \tag{14}$$

where f is the frequency and $V_{\mathrm{TH}\cdot CM}$ is the common-mode voltage at the comparator's noninverting (V_{CMPP}) and inverting (V_{CMPN}) inputs of the OLC when the inversion trigger threshold is reached. At lower supply voltages, I_1 is relatively small, making the gates of M_{P1A} and M_{P1B} more vulnerable to supply voltage fluctuations and thereby degrading low-frequency supply ripple rejection. The triple-mode overload protection maintains over 80 dB of rejection below 100 Hz across the full supply voltage range.

D. Current Consumption in Each Mode

As in Fig. 10, static power consumption data for each module under four PG modes at 40 V are listed. The total current consumption in OPP and OVP modes exceeds 30 μA, with VRC accounting for more than 90% . The dominant current components in the VRC are primarily $5I_1$ and $4I_2$. As shown in Fig. 11(a), the I_1 current is inversely proportional to R_0. To balance V_{SUPLLY} tracking speed and power consumption, R_0 was selected as 10 MΩ. Fig. 11(b) indicates that the power consumption of the VRC is nearly linear with the bandwidth. To meet the response speed requirement within tens of microseconds, the typical bandwidth of the VRC is designed to be >500 kHz. Therefore, the current consumption of the VRC is set at 28 μA to achieve an optimal tradeoff among area, bandwidth, and power consumption. Although the design metrics already indicate a power consumption reduction of over 40% compared to [28] and [29], the PCM detection technology was designed to provide multiple mode options while balancing speed and power consumption.

V. Measurement Results

The proposed PG circuit operates over a 5–40 V input range. It was fabricated in a 0.18-μm BCD process. As shown in Fig. 12, the chip effective area is 1022 μm × 340 μm. The power switch occupies 640 μm×340 μm (62.6% of the total area) and its turn-on impedance is approximately 600 mΩ.

In the OPP test result shown in Fig. 13, V_{SUPPLY} is set to 10 V with S_1 and S_2 configured to logic high. Over power condition was applied by shorting V_{OUT} to GND via a 33 Ω resistor to generate a 300-mA current pulse, as indicated by the blue trace I_{LOAD}. Since the 3W power load exceeds P_{TH} (1.2 W), the V_{PLIM} output of the OLC ramps up to pull up V_{PGB} and V_{GATE} within 16.8 μs, and total protection response time to turn off the power MOSFET (M_{P0}) is approximately 17 μs.

For the OCP test, S_1 is set to logic low and S_2 to logic high with V_{SUPPLY} set to 10 V. As shown in Fig. 14, similarly shorting V_{OUT} to GND via a 33 Ω resistor generates a 300-mA current pulse. Given that the 300-mA current load exceeds the $I_{\mathrm{TH\_SUP}}$ (106 mA), the OLC's V_{PLIM} ramps up to pull up V_{PGB} and V_{GATE} within 11.8 μs, and total protection response time to turn off M_{P0} is approximately 12 μs.

For OVP test, S_1 is configured to logic high and S_2 to logic low. As depicted in Fig. 15, V_{SUPPLY} is switched via a high-voltage NPN transistor—with its base connected to V_{SUPPLY}, collector to 10 V, and emitter initially floating before being connected to a 40 V source. The blue trace shows V_{SUPPLY} ramping up from 10 to 40 V. The V_{SUPPLY} slope detection circuit (Frame 5 in Fig. 3) responds by asserting the V_{PGB} to logic high after 0.77 μs. This signal is level-shifted, delivered to V_{GATE} in 0.23 μs, and results in the turn-off of M_{P0} within a total of approximately 1 μs. V_{PLIM} ramping up to its trigger voltage over 3.8 μs, and total over voltage protection is 4 μs.

Fig. 16 illustrates the trial reconnection test under OPP mode, with $V_{\mathrm{SUPPLY}} = 10$ V and V_{OUT} shorted to GND via a 33 Ω resistor. When M_{P0} is turned ON, the overload detection comparator identifies a 3 W overload condition and triggers M_{P0} turn-off. After M_{P0} is disabled, an internal timer times out after 110 μs to re-enable M_{P0}. After the 5 μs blanking time, the OLC detection cycle repeats as the overload condition persists.

Fig. 17 presents the hot-plug test waveforms under OVP mode, with the circuit output loaded by a 10 kΩ resistor and a 100-pF capacitor. A 23 V power supply clip is connected to V_{SUPPLY}, inducing a rapid voltage step. Upon detecting this input voltage transient, M_{P0} is turned OFF, triggering a 12 V transient overshoot on V_{OUT}. Inductive ringing caused the V_{SUPPLY} to overshoot to 45 V (the high-voltage transistor's maximum rated voltage is 49.5 V). After the internal 110 μs reclosing timer expires, M_{P0} attempts to reclose. The resulting output voltage exhibits a maximum overshoot of 23.5 V, verifying the circuit's effective protection for the downstream stage.

In Fig. 18, test results across 100 chips show a standard deviation of <0.7% . The voltage-dependent deviations of both OVP and OCP are within ±2% . Average OVP thresholds tested under 1 and 100 mA loads show negligible variation, demonstrating near-independence from load current. This can be attributed

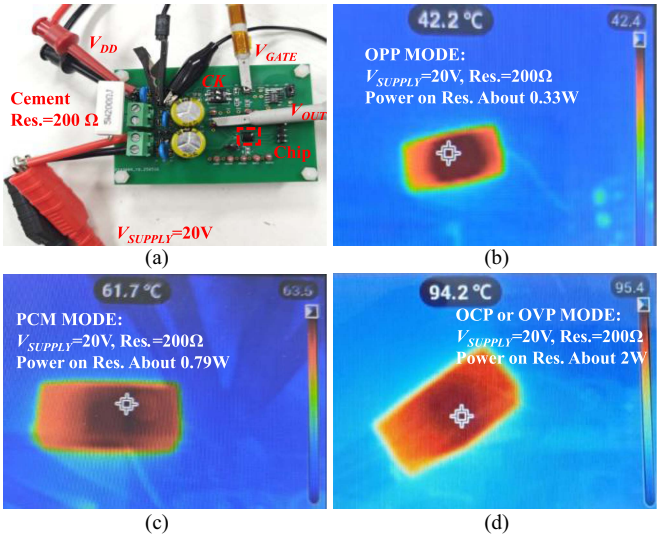

Fig. 20. Thermal imager tests under 20 V power supply with a cement resistor load. (a) Testing the peripheral PCB circuit board. (b) OPP mode. (c) PCM mode. (d) OCP mode and OVP mode.

to precise device matching in the circuit design, coupled with voltage compensation and current trimming techniques.

Under accelerated aging conditions (125 °C, 40 V supply voltage, 120 mA load current, 500-h duration), the triggering threshold voltage deviation is within 1.5% across ten chips each tested in OVP, OCP, and OPP modes, as shown in Fig. 19. This stability stems from the key thresholds including P_{TH}, $V_{\mathrm{TH\_SUP}}$, and $I_{\mathrm{TH\_SUP}}$, relying primarily on resistance ratios R_{MP2}/R_{MP0}, R_{MP2}/R_{MP4}, and R_{MP3}/R_{MP0}. These matched resistors exhibit correlated aging, enabling inherent drift compensation.

Fig. 20 evaluates the thermal performance of a cement resistor load when the chip operates in OPP, OCP, OVP, and PCM modes with a 20 V supply. At an ambient temperature of 25 °C, the output is shorted to V_{GND} via a 200 Ω cement resistor. For OPP mode, the circuit performs continuous overload protection (110 μs) and reclosing attempts (5 μs blanking time + 17 μs detection time), resulting in an equivalent power dissipation of approximately 0.33 W in the cement resistor. In contrast, for OCP and OVP modes, the power switching MOSFET (M_{P0}) remains continuously ON, leading to an equivalent power dissipation of approximately 2 W for the cement resistor. For PCM mode, after the 110 μs protection timeout and an average of approximately 72 μs of circuit reclosing detection, the cement resistor's equivalent power dissipation reaches approximately 0.79 W. All thermal imaging tests followed a standardized procedure after settling for at least 5 min. Thermal imager results indicate that OCP and OVP modes reach peak temperatures nearing 100 °C. PCM mode stabilizes at approximately 65 °C while OPP mode with continuous over-threshold conditions maintains the module temperatures below 45 °C.

Table II summarizes the performance of the proposed approach and other high-performance counterparts. A novel VRC is proposed, incorporating temperature and voltage compensation as well as trimming to enable precise setting of OPP and OVP overload thresholds with an accuracy of ±2% . A PCM strategy is designed to optimize speed of detection based on load current: it supports a 0.8 μA standby current under light-load conditions while cyclic monitoring of OCP, OPP, and OVP under heavy-load conditions. The circuit reuse architecture and common-base comparator design further improve response speed and area efficiency.

VI. Conclusion

This article presents a PG circuit that incorporates a power transistor and operates over a 5–40 V range. Power transmission is blocked within tens of microsecond once any of over-power, over-voltage, or over-current conditions is detected. A VRC is proposed to set the overload threshold. A temperature compensation mechanism is integrated to limit overload threshold deviations to within ±2% over the −40 to 125 °C range. The integrated timing control logic enables periodic reconduction of the power MOSFET to recheck overload conditions and prevent deadlock.

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