A Reconfigurable Resonant Modular Multilevel PMIC for Wide Input Voltage Range With Inherent Balancing and Soft Switching in 180 nm CMOS

Amir Mohammad Mohammadi, *Graduate Student Member, IEEE*, S. Ali Khajehoddin, *Senior Member, IEEE*, Nasrin Rezaei-Hosseinabadi, *Member, IEEE*, and Kambiz Moez, *Senior Member, IEEE*

***Abstract*—Design of integrated power converters capable of operating with a wide input voltage range in standard CMOS technologies is challenging due to the low breakdown voltage of modern transistors. This article presents a fully integrated, fully soft-switched resonant modular multilevel converter (IRMMC), designed in standard 180 nm CMOS with nominal supply voltage of 1.8 V, that enables high-efficiency power conversion over a wide input voltage range of 2–5.5 V—well beyond the safe operating limits of scaled CMOS devices. The proposed architecture combines multilevel voltage division, resonant energy conversion, and modular reconfiguration to simultaneously support wide input adaptability, inherent flying-capacitor voltage balancing, and continuous output voltage regulation. A dynamically reconfigurable multilevel converter, utilizing an additional sub-module and control logic, enables seamless mode transitions and capacitor self-balancing without the need for complex sensing or control loops. An integrated *LLC* resonant tank, using a 0.8 nH in-package series inductor, along with an active rectifier, achieves output regulation from 0.4–1.2 V and ensures full zero-voltage switching (ZVS) for all power MOSFETs across the entire operating range. The prototype converter delivers a maximum output power of 2 W with a peak efficiency of 88%, demonstrating its suitability for compact, energy-efficient power delivery in integrated system-on-chip applications.**

***Index Terms*—DC–DC converter, Li-ion battery, modular multilevel converter (MMC), power management, resonant converter, switched capacitor (SC) converter.**

I. Introduction

POWER converters are essential components in nearly all electronic devices, including modern mobile systems, IoT devices, and sensors, as they enable efficient regulation and distribution of power to meet diverse voltage and current requirements. With most of today's electronics being fully integrated on-chip to reduce cost and minimize form factor, there is an increasing demand to integrate power management functions directly on-chip to achieve a true system-on-chip (SoC) solution. As standard CMOS is the most commonly used semiconductor technology because of its low fabrication cost, high transistor density, low power consumption compared to other semiconductor technologies [1], [2], [3], [4], it is desired to develop the power management integrated circuits (PMICs) in the same technology for full system integration. Over the past decade, substantial research has focused on the design and implementation of efficient PMIC to supply integrated circuits using energy stored in batteries or supercapacitors [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. However, standard thin-oxide, short-channel-length CMOS MOSFETs typically have low breakdown voltages, which presents a significant design challenge when interfacing with standard power sources such as Li-ion batteries that operate in a voltage range of approximately 2.5 to 5 V, far more exceeding the safe operating voltages of scaled CMOS system-on-chips. To handle various input sources and provide efficient, regulated output, it is essential to design CMOS-based PMICs with a wide input voltage range and high conversion efficiency.

Power converters are generally categorized as either two-level or multilevel architectures. Two-level converters require high-voltage switches to withstand the full input voltage, which makes them unsuitable for implementation in low-breakdown voltage CMOS technologies. In contrast, multilevel converters can distribute the input voltage across multiple switching devices, enabling compatibility with lower voltage semiconductor processes. Among various multilevel converter types [29], [30], [31], flying-capacitor multilevel (FCML) converters are well-suited for integration in low-voltage semiconductor as voltage stress across switches is reduced as the input voltage is divided using multiple flying capacitors [5], [6], [7], [32], [33], [34]. However, FCML converters can still experience voltage imbalances across the flying capacitors. One approach to balance the flying capacitors is to employ a preset calibration strength for duty ratio adjustment based on direct flying-capacitor voltage monitoring [6], [35], [36]. However, this method relies on fixed calibration parameters and is therefore susceptible to process, voltage, and delay variations. In contrast, the auto-capacitor-balancing pulse-frequency-modulation (ACC-PFM)

Received 16 August 2025; revised 15 November 2025; accepted 19 December 2025. Date of publication 29 December 2025; date of current version 20 March 2026. This work was supported in part by the Alberta Innovates and the Natural Sciences and Engineering Research Council of Canada (NSERC). Recommended for publication by Associate Editor Y. Yan. *(Corresponding author: Amir Mohammad Mohammadi.)*

Amir Mohammad Mohammadi, S. Ali Khajehoddin, and Kambiz Moez are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: amirmoh3@ualberta.ca; khajeddin@ieee.org; kambiz@ualberta.ca).

Nasrin Rezaei-Hosseinabadi is with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 84156-83111, Iran (e-mail: n.rezaei@iut.ac.ir).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3649007.

Digital Object Identifier 10.1109/TPEL.2025.3649007

controller [37], [38], which combines peak and valley current-mode control, achieves adaptive self-balancing and mitigates the limitations of direct voltage monitoring. Although voltage balancing can be realized through advanced control techniques, such methods typically require numerous sensors and multiple control loops, thereby increasing system complexity.

Alternatively, the dual-path method [8], [9] can help with capacitor voltage balancing, but introduces additional charge sharing losses, which is caused by energy dissipation during charge redistribution between capacitors with different voltages.

Another category of multilevel converters, switched-capacitor (SC) converters [10], [11], [12], [13], [39], has emerged as promising candidates for these applications because of their inherent voltage balancing capability. However, their conversion ratios are discrete, and achieving finer output tuning results in increased losses due to impedance modulation [39]. To alleviate this problem, reconfigurable SC architectures, with multiple conversion ratios N, are introduced to increase the efficiency over a wide input voltage range [14]. However, the required increase in the number of power switches and drivers, along with the obvious limitation in achieving very low output impedance due to charge sharing loss and conduction loss, results in a smaller than expected increase in efficiency for the multiratio configuration [15].

To address these issues, hybrid SC converters [17], [18], [19], [32], [40], [41], [42], [43], [44] have emerged as a promising alternative. These architectures incorporate inductors into the SC structure, where the SC stage produces a high step-down pulsed output, and the inductor acts as a filter to enable continuous voltage regulation. Furthermore, the inductor facilitates soft charging of the flying capacitors [20], thus improving the overall conversion efficiency. To further reduce the converter footprint, resonant switched-capacitor (ReSC) converters have been introduced [21], [22], [23], [45], [46], [47], [48], [49]. By leveraging *LC* resonance, ReSC architectures achieve reduced passive component size and enable soft switching, which supports higher-frequency operation and, in turn, greater area efficiency [50]. ReSC converters can be classified into two categories: direct and indirect. In the direct category, the inductor is placed at the output of the converter [22], [47], [48], which enables better output voltage regulation. In contrast, in the indirect category [21], [22], [23], [46], [49], the inductor is placed in series with the flying capacitor, providing soft charging of the capacitors and reduced switching loss, but making precise output voltage regulation more challenging [22], [51].

However, the primary disadvantage of ReSC converters, is their need for high-Q magnetic components [22], making them unsuitable for integration as on-chip spiral air-core inductors tend to be lossy and consume substantial die area to realize even with modest inductance values [24]. Moreover, ReSC converters typically operate in discontinuous conduction mode (DCM), which can realize the zero-current switching (ZCS) condition. However, the ZCS approach cannot eliminate the dominant switching losses components in MOSFET-based converters, which can be more effectively mitigated using zero voltage switching (ZVS) techniques [52]. In addition, ReSC converters operating in DCM are generally optimized for light-load conditions and fixed conversion ratios. This operating mode limits their ability to regulate the output voltage when the input voltage changes. In [25], [26], [27], the switch conductance regulation (SwCR) method has been used to tune the output for low output powers. In this way, the power switch is segmented; i.e., composed of an array of transistors stacked switches, level shifters, charge pump and logic, which activates as required [28]. Although this method enhances output regulation, it also adds significant design complexity and is not well suited for high-power applications.

This article presents a reconfigurable modular multilevel converter (MMC) featuring an *LLC* resonant filter with a package-integrated series inductor, simultaneously enabling continuous output voltage regulation over a wide input voltage range with high conversion efficiency. The reconfigurable multilevel structure enables the converter to operate in a wide input voltage range by adjusting the number of active cells according to the input voltage level. In addition, using one extra cell in each operating mode provides inherent voltage balancing of the flying capacitors. Output voltage regulation is achieved through frequency control of the *LLC* resonant filter and an active rectifier. The resonant filter also guarantees full ZVS for all power MOSFETs across the entire operating range. The converter is fabricated in standard 180 nm CMOS technology, and its performance is validated through both simulation and experimental results under various load conditions and input voltages, achieving a maximum output power of 2 W and peak efficiency of 88%. This power converter structure was implemented without any extra complicated control to achieve capacitor voltage balancing.

II. Proposed Resonant Modular Multilevel PMIC

The proposed resonant MMC (RMMC), as shown in Fig. 1(a), consists of three primary stages: a reconfigurable dc-to-ac converter, a resonant tank, and an active rectifier. To build a dc–dc converter with the highest input voltage range, utilizing a semiconductor technology with a low breakdown voltage, like CMOS technology, the first step is to divide the input voltage into smaller levels which can be reliably handled by the semiconductor technology. The first stage is a dc–ac converter that can convert a wide range of dc voltage to a low-voltage ac (pulsed) signal. Utilizing a MMC topology, which divides the input dc voltage by $N-1$ by organizing N modules connected in series between two distinct upper and lower arms. The extra module enables the inherent voltage balancing of the flying capacitors in the first stage of the RMMC circuit without the need for additional balancing mechanisms, as described in Section II-A. Each module comprises one capacitor and two MOSFET'S, which enable us to either include the capacitor in the circuit or bypass it. The proposed RMMC structure can be reconfigured to operate over a large input voltage range. When the input voltage is within its high voltage range, the converter utilizes all the sub-modules (SM) in the circuit to divide the input voltage at its highest rate. As the input voltage decreases below the high voltage range, a

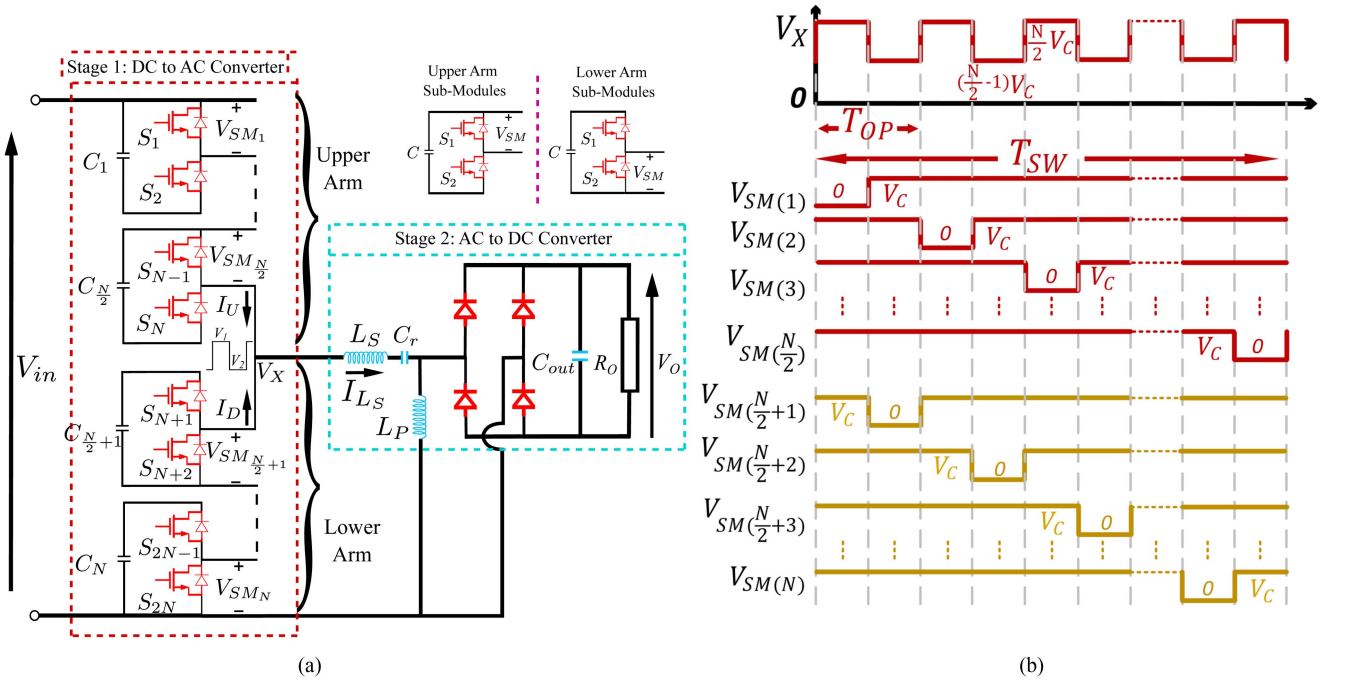

Fig. 1. Schematic and time-domain voltage waveforms of an N-level RMMC. (a) Schematic of proposed N-level RMMC. (b) Time domain key voltage waveforms of the first stage of an N-level converter.

suitable number of SM can be removed from the converter to decrease the voltage division ratio.

The second stage of the converter is an ac–dc converter, which converts the ac voltage generated by the first stage to the desired dc voltage by using an *LLC* resonant tank, which can achieve a gain lower than or higher than one and an output rectifier to convert the ac voltage into dc voltage. The topology utilizes resonant processes to achieve fully soft switching across the entire power range, improving overall efficiency.

The subsequent sections will provide detailed descriptions of the operation of both stages of the RMMC circuit along with the supporting analysis.

A. Reconfigurable DC to AC Converter

The first stage of the converter consists of two distinct arms, each containing an equal number of SM. The primary purpose of this stage is, first, to divide the input voltage into lower levels that can be handled by the low-voltage MOSFETs available in CMOS technology, and second, to generate the acvoltage required for the resonant filter in the second stage, which provides voltage regulation and soft switching for all power MOSFET'S. The following sections discuss how this objective is achieved while satisfying the design constraints.

1) Input Voltage Division With Inherent Balancing: According to the circuit shown in Fig. 1(a), in the upper arm SM, the capacitor is bypassed ("zero state:") when the upper switch is ON and the lower switch is OFF, while it is engaged in the circuit ("ON state") when the lower switch is ON and the upper switch is OFF. Conversely, in the lower arm SM, the capacitor is engaged ("ON state") when the upper switch is ON and bypassed ("zero state") when the lower switch is ON. To support the input voltage, the SM are used predominantly in the "one state" in which the module inserts the capacitor voltage into the circuit. This is arranged so that only one cell at a time is in "zero state," thus the step-down ratio of the circuit becomes dependent on the number of cells N.

To demonstrate the general operation principle, the converter in Fig. 1(a) is considered. In this figure, the output voltage of the jth ($j = 1, 2, \ldots, N$) module and the output voltage of the first stage of the converter are represented by V_{SM_j} and V_X, respectively. The converter configuration must include $N/2$ modules in both the upper and lower arms to adequately divide the input voltage. This ensures that all capacitors in the system are balanced at a fixed voltage. The switching pattern is designed such that, in each mode, all capacitors play a role in regulating the voltage across the converter. The operation consists of two primary phases, with a distribution of active modules between the upper and lower arms. In the first phase, all capacitors in the upper arm are engaged, while one capacitor in the lower arm is shorted. The input voltage V_{in} is divided across the remaining active capacitors. Assuming that all SM capacitors are sufficiently large and their voltage ripples can be ignored, the equation below can be derived based on Kirchhoff's voltage law

$$V_{\mathrm{in}} = nV_C + mV_C = (n+m)V_C \tag{1}$$

where n and m are the number of active modules in the upper arm and lower arm. In this phase, $n = (N/2)$ and $m = (N/2) - 1$, meaning one capacitor is shorted in the lower arm. In the second phase, the configuration is reversed, with all capacitors in the lower arm active, while one capacitor in the upper arm is shorted. The same voltage relationship applies, but with $n = (N/2) - 1$ and $m = (N/2)$. This switching strategy effectively balances the voltage stress across the converter, maintaining each capacitor

at a stable voltage of

$$V_C = \frac{V_{\text{in}}}{N-1}. \tag{2}$$

In [53], it is formally proven that a MMC can achieve self-balancing of all SM capacitor voltages without any voltage sensing or active balancing control, provided that

1) The converter visits a set of switching patterns in which, at each pattern, some subset of SM is inserted (their capacitor voltages sum to the dc link).
2) Over time, every SM appears in every relevant role (inserted / bypassed) in a symmetric way.

Their proof proceeds in three steps. First, for each distinct switching pattern, KVL is applied to derive linear equations relating the individual capacitor voltages V_{C1}, $V_{C2}, \ldots$ to the total dc source voltage. Second, all of these KVL equations are stacked into a single linear system $Y.V_C = V_{\text{dc}}.1$. Third, it is shown that the coefficient matrix Y has full rank. When the rank equals the number of capacitors, the system has a unique solution, implying that the only physically valid operating point is $V_{C1} = V_{C2} = \ldots$ equal capacitor voltages are therefore not just one possible solution, but the only steady-state solution consistent with the enforced switching patterns.

For the proposed N-level RMMC, Kirchhoff's voltage law can be expressed in matrix multiplication form, encompassing all the unknowns, namely the floating-point voltages, as well as the circuit equations. Since only one capacitor is removed from the circuit during each half-period, meaning that all modules are connected in one arm while only one capacitor serves as the load circuit in the other arm, Kirchhoff's voltage law can be formulated as follows:

$$\begin{bmatrix} Y_{\frac{N}{2}*\frac{N}{2}} & 1_{\frac{N}{2}*\frac{N}{2}} \\ 1_{\frac{N}{2}*\frac{N}{2}} & Y_{\frac{N}{2}*\frac{N}{2}} \end{bmatrix} \cdot \begin{bmatrix} V_{C_{\text{up}}} \\ V_{C_{\text{down}}} \end{bmatrix} = \begin{bmatrix} 1_{\frac{N}{2}*1} \\ 1_{\frac{N}{2}*1} \end{bmatrix} * V_{\text{in}} \tag{3}$$

where

$$Y_{\frac{N}{2}*\frac{N}{2}} = \begin{bmatrix} 0 & 1 & 1 & \ldots & 1 & 1 & 1 \\ 1 & 0 & 1 & \ldots & 1 & 1 & 1 \\ 1 & 1 & 0 & \ldots & 1 & 1 & 1 \\ & & & \ldots & & & \\ & & & \ldots & & & \\ 1 & 1 & 1 & \ldots & 0 & 1 & 1 \\ 1 & 1 & 1 & \ldots & 1 & 0 & 1 \\ 1 & 1 & 1 & \ldots & 1 & 1 & 0 \end{bmatrix} \tag{4}$$

and

$$V_{C_{up}} = \begin{bmatrix} V_{C1} \\ V_{C2} \\ \ldots \\ \ldots \\ V_{C\frac{N}{2}-1} \\ V_{C\frac{N}{2}} \end{bmatrix}, V_{C_{\text{down}}} = \begin{bmatrix} V_{C\frac{N}{2}+1} \\ V_{C\frac{N}{2}+2} \\ \ldots \\ \ldots \\ V_{CN-1} \\ V_{CN} \end{bmatrix} \tag{5}$$

where the left-hand side represents the voltage drops across the capacitors in different modes based on the switching pattern and the right-hand side shows that the sum of these voltage drops equals V_{in}, multiplied by the ones matrix, which essentially indicates that the total voltage is distributed across all capacitors. Since the coefficient matrix in the equation set (3) is of full rank, the solution to the system is unique. This indicates that the proposed switching pattern can inherently balance the voltages of the floating capacitors without requiring additional control mechanisms. In other words, the converter achieves intrinsic voltage balancing. This guarantees that, even in the presence of uncertainties such as timing mismatch and asynchronous module pulses, all SM capacitors remain well balanced.

In the generalized N-level case, wide input-voltage adaptability is achieved by sequentially inserting SM into the zero-state (bypassed) or reactivating them as V_{in} crosses predefined thresholds $T_1, T_2, \ldots$. Each threshold corresponds to changing the active stack height by exactly one cell, so that the effective division ratio tracks the input voltage while keeping the device stress within safe limits. By alternating which arm contributes the next zero-state cell, the symmetry of the pulsed ac node is preserved and all flying capacitors experience comparable charging and discharging intervals, which supports inherent voltage balancing without complex sensing or multiloop control. This stepwise short/add procedure maintains appropriate gate-drive levels for the active MOSFETs across the entire input range, avoids operating with an unnecessarily large stack at low V_{in} or insufficient division at high V_{in}, and thereby improves both efficiency and reliability.

It is worth mentioning that in this N-level configuration, the switching frequency is multiplied by $N/2$, as depicted in Fig. 1(b), allowing for a reduction in the required filter size.

As a design example, a 4-module RMMC operating in patterns A and B to support a wide input voltage range is considered. A more in-depth explanation of how these operating patterns comply with the two aforementioned rules for the modulation method is provided in the following sections.

2) Reconfigurable Structure for Variable Input Voltage Levels: To support the highest input voltage, all floating capacitors should be used to divide the input voltage into smaller levels, ensuring that the voltages across the components in the circuit do not exceed their maximum tolerable values. The converter functions through a series of four distinct phases, as shown in Fig. 2, which inherently balances the four flying capacitors to a voltage level of $V_{\text{in}}/3$. The switching pattern is designed so that, in each mode, only three capacitors in series are connected in parallel with the input voltage. Specifically, in modes 1, 2, 3, and 4, capacitors $[C_2, C_3, C_4]$; $[C_1, C_2, C_4]$; $[C_1, C_3, C_4]$; and $[C_1, C_2, C_3]$ are successively placed in parallel with the input voltage. This switching sequence ensures effective voltage balancing across the flying capacitors, with each capacitor independently stabilized at its designated value.

To generate the periodic pulse, as illustrated in Fig. 3, for filtering through the *LLC* resonant filter, the switching pattern must alternate the capacitor configuration between the two arms in consecutive modes, ensuring that no two consecutive modes involve the same capacitor exchange within the same arm. During normal operation, the V_X node alternates between $2V_c$ and V_c, where $V_c = V_{\text{in}}/3$, by cycling through the following

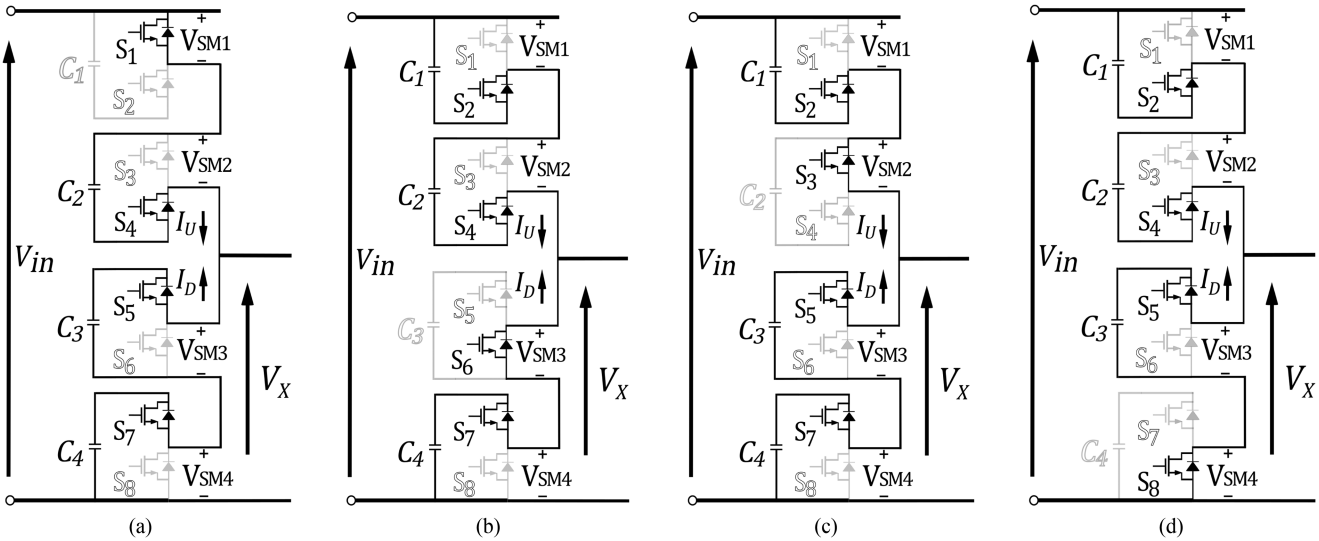

Fig. 2. Operating principle of the four-cell converter in pattern A. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

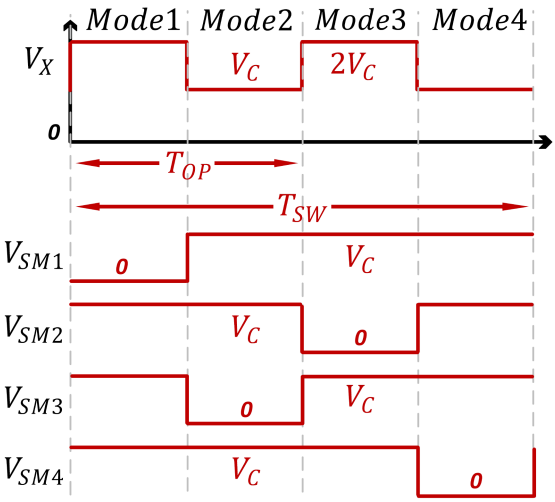

Fig. 3. Time-domain voltage waveforms of four-cell converter operating in pattern A.

sequence of modes: mode 1, mode 2, mode 3, and mode 4, with each module operating at a duty cycle of 3/4, as depicted in Fig. 3. Notably, in this configuration, the operational frequency is twice the switching frequency, offering the advantages of reduced filter size and improved efficiency.

By expressing Kirchhoff's voltage law in matrix multiplication form for the four-level RMMC with the modulation shown in Fig. 3, the same approach as for an N-level RMMC, discussed in Section II-A1, can be achieved. Assuming that all SM capacitors are sufficiently large and that their voltage ripples can be ignored, the equation below can be derived based on Kirchhoff's voltage law

$$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} * V_{\text{in}} \tag{6}$$

where the left-hand side of the equation represents the voltage drops across the capacitors in different modes, determined by the switching pattern, while the right-hand side shows that the sum of these voltage drops equals V_{in} multiplied by the ones matrix. Since the coefficient matrix in equation set (6) is of full rank, the system has a unique solution, confirming that the proposed switching pattern inherently balances the voltages of the floating capacitors and essentially indicates that the total voltage is evenly distributed across all the capacitors. As illustrated in Fig. 3, the waveforms for each module of the converter demonstrate that the blocking voltage across all MOSFETs and capacitors does not exceed $V_{\text{in}}/3$, which is the minimum possible voltage rating for a four-level topology. This reduced voltage rating helps minimize both the implementation area and associated losses. For an input voltage V_{in} up to 5 V, using 1.8-V core MOSFETs in 180-nm CMOS technology eliminates the need for stacking MOSFETs in any of the switches.

When the input voltage decreases in the four-level converter, the flying capacitor voltages drop accordingly, leading to lower driving voltages for the MOSFETs. This increases their on-resistance (R_{on}) and slows down the switching speed. Although switching losses are minimized due to the fully soft-switched operation (ZVS), higher driving voltages, still reduce R_{on} and enhance switching speed, helping to minimize conduction losses and improve overall efficiency.

In terms of designing the filter, for a wide input voltage range, maintaining a fixed output voltage requires a wider operating frequency range. However, this approach presents several challenges. First, the *LLC* converter gain is less sensitive to frequency modulation in the "over resonance $f_s > f_r$" region, therefore the switching frequency must increase much to reach the minimum voltage gain, causing extra switching losses. It also adds complexity to the control system, requiring more advanced algorithms to ensure stability across varying input conditions. In addition, managing a broad frequency spectrum can result in higher levels of electromagnetic interference (EMI), which

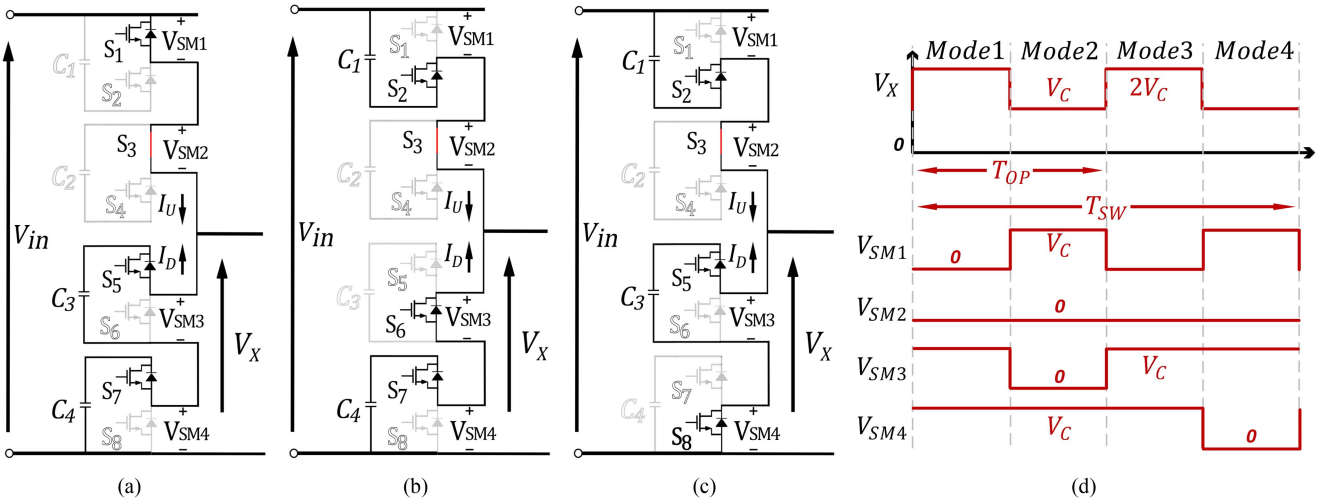

Fig. 4. Operating principle and time-domain voltage waveforms of four-cell converter operating in pattern B. (a) Mode 1, 3. (b) Mode 2. (c) Mode 4. (d) voltage waveforms in pattern B.

necessitates additional filtering to mitigate, further complicating the design.

To address the mentioned issues, an alternative operation is proposed. Given the modular nature of the topology, the number of cells can be reduced by shorting certain modules. As shown in Fig. 4, the second module is shorted, leaving the other three modules active. The operating pattern remains similar to the original. The converter operates through four phases, where two capacitors are connected in series and placed in parallel with the input voltage during each mode: in modes 1 and 3, capacitors C_3 and C_4 are connected; in mode 2, capacitors C_1 and C_4; and in mode 4, capacitors C_1 and C_3. This ensures effective voltage balancing of the flying capacitors. as depicted in Fig. 4(d), The V_X node alternates between $2V_c$ and V_c (where $V_c = V_{\text{in}}/2$), with the lower arm modules operating at a 3/4 duty cycle, while the upper arm operates at double the frequency with a 0.5 duty cycle.

By expressing Kirchhoff's voltage law in matrix multiplication form for the three-level RMMC with the modulation shown in Fig. 4, the equation below can be derived

$$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C3} \\ V_{C4} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} * V_{\text{in}}. \tag{7}$$

Similarly, for this configuration, since the coefficient matrix in the equation set (7) is full rank, the system has a unique solution, ensuring that the converter achieves intrinsic voltage balancing. As shown in Fig. 4(d), the waveforms for each module of the converter indicate that the blocking voltage across all MOSFETs and capacitors remains below $V_{\text{in}}/2$. For an input voltage V_{in} below 3.6 V, utilizing 1.8-V core MOSFETs in 180-nm CMOS technology, this pattern proves more efficient than pattern A.

B. Resonant Tank

Now that the first stage has divided the input voltage and generated a periodic ac voltage, a resonant tank can be used for voltage regulation. While the primary objective is to generate the dc voltage, achieving fully soft switching along with soft charge sharing of the capacitors is crucial for enhancing the overall efficiency of the converter. Fig. 5(a) shows the equivalent circuit of the proposed N-level RMMC, Taking one half-switching cycle $[0, T_{op}/2)$ as an example. The multiple series connected SMs capacitors in each arm are merged into one, represented by C_{up} and C_{down}. The rest of the circuit, including the resonant tank and the LV side, is approximated as a sinusoidal current source I_r. Considering that the total number of series connected SMs capacitors in upper and lower arm are k and h and that the input voltage remains constant and ignoring the parasitic parameters, the ac part of arm currents can be described as

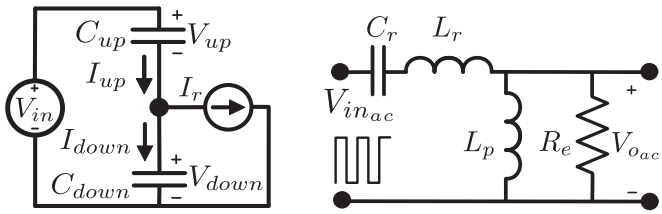

Fig. 5. Equivalent circuit of: (a) modular structure of the proposed N-level RMMC and (b) ILLC resonant tank.

$$\begin{cases} I_{\text{up-ac}}(t) = \frac{h}{h+k} I_r(t) \\ I_{\text{down-ac}}(t) = -\frac{k}{h+k} I_r(t) \end{cases}, \quad t \in [0, T_{\text{op}}/2) \tag{8}$$

where $I_{\text{up-ac}}(t)$ and $I_{\text{down-ac}}(t)$ are the ac part of the arm currents. It can be derived that the arm current is proportional to C_{up} and C_{down}. As illustrated in Fig. 6, the resonant current is split between both arms according to the number of inserted SMs.

Besides the ac arm current, a circulating current exists in modular multilevel structures. It can be decomposed as

$$i_c(t) = I_{\text{dc}} + i_{2\omega}(t) \tag{9}$$

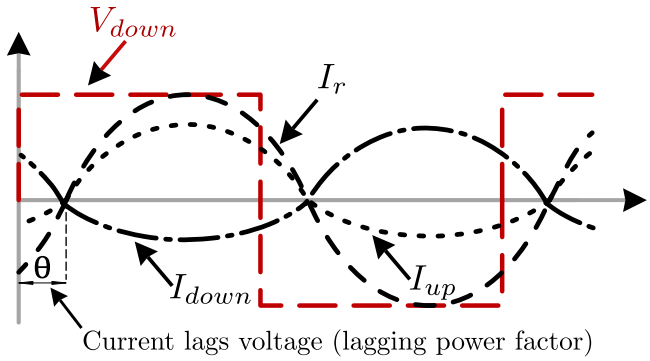

Fig. 6. Theoretical waveforms of the converter.

where the first term $I_{\text{dc}} = \frac{P_{\text{out}}}{V_{\text{in}}}$ is set by the output power, and the second term $i_{2\omega}(t)$ arises from the double-frequency energy exchange whose amplitude scales with ac power (i.e., increases with load) [54]. Collectively, these components add to the arm currents and vertically shift their instantaneous values, thus, ZVS for one switch in each arm could be jeopardized if the net turn-ON current becomes positive. The effect of this circulating current will be investigated in Section IV.

The *LLC* converter can operate with a switching frequency at, below, or above the resonant frequency. In an *LLC* resonant converter, soft switching is achieved by operating in the inductive region, where the resonant current I_r lags the voltage across the resonant tank. This lagging characteristic plays a crucial role in enabling ZVS during turn-ON (ZVS-ON) for the power switches. This lagging behavior ensures that, during the transition phase of a switching cycle, the current direction forces the body diode of the complementary MOSFET to conduct before its gate drive signal turns it ON.

C. Active Rectifier

Since the *LLC* filter produces a sinusoidal output voltage, a rectifier is required between the filter and the load. Traditional passive rectifiers are not ideal due to their high conduction losses and significant voltage drops caused by the presence of two diodes in the power path. To address this issue, this work employs an active rectifier, depicted in Fig. 7, which is more suitable for low-power and low-amplitude ac input signals. Unlike passive diodes, active full-wave rectifiers utilize controlled switches, known as active diodes, which are typically implemented using MOSFETs driven by comparators. This approach eliminates the large voltage drops and reverse leakage currents associated with conventional diodes. The comparators operate by comparing the ac input voltages (e.g., V_{AC1} and V_{AC2} in Fig. 7) against a reference level, effectively enabling a differential comparison between the two input terminals. This configuration also enables fully ZVS turn-ON for all active rectifier switches, as the comparators turn the MOSFETs on after their drain-source voltages have dropped to zero.

Beside the rectifier configuration described earlier, another configuration shown in Fig. 8 can be used for those applications that require a common ground between the output and the battery. In this case, the parallel inductor L_P is replaced by a $1:1$ coupled inductor whose magnetizing inductance equals L_P, the primary winding remains in the resonant tank, while the secondary winding feeds the rectifier. This modification connects the rectified output to the same ground as the input. In this case, if there is any leakage between primary and secondary, that will be added to the tank inductance Lr and does not create any challenge.

TABLE I
DESIGN PARAMETERS OF THE 4-CELL RMMC

Parameter	Value
$V_{\text{in}}^{\text{min}} - V_{\text{in}}^{\text{max}}$	$2.4 - 5$ V
V_{out}	1.2 V
$P_{\text{out}}^{\text{max}}$	2 W
$f_{\text{op}^{\text{min}}}$	2.5 MHz

III. CIRCUIT DESIGN AND IMPLEMENTATION

The objective of this section is to design the converter based on the parameters listed in Table I to efficiently convert a Li-Ion battery voltage of $2.5 - -5$ V into a typical output voltage of 1.2 V suitable for powering the majority of semiconductor ICs with a maximum power rating of 2 W. Detailed procedures for the design and implementation of the dc–ac converter, resonant filter, output stage, and associated control circuits are presented in the following sections.

The proposed RMMC was fabricated using a standard 180 nm CMOS process. This technology enables compatibility with advanced SoC and mixed-signal designs, allowing seamless co-integration within a unified platform. The process provides CMOS transistors optimized for the converter's operating range. However, the limited density and low quality factor (Q-factor) of integrated passive components, such as capacitors and inductors, pose challenges to achieving high power density and efficiency in practical power converter implementations.

To address these limitations, a hybrid integration approach is employed. The series resonant inductor (L_S) is implemented using wire-bond inductance, while the parallel inductor (L_P) is realized with external discrete components mounted on the PCB. Similarly, the flying capacitors and bootstrap capacitors are implemented as a combination of small on-chip capacitors ($0.2, 0.3$ nF) and external discrete components. This hybrid configuration balances integration constraints with the performance requirements of high power density and efficiency.

Fig. 7 illustrates the high-level schematic of the RMMC, highlighting the key power switches and passive components. The design integrates the power switches and diode bridge, along with the corresponding gate drivers and level shifters, into a fully monolithic solution. Further implementation details are provided in the subsequent sections.

A. Implementation of Reconfigurable DC to AC Converter

The integrated section of the first stage of the IRMMC circuit consists of power MOSFETs, gate drivers, level shifters, a

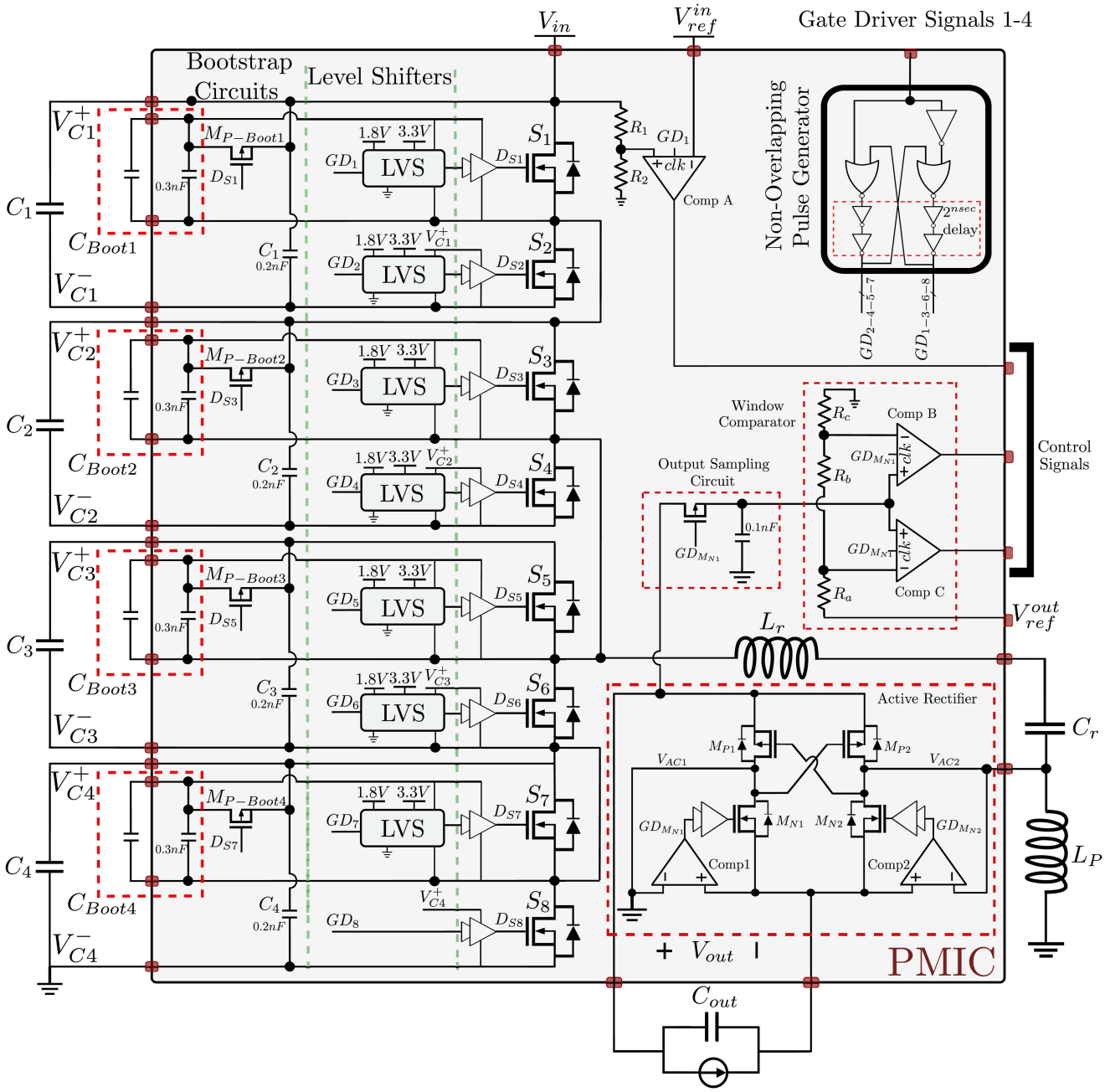

Fig. 7. Full schematic of the prototyped converter (The components shown inside the grey box are implemented on-chip, whereas outside components are off-chip.

nonoverlapping pulse generator, and control logic, all of which will be discussed in more detail in the following sections.

1) Power MOSFET Realization: In the employed 180 nm CMOS technology, each switch is realized with a 1.8 V core MOSFET and can be implemented as either NMOS or PMOS. NMOS transistors offer several advantages over PMOS, including higher electron mobility, which results in faster switching speeds, lower ON resistance for reduced power dissipation, and better current-driving capabilities. In addition, NMOS devices can be smaller for the same drive current, making them more suitable for high-performance and high-density applications. Based on these advantages, NMOS is more suitable than PMOS for implementing power switches. Consequently, all the power switches in the modules are implemented as NMOS.

Although implementing all the power MOSFETs as NMOS is challenging due to gate-driving complexity, a bootstrap technique is employed using each module's flying capacitor to charge the corresponding bootstrap capacitor. In addition to gate drive considerations, achieving full ZVS across the wide input voltage range requires preserving the intrinsic body diode of the NMOS transistors, which facilitates lossless turn-ON by conducting just before the gate signal activates the switch. In standard CMOS processes, NMOS bodies are tied to the p-substrate (typically at ground), and when the source floats, common in this

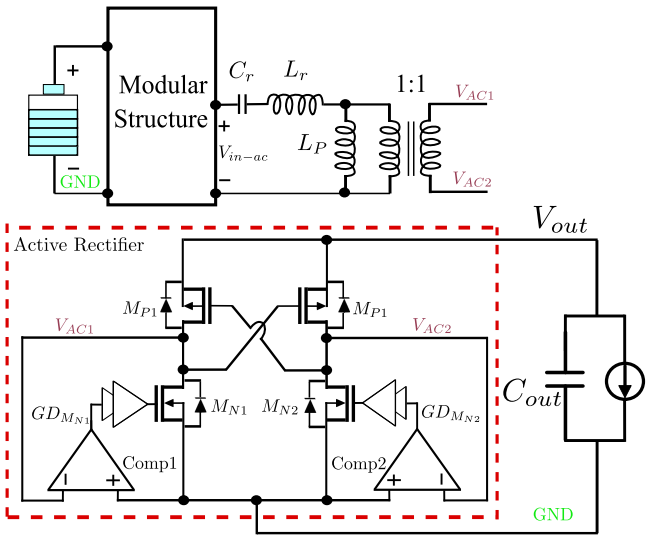

Fig. 8. Common-ground configuration of rectifier using a 1 : 1 transformer.

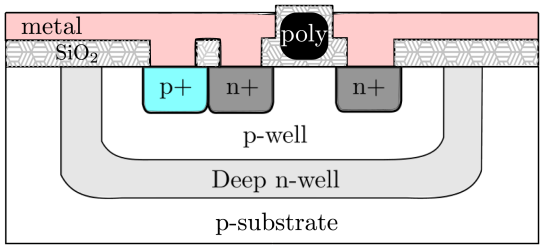

Fig. 9. Well structure in triple-well process.

architecture, this configuration disables the body diode and prevents achieving ZVS. To retain body diode functionality, the NMOS body must track its source voltage, which necessitates electrical isolation from the substrate. This is achieved using a triple-well (or deep n-well) process, wherein each NMOS is placed in an isolated p-well embedded in a deep n-well, as illustrated in Fig. 9. The deep n-well enables the body to be biased to the local source potential, ensuring correct diode orientation, preventing latch-up, and minimizing substrate noise. Hence, all the NMOS switches, except for S_8, are implemented in deep n-well to ensure proper operation and isolation. Since the source of S_8 is always at substrate potential and its body is shorted to the source to use the intrinsic body diode, there is no need to isolate it in a deep n-well. Implementing S_8 in a deep n-well would only increase area and layout complexity, so it is instead realized as a conventional NMOS directly in the p-substrate.

2) Gate Drivers: Since the power train was implemented exclusively with n-channel devices, the gate driver design required careful attention. As shown in Fig. 7, only the power MOSFET S_8 is referenced to a constant voltage, allowing it to be driven by a conventional tapered buffer structure with a fixed supply.

In contrast, the remaining power switches are referenced to their respective source terminals, requiring a floating gate drive structure capable of reliably driving the transistors relative to the voltage swing at their sources. Within each module, the bottom switch (S_2, S_4, S_6, and S_8 in Fig. 7) can be driven using the module's capacitor, as the source terminal of these transistors is connected to the lower terminal of the corresponding capacitor. This configuration ensures that the transistor experiences a constant voltage in steady-state operation, enabling the module capacitor to function effectively as the gate driver for the lower switches.

For the upper switches in each module (S_1, S_3, S_5, and S_7 in Fig. 7), a bootstrapped gate drive structure with active PMOS bootstrap diodes ($M_{P-\text{BOOT1}}$ to $M_{P-\text{BOOT4}}$ in Fig. 7) has been employed. This bootstrap structure operates as follows: when the lower-side device is turned ON, the PMOS bootstrap device is also activated, allowing the bootstrap capacitor to charge to the same voltage as the corresponding module capacitor. During this time, the switching node remains low. Once the PMOS bootstrap device is turned off, the bootstrap capacitor floats with the switching node, enabling it to supply the necessary gate-drive voltage for the upper switch when it is turned ON.

3) Level Shifter and Non-Overlapping Pulse Generation: As shown in Fig. 7, all eight power MOSFETs are driven by four control pulses generated by the micro-controller. These four pulses are expanded into eight nonoverlapping pulses by four nonoverlapping pulse generator blocks. Each pulse generator block consists of an inverter, a latch, and two nanosecond delay blocks, producing output pulses with voltage levels of 0 and 1.8 V.

As previously mentioned, since the source terminals of the power MOSFETs float with respect to ground, the output of the nonoverlapping pulse generator blocks cannot be used directly to drive the switches. This limitation necessitates the use of two level shifters for each power MOSFET in each module. The internal circuit of the modified level shifter, proposed in [55], is shown in Fig. 10.

In the first stage of the level shifter, the input voltage is translated into a current that flows through a pull-up resistor, R_2. By appropriately selecting R_2, the resulting voltage drop across it can meet the condition $V_{\text{th}(p)} < R_2 I_2$, where $V_{\text{th}(p)}$ is the threshold voltage of the PMOS transistors. This current-to-voltage conversion helps decouple the input and output voltage domains. Consequently, the output of the level shifter can drive power switches without exceeding the voltage limits of transistors in the given CMOS technology.

4) Feedback Network and Control Logic: As shown in Fig. 7, a dynamic two-stage comparator is placed at the input to sense the input voltage and generate a digital signal that determines the operating pattern of the converter. When V_{in} is high (e.g., $5, \text{V}$), this signal configures the gate-driving logic so that all three SM are active and the input is divided to approximately $V_{\text{in}}/3$ across each cell, ensuring uniform voltage sharing. As V_{in} decreases and crosses a defined threshold (around $3.6, \text{V}$), the comparator toggles its output and the control logic forces one submodule into a zero-state mode, so that only two SM remain active and the input is divided to approximately $V_{\text{in}}/2$. This stepwise reconfiguration enables smooth mode transition, extends the usable input-voltage range without overstressing

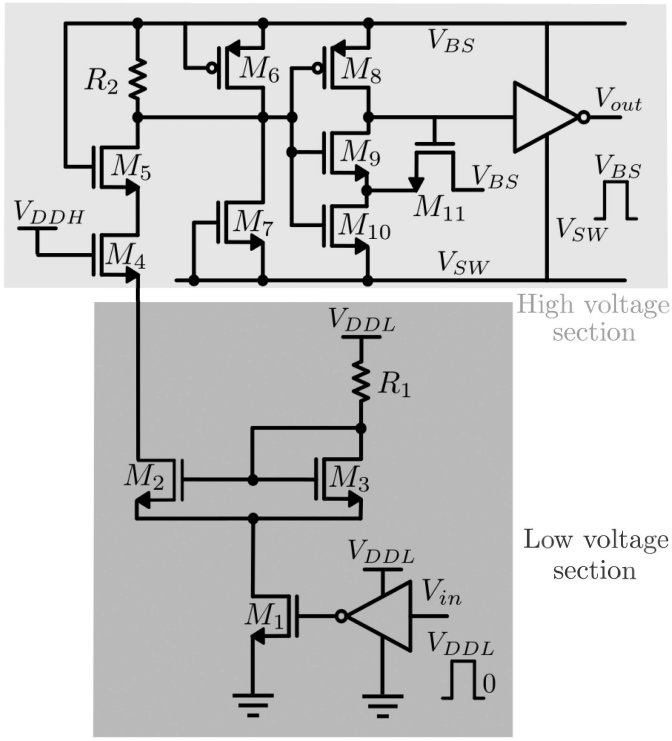

Fig. 10. Schematic of level shifter.

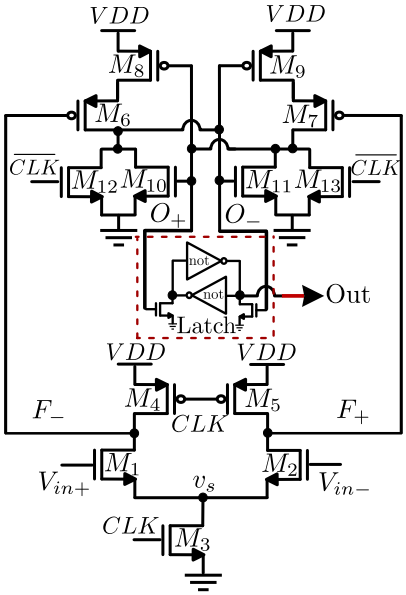

Fig. 11. Schematic of energy-efficient dynamic two-stage comparator followed by SR latch.

any device, and maintains proper gate-drive levels for the active MOSFETs.

At the output, a sampling circuit is used in conjunction with a window comparator, using the same comparator architecture as in the input stage, to generate control signals to adjust the switching frequency. As it can be seen in Fig. 12, these control signals are processed externally by a simple UP/DOWN controller and tri-state charge pump that drive the VCO control

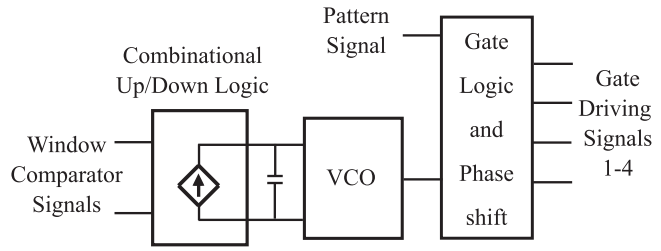

Fig. 12. Frequency-control and gate-generation blocks for the IRMMC.

capacitor, increasing or decreasing the oscillation frequency to keep V_{OUT} within the desired regulation band [56]. A subsequent phase-shift and gate-generation block then derives the required drive signals for the converter modules from the VCO clock. Once the gate-driver signals are generated with the desired pattern and frequency, a dead time is inserted between complementary transitions using a simple nonoverlapping pulse-generator block. This ensures that the corresponding switches are never on simultaneously, so even in the presence of small timing mismatches or asynchronous module pulses, shoot-through currents are effectively prevented. The dynamic two-stage comparator is shown in Fig. 11. The first stage is a voltage amplification stage, accepting differential inputs $V_{\text{in}+}$ and $V_{\text{in}-}$ and producing differential outputs F_+ and F_-. The subsequent stage incorporates both a basic voltage amplifier and a positive feedback amplifier to generate a rail-to-rail digital output. An SR latch then stores the result, ensuring a stable digital output [57].

B. Design Methodology of Resonant Components

The first harmonic approximation (FHA) method is used to analyze the equivalent circuit and gain characteristics of the half-bridge *LLC* resonant converter. It provides a simple and fast mathematical representation by approximating voltage and current waveforms as sinusoidal, neglecting higher-order harmonics. Under steady-state conditions, FHA is an acceptable approach, as it simplifies the circuit analysis. Fig. 5(b) illustrates the converter model based on FHA, where $V_{\text{in}-\text{ac}}$ and $V_{o-\text{ac}}$ represent the fundamental components of the resonant tank input voltage and output voltage, respectively, with R_e as the equivalent load resistance. Regarding Figs. 1 and 5(b), the voltage gain G of the RMMC is determined by the product of the modular structure voltage gain G_{MS} and the resonant tank voltage gain G_t, expressed as

$$G = G_{\text{MS}} * G_t = \left| \frac{V_{\text{in}-\text{ac}}}{V_{\text{in}}} \right| * \left| \frac{V_{o-\text{ac}}}{V_{\text{in}-\text{ac}}} \right| \tag{10}$$

where $V_{\text{in}-\text{ac}}$ represents the amplitude of the resonant tank MV-side voltage, while $V_{o-\text{ac}}$ corresponds to the LV-side voltage. The value of $V_{\text{in}-\text{ac}}$ is obtained by subtracting V_X from the dc voltage, which is blocked by the resonant capacitor. Given that the number of SM in the lower arm is h, the dc voltage is expressed as

$$V_{\text{in}-\text{ac}} = V_X - V_{DC} = V_X - \left[\left(\frac{2h-1}{2} \right) V_C \right]. \tag{11}$$

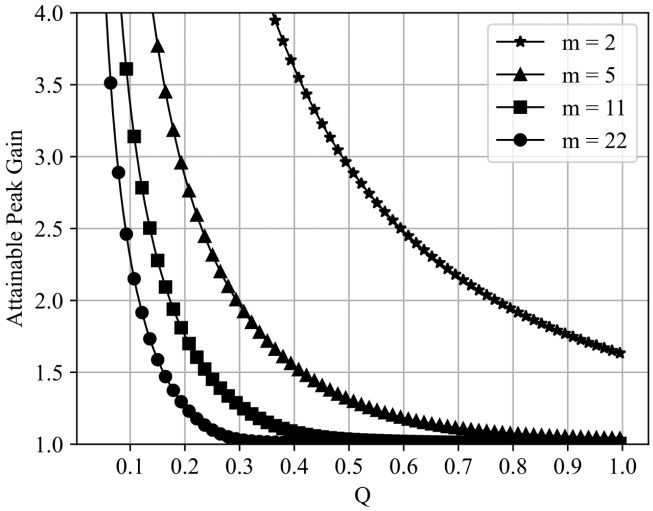

Fig. 13. Peak gain curves.

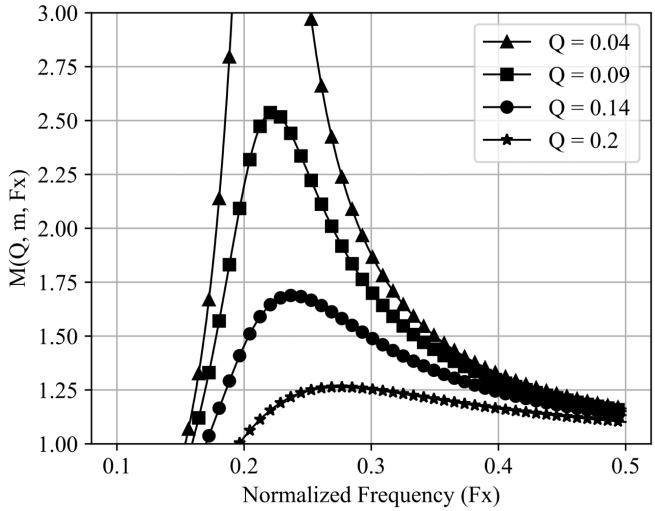

Fig. 14. Gain curves for different Q values over the normalized frequency range [0, 0.5].

G_{MS} varies with the gate signals for SMs, whereas G_t varies with the switching frequency. G_t can be expressed as follows:

$$G_t(Q, m, F_x) = \left| \frac{V_{o\_\text{ac}}(s)}{V_{\text{in\_ac}}(s)} \right| = \frac{(m-1)F_x^2}{\sqrt{(mF_x^2-1)^2 + F_x^2(F_x^2-1)^2(m-1)^2Q^2}} \tag{12}$$

where the quality factor (Q) is $(\sqrt{L_r/C_r})/R_{\text{ac}}$, the reflected load resistance (R_{ac}) is $(8/\pi^2)\cdot R_o$, the normalized switching frequency (F_x) is f_{op}/f_r, the resonant frequency (f_r) is $1/(2\pi\sqrt{L_r \cdot C_r})$ and the ratio of total inductance to resonant inductance (m) is $(L_r + L_p)/L_r$.

Assuming design parameters given in Table I, the design methodology for the proposed 4-cell RMMC can be outlined in five steps.

Step 1: Determine the minimum and maximum voltage gains $(M_g^{\min}, M_g^{\max})$: Since the converter operates in pattern A, when the input voltage is between $3.6 - 5$ V, and operates in pattern B, when the input voltage is between $2.4 - 3.6$ V, the corresponding gains can be described as follows:

$$M_g^{\min} = \frac{V_{\text{out}}^{\min}}{|V_{\text{in-ac}}^{\max}|} = \frac{2*2*1.2}{3.6} = 1.34 \tag{13}$$

$$M_g^{\max} = \frac{V_{\text{out}}^{\max}}{|V_{\text{in-ac}}^{\min}|} = \frac{2*2*1.2}{2.4} = 2. \tag{14}$$

Step 2: Choose inductor ratio (m) and quality factor (Q): Fig. 13 shows the peak gain curves, and it is plotted using (12). Q is the horizontal axis and the attainable peak gain (G_t) is the vertical axis with respect to various values m on the curve. values are obtained using different values of m and Q in the $[0, 0.5]$ interval of normalized frequency F_x. In the design, the selected G_t should be greater than $G_t^{\max}$ at reasonable m curve. Based on the curves shown in Fig. 13, the decided values of the parameters are $G_t^{\max} = 2.5$, $m = 22$, and $Q = 0.09$. Choosing a high value for m, makes it possible to take advantage of low circulating current in the converter. The normal side effect of choosing a high m value is to lose soft switching in light load conditions. However, since the on-chip parasitics are very small, m value can be selected at 20 or higher.

Step 3: Determine the equivalent load resistance (R_{ac}): At full load, R_{ac} is determined from the following:

$$R_{\text{ac}} = \frac{8}{\pi^2} \cdot R_o. \tag{15}$$

Step 4: Determining the Minimum Normalized Switching Frequency: After selecting a value for $Q_{\max}$, an initial value for m, and the equivalent load resistance R_{ac}, the next step is to determine the minimum normalized switching frequency that ensures inductive operation under the condition $Q_{\max}$ (maximum load). This frequency also guarantees inductive operation for all other load conditions.

The minimum normalized switching frequency corresponds to the peak gain of the $Q_{\max}$ curve. It can be determined by solving (16) or it can be visually identified from the gain plot in Fig. 14

$$\frac{d}{dF_x} G_t(Q, m, F_x^{\min}) = 0. \tag{16}$$

Solving for $F_x^{\min}$ yields the required minimum normalized switching frequency.

Step 5: Determining Resonant Parameters (C_r, L_r, and L_m): The resonant circuit parameters at full load are determined based on the resonant frequency

$$C_r = \frac{1}{2\pi f_r Q R_{\text{ac}}} \tag{17}$$

$$L_r = \frac{1}{(2\pi f_r)^2 C_r} \tag{18}$$

$$L_p = (m-1)L_r. \tag{19}$$

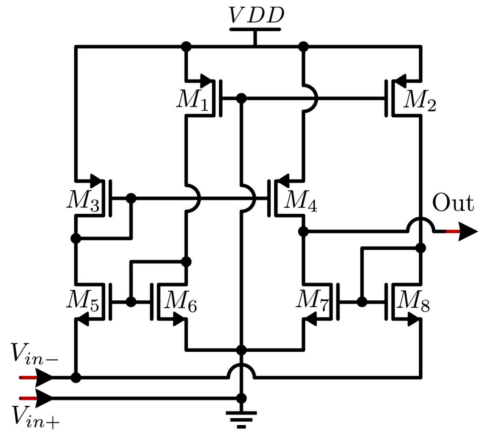

Fig. 15. Schematic of self-biased CGC used in the active rectifier [58].

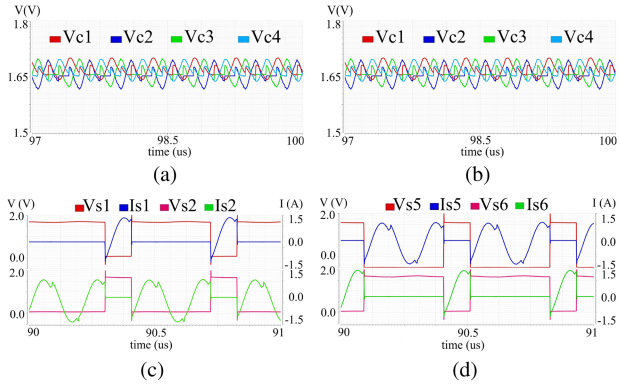

Fig. 16. Simulation results for a four-module converter operating in Pattern A: (a) SM capacitor voltages balanced at 1.67 V for $V_{\text{in}} = 5$ V. (b) Voltage and current of the resonant tank. (c) Drain-source voltage and current of the upper-arm power switches. (d) Drain-source voltage and current of the lower-arm power switches in the first module.

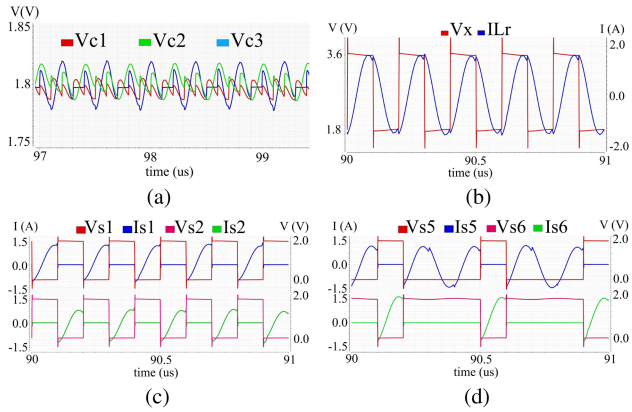

Fig. 17. Simulation results for a four-module converter operating in Pattern B: (a) SM capacitor voltages balanced at 1.8 V for $V_{\text{in}} = 3.6$ V. (b) Voltage and current of the resonant tank. (c) Drain-source voltage and current of the upper-arm power switches in the first module. (d) Drain-source voltage and current of the lower-arm power switches in the first module.

Using the resonant parameters calculated in Step 4, suitable component values are selected: $C_r = 290$ nF, $L_r = 0.8$ nH, and $L_p = 17$ nH.

1) Active Rectifier: The adopted topology, illustrated in Fig. 7, consists of a P-side cross-coupled core rectifier (CR), while two self-biased common-gate comparators (CGCs), shown in Fig. 15, are responsible for driving the NMOS transistors in the CR.

The biasing for COMP1 is supplied through transistors M_1 and M_2 when $V_{\text{AC2}} > 0$ and $V_{\text{AC1}} < 0$, while COMP2 operates under the opposite conditions. The negative terminal of the rectifier output is considered the reference potential for the load (denoted as $V_{\text{out}-}$). When V_{AC1} (V_{AC2}) falls below 0 V, transistor M_5 conducts more current than M_6. Simultaneously, the diode-connected transistor M_8 experiences a gate voltage drop in response to V_{AC1} (V_{AC2}), which in turn reduces V_{GS7}. Transistor M_5 also biases the current mirror formed by $M_3 - M_4$, leading to a higher current flow through M_4 compared to M_7. As a result, the output node is driven to a high level, and CMOS buffers restore the signal, ultimately switching on transistor M_{N1} (M_{N2}) [58].

It is essential to highlight that transistors $M_5 - M_8$ and $M_6 - M_7$ are fabricated within a deep n-well, allowing their source and isolated bulk terminals to be connected to V_{AC1} (V_{AC2}) and the reference potential of the output load ($V_{\text{out-}}$), respectively. This design ensures that the p-substrate of the silicon die remains at $V_{\text{out-}}$ potential, reducing the risk of unwanted leakage currents and substrate noise while maintaining proper circuit isolation.

IV. Simulation and Measurement Results

In this section, the performance of the proposed PMIC is first validated through simulation results obtained using Cadence. Subsequently, experimental results are presented based on the calculated values of the capacitance C_r, inductances L_s and L_p, and the designed IC discussed in Section II-B. Fig. 16 illustrates the key waveforms of the designed converter when the input voltage is 5 V and it operates in Pattern A. To verify the self-voltage balancing capability of the flying capacitors, a small timing mismatch is intentionally introduced in the gate driver signals. As shown in Fig. 16(a), all capacitors remain balanced at 1.67 V despite the timing mismatch. Fig. 16(b)–(d), respectively, show the pulsed voltage generated by the dc–ac converter, the resonant current, and the drain-source voltage and current of the switches in the first module of the upper and lower arms, demonstrating the presence of ZVS in the power MOSFETs. Similarly, Fig. 17 presents the converter waveforms for an input voltage of 3.6 V operating in Pattern B. As seen, the capacitors are balanced at 1.8 V under timing mismatch conditions, and ZVS is achieved across all switches.

An important consideration is to verify ZVS across the entire operating range of the converter, accounting for load and input-voltage variations over the full output-voltage span. First, the impact of circulating current on the ZVS condition of both switches in each module must be assessed. Second, the influence of higher-order harmonics across the frequency range should be included, since FHA captures only the fundamental; notably, capacitive pockets may appear during harmonic transitions [59]. To jointly validate the effects of circulating current and

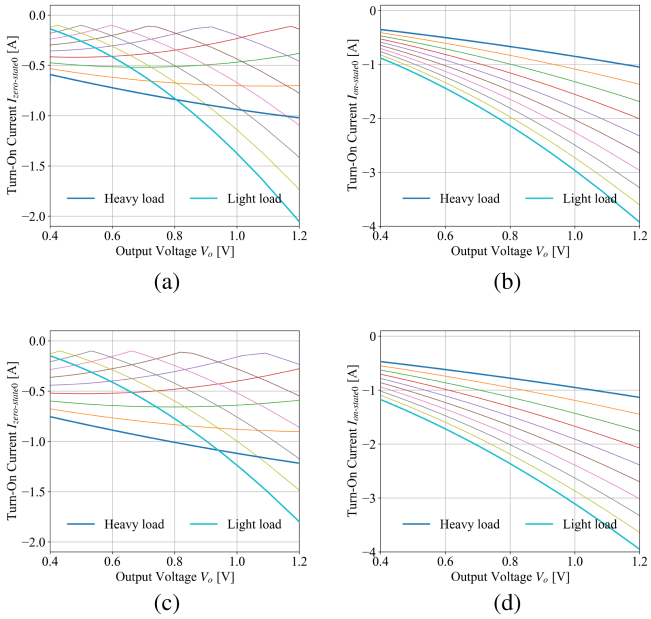

Fig. 18. Simulation results of switch turn-on current versus output voltage for loads ranging from heavy to light: (a) on-state switch at $V_{\text{in,ac}} = 0.6\,\text{V}$; (b) zero-state switch at $V_{\text{in,ac}} = 0.6\,\text{V}$; (c) on-state switch at $V_{\text{in,ac}} = 0.9\,\text{V}$; and (d) zero-state switch at $V_{\text{in,ac}} = 0.9\,\text{V}$.

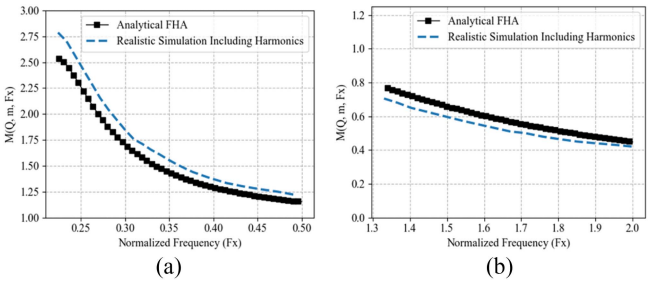

Fig. 19. Comparison of analytical FHA and time-domain simulation gain curves versus normalized frequency (F_x): (a) $V_{(o,\text{max})} = 1.2\,\text{V}$. (b) $V_{(o,\text{min})} = 0.4\,\text{V}$.

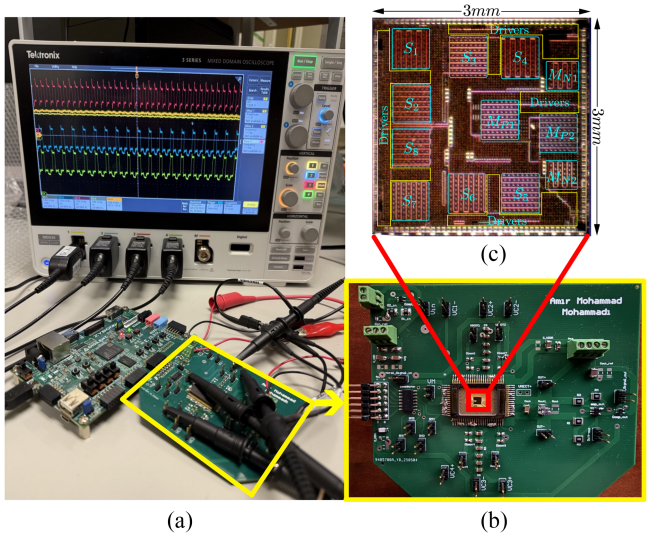

Fig. 20. Photographs of (a) test-bench, (b) test-board, and (c) fabricated CMOS chip.

harmonics on ZVS, we rely on time-domain simulations. Fig. 18 reports the switch turn-ON current versus output voltage for loads ranging from heavy to light. In this figure, the switch that, when turned ON, places its module in the ON state is the ON-state switch (plotted as $I_{\text{on}-\text{state0}}$), and the switch that, when turned ON, places its module in the zero state is the zero-state switch (plotted as $I_{\text{zero}-\text{state0}}$). Across all cases, the turn-ON current of both switches remains nonpositive. While the light-load curves of the zero-state switch approach zero at certain points, they stay slightly negative—already sufficient for ZVS given the small on-chip node/output capacitances. Hence, even when considering the dc-circulating component and all relevant harmonics over the operating range, ZVS is preserved for all switches due to the low on-chip parasitics. It also demonstrates that with the chosen tank ratio $m = 22$, the *LLC*-tank–related circulating current is minimized, while the ZVS condition of both switches in each module remains uncompromised across the entire operating range.

Another important concern is to validate the gain curve considering all the harmonics. To achieve this, we have investigated the gain curve both analytically and through time-domain simulations that inherently include higher-order harmonics and circuit parasitics. In particular, the FHA-based expression for gain is compared against transient simulation results at the two worst-case operating points, $V_{o,\text{max}} = 1.2\,v$ and $V_{o,\text{min}} = 0.4\,v$. As shown in Fig. 19, the simulated curves closely follow the FHA prediction over the full normalized-frequency range of interest, confirming that FHA remains an accurate design tool for this converter.

To evaluate the performance of the designed converter, the RMMC converter was manufactured in a standard 180 nm CMOS process. Fig. 20 presents a photograph of the die along with the employed test board and test bench to measure the performance of the fabricated converter. In this implementation, a 0.8 nH wirebonding inductor serves as the resonant inductor. All flying capacitors and bootstrap capacitors are realized using $6 * 0.47\,\mu\text{F}$ and $2 * 0.1\,\mu\text{F}$ capacitors with C0G dielectric material. In addition, a 17 nH parallel inductor a C0G 290 nF resonant capacitor for the *LLC* filter and an X7R $1\,\mu\text{F}$ output capacitor were mounted on the PCB. The converter operates with an input voltage range of $2.4 - -5\,\text{V}$ and delivers an output voltage from 0.4 to 1.2 V, supporting a maximum load current of 1.7A.

To start the converter safely, the input voltage is ramped so that each sub-module capacitor is first pre-biased to approximately the NMOS threshold (≈ 0.4–$0.6\,\text{V}$), enabling the gate drivers without overstressing any device. As the input rises to about 1.8–2.0 V, the series connection naturally distributes this voltage so that all SM capacitors reach the required level and normal switching can begin, after which the modulation equalizes any residual mismatch. In practice, the Li-ion source and an input capacitor C_{in} form an RC network ($R_s \approx 50\,\text{m}\Omega$, $\tau = R_s C_{\text{in}}$), and choosing τ to be a few switching periods (e.g., $\tau \approx 4\,\mu\text{s}$, $C_{\text{in}} \approx 80\,\mu\text{F}$) provides a controlled input ramp for reliable start-up.

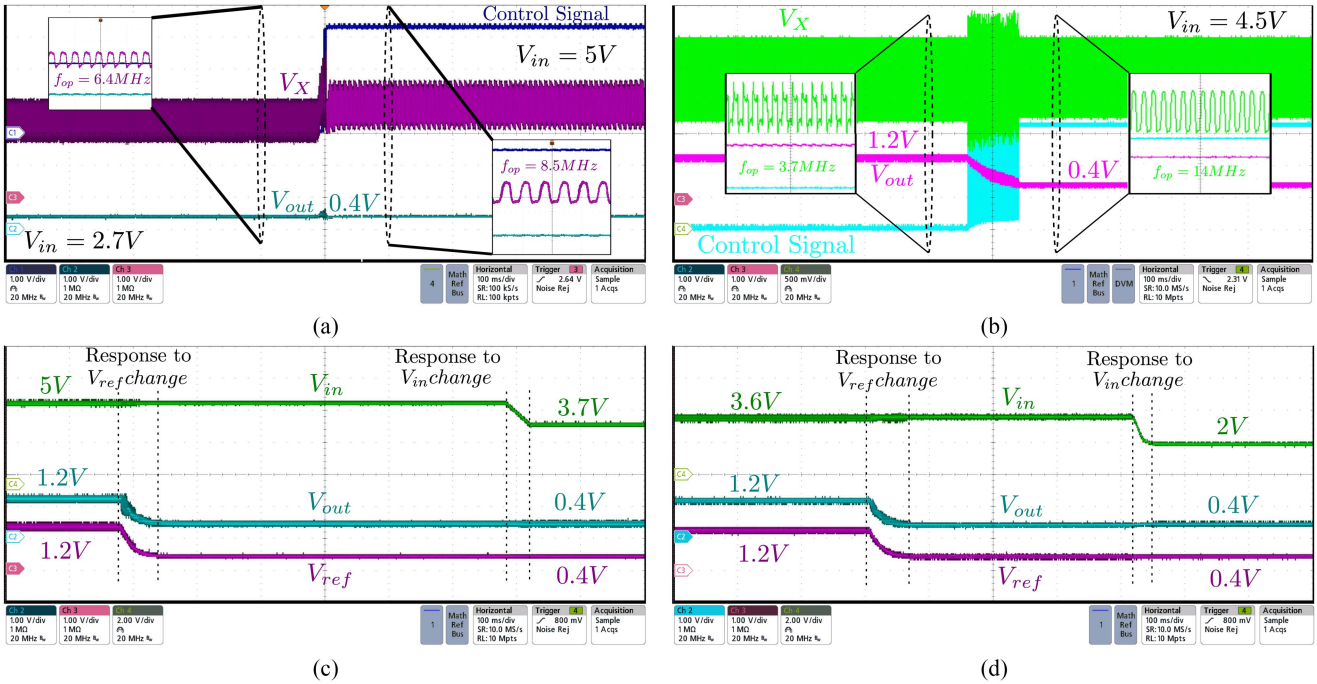

Fig. 21. Measured waveforms of the converter response under the following conditions: (a) Switching pattern change triggered by a step in input voltage from 2.7 V to 5 V. (b) Reference voltage V_{ref} changed from 1.2 V to 0.4 V while maintaining a fixed input voltage of 4.5 V while the converter operates in Pattern A. (c) A single change in V_{ref} from 1.2 V to 0.4 V, followed by a change in V_{in} from 5 V to 3.7 V while the converter operates in Pattern A. (d) A single change in V_{ref} from 1.2 V to 0.4 V, followed by a change in V_{in} from 3.6 V to 2 V while the converter operates in Pattern B.

Measurements from the transient tests in Fig. 21, where V_{in} is swept from 2 to 5 V, demonstrate that node V_X transitions symmetrically to the corresponding voltage levels. This behavior indicates proper voltage balancing of the flying capacitors. Fig. 21(a) illustrates the transition of the converter between operating patterns: from pattern B, activated when V_{in} is below 3.6 V, where only three of the four modules are enabled, to pattern A, where all four modules are activated as V_{in} rises above 3.6 V. The steady-state waveforms of node V_X confirm effective capacitor voltage balancing in both patterns.

Fig. 21(b) shows the dynamic response of the converter to a V_{ref} step from 1.2 to 0.4 V, with an approximate fall time of 100 ms, along with the corresponding output of the window comparator. The control loop demonstrates fast and accurate tracking of the reference voltage during the transition. Fig. 21(c) and (d) further illustrate the output voltage regulation under two test conditions: 1) a single-step transition in V_{ref} from its maximum to minimum value, and 2) a full-range sweep of V_{in} while operating under both Pattern A and Pattern B. Measured efficiency data for a range of input voltages, output voltages, and load currents are presented in Fig. 22, covering the full operating envelope of the converter. A peak efficiency of 88% is achieved. The converter's power losses are primarily proportional to the load current and only weakly dependent on the output voltage. As a result, under similar load conditions, the efficiency decreases at lower output voltages, as shown in Fig. 22, due to reduced output power while losses remain relatively constant. Measured efficiency data for a range of input voltages, output voltages, and load currents are presented in Fig. 22, covering the full operating envelope of the converter. A peak efficiency of 88% is achieved. The converter's power losses are primarily proportional to the load current and only weakly dependent on the output voltage; therefore, under similar load conditions, the efficiency decreases at lower output voltages, as shown in Fig. 22, because the output power is reduced while losses remain relatively constant. From these measured efficiency curves, the maximum power loss of the converter is approximately 0.5 W, which determines the worst-case heat dissipation in the IC. Since the IC is placed at the center of a CQFP-type package and connected to the package pads by wire bonds, heat can be dissipated through three main paths, as illustrated in Fig. 24. First direct junction-to-air exchange from the exposed die surface inside the cavity. second, junction-to-case conduction through the backside of the die into the package body and thermal pad, and third, junction-to-pins via the wire bonds and package leads into the PCB copper. The thermal resistances of these paths are denoted $R_{\theta JA}$, $R_{\theta JC}$, and $R_{\theta JP}$, respectively. For a conservative estimate, we consider only the junction-to-case path; assuming a typical value of $R_{\theta JC} \approx 2\,^{\circ}\text{C/W}$ for a CQFP package and $P_{c,\max} \approx 0.5\,\text{W}$, the junction temperature can be approximated as

$$T_{\text{j}} = T_{\text{ambient}} + R_{\theta JC} P_{D,\max} \approx 28\,^{\circ}\text{C}$$

indicating that the temperature rise is negligible and no heatsink is required for this converter.

To further analyze the efficiency, Fig. 23 presents an estimated breakdown of loss components across different operating points. At high load currents, losses are predominantly due to parasitic resistances from both the on-chip interconnects and package

TABLE II
COMPARISON OF THE PROPOSED IRMMC CONVERTER WITH STATE-OF-THE-ART CONVERTERS

Publication	[19] JSSC'2022	[8] TPEL'2021	**This Work**	[27] APEC'2020	[7] JSSC'2019	[23] TCAS'2021
Technology	180 nm bulk	130 nm BCD	**180 nm**	130 nm	28 nm FDSOI	65 nm
Topology	Hybrid (Cascaded SC)	Three-Level Buck	**IRMMC**	3Φ-ReSC	Four-Level Buck	3Φ-ReSC
Power MOSFET Type	5, 1.8 V	5 V	**1.8 V**	2 * 1.5 V Switches (Segmented)	1.5 V	1.2 V
V_{in}	4-6 V	8 V	**2 - 5.5 V**	3-4.5 V	2.8 - 4.2 V	2.3 – 2.5 V
V_{out}	0.4 – 1.2 V	1.8 - 3.3 V	**0.4 – 1.2 V**	1.2 – 1.8 V	0.6 - 1.2 V	0.4 – 0.625 V
F_{sw}	1.4 -1.6 MHz	0.8 - 1 MHz	**1.25 - 25 MHz**	$\leq$ 47.5 MHz	$\leq$ 67 MHz	10 MHz
Inductor	240 nH	10 μ H	**0.8 nH (on-package)+ 17 nH**	9 nH (on-chip), 10 nH	3 nH (on-chip)	10 nH
$C_{fly-resonant}$	2 * 4.7 μ F, 10 μ F	2 * 4.7 μ F	**4 * (6 * 0.47 μ F) − 290 nF resonant**	2 * 1 nF (on-chip)	2 * 5 nF (on-chip)	5.6 nF (on-chip) + 5.6 nF
C_{OUT}	14.4 μ F	NR	**1 μF**	10 nF (on-chip), 100 nF	NR	22 nF
Peak I_{OUT}	1 A	550 mA	**1.7 A**	120 mA	12 mA	130 mA
Chip area	7.82 mm^2	20.25 mm^2	**9 mm^2**	8.41 mm^2	1.5 mm^2	1.39 mm^2
Peak Output Power	1.1 W	1.35 W	**2 W**	216 mW	40 mW	81.25 mW †
Peak Power Density (W / mm^2)	0.14	0.067	**0.22**	0.026	0.027	0.059
Peak efficiency @ P_{out}	96.9% @ 0.18 W	88.6% @ 1.2 W	**88% @ 0.98** W	NA	NA	NA

† Estimated from the reference
NR - Not Reported
NA - Not Applicable

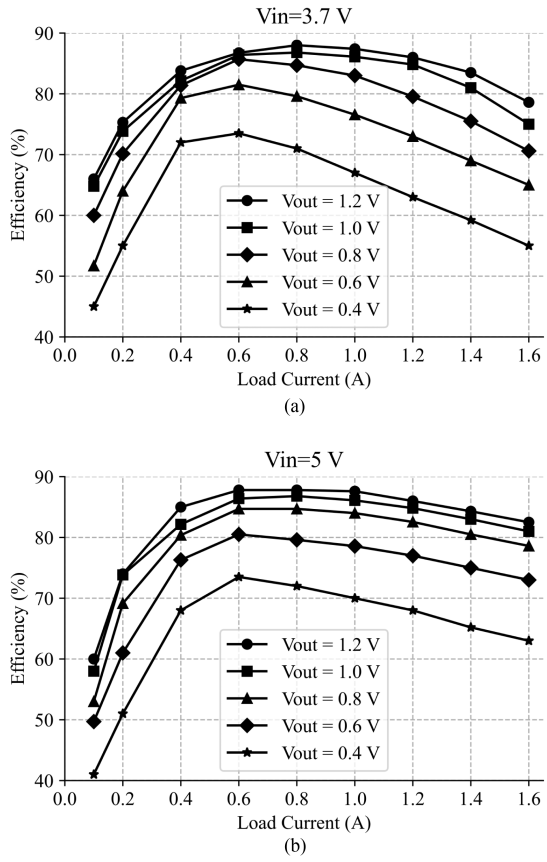

Fig. 22. Measured efficiency across various input voltages, load currents, and output voltages. (a) $V_{\text{in}} = 3.7\,\text{V}$. (b) $V_{\text{in}} = 5\,\text{V}$

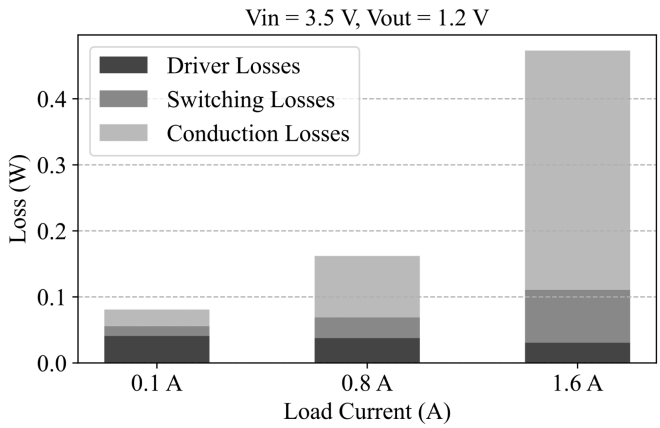

Fig. 23. Estimated power loss breakdown for $V_{\text{in}} = 3.5\,\text{V}$ and $V_{\text{out}} = 0.9\,\text{V}$ under pattern B operation of the converter.

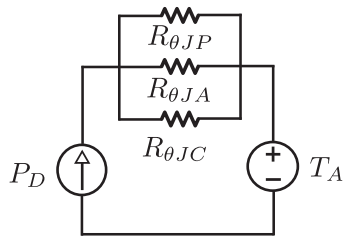

Fig. 24. Thermal equivalent circuit of the IC.

traces. This highlights the potential for significant efficiency improvement through enhanced packaging technologies, particularly under high-current conditions.

Table II summarizes the performance of the IRMMC converter and compares it with prior-art hybrid converters that are Li-ion compatible. The IRMMC converter achieves the highest power density per the total die area of $0.22\,\text{W/mm}^2$, where the paek efficiency at this point is 81.3%. Notably, this converter supports the widest input voltage range $(2 - -5.5\,\text{V})$

and delivers the highest peak output power $(2\,\mathrm{W})$, significantly outperforming others in terms of load capacity. The reported papers are categorized into two groups. low-power/high-frequency and high-power/low-frequency designs. In most integrated implementations, watt-level converters are constrained to relatively low switching frequencies (typically below a few megahertz), whereas converters operating at tens of megahertz are usually limited to tens of milliwatts. This indicates that the proposed IRMMC occupies an intermediate design space, achieving nearly watt-level output power while still operating up to $25\,\mathrm{MHz}$, thereby combining performance characteristics that are traditionally separated in prior art. While reference [19] reports a higher peak efficiency, it employs $5\,\mathrm{V}$ devices, which limits both its portability to advanced CMOS nodes and its applicability in systems with varying or battery-based inputs. Also it has a relatively narrow $4 - -6\,\mathrm{V}$ input range, larger off-chip passives, and dedicated active balancing circuitry. Jung et al. [8] also uses high-voltage devices with a fixed input voltage. Moreover, due to the use of relatively large external inductors and capacitors, its practical power density is reduced once passives are accounted for. On the other hand, the IRMMC is implemented entirely with low-voltage standard CMOS devices, maintains soft-switched operation over a wider input range, and leverages resonant energy transfer with compact passives. As a result, the proposed IRMMC achieves higher usable output current and peak power density with a simpler, inherently self-balancing control core.

V. Conclusion

This article presents a fully soft-switched reconfigurable integrated resonant modular multilevel converter (IRMMC) implemented in $180\,\mathrm{nm}$ CMOS, combining multilevel voltage division, resonant power conversion, and modular reconfiguration to enable high efficiency and wide input voltage operation without complex control. A dc to ac module in the first stage, dynamically controlled based on input voltage, extends the input range. A unified capacitor balancing strategy maintains equal flying capacitor voltages across all modes, simplifying design and improving reliability. The integration of an *LLC* resonant tank and active rectifier enables fully ZVS for all power switches, minimizing losses and supporting high-frequency operation with compact passives. Frequency control provides continuous, wide-range output voltage regulation under varying input and load conditions, without added control complexity. Measurements confirm 88% peak efficiency, $2\,\mathrm{W}$ maximum output power, and excellent regulation from 2 to $5.5\,\mathrm{V}$ input. Compared to prior art, IRMMC achieves superior power density $(0.22\,\mathrm{W/mm^2})$, higher load support, and competitive efficiency, making it ideal for on-chip or package-integrated power management in compact, battery-powered devices.

References

[1] M. Araghchini et al., "A technology overview of the powerchip development program," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4182–4201, Sep. 2013.

[2] C. R. Sullivan, D. V. Harburg, J. Qiu, C. G. Levey, and D. Yao, "Integrating magnetics for on-chip power: A perspective," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4342–4353, Sep. 2013.

[3] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[4] G. Villar-Piqué, H. J. Bergveld, and E. Alarcón, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4156–4167, Sep. 2013.

[5] X. Liu, C. Huang, and P. K. T. Mok, "A 50MHz 5V 3W 90% efficiency 3-level buck converter with real-time calibration and wide output range for fast-DVS in 65 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, 2016, pp. 1–2.

[6] P. Kumar et al., "A 0.4V 1V 0.2A/mm^2 70% efficient 500MHz fully integrated digitally controlled 3-level buck voltage regulator with on-die high density mim capacitor in 22 nm tri-gate CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2015, pp. 1–4.

[7] S. S. Amin and P. P. Mercier, "A fully integrated li-ion-compatible hybrid four-level DC–DC converter in 28-nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019.

[8] W. Jung et al., "Dual-path three-level buck converter with loop-free autocalibration for flying capacitor self-balancing," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 51–55, Jan. 2021.

[9] A. Abdulslam and P. P. Mercier, "A symmetric modified multilevel ladder PMIC for battery-connected applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 767–780, Mar. 2020.

[10] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[11] N. Butzen and M. Steyaert, "12.2 a 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40 nm CMOS using scalable parasitic charge redistribution," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 220–221.

[12] R. Jain et al., "A 0.45–1 V fully-integrated distributed switched capacitor DC-DC converter with high density mim capacitor in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[13] H. Meyvaert, G. Villar Piqué, R. Karadi, H. J. Bergveld, and M. S. J. Steyaert, "A light-load-efficient 11/1 switched-capacitor DC-DC converter with 94.7% efficiency while delivering 100 mw at 3.3 v," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2849–2860, Dec. 2015.

[14] J. Jiang, W.-H. Ki, and Y. Lu, "Digital 2-/3-phase switched-capacitor converter with ripple reduction and efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1836–1848, Jul. 2017.

[15] D. Lutz, P. Renz, and B. Wicht, "12.4 a 10mw fully integrated 2-to-13v-input buck-boost SC converter with 81.5% peak efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 224–225.

[16] A. Amoorezaei, S. A. Khajehoddin, N. Rezaei-Hosseinabadi, and K. Moez, "A low-cost cell-level differential power processing CMOS IC for single junction photovoltaic cells," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13985–14001, Dec. 2021.

[17] P. Assem, W.-C. Liu, Y. Lei, P. K. Hanumolu, and R. C. N. Pilawa-Podgurski, "Hybrid dickson switched-capacitor converter with wide conversion ratio in 65-nm cmos," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, Sep. 2020.

[18] X. Yang et al., "A 5V input 98.4% peak efficiency reconfigurable capacitive-sigma converter with greater than 90% peak efficiency for the entire 0.4 1.2V output range," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 108–110.

[19] Z. Xia and J. T. Stauth, "A cascaded hybrid switched-capacitor DC–DC converter capable of fast self startup for USB power delivery," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1854–1864, Jun. 2022.

[20] T. S. Chang et al., "Design and implementation of hybrid DC-DC converter: A review," *IEEE Access*, vol. 11, pp. 30498–30514, 2023.

[21] P. H. McLaughlin, Z. Xia, and J. T. Stauth, "11.2 a fully integrated resonant switched-capacitor converter with 85.5% efficiency at 0.47w using on-chip dual-phase merged-LC resonator," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2020, pp. 192–194.

[22] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6966–6977, Dec. 2015.

[23] C. Wang, Y. Lu, and R. P. Martins, "A highly integrated 3-phase 4:1 resonant switched-capacitor converter with parasitic loss reduction and fast pre-charge startup," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2608–2612, Jul. 2021.

[24] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jun. 2012.
[25] P. Renz, M. Kaufmann, M. Lueders, and B. Wicht, "8.6 a fully integrated 85%-peak-efficiency hybrid multi ratio resonant DC-DC converter with 3.0-to-4.5V input and 500 μA -to-120Ma load range," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2019, pp. 156–158.
[26] P. Renz, N. Deneke, and B. Wicht, "Dynamic modeling and control of a resonant switched-capacitor converter with switch conductance regulation," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, 2020, pp. 1–4.
[27] P. Renz, M. Lueders, and B. Wicht, "A 47 MHz hybrid resonant SC converter with digital switch conductance regulation and multi-mode control for li-ion battery applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 15–18.
[28] J. Castellanos, "Integrated hybrid switched converters: A review," *J. Integr. Circuits Syst.*, vol. 17, no. 1, pp. 1–12, 2022.
[29] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[30] S. Alatai et al., "A review on state-of-the-art power converters: Bidirectional, resonant, multilevel converters and their derivatives," *Appl. Sci.*, vol. 11, no. 21, 2021, Art. no. 10172. [Online]. Available: https://www.mdpi.com/2076-3417/11/21/10172
[31] A. Benevieri, S. Cosso, A. Formentini, M. Marchesoni, M. Passalacqua, and L. Vaccaro, "Advances and perspectives in multilevel converters: A comprehensive review," *Electronics*, vol. 13, no. 23, 2024, Art. no. 4736. [Online]. Available: https://www.mdpi.com/2079-9292/13/23/4736
[32] D. Kim et al., "A 4.2-to-0.5-V, 0.8-μA–0.8-mA, power-efficient three-level simo buck converter for a quad-voltage RISC-V microprocessor," *IEEE Trans. Very Large Scale Integration Syst.*, vol. 33, no. 1, pp. 193–206, Jan. 2025.
[33] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.
[34] S. da Silva Carvalho, M. Halamıček, N. Vukadinović, and A. Prodić, "Digital pwm for multi-level flying capacitor converters with improved output resolution and flying capacitor voltage controller stability," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, 2018, pp. 1–7.
[35] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-dvs," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, Feb. 2018.
[36] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11429–11441, Nov. 2019.
[37] W. C. Liu, R. Pilawa-Podgurski, and P. H. Ng, "An 83mA 96.8% peak efficiency 3-level boost converter with full-range auto-capacitor-calibrating pulse frequency modulation," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2019, pp. 1–4.
[38] W. C. Liu, P. H. Ng, and R. Pilawa-Podgurski, "A three-level boost converter with full-range auto-capacitor-compensation pulse frequency modulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 744–755, Mar. 2020.
[39] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[40] X. Zhang et al., "An outphase-interleaved switched-capacitor hybrid buck converter with relieved capacitor inrush current and cout-free operations," *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 1078–1092, Apr. 2024.
[41] Q. Ma et al., "A cross-coupled hybrid switched-capacitor buck converter with extended conversion range and enhanced DCR loss reduction," *IEEE J. Solid-State Circuits*, vol. 59, no. 10, pp. 3192–3203, Oct. 2024.
[42] C. Chen, J. Liu, and H. Lee, "A 92.7%-efficiency 30A 48V-to-1V dual-path hybrid Dickson converter for PoL applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 1989–1994.
[43] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with softcharging switched-capacitor energy transfer," in *Proc. IEEE Power Electron. Specialists Conf.*, 2008, pp. 4008–4015.
[44] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of double step-down two-phase buck converter for VRM," in *Proc. 27th Int. Telecommun. Conf.*, 2005, pp. 497–502.
[45] G. Cai, R. P. Martins, and Y. Lu, "A resonant switched-capacitor parallel inductor hybrid buck converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 72, no. 5, pp. 2432–2443, May 2025.
[46] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10903–10919, Sep. 2022.
[47] C. Schaef and J. T. Stauth, "A highly integrated series–parallel switched-capacitor converter with 12 V input and quasi-resonant voltage-mode regulation," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 456–464, Jun. 2018.
[48] S. R. Pasternak, M. H. Kiani, J. S. Rentmeister, and J. T. Stauth, "Modeling and performance limits of switched-capacitor DC–DC converters capable of resonant operation with a single inductor," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1746–1760, Dec. 2017.
[49] P. H. McLaughlin, Z. Xia, and J. T. Stauth, "A monolithic resonant switched-capacitor voltage regulator with dual-phase merged-LC resonator," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3179–3188, Dec. 2020.
[50] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.
[51] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4946–4958, May 2020.
[52] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Berlin, Germany: Springer Science & Business Media, 2007.
[53] Y. Liu and F. Z. Peng, "A modular multilevel converter with self-voltage balancing part I: Mathematical proof," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1117–1125, Jun. 2020.
[54] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015.
[55] B. Yuan, L.-Q. Xiao, B.-Y. Wang, and J. Ying, "High-speed dynamic level shifter for high-side bootstrapped gate driver in high-voltage buck regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 9, pp. 3083–3087, Sep. 2021.
[56] A. Amoorezaei, S. A. Khajehoddin, and K. Moez, "A compact cuk-based differential power processing IC with integrated magnetics and soft-switching controller for maximized cell-level power extraction," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 4473–4490, Apr. 2024.
[57] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.
[58] A. Ballo, A. D. Grasso, and M. Privitera, "A design procedure for sizing comparators in active rectifiers using g_m/I_D technique," in *Proc. 35th SBC/SBMicro/IEEE/ACM Symp. Integr. Circuits Syst. Des.*, 2022, pp. 1–6.
[59] D. Jiao, Z. Hou, and J.-S. Lai, "LLC type resonant converter adopting peak current shaving with third harmonics injection for wide output voltage range application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2024, pp. 2232–2238.

Amir Mohammad Mohammadi (Graduate Student Member, IEEE) received the M.Sc. degree in electrical and computer engineering from the Isfahan University of Technology, Isfahan, Iran, in 2023. He is currently working toward the Ph.D. degree in electrical and computer engineering with the University of Alberta, Edmonton, AB, Canada.

From 2021 to 2023, he served as a national patent referee at the Intellectual Property Center of the Islamic Republic of Iran (IRI), Isfahan, Iran. His research interests include the design and optimization of power management integrated circuits, with a focus on resonant and multilevel power conversion techniques.

S. Ali Khajehoddin (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Queen's University, Kingston, ON, Canada, in 2010.

He currently holds a Senior University of Alberta Engineering Research Chair (UAERC) and is a Professor and Director of the University of Alberta Power Electronics Lab (uAPEL) in Edmonton, AB, Canada. He has co-founded several startups, including Behineh Niru, focused on smart metering and power analyzer technologies; SPARQ Systems, based on his Ph.D. research on durable photovoltaic microinverters and later taken public in 2021; and Enerbund, dedicated to developing scalable, grid-forming energy storage solutions. His research interests include the design and implementation of high-power-density power converters using advanced modeling techniques, innovative topologies, and modern control approaches for energy systems.

Dr. Khajehoddin was a recipient of several recognitions, including the University of Alberta Engineering Research Chair, the IEEE Canada Research Excellence Award, and several best paper awards at leading international conferences and journals, notably in IEEE TRANSACTIONS ON POWER ELECTRONICS (TPEL) in 2022 and 2024. He received the IEEE TPEL Associate Editor Excellence Award in 2025, served as an Associate Editor for IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, and is currently the Co-EIC of IEEE TRANSACTIONS ON POWER ELECTRONICS LETTERS.

Nasrin Rezaei-Hosseinabadi (Member, IEEE) was born in Isfahan, Iran, in 1986. She received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Isfahan University of Technology (IUT), Isfahan, in 2008, 2010, and 2016, respectively.

She has been an Assistant Professor with the Department of Electrical and Computer Engineering, IUT since 2016. She was a Visiting Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, in 2019. Her research interests include power management integrated circuit and energy harvesting system design.

Kambiz Moez (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tehran, Iran, in 1999, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Waterloo, Waterloo, Ontario, Canada, in 2002 and 2006, respectively.

Since 2007, he has been with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada, where he is currently a Professor and Associate Dean of Undergraduate Students - ECE. He has authored or co-authored more than 110 peer-reviewed journal articles and conference papers in his field of research. His research interests include the analysis and design of analog, radio frequency, and millimeter-wave CMOS integrated circuits and systems for a variety of applications, including wired/wireless communications and sensors, radio frequency energy harvesting, biomedical imaging, instrumentations, radars, and power electronics.

Dr. Moez is a Registered Professional Engineer in the province of Alberta. He has served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: Regular Papers from 2021 to 2023. He is currently serving as an Associate Editor for *IET Electronics Letters*.