A Numerically Efficient and Accurate Model for Real-Time Simulation of Solid-State Transformer Using Implicit-Explicit Integration Methods

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***Abstract*—Electromagnetic transient (EMT) models of power electronic converters are essential for converter design, control, and fault analysis. This article proposes a switching-function-based detailed equivalent model (SFB-DEM) using combined implicit and explicit (ImEx) multistep Gear's integration methods for numerically efficient and accurate EMT simulation. The proposed SFB-DEM integrates the benefits of ImEx solvers, featuring converter circuit decoupling, node number reduction, and constant nodal-network conductance(G)-matrix in the EMT model. The SFB-DEMs employing the ImEx 2nd and 3rd order Gear's (i.e., ImEx-G2O and ImEx-G3O) methods are implemented for solid-state transformer (SST) simulation. In addition, a switching interpolation technique is proposed and integrated with the ImEx-G2O and ImEx-G3O solvers to account for intra-time-step switching events. The proposed SST SFB-DEMs greatly accelerate the EMT simulation, compared to the conventional detailed model (DM) and variable conductance(G)-matrix DEM (VG-DEM). For the SST with 60 SMs, the proposed SFB-DEM with ImEx-G3O method achieves the EMT simulation speedup by 171 and 7.5 folds, compared to the DM and VG-DEM, respectively.**

***Index Terms*—Constant G-matrix, electromagnetic transient (EMT) program, implicit-explicit backward differentiation formula, solid-state transformer (SST), switching interpolation technique, switching-function-based detailed equivalent model (SFB-DEM).**

Nomenclature

SFB-DEM	Switching-function-based detailed equivalent model.
VG-DEM	Variable G-matrix detailed equivalent model.
A-stability	Absolute stability.
L-stability	Strong form of A-stability with limit of $\lim_{z\to-\infty} R(z) = 0$.
BDF	Backward differentiation formula.
TBE	Trapezoidal rule switching to Backward Euler.
ImEx-G2O	Implicit-explicit Gear's 2nd order method.
ImEx-G3O	Implicit-explicit Gear's 3rd order method.
ISOP	Input-series-output-parallel.
MFT	Medium-frequency transformer.

Received 13 August 2025; revised 30 November 2025; accepted 27 December 2025. Date of publication 2 January 2026; date of current version 20 March 2026. This work was supported by the Natural Sciences and Engineering Research Council (NSERC) of Canada. Recommended for publication by Associate Editor Z. Li. *(Corresponding author: Liwei Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3650144.

Digital Object Identifier 10.1109/TPEL.2025.3650144

I. Introduction

THE development of solid-state transformer (SST) (also known as a power electronic transformer) has attracted much attention from industry and academia [1], [2], [3], [4], [5]. The SST circuit topologies are commonly categorized into four types, i.e., single-stage, two-stage with low voltage dc (LVdc) link, two-stage with medium voltage dc (MVdc), and three-stage topologies [3], [4], [5], as presented in Fig. 1. An ISOP configuration is typically employed for the SST, realizing medium voltage ac (MVac) to LVdc conversion [2]. A three-phase SST following ISOP configuration often uses multilevel ac–dc converter as its Stage I, composed of ac chain-links with cascaded full-bridge submodules (FBSMs). Meanwhile, multiple dual-active-bridge (DAB) dc–dc converters are coupled with the cascaded FBSMs through MVdc capacitors as its Stage II. The DAB dc–dc converters play an important role to provide galvanic isolation between the MVdc and LVdc through MFTs, enabling bidirectional power flow and achieves high power density [6], [7].

However, the detailed model (DM) of the SST imposes tremendous computational burdens to electromagnetic transient (EMT) simulation due to its detailed representation of massive semiconductor switches and discrete circuit components. In order to enhance the numerical accuracy and simulation efficiency of the SST, various equivalent circuit modeling approaches were introduced in the prior art. A high-speed EMT modeling strategy of the SST was proposed in [8] and [9], which uses Norton equivalents to simplify the SST circuit into a two-port system for node number reduction. However, the SST system is decoupled through the ac voltages of the MFTs, which may lead to numerical inaccuracy for fast switching state changes of the FBSMs in DABs. An alternative circuit decoupling through a

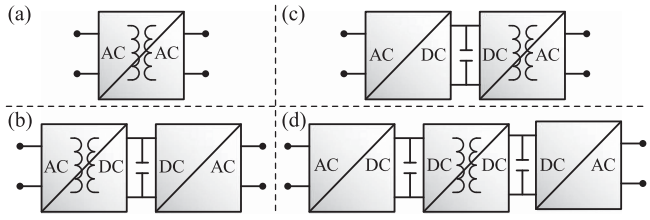

Fig. 1. SST configurations. (a) Single-stage. (b) Two-stage with LVdc link. (c) Two-stage with MVdc link. (d) Three-stage topology.

dc-link capacitor was achieved by employing the cut-set-matrix algorithm in [10], which boosted the simulation efficiency of the SST. However, the network G-matrix of this approach is time-variant since the semiconductor switches are represented by binary-value resistors, imposing a high computational burden due to frequent re-factorization of the G-matrix.

To address the abovementioned issues, various modeling efforts have been carried out to realize a constant network G-matrix. A discrete-time switch model was developed in [11] and [12], which features constant G-matrix by representing a semiconductor switch as an L or C element, depending on its switching states. However, the use of L/C incurs undesired fictitious voltage and current oscillations during switching transitions. Moreover, it can introduce unrealistically high virtual power losses [13]. In [14], [15], [16], [17], another type of modeling approach that leads to a constant G-matrix, namely, SFB-DEMs were proposed for modular multilevel converter (MMC) and multimodule SST. Thevenin equivalent circuit is used to represent cascaded submodules (SMs) in discrete-time domain and is updated based on switching functions and capacitor voltages of the SMs. Combined implicit- and explicit-type (ImEx-type) integration methods are employed in [14], [15], [16], [17] to discretize circuit components, i.e., the SM capacitor voltages using Forward Euler's (FE) method for network decoupling, and the rest of the network by implicit trapezoidal rule (TR) for the 2nd order numerical accuracy and absolute stability (A-stability).

However, there are two drawbacks when employing the TR-FE method in the EMT simulation of power converters. First, the numerical accuracy is limited due to the use of the 1st order solver, i.e., FE method. Second, the TR method may experience numerical oscillations due to its A-stability, but not L-stability [18], when system discontinuity presents, e.g., switching operations. The numerical oscillations can be eliminated by changing the solver from TR to Backward Euler (BE), namely TBE when switching transition occurs (also known as critical damping adjustment) [19], [20]. However, the numerical accuracy has to be sacrificed especially when the switching frequency is high, since the BE method has 1st-order accuracy [21].

To circumvent the abovementioned drawbacks, this article employs combined implicit and explicit (ImEx) Gear's 2nd or 3rd order methods (i.e., namely ImEx-G2O or ImEx-G3O) to discretize the circuit elements of the SST. Implicit Gear's method, (also known as backward differentiation formula, i.e., BDF), is a linear multistep ordinary differential equation (ODE) solver, especially designed for stiff ODEs [18]. While Gear's 2nd order method has both A- and L-stability, the stability region of Gear's 3rd order method contains a large part of the left half-plane and in particular the whole negative real axis. Thus, the high-order implicit Gear's methods have much larger numerical stability regions than other implicit multistep methods, such as Adams-Moulton methods. Similarly, the explicit Gear's methods (also known as explicit BDF methods [22], [23]) have larger numerical stability regions than the explicit Adams methods (Adams-Bashforth methods) with the same order. Therefore, combined ImEx Gear's methods integrate the merits of superior numerical accuracy due to the use of high-order multistep Gear's solvers and SST circuit decoupling because explicit Gear's method is used to discretize the dc-link capacitors of the SST.

For fixed-time-step EMT simulation of power converters, switching events may occur in between two consecutive integer time steps. Inaccurate switching event location will introduce significant numerical errors to the simulation results. Switching interpolation techniques were proposed and implemented in [24], [25], [26], [27], [28], [29], [30] to account for intrastep switching for the TR method. However, a switching interpolation technique for the SFB-DEMs with combined ImEx multistep ODE solvers is missing in the literature.

As shown in Table I, the comparisons of different modeling approaches are performed regarding their computational efforts, capability of representing converter blocking mode, and numerical accuracy by high-order integration rules and switching interpolation. Most of the prior-art equivalent circuit models, e.g., [8], [9], [10], [31], and [32], achieve internal node elimination to accelerate the EMT-type simulation for large-scale converter system. However, these methods commonly represent the semiconductor switches by two-value resistors. Consequently, refactorization of the network conductance (G)-matrix becomes inevitable, which result in tremendous computational burdens. The EMT modeling strategy in [31] achieves a constant G-matrix by adopting conventional L/C-associated discrete circuit [11]. Nevertheless, it introduces spurious numerical ringing in voltages and currents when encountering switching transients. In addition, several efficient EMT modeling approaches have been compared and analyzed in [29] and [30], where dynamic behaviors of the power converters are represented by switching functions which achieve a constant network G-matrix. Nevertheless, these modeling approaches in [29] and [30] use basic two-level power converters and have not achieved a reduction in circuit nodes and circuit decoupling. A high-fidelity device-level EMT modeling strategy has been proposed for numerically efficient parallel simulation of MMC in [33]. It is assumed that the MMC arm current is constant for two adjacent time steps to decouple the SMs from a converter arm. This equivalent circuit model achieves a constant G-matrix using the transmission line model (TLM) technique [34]. However, the efficient parallel MMC model in [33] cannot represent the converter in the IGBT-blocked state and has four node voltages to be solved in each SM.

From the perspective of numerical accuracy, the prior-art equivalent circuit models use either implicit TR, which leads to a coupled network with a high-dimensional G-matrix, or employ a

TABLE I
COMPARISON OF EQUIVALENT CIRCUIT MODELS FOR EFFICIENT EMT SIMULATION

Model Type	Internal Node Reduction	Converter Stage Decoupling	Constant Network G-matrix	IGBT Blocked Mode	2nd-order or Higher Numerical Accuracy	Switching Interpolation
VG-DEM in [8]–[10]	✓	✓	×	✓	✓	×
FPGA DEM in [31]	✓	✓	✓	×	×	×
FPGA DEM in [32]	✓	✓	×	×	×	×
Multitimescale EMT Model in [35]	✓	✓	×	×	×	×
Inverter Model in [29]	×	×	✓	×	✓	✓
Efficient EMT Models in [30]	×	×	✓	✓	✓	✓
High-Fidelity EMT Model in [33]	✓	✓	✓	×	✓	×
SFB-DEM in [16]	✓	✓	✓	✓	×	✓
Proposed SFB-DEMs	✓	✓	✓	✓	✓	✓

combination of TR and FE to achieve circuit decoupling, which sacrifices numerical accuracy since the FE method achieves only 1st-order accuracy. Compared to the prior-art EMT modeling strategies, the proposed SFB-DEMs with combined implicit-explicit-type multistep solvers fulfill all the modeling features listed in Table I, which achieve superior 2nd-order (ImEx-G2O) or 3rd-order (ImEx-G3O) accuracy and accelerated simulation speed simultaneously. The novelty and main contributions of this article are summarized below.

1) A combined multistep ImEx Gear's solver is proposed to discretize the circuit elements of the multimodule SST. The use of explicit Gear's method to discretize DC-link capacitors enables converter decoupling and constant nodal-network G-matrix, which greatly accelerates the EMT simulation.
2) The proposed high-order ImEx Gear's (ImEx-G2O or ImEx-G3O) solver offers better numerical accuracy compared to the first-order solvers, e.g., BE+FE or mixed 1st and 2nd order solver, TBE. Numerical oscillations because of the TR solver to simulate switching operations are also avoided by the implicit Gear's solvers.
3) Switching interpolation technique is proposed for the ImEx-Gear's solver in the SST. The simulation accuracy is enhanced for the cases of large time-step EMT simulation.
4) The proposed SFB-DEM with ImEx Gear's solver provides a universal modeling framework for an arbitrary voltage source converter with a dc-link capacitor. It permits high flexibility in representing de-blocking and blocking modes of the power converters with a reduced number of nodes, compared to the binary-value resistor or L/C switch modeling.

II. COMPARISON OF DEMS WITH VARIOUS NUMERICAL INTEGRATION METHODS

From the perspective of nodal-network G-matrices, the detailed equivalent models (DEMs) can be broadly categorized into two groups, i.e., DEMs with variable G-matrices (VG-DEMs), and switching-function-based DEMs (SFB-DEMs) with constant G-matrices. Meanwhile, it is also crucial to select numerical integration methods that provide high numerical accuracy, stability, and low computational complexity for the EMT simulation.

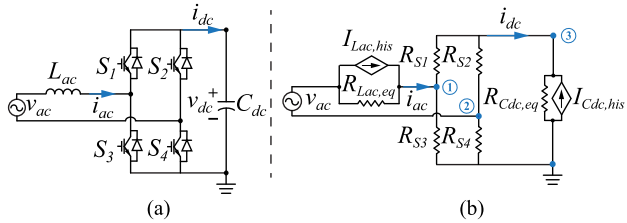

Fig. 2. Schematic of FB converter. (a) Circuit in continuous-time domain. (b) RSM in discrete-time domain.

A. Full-Bridge Converter

This subsection compares two EMT modeling strategies, i.e., the resistive switch model (RSM) and SFB-DEM for a full-bridge (FB) converter.

1) Resistive Switch Model: In the RSM, two-value (ON/OFF) resistor with a small resistance for ON state and a large resistance for OFF state is used to represent a semiconductor switch [36]. Fig. 2 shows the schematic of the FB converter and its RSM, where the line inductor L_{ac} and dc-link capacitor C_{dc} are discretized using implicit integration methods (e.g., BE or TR) and are expressed in Norton equivalent. As shown in Fig. 2(b), the historical terms of the ac line inductor L_{ac} and dc capacitor C_{dc} are denoted by $I_{\text{Lac,his}}$ and $I_{\text{Cdc,his}}$, which are in parallel with their equivalent resistors, $R_{\text{Lac,eq}}$ and $R_{\text{Cdc,eq}}$, in the discrete-time domain. $R_{S1} - R_{S4}$ are the binary-value resistors, corresponding to the switches $S_1 - S_4$. As presented in Fig. 2(b), the RSM of the FB converter has 3 node voltages $v_1 - v_3$ to be solved. The nodal equation G-matrix is time-variant due to the semiconductor switching and has to be refactorized when switching states are changed.

2) SFB-DEM: An FB converter can operate in positive insertion, negative insertion, bypass, and IGBT-blocked (diode) modes, as shown in Fig. 3. The proposed SFB-DEM is derived by using the ac-side output voltages of the FB converter for positive and negative ac current directions. As shown in Fig. 3(e), the proposed SFB-DEM consists of two equivalent voltage sources, V_{sp} and V_{sn} corresponding to positive and negative ac current directions. Two diodes are in series with the two equivalent voltage sources to represent the blocking mode of the FB converter.

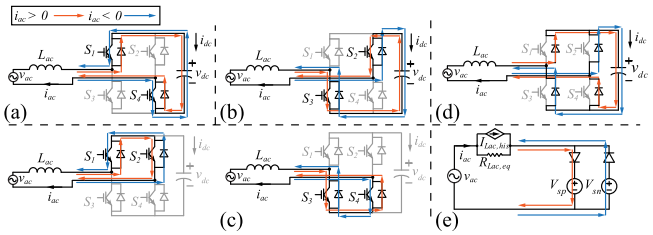

Fig. 3. Switching modes of SFB-DEM for FB converter. (a) Positive insertion. (b) Negative insertion. (c) Bypass. (d) Blocking. (e) Circuit of SFB-DEM.

TABLE II
EQUIVALENT SOURCE VOLTAGES UNDER DIFFERENT SWITCHING STATES

Switching Mode	S_1	S_2	S_3	S_4	V_{sp}	V_{sn}
Positive Insertion	1	0	0	1	v_{dc}	
Negative Insertion	0	1	1	0	$-v_{dc}$	
Bypass	1	1	0	0	0	
	0	0	1	1	0	
Blocking (Diode)	0	0	0	0	v_{dc}	$-v_{dc}$

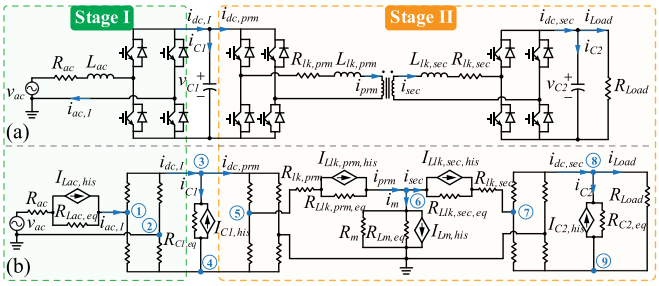

Fig. 4. Schematic of 2-stage AC–DC–DC converter. (a) DM. (b) VG-DEM.

For the purpose of network decoupling, the dc-link capacitor is discretized by using an explicit integration solver, e.g., FE as

$$v_{\mathrm{dc}}\ (t+\Delta t) = v_{\mathrm{dc}}\ (t) + \frac{\Delta t}{C_{\mathrm{dc}}} i_{\mathrm{dc}}\,(t) \tag{1}$$

where Δt denotes the simulation time step. In the deblocking mode, as shown in Fig. 3(a)–(c), the values of V_{sp} and V_{sn} are derived according to the switching modes in Table II. When the FB converter operates in the IGBT-blocking mode, as shown in Fig. 3(d), the ac current conducts through the diodes. Therefore, the values of V_{sp} and V_{sn} are opposite according to the ac current direction as shown in Fig. 3(e).

B. 2-Stage AC–DC–DC Converter

This section proposes the SFB-DEM and compares it with the conventional VG-DEMs in a two-stage ac–dc–dc converter, which is recognized as a single module of the multilevel multi-module SST converter.

1) Detailed Model: As presented in Fig. 4(a), the converter DM comprises two converter stages, i.e., an FB ac/dc converter in Stage I and a DAB dc–dc converter in Stage II, coupled through MVdc-link capacitor C_1.

In Stage I, MVac terminal of the FB converter is connected to an ac voltage source v_{ac} through line resistance R_{ac} and inductance L_{ac} while $i_{\mathrm{ac},I}$ and $i_{\mathrm{dc},I}$ are the ac and dc currents. In Stage II, the DAB converter contains an MFT whose winding resistances and leakage inductances on primary and secondary sides are denoted by $R_{lk,\mathrm{prm}}$, $L_{lk,\mathrm{prm}}$, $R_{lk,\mathrm{sec}}$,and $L_{lk,\mathrm{sec}}$, respectively. In Stage II, C_2 denotes the LVdc-link capacitor, which is in parallel with a resistive load R_{Load}. i_{prm}, i_{sec}, and $i_{\mathrm{dc,prm}}$, $i_{\mathrm{dc,sec}}$ are the ac and dc currents on both sides of the MFT, respectively.

2) VG-DEM of 2-Stage Converter: This section evaluates the VG-DEMs implemented by various implicit-type solvers, such as BE, TR, implicit G2O (Im-G2O), and G3O (Im-G3O). As depicted in Fig. 4(b), the VG-DEM is formulated by the companion circuits of inductors and capacitors in the discrete-time domain, i.e., historical current sources in parallel with equivalent resistances. A semiconductor switch is represented using a binary-value resistor with its resistance equal to R_{ON} or R_{OFF}, which is time-variant in accordance with the switching states of the semiconductor device. In Stage II, a T-equivalent circuit is employed to model the MFT with all secondary variables referred to the primary side.

Initially, the historical current and equivalent resistance of each circuit component are computed, based on a selected solver. Table III provides a detailed summary of the Norton equivalents of inductors and capacitors in the discrete-time domain for various implicit-type solvers. In Table III, t_{k+1} denotes the present simulation time step and t_{k+1-n} represents the previous nth time step. As depicted in Fig. 4(b), $I_{\mathrm{Lac,his}}$ and $I_{C1,\mathrm{his}}$ are the historical currents of the Stage I ac line inductor and MVdc-link capacitor, respectively. In Stage II, $I_{Llk,\mathrm{prm,his}}$, $I_{Llk,\mathrm{sec,his}}$, $I_{Lm,\mathrm{his}}$, and $I_{C2,\mathrm{his}}$ are the historical currents of $L_{lk,\mathrm{prm}}$, $L_{lk,\mathrm{sec}}$, L_m, and C_2, which are in parallel with their equivalent resistances, correspondingly.

Since the discretization of the MVdc-link capacitor C_1 using an implicit solver produces $R_{C1,\mathrm{eq}}$ in parallel with $I_{C1,\mathrm{his}}$ as shown in Fig. 4(b), the two converter stages become inherently coupled and must be solved all together in one nodal equation. Thereafter, the nodal equation is formulated as

$$\boldsymbol{G}_{\boldsymbol{N}\times\boldsymbol{N}}\boldsymbol{V}_{\mathbf{node},\boldsymbol{N}\times 1}\ (t_{k+1}) = \boldsymbol{I}_{\mathbf{his},\boldsymbol{N}\times 1}\ (t_k) \tag{2}$$

wherein N denotes the node number.

The node voltages $\boldsymbol{V}_{\mathbf{node},\boldsymbol{N}\times 1}$ at t_{k+1} can be solved from the linear system (2) using matrix factorization such as LU factorization. It is noted in Fig. 4(b) that the VG-DEM contains nine nodes in total, leading to a high-dimensional network G-matrix. With $\boldsymbol{V}_{\mathbf{node},\boldsymbol{N}\times 1}(t_{k+1})$ known, the present time-step network solutions, including the voltages and currents from the ac and dc sides of the converter, can be updated accordingly. In summary, both frequent refactorization of the network G-matrix and computation of the high-dimensional nodal equation of the VG-DEM impose large computational burdens.

3) SFB-DEM of 2-Stage Converter: This subsection proposes the SFB-DEM for the two-stage ac–dc–dc converter, which combines the implicit-type (see Table III) and explicit-type solvers (see Table IV) (i.e., ImEx-type solvers) to discretize different circuit components. As depicted in Fig. 5, the inductors from the two converter stages are commonly discretized and

TABLE III
NORTON EQUIVALENT BY IMPLICIT-TYPE NUMERICAL INTEGRATION METHODS

Component	R_{eq} &I_{his}	BE	TR	Implicit G2O (Im-G2O)	Implicit G3O (Im-G3O)
Capacitor	$R_{C,\text{eq}}$	$\Delta t/C$	$\Delta t/2C$	$2\Delta t/3C$	$6\Delta t/11C$
	$I_{C,\text{his}}$	$-\frac{1}{R_{C,eq}}v_C(t_k)$	$-i_C(t_k)-\frac{1}{R_{C,\text{eq}}}v_C(t_k)$	$-\frac{1}{R_{C,\text{eq}}}\left(\frac{4}{3}v_C(t_k)-\frac{1}{3}v_C(t_{k-1})\right)$	$-\frac{1}{R_{C,\text{eq}}}\left(\frac{18}{11}v_C(t_k)-\frac{9}{11}v_C(t_{k-1})+\frac{2}{11}v_C(t_{k-2})\right)$
Inductor	$R_{L,\text{eq}}$	$L/\Delta t$	$2L/\Delta t$	$3L/2\Delta t$	$11L/6\Delta t$
	$I_{L,\text{his}}$	$i_L(t_k)$	$i_L(t_k)+(1/R_{L,\text{eq}})\cdot v_L(t_k)$	$\frac{4}{3}i_L(t_k)-\frac{1}{3}i_L(t_{k-1})$	$\frac{18}{11}i_L(t_k)-\frac{9}{11}i_L(t_{k-1})+\frac{2}{11}i_L(t_{k-2})$

TABLE IV
DISCRETIZATION OF CAPACITOR VOLTAGE EQUATION USING EXPLICIT-TYPE NUMERICAL INTEGRATION METHODS

	FE	Explicit G2O (Ex-G2O)	Explicit G3O (Ex-G3O)
$v_C(t_{k+1})$	$v_C(t_k)+\frac{\Delta t}{C}i_C(t_k)$	$\frac{4}{3}v_C(t_k)-\frac{1}{3}v_C(t_{k-1})$ $+\frac{2\Delta t}{3C}(2i_C(t_k)-i_C(t_{k-1}))$	$\frac{18}{11}v_C(t_k)-\frac{9}{11}v_C(t_{k-1})+\frac{2}{11}v_C(t_{k-2})$ $+\frac{6\Delta t}{11C}(3i_C(t_k)-3i_C(t_{k-1})+i_C(t_{k-2}))$

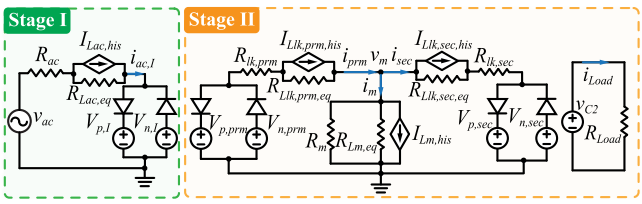

Fig. 5. Schematic of SFB-DEM for 2-stage AC–DC–DC converter.

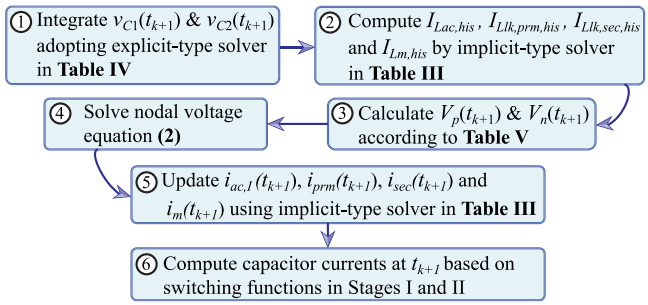

Fig. 6. Simulation flowchart of SFB-DEM for 2-stage AC–DC–DC converter.

TABLE V
VALUES OF EQUIVALENT AC VOLTAGE SOURCES

Converter Stage	Stage I		Stage II			
Equivalent Voltage	$V_{p,I}$	$V_{n,I}$	$V_{p,\text{prm}}$	$V_{n,\text{prm}}$	$V_{p,\text{sec}}$	$V_{n,\text{sec}}$
Positive Insertion	v_{C1}		v_{C1}		v_{C2}	
Negative Insertion	$-v_{C1}$		$-v_{C1}$		$-v_{C2}$	
Bypass	0		0		0	
Blocking	v_{C1}	$-v_{C1}$	v_{C1}	$-v_{C1}$	v_{C2}	$-v_{C2}$

expressed in the form of Norton equivalents in discrete-time domain using the implicit-type solvers in Table III. Different from the VG-DEM, the MV- and LVdc-link capacitor voltages in the SFB-DEM are integrated employing explicit-type solvers, as shown in Table IV. Hence, circuit decoupling between the two converter stages can be achieved through the dc-link capacitors since only historical information from the previous time steps are required while integrating the capacitor voltages.

As presented in Fig. 5, the SFB-DEM simplifies the circuit by representing the FB converter's ac terminals with positive and negative equivalent voltage sources in series with anti-parallel diodes, wherein $V_{p,I}$ and $V_{n,I}$ are the positive and negative equivalent ac voltage sources in Stage I. $V_{p,\text{prm}}$, $V_{n,\text{prm}}$, $V_{p,\text{sec}}$ and $V_{n,\text{sec}}$ represent the equivalent voltages on primary- and secondary-side of the DAB in Stage II.

Table V illustrates the values of the equivalent ac voltage sources regarding the switching modes of the FB converter, i.e., positive insertion, negative insertion, bypass, and IGBT-blocking modes. In the deblocking mode, the ac voltage is computed by multiplying dc-link voltage with the switching function correspondingly. In the blocking mode, the ac current only flows through one of the two antiparallel diodes, which connects the equivalent voltage source, i.e., V_p or V_n to the circuit.

Fig. 6 outlines the simulation algorithm of the SFB-DEM with ImEx-type solvers. As discussed hereinbefore, the two converter stages are decoupled through MVdc-link using explicit-type solver. Therefore, it is noted in Fig. 5 that Stage II contains only one node which is connected to the DAB primary-, secondary- and magnetizing-branches, where the nodal voltage is denoted by V_m. With the nodal voltage solved, the latest time-step values of i_{prm}, i_{sec}, and i_m can be updated using the implicit-type integration rules in the two converter stages, respectively. Finally, the dc-link capacitor currents can be derived by multiplying ac currents with their switching functions in each stage, correspondingly.

The proposed SFB-DEM with ImEx-type solver can improve simulation efficiency as it alleviates computational burdens due to circuit decoupling through dc-link capacitors, constant network G-matrix, and significant node reduction. Meanwhile, its

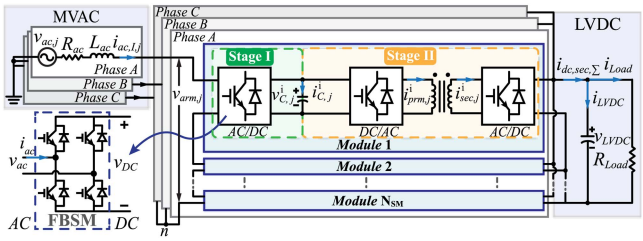

Fig. 7. Schematic diagram of multimodule SST.

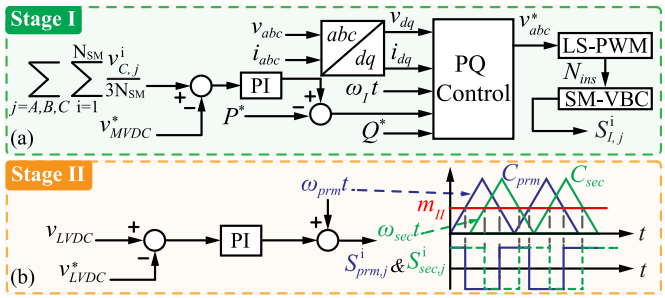

Fig. 8. Control strategy of SST. (a) Stage I voltage and reactive power controls. (b) Stage II LVdc-link voltage control.

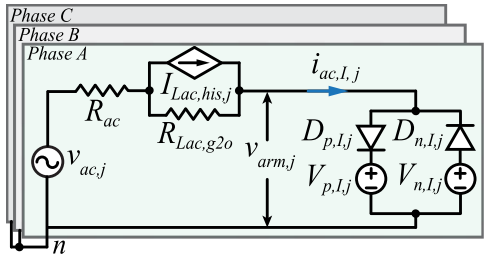

Fig. 9. SFB-DEM of multimodule SST Stage I AC–DC converter.

numerical accuracy can be improved by adopting high-order numerical solver as elaborated in Tables III and IV. The illustration of the SFB-DEM strategy in the two-stage converter functions as a stepping stone for the numerically efficient and accurate modeling of multilevel multimodule SST to be introduced in the next section.

III. SFB-DEM With Multistep ImEx-Type Integration Methods for Multimodule SST

This section proposes the SFB-DEM for the multilevel multimodule SST based on aforementioned ImEx-type solvers. First, the multimodule SST circuit configuration and its control strategy are introduced in Section III-A. Then, the proposed SFB-DEMs with multistep ImEx-G2O and ImEx-G3O solvers are derived in Sections III-B and III-C, respectively. Finally, Section III-D proposes the switching interpolation technique for the SFB-DEMs with multistep ImEx-type solvers.

A. Multimodule SST Circuit Topology

As illustrated in Fig. 7, the multimodule SST is composed of two converter stages, which are coupled through MVdc-link capacitors. The multimodule SST Stage I contains a chainlink ac–dc converter with cascaded FBSMs. Throughout this article, the subscript index $j \in \{A, B, C\}$ is reserved to denote the phases. In Stage I, $i_{\mathrm{ac},I,j}$ and $i^i_{\mathrm{dc},I,j}$ are the ac and dc currents, while $v^i_{C,j}$ and $i^i_{C,j}$ are the MVdc-link capacitor voltage and current of the ith FBSM in phase j, respectively. $v_{\mathrm{arm},j}$ denotes the arm voltage of the ac/dc converter. In Stage II, $i^i_{\mathrm{prm},j}$ and $i^i_{\mathrm{sec},j}$ are the primary- and secondary-side ac currents of the ith DAB module.

Following the ISOP configuration, all the DAB secondary dc terminals are connected in parallel to the LVdc-link capacitor whose voltage is v_{LVDC}. R_{Load} denotes a resistive load, in parallel to the LVdc-link capacitor. Thus, v_{LVDC} can be integrated using the summation of DAB secondary dc currents $i_{\mathrm{dc,sec},\Sigma}$ and load current i_{Load}.

B. SST Control Strategy and Operation Principle

As demonstrated in Fig. 8, higher- and lower-level control strategies are applied to Stages I and II, independently. In Stage I, MVdc-link energy balance control is implemented by comparing the measured average value of MVdc-link capacitor voltages of N_{SM} cascaded FBSMs in three phases with the MVdc reference voltage, v^*_{MVDC}. The difference between the measured and reference voltage is processed by PI controller and then considered as a part of real power reference P^*. Thus, the VQ-control in dq-frame is employed to regulate active and reactive power at point of common coupling on MVac-grid side [15]. The modulating signals v^*_{abc} are generated and sent to a level-shifted PWM (LS-PWM) scheme to produce the number of inserted chainlink SMs, N_{ins} which comprises $2N_{\mathrm{SM}} + 1$ discrete voltage steps. Subsequently, a sorting algorithm-based SM voltage-balance-control is implemented to balance the MVdc-link capacitor voltages. Finally, Stage I switching function for each individual FBSM, $S^i_{I,j}$, can be generated accordingly.

In Stage II, as Fig. 8(b) depicts, an outer-loop LVdc-link voltage control is employed to regulate active power transfer in the DAB modules. $\omega_{\mathrm{prm}}t$ and $\omega_{\mathrm{sec}}t$ represent the phase angles of DAB primary- and secondary-side carrier signals, C_{prm} and C_{sec} are carriers in a single-phase-shift PWM scheme, respectively. m_{II} denotes a constant modulating signal whose duty ratio is 50% . Thus, DAB primary- and secondary-side switching functions, $S^i_{\mathrm{prm},j}$ and $S^i_{\mathrm{sec},j}$ can be obtained accordingly.

C. SFB-DEM With ImEx-G2O Solver

This section provides the mathematical derivation of the proposed SFB-DEM for the multimodule SST. The circuit components of the SST are discretized using ImEx-G2O solver. More specifically, the MV and LVdc-link capacitors are discretized using explicit G2O solver while the other circuit components are discretized using implicit G2O method, according to Tables III and IV.

1) Stage I AC–DC Converter With Cascaded FBSMs: Fig. 9 depicts a schematic diagram of the proposed multimodule SST SFB-DEM for Stage I. First, the MVdc-link capacitor voltages

are integrated using explicit G2O method as

$$v^i_{C,j}\ (t_{k+1}) = \frac{4}{3}\, v^i_{C,j}\,(t_k) - \frac{1}{3} v^i_{C,j}\,(t_{k-1}) + \frac{2\Delta t}{3C_1} \cdot \left(2i^i_{C,j}\,(t_k) - i^i_{C,j}\,(t_{k-1})\right) \tag{3}$$

where C_1 is MVdc-link SM capacitance and the ith MVdc capacitor current $i^i_{C,j}$ from the previous two steps, i.e., t_k and t_{k-1} is solved in (4), assuming de-blocking mode operation

$$i^i_{C,j} = S^i_{I,j}\ \cdot i_{\mathrm{ac},I,j} - S^i_{\mathrm{prm},j} \cdot i^i_{\mathrm{prm},j} \tag{4}$$

where $S^i_{I,j} \in \{1,-1,0\}$is the switching function of the ith FBSM in Stage I and $S^i_{\mathrm{prm},j} \in \{1,-1,0\}$ denotes the primary-side switching function of the ith DAB module, corresponding to the switch modes of positive insertion, negative insertion and bypass. As shown in (3), the integration of $v^i_{C,j}(t_{k+1})$ only requires historical terms from previous time steps such that decoupling between two converter stages can be achieved through MVdc-link capacitor of each module.

While the system is operating in the de-blocking mode, the arm voltage $v_{\mathrm{arm},j}$ is computed as

$$v_{\mathrm{arm},j}\ (t_{k+1}) = \sum_{i=1}^{N_{SM}} S^i_{I,j}\,(t_{k+1}) \cdot\ v^i_{C,j}\,(t_{k+1})\,. \tag{5}$$

As depicted in Fig. 9, $V_{p,I,j}$ and $V_{n,I,j}$ denote the positive and negative ac equivalent voltages in phase j, which are in series with the antiparallel diodes, $D_{p,I,j}$ and $D_{n,I,j}$, respectively. The flowing direction of $i_{\mathrm{ac},I,j}$ determines either $V_{p,I,j}$ or $V_{n,I,j}$ is connected to the equivalent circuit. In deblocking mode, values of the equivalent voltages are computed as

$$V_{p,I,j}\ (t_{k+1}) = V_{n,I,j}\ (t_{k+1}) = v_{\mathrm{arm},j}\ (t_{k+1})\,. \tag{6}$$

In blocking mode, the equivalent voltage sources are derived as

$$\begin{cases} V_{p,I,j}\ (t_{k+1}) = \sum_{i=1}^{N_{\mathrm{SM}}} v^i_{C,j}\,(t_{k+1}) \\ V_{n,I,j}\ (t_{k+1}) = -\sum_{i=1}^{N_{\mathrm{SM}}} v^i_{C,j}\,(t_{k+1}) \end{cases}. \tag{7}$$

Accordingly, the MVdc-link capacitor current is computed as

$$i^i_{C,j} = \left|i_{\mathrm{ac},I,j}\right| + \left|i^i_{\mathrm{prm},j}\right|. \tag{8}$$

Based on Fig. 9 and Table III, the MVac line inductor L_{ac} is discretized using implicit G2O method and expressed as a historical current source $I_{\mathrm{Lac,his},j}$ in parallel with its equivalent resistance $R_{\mathrm{Lac},g2o}$. Subsequently, the present time-step solution of the Stage I ac current $i_{\mathrm{ac},I,j}(t_{k+1})$ is solved as

$$i_{\mathrm{ac},I,j}\,(t_{k+1}) = \frac{R_{\mathrm{Lac},g2o}}{R_{\mathrm{Lac},g2o}+R_{\mathrm{ac}}}\left(\frac{4}{3} i_{\mathrm{ac},I,j}\,(t_k) - \frac{1}{3} i_{\mathrm{ac},I,j}\,(t_{k-1})\right) + \frac{1}{R_{\mathrm{Lac},g2o}+R_{\mathrm{ac}}}\left(v_{\mathrm{ac},j}\,(t_{k+1}) - V_{x,I,j}\,(t_{k+1})\right) \tag{9}$$

where $V_{x,I,j}$ $(x \in \{p,n\})$ corresponds to the positive and negative ac voltages in Stage I, as derived in (6) or (7).

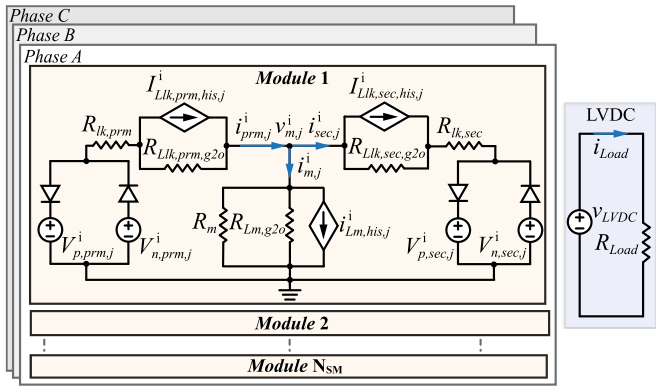

Fig. 10. SFB-DEM of multimodule SST Stage II DAB DC–DC converter.

2) Stage II DAB DC–DC Converter: Fig. 10 depicts a schematic diagram of the proposed SST SFB-DEM for Stage II. Similarly, the derivation of the Stage II SFB-DEM commences with integration of the dc-link capacitor voltages using Ex-G2O method. With the MVdc-link voltage solved in (3), the LVdc-link capacitor voltage at t_{k+1} can also be derived as

$$v_{\mathrm{LVDC}}\ (t_{k+1}) = \frac{4}{3}\, v_{\mathrm{LVDC}}\,(t_k) - \frac{1}{3} v_{\mathrm{LVDC}}\,(t_{k-1}) + \frac{2\Delta t}{3C_2} \cdot \left(2i_{\mathrm{LVDC}}\,(t_k) - i_{\mathrm{LVDC}}\,(t_{k-1})\right) \tag{10}$$

where C_2 is LVdc-link SM capacitance and i_{LVDC} is the LVdc-link capacitor current.

In deblocking mode, i_{LVDC} from the previous two steps, i.e., $i_{\mathrm{LVDC}}(t_k)$ and $i_{\mathrm{LVDC}}(t_{k-1})$ can be computed by applying KCL at the LVdc terminal as

$$i_{\mathrm{LVDC}} = i_{\mathrm{dc,sec},\Sigma}\ - v_{\mathrm{LVDC}}/R_{\mathrm{Load}} \tag{11}$$

where $i_{\mathrm{dc,sec},\Sigma}$ is derived as

$$i_{\mathrm{dc,sec},\Sigma} = \sum_{j=A,B,C} \sum_{i=1}^{N_{\mathrm{SM}}} S^i_{\mathrm{sec},j} \cdot i^i_{\mathrm{sec},j}. \tag{12}$$

Here, $S^i_{\mathrm{sec},j} \in \{1,-1,0\}$ is the secondary-side switching function of the ith DAB module corresponding to positive insertion, negative insertion, and bypass modes. Subsequently, the present time-step values of the DAB primary and secondary ac voltages, i.e., $v^i_{\mathrm{prm},j}(t_{k+1})$ and $v^i_{\mathrm{sec},j}(t_{k+1})$ are computed by

$$\begin{cases} v^i_{\mathrm{prm},j}\ (t_{k+1}) = S^i_{\mathrm{prm},j}\ (t_{k+1}) \cdot v^i_{C,j}\,(t_{k+1}) \\ v^i_{\mathrm{sec},j}\ (t_{k+1}) = S^i_{\mathrm{sec},j}\ (t_{k+1}) \cdot v_{\mathrm{LVDC}}\,(t_{k+1}) \end{cases}. \tag{13}$$

In deblocking mode, the DAB primary and secondary equivalent ac voltages are derived as

$$\begin{cases} V^i_{p,\mathrm{prm},j}\ (t_{k+1}) = V^i_{n,\mathrm{prm},j}\ (t_{k+1}) = v^i_{\mathrm{prm},j}\ (t_{k+1}) \\ V^i_{p,\mathrm{sec},j}\ (t_{k+1}) = V^i_{n,\mathrm{sec},j}\ (t_{k+1}) = v^i_{\mathrm{sec},j}\ (t_{k+1}) \end{cases}. \tag{14}$$

In the blocking mode, the equivalent ac voltages are computed following the identical formulae in the Table V, which are not derived here for space consideration. The LVdc-link capacitor

current is calculated as

$$i_{\text{LVDC}} = \sum_{j=A,B,C} \sum_{i=1}^{N_{\text{SM}}} \left| i^i_{\text{sec},j} \right| - v_{\text{LVDC}}/R_{\text{Load}}. \quad (15)$$

As demonstrated in Fig. 10, the inductors from three circuit branches in the DAB transformer T-equivalent circuit are discretized using the implicit G2O method and expressed in the form of Norton equivalents, given in Table III. The equivalent resistors of the primary leakage, secondary leakage and magnetizing inductors of the MFT are denoted by $R_{Llk,\text{prm},g2o}$, $R_{Llk,\text{sec},g2o}$ and $R_{Lm,g2o}$, which are in parallel with their corresponding historical current sources $I^i_{Llk,\text{prm,his},j}$, $I^i_{Llk,\text{sec,his},j}$ and $I^i_{Lm,\text{his},j}$. To simplify the derivation of nodal voltage equation, circuit component reduction is realized in each *RL*-branch to further reduce number of nodes in the DAB equivalent circuit of Fig. 10. Thus, the equivalent conductance and historical currents from the primary- and secondary-side branches are formulated as

$$\begin{cases} G_{\text{prm},g2o} = 1/\left(R_{Llk,\text{prm},g2o} + R_{lk,\text{prm}}\right) \\ G_{\text{sec},g2o} = 1/\left(R_{Llk,\text{sec},g2o} + R_{lk,\text{sec}}\right) \end{cases} \quad (16)$$

$$\begin{cases} I^i_{\text{prm,his},j} = G_{\text{prm},g2o} \cdot R_{Llk,\text{prm},g2o} \cdot I^i_{Llk,\text{prm,his},j} \\ I^i_{\text{sec,his},j} = G_{\text{sec},g2o} \cdot R_{Llk,\text{sec},g2o} \cdot I^i_{Llk,\text{sec,his},j} \end{cases}. \quad (17)$$

Similarly, the magnetizing-branch equivalent conductance $G_{m,g2o}$ can also be derived as

$$G_{m,g2o} = \frac{R_{Lm,g2o} + R_m}{R_{Lm,g2o} \cdot R_m}. \quad (18)$$

Using (16)–(18) to formulate nodal voltage equation, the magnetizing-branch node voltage $v^i_{m,j}(t_{k+1})$ is computed as

$$\begin{aligned} v^i_{m,j}\ (t_{k+1}) = &\left(G_{\text{prm},g2o} + G_{\text{sec},g2o} + G_{m,g2o}\right)^{-1} \\ &\left(I^i_{\text{prm,his},j} - I^i_{\text{sec,his},j} - I^i_{Lm,\text{his},j} + G_{\text{prm},g2o}\right. \\ &\left.\cdot V^i_{x,\ \text{prm},j}\left(t_{k+1}\right) + G_{\text{sec},g2o} \cdot V^i_{x,\text{sec},j}\left(t_{k+1}\right)\right) \end{aligned} \quad (19)$$

where $V^i_{x,\ \text{prm},j}$ and $V^i_{x,\text{sec},j}$ $(x \in \{p,n\})$ are the positive and negative equivalent ac voltages on primary- and secondary-sides of the DAB in accordance with (14) and Table V.

Finally, with $v^i_m(t_{k+1})$ obtained, the ac current from each circuit branch can be updated as

$$\begin{cases} i^i_{\text{prm},j}\ (t_{k+1}) = I^i_{\text{prm,his},j} + G_{\text{prm},g2o} \\ \cdot \left(V^i_{x,\text{prm},j}\left(t_{k+1}\right) - v^i_{m,j}\left(t_{k+1}\right)\right) \\ i^i_{\text{sec},j}\ (t_{k+1}) = I^i_{\text{sec,his},j} + G_{\text{sec},g2o} \\ \cdot \left(v^i_{m,j}\left(t_{k+1}\right) - V^i_{x,\text{sec},j}\left(t_{k+1}\right)\right) \\ i^i_{m,j}\ (t_{k+1}) = I^i_{Lm,\text{his},j} + G_{m,g2o} \cdot v^i_m\left(t_{k+1}\right) \end{cases}. \quad (20)$$

D. SFB-DEM With ImEx-G3O Solver

To further improve numerical accuracy, an SST SFB-DEM with the 3rd-order solver, i.e., ImEx-G3O method is illustrated in this section. Since the derivations of network solutions for the SFB-DEM with ImEx-G3O method are very similar to those of the ImEx-G2O solver, this section only focuses on the discretization of circuit components adopting the ImEx-G3O method, particularly.

1) Stage I AC–DC Converter With Cascaded FBSMs: The MVdc-link capacitor voltage is integrated using the explicit G3O method, which requires historical information from previous 3 time steps as

$$\begin{aligned} v^i_{C,j}\ (t_{k+1}) = &\frac{18}{11} v^i_{C,j}\left(t_k\right) - \frac{9}{11} v^i_{C,j}\left(t_{k-1}\right) + \frac{2}{11} v^i_{C,j}\left(t_{k-2}\right) \\ &+ \frac{6\Delta t}{11 C_1} \cdot \left(3 i^i_{C,j}\left(t_k\right) - 3 i^i_{C,j}\left(t_{k-1}\right) + i^i_{C,j}\left(t_{k-2}\right)\right). \end{aligned} \quad (21)$$

Different from Section III-C.1, the Stage I inductors are discretized using implicit G3O method, where the historical current $I_{\text{Lac,his},j}$ and equivalent resistance $R_{\text{Lac},g3o}$ are derived following Table III. Therefore, the Stage I circuit solution can be sought using (4)–(8), similarly. The Stage I ac current is derived as

$$\begin{aligned} &i_{\text{ac},I,j}\ (t_{k+1}) \\ &= \frac{R_{\text{Lac},g3o}}{R_{\text{Lac},g3o} + R_{\text{ac}}} \left(\frac{18}{11} i_{\text{ac},I,j}\left(t_k\right) - \frac{9}{11} i_{\text{ac},I,j}\left(t_{k-1}\right)\right. \\ &\quad \left. + \frac{2}{11} i_{\text{ac},I,j}\left(t_{k-2}\right)\right) + \frac{1}{R_{\text{Lac},g3o} + R_{\text{ac}}} \\ &\quad \cdot \left(v_{\text{ac},j}\left(t_{k+1}\right) - V_{x,I,j}\left(t_{k+1}\right)\right). \end{aligned} \quad (22)$$

2) Stage II DAB DC–DC Converter: In this section, circuit components in the DAB modules are discretized using ImEx-G3O method. Similar to Stage I, the derivation of Stage II SFB-DEM starts with the integration of LVdc-link capacitor voltages employing the Ex-G3O method as

$$\begin{aligned} v_{\text{LVDC}}\ (t_{k+1}) = &\frac{18}{11} v_{\text{LVDC}}\left(t_k\right) \\ &- \frac{9}{11} v_{\text{LVDC}}\left(t_{k-1}\right) + \frac{2}{11} v_{\text{LVDC}}\left(t_{k-2}\right) \\ &+ \frac{6\Delta t}{11 C_2} \cdot \left(3 i_{\text{LVDC}}\left(t_k\right) - 3 i_{\text{LVDC}}\left(t_{k-1}\right) + i_{\text{LVDC}}\left(t_{k-2}\right)\right) \end{aligned} \quad (23)$$

where i_{LVDC} is computed by (11) and (12) in deblocking mode or (15) in blocking mode.

As shown in Fig. 10 and Table III, the inductors from three DAB circuit branches are discretized using implicit G3O method and expressed in form of companion circuits. Since the derivation of the DAB SFB-DEM using the ImEx-G3O is similar to what had been discussed in Section III-C.2, the derivation detail is omitted here for space consideration.

Compared to the 2nd-order solvers such as ImEx-G2O and TR, the ImEx-G3O improves numerical accuracy of the network solutions as it achieves the 3rd order accuracy in dynamic simulation. It is noted that the modeling complexity of the ImEx-G3O increases slightly, compared to the 2nd-order solvers since the use of ImEx-G3O requires historical information from 3 consecutive time steps to extrapolate the present time-step solution. Also, there are additional requirements for storages of circuits' historical information during the simulation execution. Hence, this paper proposes both ImEx-G2O and ImEx-G3O methods

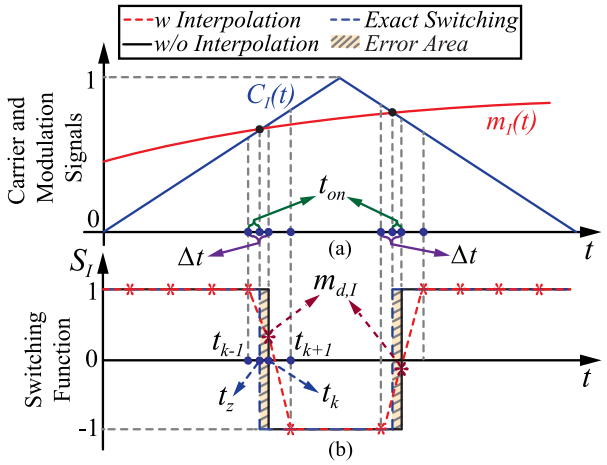

Fig. 11. Switching interpolation technique in Stage I. (a) Carrier and modulation signals of single FBSM. (b) Switching function of single FBSM.

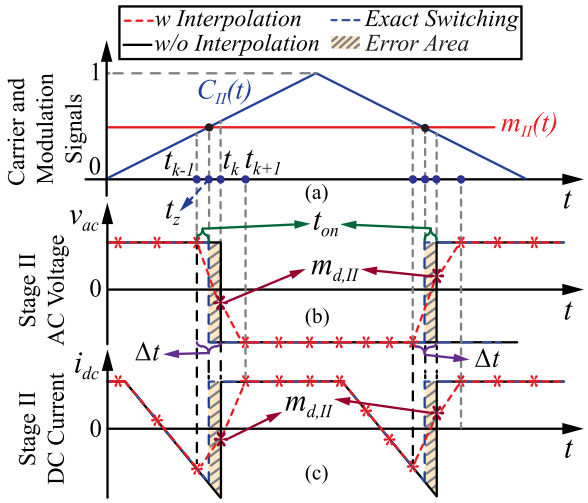

Fig. 12. Switching interpolation technique in Stage II. (a) Carrier and modulation signals. (b) AC voltage. (c) DC current.

for implementing the SFB-DEMs such that users can flexibly choose solver preferences based on specific requirements for numerical accuracy or modeling simplicity.

E. Switching Interpolation for Multistep ImEx-Type Solver

This section proposes a switching interpolation technique for the SFB-DEMs and illustrates its application to the multistep ImEx-type solvers. Figs. 11 and 12 show the PWM scheme for a single FBSM in the SST as an example to demonstrate switching interpolation technique. In Figs. 11 and 12, the legends, w and w/o are corresponding to the SFB-DEMs with and without switching interpolation applied, respectively. t_z represents the precise switching event instance which occurs in between two integer time steps, i.e., t_{k-1} and t_k. Black-solid line denotes the switching function without employing switching interpolation. It is noted that the switching status variation can only be detected at next integer time point t_k. Accordingly, the yellow-shaded

TABLE VI
POSITIVE INSERTION TIME WITHIN ONE INTEGRATION INTERVAL

Relationship between m and C	t_{ON}
$m(t_k) > C(t_k)$ & $m(t_{k-1}) < C(t_{k-1})$	$\Delta t/(1-\frac{C(t_{k-1})-m(t_{k-1})}{C(t_k)-m(t_k)})$
$m(t_k) > C(t_k)$ & $m(t_{k-1}) > C(t_{k-1})$	Δt
$m(t_k) < C(t_k)$ & $m(t_{k-1}) > C(t_{k-1})$	$\Delta t/(1-\frac{C(t_k)-m(t_k)}{C(t_{k-1})-m(t_{k-1})})$
$m(t_k) < C(t_k)$ & $m(t_{k-1}) < C(t_{k-1})$	0

areas in Figs. 11 and 12 indicate the errors between original and exact switching functions within one simulation time interval.

As presented in Fig. 11(b), t_{on} denotes positive insertion time within one integration interval within which a switching event occurs. t_{on} can be derived based on modulating signal $m_I(t)$ and carrier signal $C_I(t)$ at the time steps of t_k and t_{k-1}, as shown in Table VI. The average value of the exact switching function within the interval $[t_{k-1}, t_k]$ is expressed as

$$S_I^* = m_{d,I} = \frac{2t_{\text{on}}}{\Delta t} - 1 \tag{24}$$

where Δt is integration time step. It is noted that (24) can be used to modify the switching function S_I at t_k, as shown in Fig. 11(b) by the red dotted curve. The switching function $S_{I,j}^i$ in the ith FBSM in phase j of Stage I ac–dc converter can also be modified by the corresponding interpolated ratio $m_{d,I}$ within the interval where a switching event occurs. Thus, the interpolated ratio $m_{d,I}$ is applied to (4) and (5) to account for intra-step switching event in the cascaded FBSMs in Stage I of the SST.

Fig. 12(b) and (c) shows the ac voltage and dc current in an FBSM in either primary or secondary side of a DAB module in Stage II of the SST. The derivation of t_{on} in Fig. 12(b) is the same as in Fig. 11 and Table VI. The interpolated ratio $m_{d,II}$ [as shown in Fig. 12(b) and (c)] is calculated by (24) and is used to replace the original switching functions $S_{\text{prm},j}^{i*}$ and $S_{\text{sec},j}^{i*}$ in (4), (12), and (13). The proposed switching interpolation technique is designed for the SFB-DEM and can be integrated into the proposed multistep ImEx-type solvers to improve both numerical accuracy and simulation efficiency for large-time-step simulation.

IV. SIMULATION STUDIES

This section validates the model accuracy and efficiency of the proposed SFB-DEMs with various numerical solvers for single-module ac–dc–dc converter and multimodule SST, respectively. All converter models are executed on a PC with 3.20 GHz Intel Core i9-12900k CPU, 128 GB RAM, and Microsoft Windows 11 operating system. In the case studies, the DM is implemented using MATLAB/Simulink/Simscape Electrical Toolbox while the VG-DEMs and SFB-DEMs are programmed by MATLAB scripts (m-files). Initially, all models are simulated using a small time step, i.e., $T_s = 1\ \mu$s to validate their numerical accuracy. It is verified that the simulation results of all SFB-DEMs converge with the DM. Thus, the DM with $T_s = 1\ \mu$s is selected as the reference (Ref) to validate the numerical accuracy of the

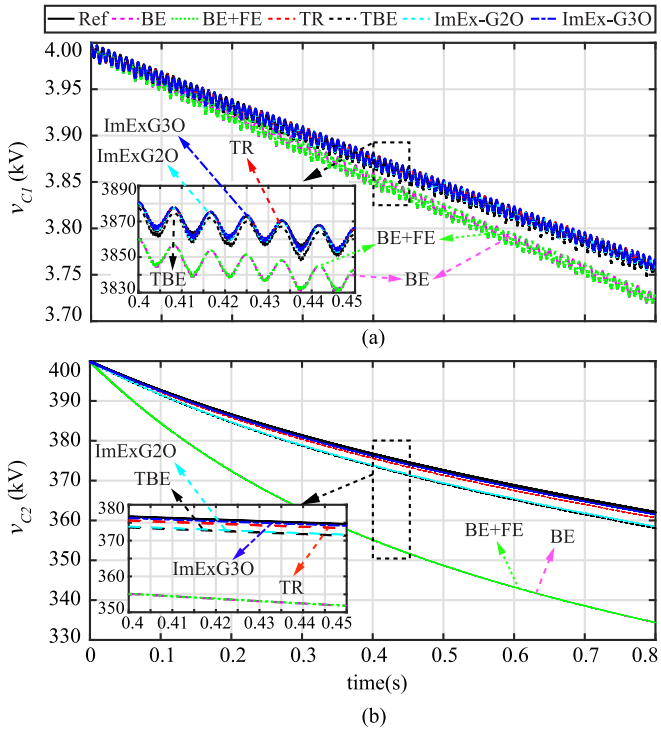

Fig. 13. DC-link capacitor voltages. (a) MVdc-link capacitor voltage. (b) LVdc-link capacitor voltages.

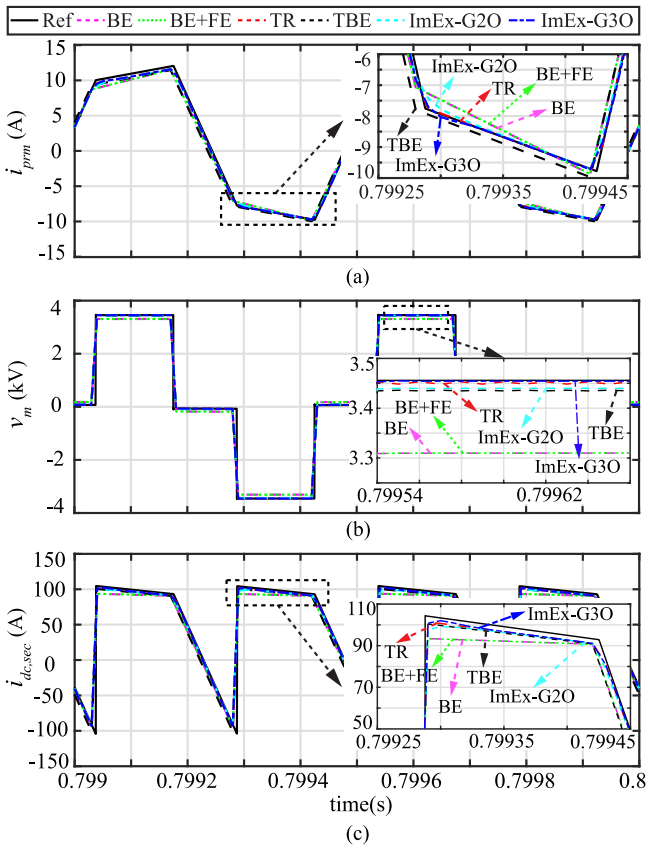

Fig. 14. Stage II DAB simulation performance. (a) Primary-side AC current. (b) Magnetizing-branch voltage. (c) Secondary-side DC current.

DEMs. The tested SFB-DEMs use a large time step of $T_s = 10\ \mu$s in the case studies in Sections IV-A and B.1)–6) and $T_s = 5\ \mu$s in B.7). Meanwhile, the switching interpolation technique is implemented in all tested models to locate switching events precisely.

A. *Validation of 2-Stage AC–DC–DC Converter SFB-DEM*

The numerical accuracy of the proposed SFB-DEMs with the ImEx-type methods including BE+FE, ImEx-G2O and ImEx-G3O are compared to the VG-DEMs with implicit-type solvers including BE, TR, and TBE. For straightforward comparison and benchmarking of model accuracy, the MV and LVdc-link capacitors discharging transients are used in the simulation study of 2-stage ac–dc–dc converter.

As observed in Fig. 13, the numerical accuracy of the MV- and LVdc-link capacitor voltages using various integration rules are ranked as follows: SFB-DEM (ImEx-G3O) $>$ VG-DEM (TR) $>$ SFB-DEM (ImEx-G2O) $>$ VG-DEM (TBE) $>$ SFB-DEM (BE-FE) $\approx$ VG-DEM (BE). In Fig. 13(b), minor numerical oscillations are observed in the DAB magnetizing branch voltage when using the TR method (red dashed curve) during abrupt variations in the switching states of FB converters at both sides of the MFT. Although, the numerical oscillations can be damped out by switching TR back to BE, i.e., TBE method (black dashed curve), the numerical accuracy is reduced consequently.

It is observed in Figs. 13 and 14 that the simulation results of the proposed SFB-DEM with ImEx-G3O method match well to the reference solution, whereas the performance of the 1st-order BE+FE solver exhibits significant numerical error throughout the simulation. Meanwhile, it has also been validated that the proposed SFB-DEM solved by ImEx-G3O solver is immune to numerical oscillations even when the system stiffness is high.

B. *Validation of Multimodule SST SFB-DEMs*

This subsection validates the proposed SFB-DEMs with ImEx-G2O and ImEx-G3O methods for simulating multimodule SST. The system parameters are provided in Table IX of the Appendix. Without loss of generality, dynamic performances of the proposed SFB-DEMs are presented with different operating scenarios, including steady-state, real-power-change, LVdc-link pole-to-pole fault, and single-phase ac fault. The effectiveness of the proposed switching interpolation technique is verified in Case Study 7) along with the multistep ImEx-type solver. Finally, simulation efficiency of the VG-DEMs and the proposed SFB-DEMs are compared to the MATLAB/Simulink DMs for different numbers of SMs in the multimodule SST.

1) Steady State Performance: As presented in Fig. 15, the Stage I arm voltages and currents using the 2nd-order methods i.e., TR+Ex-G2O (yellow dashed curve), ImEx-G2O (magenta dotted curve), and ImEx-G3O (cyan dashed curve) match with the reference solutions (black solid curve) very well. On the other hand, the SFB-DEM with BE+FE solver (blue dashed curve) has noticeable difference to the reference solution. Compared to TR+Ex-G2O, the SFB-DEM with ImEx-G2O or ImEx-G3O

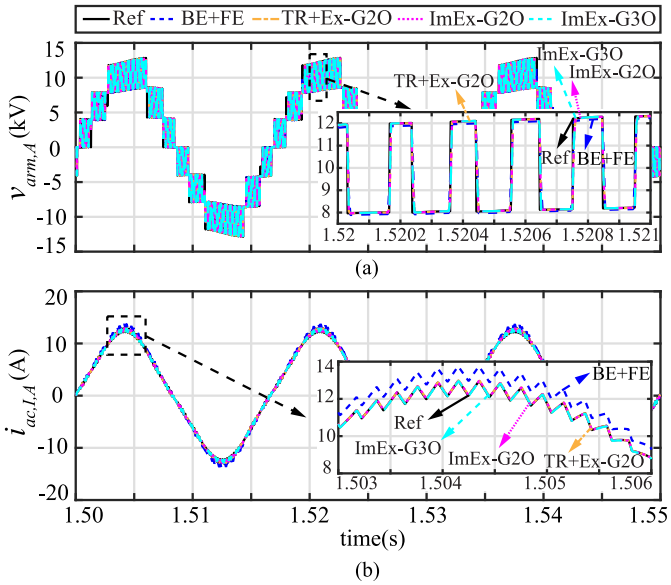

Fig. 15. SST Stage I arm voltage and current. (a) Stage I arm voltage. (b) Stage I arm current.

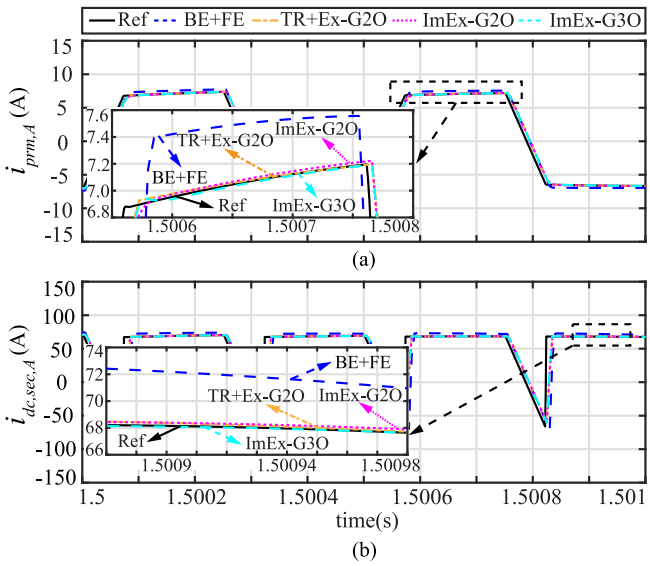

Fig. 16. Stage II DAB AC and DC currents. (a) Primary-side AC current. (b) Secondary-side DC current.

emerge as preferred modeling strategy since it achieves high numerical accuracy without numerical oscillation.

Fig. 16 presents the SST Stage II DAB simulation results. It is noted in the primary ac and secondary dc currents that the SFB-DEM solved by ImEx-G3O method achieves the best numerical accuracy as it converges with the reference solutions well, while the two SFB-DEMs solved by the 2nd-order methods, i.e., TR+Ex-G2O and ImEx-G2O are slightly less accurate. More importantly, the simulation results by the 1st-order BE+FE method present noticeable magnitude differences compared to the other solutions.

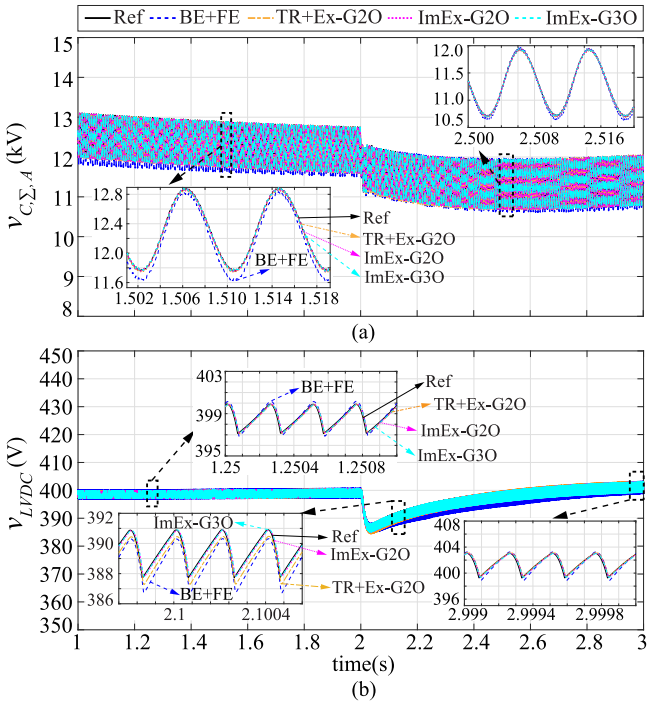

Fig. 17. SST dc-link voltages. (a) Summation of MVdc-link capacitor voltages. (b) LVdc-link capacitor voltage.

2) Real Power Change Operation: The real power reference is initialized at 1 p.u. and commanded to vary from 1 to 0.8 p.u. at $t = 2$ s. This case study is used to validate the numerical accuracy of the proposed SFB-DEMs solved by ImEx-G2O and ImEx-G3O methods when the system experiences power-change transient. It is observed in Fig. 17 that both the 2nd- and 3rd-order methods achieve superior numerical accuracy in MVdc- and LVdc-link capacitor voltages compared to 1st-order BE+FE method during the steady-state periods before and after the real-power-change operation. Furthermore, as observed in Fig. 17(b) at $t = 2$ s, the LVdc-link capacitor voltage is gradually regulated back to its rated value due to the effectiveness of outer-loop voltage control. During this transient period, it is noted that the proposed SFB-DEMs solved by both ImEx-G2O and ImEx-G3O converge with the reference better than that of the BE+FE solver, which validates the merit of the proposed modeling approach in numerical accuracy.

3) Load Change Operation:

a) Dynamic performance: This section presents a case study with a higher step load change of real power from 0.5 to 1 p.u. The real power reference is given in Parameter List of Case 1 in Table IX in the Appendix. Fig. 18(a) presents dynamic performance of individual MVdc-link capacitor voltages produced by the DEMs with different ODE solvers and the DM reference. It is noted in Fig. 18(a) that the MVdc capacitor voltages experience fast transient when the load-change occurs at $t = 3$ s. After that, the magnitudes of the MVdc capacitor voltages are regulated back to its rated value due to the MVdc-link voltage/energy control and SM capacitor voltage balancing control. In addition, as demonstrated in Fig. 18(b), the magnitude

TABLE VII
RELATIVE ERRORS OF SFB-DEMS WITH VARIOUS IMEX-TYPE INTEGRATION METHODS

Simulation Time Step	Stage I Arm Current $\varepsilon_{i_{\text{arm},j}}(\%)$			Sum of MVDC Capacitor Voltages $\varepsilon_{v_{C,\Sigma,j}}(\%)$			LVDC-link Capacitor Voltages $\varepsilon_{v_{\text{lvdc}}}$ (%)		
	BE+FE	ImEx-G2O	ImEx-G3O	BE+FE	ImEx-G2O	ImEx-G3O	BE+FE	ImEx-G2O	ImEx-G3O
2 μs	2.731	0.102	0.101	0.224	0.005	0.003	0.200	0.006	0.006
5 μs	7.257	0.464	0.440	0.306	0.037	0.032	0.458	0.033	0.027
10 μs	16.064	1.023	0.921	1.982	0.106	0.095	2.120	0.099	0.084

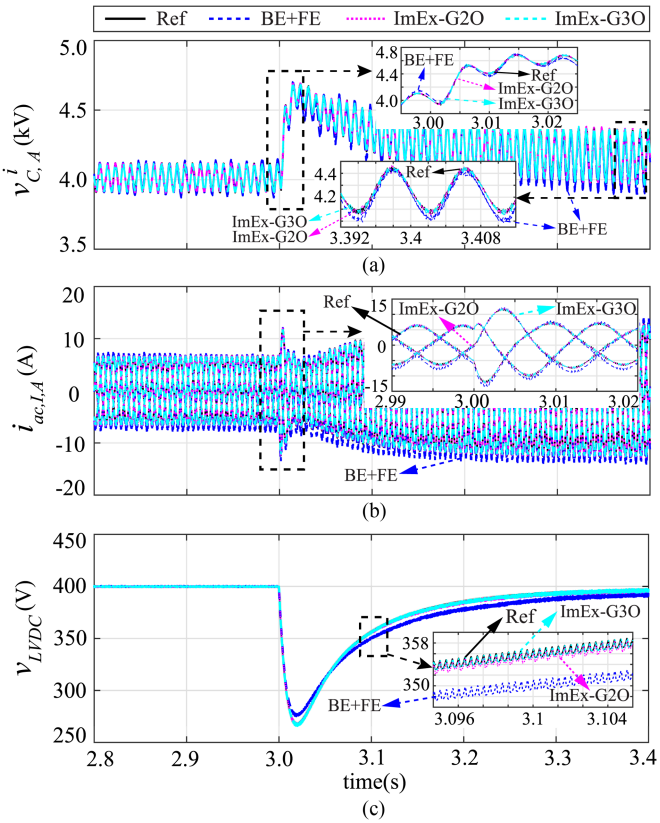

Fig. 18. Dynamic performances of load-change operation. (a) MVdc-link capacitor voltages. (b) Stage I arm current. (c) LVdc-link capacitor voltage.

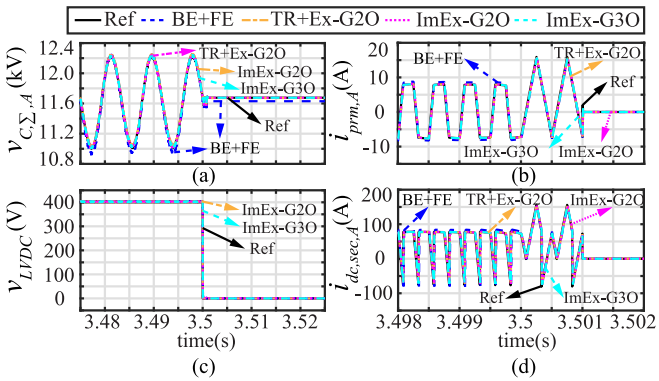

Fig. 19. LVdc-link pole-to-pole short-circuit fault operation. (a) Summation of MVdc-link capacitor voltages. (b) DAB primary-side AC current. (c) LVdc-link capacitor voltage. (d) DAB secondary-side DC current.

of Stage I arm current is doubled in its magnitude in the steady state due to the real power change. Meanwhile, it is also observed in Fig. 18(c) that the LVdc-link capacitor voltage drops instantaneously when the load power is increased. Thereafter, the LVdc-link voltage gradually recovers back to its rated value, owing to the effective outer-loop voltage controller. It is observed in Fig. 18 that the proposed DEMs employing ImEx-G2O and ImEx-G3O demonstrate superior numerical accuracy compared to the DEM with 1st-order BE+FE method, especially during the transient period of the load change.

b) Sensitivity analysis regarding simulation time step: This section presents the relative errors for the proposed SFB-DEMs with the BE+FE, ImEx-G2O and ImEx-G3O integration methods at different time steps, i.e., $\Delta t = 2,\ 5$, and 10 μs, and compare them with the DM reference simulated with the small time step of 1 μs. The real power reference is initialized with 0.5 p.u. and is commanded to step up to 1 p.u at $t = 3$ s. The relative errors for the proposed SFB-DEM with different solvers are calculated as

$$\varepsilon_r\ (\%) = \frac{\sum_{i=N1}^{i=N2} |x_{\text{DEM}}(i) - \hat{x}(i)|}{\sum_{i=N1}^{i=N2} |\hat{x}(i)|} \times 100\% \qquad (25)$$

where $\hat{x}(i)$ denotes reference solution at the ith time step; N_1 and N_2 are corresponding to the starting and ending points of the time window where the relative errors are calculated.

Table VII demonstrates the relative errors for Stage I arm current $\varepsilon_{i_{\text{arm},\ j}}$, the sum of MVdc capacitor voltages $\varepsilon_{v_{C,\Sigma,\ j}}$ and LVdc-link capacitor voltages $\varepsilon_{v_{\text{LVDC}}}$. It is noted in Table VII that the relative errors of the SFB-DEM using 1st-order BE+FE solver are always the largest, compared to the higher order multistep integration methods. In particular, the relative error of the Stage I arm current $\varepsilon_{i_{\text{arm},\ j}}$ using the BE+FE method is around 16 folds larger than those employing ImEx-G2O and ImEx-G3O methods. It is also noted that the relative errors of the BE+FE method grow significantly as the time step-sizes increase from 2 to 10 μs, whereas the errors of the proposed multistep methods exhibit only a slight increase. Overall, the SFB-DEM with ImEx-G3O demonstrates the best numerical accuracy within all tested cases.

4) LVDC Pole-to-Pole Fault Operation: This section validates the blocking mode operation in the proposed SST SFB-DEMs using a dc-link pole-to-pole short-circuit fault case study. As presented in Fig. 19, the LVdc-link pole-to-pole fault occurs at 3.5 s and is detected 1 ms later at 3.501 s. Hereafter, the FBSMs in the SFB-DEMs are switched into blocking mode and the ac currents are only conducted through the antiparallel diodes as depicted in Figs. 5, 9, and 10. Therefore, the flowing directions of

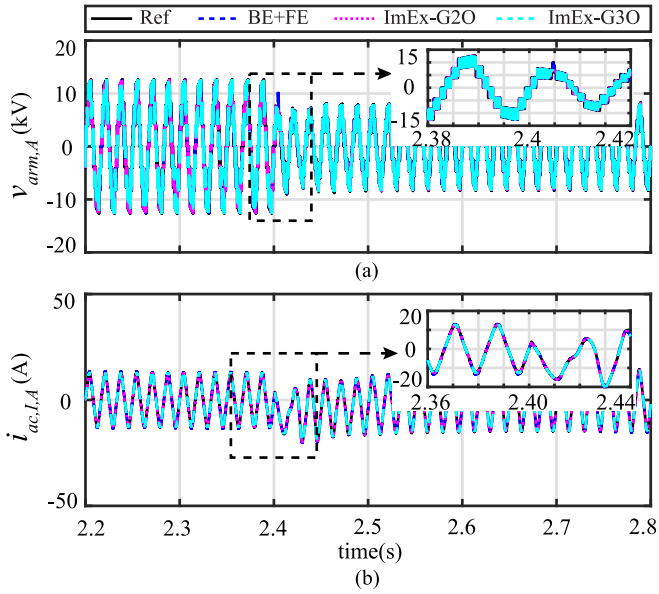

Fig. 20. SST Stage I arm voltage and current under single-phase-to-ground AC fault in phase-A. (a) Arm voltage. (b) Arm current.

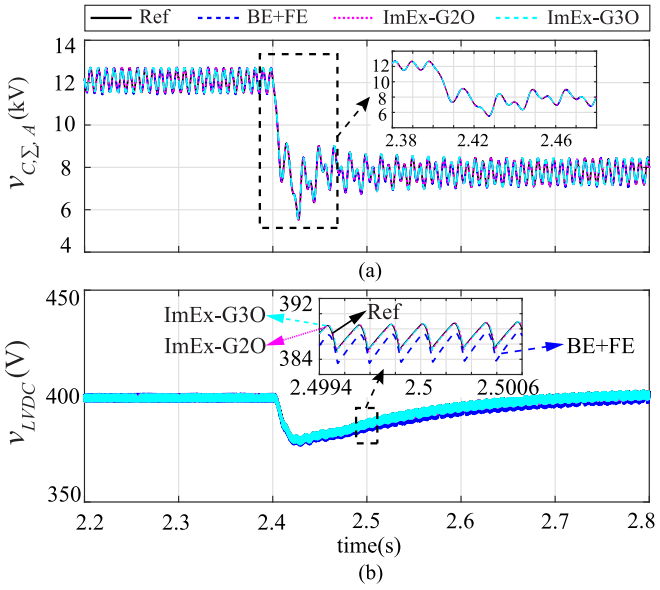

Fig. 21. SST DC-link voltages under single-phase-to-ground AC fault in phase-A. (a) Summation of MVdc-link capacitor voltage. (b) LVdc-link capacitor voltage.

the ac currents in Stages I and II are determined by the switching states of the diodes.

In Stage I, the ac–dc converter's FBSMs counteract with the MVac grid voltage to suppress the short-circuit fault current flowing from the MVac to the MVdc-link. In stage II, the DAB primary-side ac currents and secondary-side dc currents drop to zero instantaneously when the fault occurs at 3.5 s, as presented in Fig. 19(b) and (d). It is noted that the proposed multistep ImEx-G2O and ImEx-G3O methods demonstrate superior numerical accuracy, compared to the 1st-order BE+FE method.

5) Single-Phase AC Fault Simulation: Asymmetrical system faults are identified as the major causes of the unbalanced voltage sags [37], [38], [39]. Accordingly, an additional operating scenario with asymmetrical single-phase-to-ground fault is used to further validate the proposed SFB-DEM and the numerical accuracy improvement by employing the combined multistep integration methods, i.e., ImEx-G2O and ImEx-G3O. In the asymmetric fault case, as presented in Fig. 20(a) and (b), MVac grid is subject to a short-circuit fault between phase-A and the ground at $t = 2.4$ s. Meanwhile, the real power reference is maintained constant at 1 p.u. throughout the dynamic simulation.

As shown in Figs. 20(a) and 21(a), voltage sags are observed in the SST Stage I arm voltages when the asymmetrical ac fault occurs, and meanwhile the summations of MVdc-link capacitor voltages experience abrupt reduction in magnitude. It is also noted in Fig. 20(b) that the magnitude of MVac fault current increases when the fault happens. In addition, the LVdc-link capacitor voltage drops instantaneously due to the ac fault at $t = 2.4$ s and afterwards gradually recovers to its rated value due to the outer-loop voltage controller. It is observed in Figs. 20 and 21 that the proposed SFB-DEMs with multistep methods, i.e., ImEx-G2O and ImEx-G3O achieve better numerical accuracy during both the steady-state period and voltage sag transient than that of the BE+FE solver.

6) Validation of SFB-DEM With High Switching Frequency: To further validate the modeling accuracy of the proposed DEMs, a case study is conducted with increased switching frequency of the DAB modules, i.e., 40 kHz, as presented in Case 2 of Table IX in the Appendix. To ensure there is a sufficient number of computation points in each switching cycle, the simulation time step in Case 2 is reduced to 500 ns in accordance with the smaller switching period of 40 kHz. Thus, there are 50 computation points per switching cycle for the proposed DEMs, which is consistent with Case 1. The reference model is simulated with a small time step of 200 ns, leading to 125 computation points per switching cycle.

The simulation results of the SST with increased switching frequency (40 kHz) of the DAB modules are illustrated in Fig. 22, where the discrepancy in numerical accuracy for the DEMs with different ODE solvers, i.e., BE+FE, ImEx-G2O, and ImEx-G3O are observed. As shown in Fig. 22, the SFB-DEM using ImEx-G3O demonstrates the best accuracy. On the contrary, obvious magnitude differences are observed in the simulation results using the BE+FE solver compared to the reference, since it only achieves 1st-order numerical accuracy.

7) Validation of Switching Interpolation Technique: This section validates the effectiveness of the switching interpolation technique in the SST SFB-DEM using ImEx-G3O method. The dynamic performance with and without switching interpolation is compared in the case study. The real power reference is commanded to step down from 1 to 0.8 p.u. at $t = 2$ s. The tested models are simulated with the time step of 5 μs and compared against a reference model with the time step of 1 μs.

It is noted in Fig. 23 that the simulation results without interpolation (blue dashed curve) get distorted dramatically

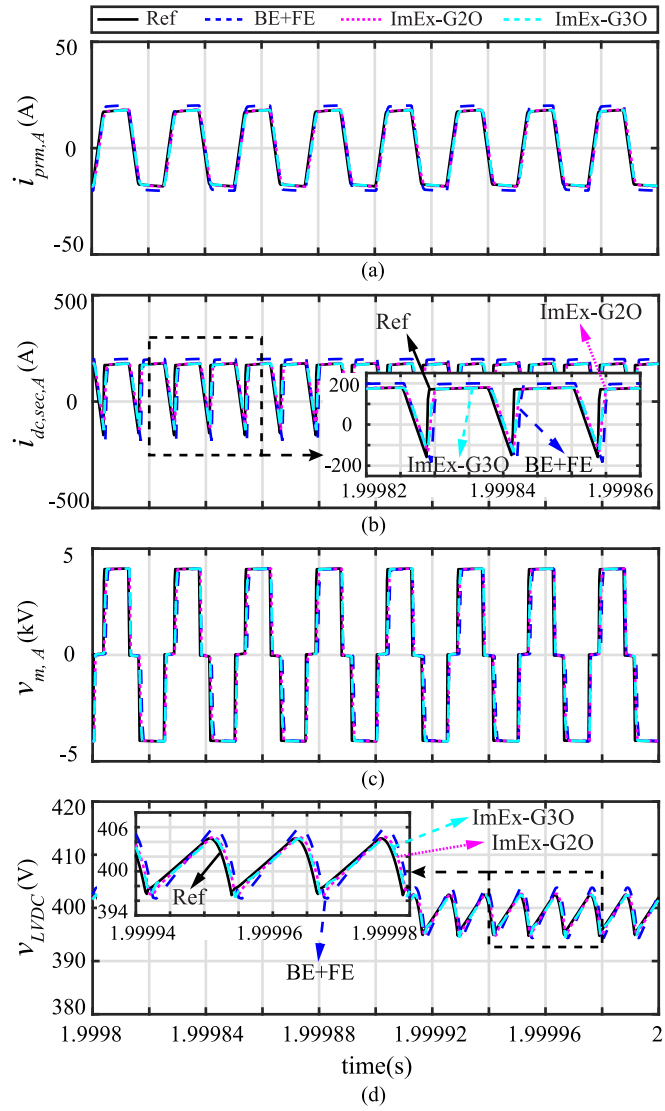

Fig. 22. Simulation performances of SST with 40 kHz switching frequency. (a) DAB primary AC current. (b) DAB secondary DC current. (c) DAB magnetizing-branch voltage. (d) LVdc-link capacitor voltage.

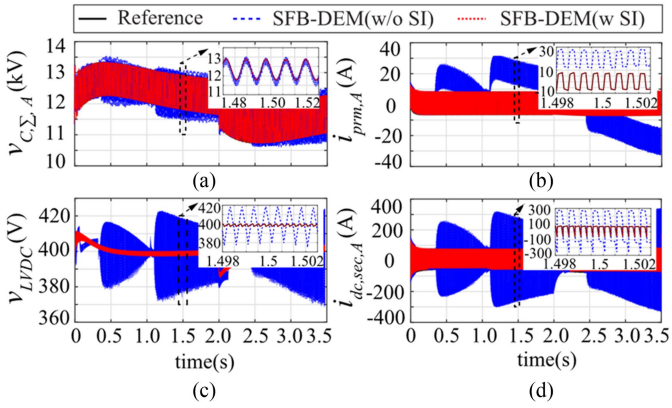

Fig. 23. Validation of switching interpolation technique. (a) Summation of MVdc-link capacitor voltages. (b) DAB primary AC current. (c) LVdc-link capacitor voltage. (d) DAB secondary-side DC current.

TABLE VIII
CPU EXECUTION TIME COMPARISONS FOR MULTIMODULE SST SIMULATION

Number of SMs (3 phases)	15	30	45	60
MATLAB/Simulink DM reference (TR)	134.71 s	571.67 s	1589.44 s	4065.89 s
VG-DEM (TR)	44.69 s	89.53 s	133.97 s	179.47 s
SFB-DEM (BE+FE)	15.80 s	18.21 s	20.64 s	23.18 s
SFB-DEM (ImEx-G2O)	15.97 s	18.65 s	21.00 s	23.47 s
SFB-DEM (ImEx-G3O)	16.49 s	19.18 s	21.45 s	23.76 s

due to inaccurate switching events detection. Comparatively, the SFB-DEM with switching interpolation (red dotted curve) demonstrates high numerical accuracy, since it matches with the reference solution, shown in Fig. 23. Moreover, this conclusion holds true across the two SST converter stages. By integrating the proposed multistep ImEx-type methods with the switching interpolation technique, the numerical accuracy of the EMT simulation is noticeably improved in the SFB-DEMs, particularly for a large time-step size.

8) Simulation Efficiency Comparison: The proposed SFB-DEMs with ImEx-type solvers not only achieve high numerical accuracy but also boost simulation efficiency significantly. As discussed previously, the computational burdens are alleviated in the proposed SFB-DEMs as they feature circuit decoupling, node elimination, and most importantly, constant nodal-network G-matrices.

Table VIII compares the CPU execution times of the SST SFB-DEMs with various ImEx-type solvers against the DM and VG-DEMs by increasing the scale of the SST with more SMs, i.e., 15, 30, 45 and 60 SMs (in three phases). For the VG-DEMs implementation, the circuit components are discretized using TR method while the semiconductor switches are represented by binary-value resistors, as demonstrated in Section II-B. Furthermore, the VG-DEMs are developed based on a 2-port Norton's equivalent circuits to accelerate the EMT simulation [8], [9]. For all tested models, the simulation duration is set to 1 s and the time step is 1 μs.

A nearest-level-control scheme is implemented in Stage I instead of LS-PWM to approximate the insertion number of the cascaded FBSMs of ac–dc converter in Stage I. As observed in Table VIII, the execution time of the SST DM increases exponentially with the numbers of SMs. Comparatively, the VG-DEM accelerates the EMT simulation significantly. However, its variable conductance matrix limits further improvement in simulation efficiency. On the other hand, the proposed SFB-DEMs with ImEx-type solvers are shown to be superior in boosting the simulation efficiency, especially when the SST scale is large. For the SST with 60 SMs, the proposed SFB-DEM with ImEx-G3O method greatly accelerates the EMT simulation by 171 and 7.5 folds, compared to the DM and VG-DEM, respectively. Meanwhile, the simulation efficiency of the SFB-DEMs with different orders of solvers are comparable. It is noted in Table VIII that the SFB-DEMs using ImEx-G2O and ImEx-G3O methods only incur less than 3% increase in execution time compared to the one with BE+FE solver. This characteristic holds true regardless of the increase in the number of SMs of the SST.

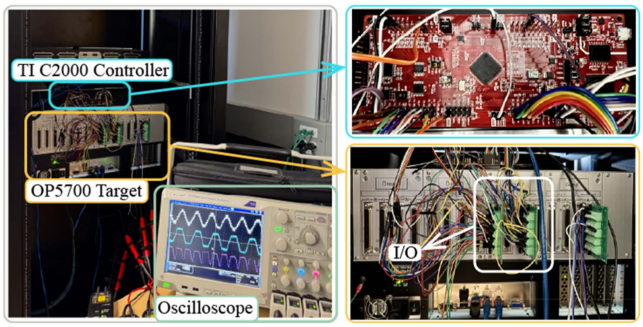

Fig. 24. CHIL real-time simulation platform setup.

V. Dynamic Performance of CHIL Experiments

In order to further validate the modeling fidelity of the proposed SFB-DEMs with multistep integration methods, experimental tests of controller-hardware-in-the-loop (CHIL) simulation are performed in this section. In the CHIL case study, an SST SFB-DEM (3 SMs per phase) is programmed using MATLAB script (m-file) and executed in CPU of OPAL-RT OP5700 real-time simulator. The network solution of the SFB-DEM is formulated using the ImEx-G2O method. Meanwhile, the switching interpolation technique is implemented to locate the switching events accurately.

As shown in Fig. 24, voltage mode controls of the SST are prototyped in a digital control platform (TI DSP) to regulate MVdc- and LVdc-link voltages. A Texas Instruments (TI) C2000 real-time digital microcontroller, i.e., TI LAUNCHXL-F280025C hardware is interfaced with the OP5700 real-time simulator through digital IOs.

Initially, dynamic performance of the real-time simulation has been validated against the off-line reference. Furthermore, as depicted in Fig. 8, the Stage I MVdc-link energy balance control and Stage II LVdc-link outer-loop voltage control have been replaced with the TI LAUNCHXL-F280025C digital controllers for the CHIL implementation. In this case study, the real-time simulation of the proposed SST SFB-DEM is tested with the time step of 20 μs. The real power reference is initialized at 1 p.u. and commanded to vary to 0.75 p.u. at $t = 20$ s, and restored back to 1 p.u. at $t = 22$ s.

Fig. 25 presents comparison of simulation results between CHIL tests acquired from the oscilloscope and the off-line reference. As shown in Fig. 25(a) and (b), the summation of MVdc-link capacitor voltages drops instantaneously at $t = 20$ s when the power reference steps down. Thereafter, the voltage magnitude gradually recovers to its rated value due to the effectiveness of the MVdc-link energy balance control. As Fig. 25(i) and (j) present, similar responses can be observed in the performances of the LVdc-link voltage, which is regulated by the outer-loop voltage control. Afterwards, both MVdc- and LVdc-link voltages recover back to their nominal values after the power reference is restored to 1 p.u. at $t = 22$ s. Overall, it has been validated that the performance of the CHIL experiments match well with the off-line reference during both steady-state periods and transients of the real-power-change operation.

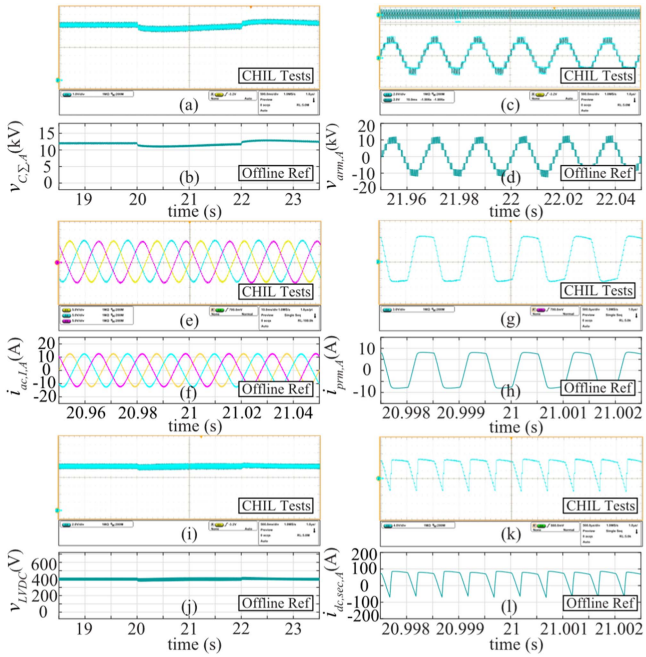

Fig. 25. Validation of CHIL experimental results. Sum of MVdc capacitor voltages in (a) CHIL test and (b) off-line simulation. Stage I arm voltage in (c) CHIL test and (d) off-line simulation. Stage I arm current in (e) CHIL test and (f) off-line simulation. Stage II DAB primary AC current in (g) CHIL test and (h) off-line simulation. LVdc-link voltage in (i) CHIL test and (j) off-line simulation. Stage II DAB secondary-side DC current in (k) CHIL test and (l) off-line simulation.

VI. Hardware Verification

This section validates the proposed DEMs using hardware tests of a scaled-down SST prototype circuit, which has single-phase chainlink circuit with three full-bridge SMs and three DAB dc–dc modules in the chainlink. A dc power supply is applied to the parallel-connected LVdc-link capacitor of the SST to send the power to the ac–dc chainlink converter in the MVac side. The hardware setup is built using Imperix power electronics testbench, controlled by OPAL-RT OP5707XG FPGA and digital I/Os, as shown in Fig. 26. The SST FB converters are realized using nine Imperix PEH4010 FB converters that are connected to external transformers, a dc power supply, and an ac-side inductive-resistive load. The OPAL-RT OP5707XG is used as a real-time controller to balance the capacitor voltages of the FBSMs and to regulate the power transferred across the DABs. The switching frequency of the DAB converter is 2 kHz, while the chainlink FBSMs use nearest level control to modulate the ac-side voltage.

Fig. 27 shows the measured ac-side chainlink (arm) voltage and current as well as the DAB primary-side current. In order to validate the proposed DEM in a dynamic case study, the ac-side modulating signal increases its frequency from 60 to 120 Hz once the steady state is reached. As shown in Fig. 27(a), the ac-side frequency step-change causes a corresponding change in the arm voltage and ac current waveforms. The hardware waveforms obtained in Fig. 27 are overlapped with the simulation results of the DM reference obtained by Simulink/Simscape

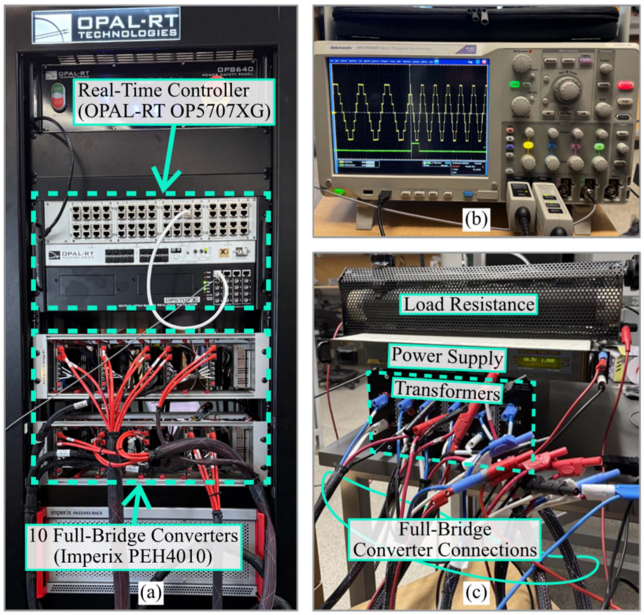

Fig. 26. Laboratory hardware setup. (a) OPAL-RT power electronics test-bench. (b) Oscilloscope measurement. (c) Electrical hardware components.

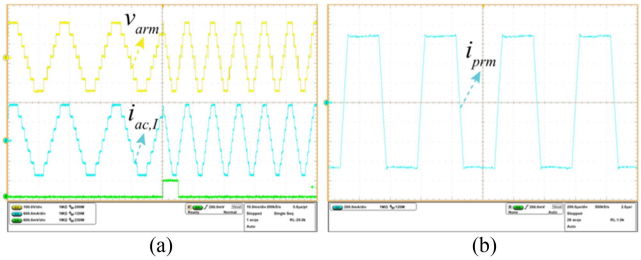

Fig. 27. Dynamic frequency-change system response. (a) Arm current and arm voltage. (b) DAB primary ac current.

Electrical Toolbox and the proposed SFB-DEM employing a multistep ImEx-G3O solver, as shown in Fig. 28. As shown in Fig. 28, the simulation results of the proposed SFB-DEM align well with those of the hardware and the DM reference. Hence, the modeling fidelity of the proposed SFB-DEM has been further validated by laboratory hardware results.

VII. Discussion

This section presents the analysis of the stability regions for various explicit-type integration methods including FE, 2nd-order Adams-Bashforth, 3rd-order Adams-Bashforth, the Ex-G2O, the Ex-G3O, and the implicit-type solvers including implicit Gear's 2nd-order (Im-G2O) and implicit Gear's 3rd-order methods, as shown in Fig. 29. The derivation of numerical stability regions of the Ex-G2O is given below as example. The derivation of numerical stability regions of the Ex-G3O is omitted for space consideration, but can be derived following the same procedure for Ex-G2O stability analysis. A general

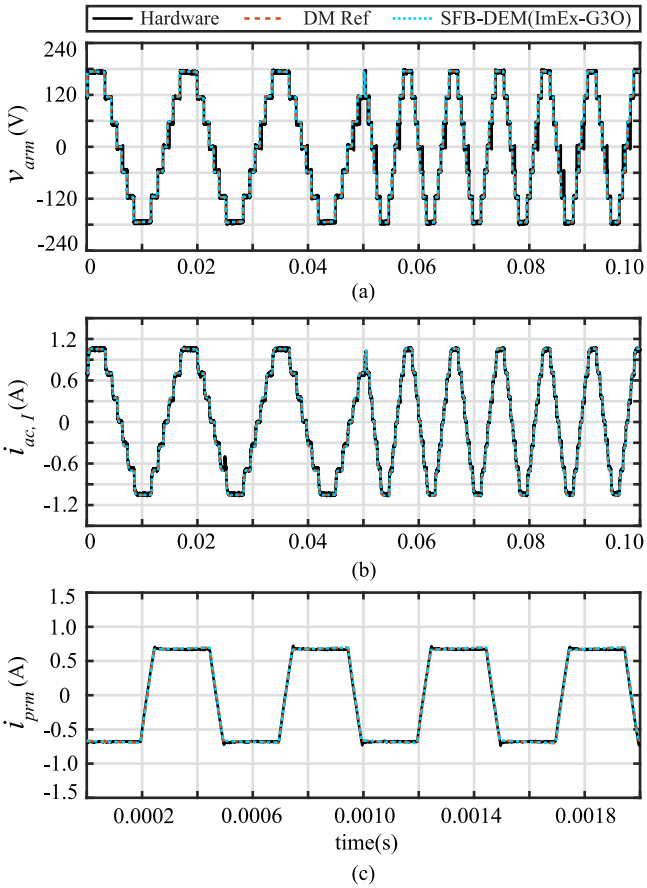

Fig. 28. Hardware validation results. (a) AC-side arm voltage. (b) AC-side current. (c) DAB AC primary transformer current.

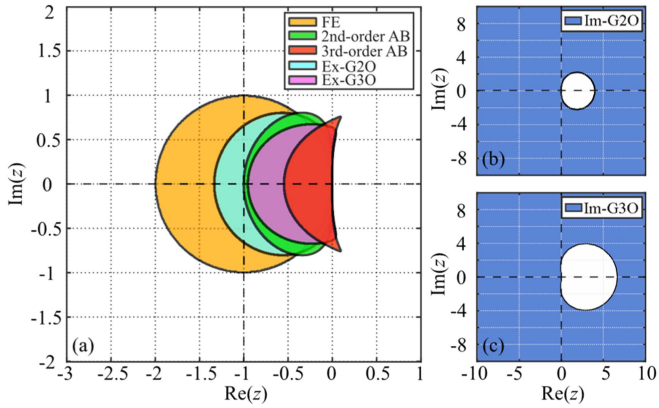

Fig. 29. Stability regions of numerical integration methods. (a) Explicit integration methods. (b) Implicit Gear's 2nd order method. (c) Implicit Gear's 3rd order method.

formula of Ex-G2O integration method is provided in (26), where t_{k+1} denotes the present simulation step

$$y\ (t_{k+1}) = \left(\frac{4}{3}y\,(t_k) - \frac{1}{3}y\,(t_{k-1})\right) + \frac{2\Delta t}{3} \cdot \left(2f\,(y\,(t_k)) - f\,(y\,(t_{k-1}))\right). \tag{26}$$

The stability parameter is denoted by Z_{ExG2O} and computed in (27), where λ_{ExG2O} denotes the eigenvalue of the ODE system using Ex-G2O method

$$Z_{\text{ExG2O}} = \lambda_{\text{ExG2O}}\, \Delta t. \tag{27}$$

By employing standard linear equation, $f\ (y) = \frac{dy}{dt} = \lambda_{\text{ExG2O}}\ y$ in (26)

$$\begin{aligned} y\ (t_{k+1}) &= \left(\frac{4}{3}y\,(t_k) - \frac{1}{3}y\,(t_{k-1})\right) + \frac{2\Delta t}{3} \\ &\quad \cdot (2\lambda_{\text{ExG2O}} \cdot y\,(t_k) - \lambda_{\text{ExG2O}} \cdot y\,(t_{k-1})) \\ &= \frac{1}{3}\left[(4 + 4Z_{\text{ExG2O}}) \cdot y\,(t_k) - (1 + 2Z_{\text{ExG2O}}) \cdot y\,(t_{k-1})\right]. \end{aligned} \tag{28}$$

Substituting $y(t_{k+1})$ with ξ^{k+1} where ξ is amplification factor, the characteristic equation can be derived from (28) as

$$\begin{aligned} \xi^{k+1} - \frac{1}{3} \cdot (4 + 4Z_{\text{ExG2O}}) \cdot \xi^k + \frac{1}{3} \\ \cdot (1 + 2Z_{\text{ExG2O}}) \cdot\ \xi^{k-1} =\ 0. \end{aligned} \tag{29}$$

The characteristic equation of Ex-G2O can be obtained by dividing ξ^{k-1} at both sides of (29) as

$$3\xi^2 - (4 + 4Z_{\text{ExG2O}}) \cdot \xi +\ (1 + 2Z_{\text{ExG2O}}) =\ 0. \tag{30}$$

The stability region of the Ex-G2O method can be plotted in complex z-plane. This method is stable for all values of z when the roots of the characteristic (30) satisfy

$$|\xi\,(Z_{\text{ExG2O}})| \leq 1. \tag{31}$$

The numerical stability regions of various integration methods are plotted in Fig. 29 as the shaded areas. As shown in Fig. 29, the stability regions decrease when the orders of the explicit integration methods increase. In comparison of various explicit integration methods, the 1st-order FE method processes the largest stability region. It is also noted that the Explicit Gear's methods always have larger stability region than those of the AB methods with the same numerical order. Meanwhile, as observed in Fig. 29(b) and (c), the stability region of the Im-G2O occupies the whole left-half plane while the stability region of the Im-G3O covers a majority of the left-half plane. Hence, it further explains why the combined ImEx-type multistep Gear's methods become an appropriate choice for formulating network solutions of the proposed SFB-DEMs. However, when a dc-link capacitor is subjected to fast transient, such as short-circuit/shoot-through fault, numerical instability may occur when the multistep explicit-type methods are used to discretize the dc-link capacitors. In order to avoid numerical instability, either the simulation time steps have to be reduced to capture the fast short-circuit transient or the explicit integration method needs to be replaced by an implicit integration method, such as TR for discretizing the dc-link capacitor.

VIII. Conclusion

This article proposes an SFB-DEM with multistep ImEx Gear's solver for numerically efficient and accurate EMT simulation of multimodule SST. Converter circuit decoupling is achieved by applying explicit G2O or G3O to integrate dc-link capacitor voltages. The use of switching function to model the FBSMs achieves significant node number reduction and constant nodal-network G-matrix, which accelerates the EMT simulation of the SST. Meanwhile, the use of implicit G2O or G3O methods for the other circuit elements than the dc-link capacitors improve the numerical accuracy, compared to the 1st order methods, e.g., FE and BE methods and is immune to fictitious numerical oscillations compared to the TR method. The switching interpolation technique is proposed and integrated to the ImEx-G2O and ImEx-G3O solvers to improve numerical accuracy for large-time-step simulation. The simulation accuracy and efficiency of the proposed SFB-DEMs are validated by performing multiple off-line case studies and CHIL experiment tests. It is shown in the case studies that the proposed SFB-DEM with ImEx-Gear's methods achieve significant speedups in EMT simulation (e.g., 171 and 7.5 folds by ImEx-G3O), compared to the DM and VG-DEM for the SST with 60 SMs, respectively.

Appendix

TABLE IX
System Parameters of Multimodule SST

Items	Symbols	Values	
MVDC-link rated voltage	v_{MVDC}	4 kV	
LVDC-link rated voltage	v_{LVDC}	0.4 kV	
Number of SMs per phase	N_{SM}	3	
MVAC line inductance	L_{ac}	250 mH	
Stage I carrier frequency	f_I	5 kHz	
Transformer turns ratio	N_r	10	
Transformer primary and secondary leakage inductances	$L_{lk,\text{prm}}$ $L_{lk,sec}$	21 mH	
Case Studies		Case 1	Case 2
Stage II DAB switching frequency	f_{DAB}	2 kHz	40 kHz
MVDC-link capacitance	C_1	37.5 μF	187.5 μF
LVDC-link capacitance	C_2	11.2 mF	0.56 mF
Real power rating	P_{ref}	180 kW	450 kW
LVDC-side load	R_{Load}	0.889 Ω	0.3556 Ω
Time step of reference	$T_{s,\text{ref}}$	1 μs	200 ns
Time step of tested models	T_s	10 μs	500 ns

References

[1] X. She, A. Q. Huang, and R. Burgos, "Review of Solid-State Transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[2] J. E. Huber and J. W. Kolar, "Applicability of solid-State transformers in today's and future distribution grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.

[3] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE PES Gen. Meeting*, 2010, pp. 1–8.

[4] M. A. Hannan, P. J. Ker, M. S. H. Lipu, Z. H. Choi, M. S. A. Rahman, and K. M. Muttaqi, "State of the art of solid-State transformers: Advanced topologies, implementation issues, recent progress and improvements," *IEEE Access*, vol. 8, pp. 19113–19132, 2020.

[5] K. G. D, S. T N, and N. N, "Solid State transformers for smart grid control and applications — A review," in *Proc. Int. Conf. Futuristic Tech. Control Sys. Renewable Energy*, 2022, pp. 1–6.
[6] A. R. Rodríguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional DC/DC conversion," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1129–1135.
[7] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
[8] J. Xu et al., "High-speed electromagnetic transient (EMT) equivalent modelling of power electronic transformers," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 975–986, Apr. 2021.
[9] C. Gao, M. Feng, J. Ding, H. Zhang, J. Xu, and C. Zhao, "Accelerated electromagnetic transient (EMT) equivalent model of solid-state transformer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 3721–3732, Aug. 2022.
[10] M. Feng, C. Gao, J. Xu, C. Zhao, and G. Li, "A novel decoupled EMT approach and parallel simulation framework for modularized solid-state transformers," *IEEE Trans. Power Del.*, vol. 38, no. 5, pp. 3285–3295, Oct. 2023.
[11] P. Pejovic and D. Maksimovic, "A method for fast time-domain simulation of networks with switches," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 449–456, Jul. 1994.
[12] P. Pejovic and D. Maksimovic, "A new algorithm for simulation of power electronic systems using piecewise-linear device models," *IEEE Trans. Power Electron*, vol. 10, no. 3, pp. 340–348, May 1995.
[13] L. Qi, S. Woodruff, and M. Steurer, "Study of power loss of small time-step VSC model in RTDS," in *Proc. IEEE Power Eng. Soc. Gen. Meeting*, 2007, pp. 1–7.
[14] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time HIL test bench," *IEEE Trans. Power Del.*, vol. 31, no. 5, pp. 2401–2409, Oct. 2016.
[15] R. Parvari, S. Filizadeh, and D. Muthumuni, "An accelerated detailed equivalent model for modular multilevel converters," *Electric Power Syst. Res.*, vol. 223, 2023, Art. no. 109648.
[16] F. Zhang and W. Li, "An equivalent circuit method for modeling and simulation of dual active bridge converter based marine distribution system," in *Proc. IEEE Electric Ship Technol. Symp.*, 2019, pp. 382–387.
[17] X. Meng and W. Li, "Equivalent circuit modeling method for real-time simulation of multi-active bridge based solid-state transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 798–802.
[18] E. Hairer and G. Wanner, *Solving Ordinary Differential Equations II: Stiff and Differential Algebraic Problems* (Springer Series in Computational Mathematics), 2nd rev. ed. New York, NY, USA: Springer, 2002.
[19] J. R. Marti and J. Lin, "Suppression of numerical oscillations in the EMTP power systems," *IEEE Trans. Power Syst.*, vol. 4, no. 2, pp. 739–747, May 1989.
[20] L. F. R. Ferreira et al., "Comparative solutions of numerical oscillations in the trapezoidal method used by EMTP-based programs," in *Proc. Int. Conf. Power Syst. Transients*, 2015, pp. 147–153.
[21] J. Tant and J. Driesen, "On the numerical accuracy of electromagnetic transient simulation with power electronics," *IEEE Trans. Power Del.*, vol. 33, no. 5, pp. 2492–2501, Oct. 2018.
[22] U. M. Asher, S. J. Ruuth, and B. T. R. Wetton, "Implicit-explicit methods for time-dependent partial differential equations," *SIAM J. Numer. Anal.*, vol. 32, no. 3, pp. 797–823, 1995.
[23] B. Li, K. Wang, and Z. Zhou, "Long-time accurate symmetrized implicit-explicit BDF methods for a class of parabolic equations with non-self-adjoint operators," *SIAM J. Numer. Anal.*, vol. 58, no. 1, pp. 189–210, 2000.
[24] B. De Kelper, L. A. Dessaint, V. Q. Do, and J. C. Soumagne, "An algorithm for accurate switching representation in fixed-step simulation of power electronics," in *Proc. IEEE Power Eng. Soc. Winter Meeting. Conf. Proc.*, 2000, pp. 762–767.
[25] B. De Kelper, L. A. Dessaint, K. Al-Haddad, and H. Nakra, "A comprehensive approach to fixed-step simulation of switched circuits," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 216–224, Mar. 2002.
[26] A. M. Gole, I. T. Fernando, G. D. Irwin, and O. B. Nayak, "Modeling of power electronic apparatus: Additional interpolation issues," in *Proc. Int. Conf. Power Syst. Transients*, Jun. 1997, pp. 23–28.
[27] C. Dufour, J. Mahseredjian, and J. Bélanger, "A combined State-space nodal method for the simulation of power system transients," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 928–935, Apr. 2011.
[28] W. Li and F. Zhang, "A general interpolated model of voltage source converters for real-time simulation and HIL test applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 6155–6616.
[29] S. Horiuchi, K. Sano, and T. Noda, "An inverter model simulating accurate harmonics with low computational burden for electromagnetic transient simulations," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5389–5397, May 2021.
[30] K. Sano, S. Horiuchi, and T. Noda, "Comparison and selection of grid-tied inverter models for accurate and efficient EMT simulations," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3462–3472, Mar. 2022.
[31] J. Xu et al., "FPGA-based submicrosecond-level real-time simulation of solid-State transformer with a switching frequency of 50 kHz," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4212–4224, Aug. 2021.
[32] Z. Li, J. Xu, K. Wang, G. Li, P. Wu, and L. Zhang, "An FPGA-based hierarchical parallel real-time simulation method for cascaded solid-State transformer," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3847–3856, Apr. 2023.
[33] B. Shang, N. Lin, and V. Dinavahi, "Detailed nonlinear modeling and high-fidelity parallel simulation of MMC with embedded energy storage for wind farm grid integration," *IEEE Open Access J. Power Energy*, vol. 11, pp. 196–206, 2024.
[34] K. Fung and S. Hui, "Fast simulation of multistage power electronic systems with widely separated operating frequencies," *IEEE Trans. Power Electron.*, vol. 11, no. 3, pp. 405–412, May 1996.
[35] Z. Guo, L. Li, Z. Liu, K.-J. Li, K. Sun, and J. Feng, "Multi-time-scale electromagnetic modeling of a battery-integrated solid-State transformer," *IEEE Trans. Ind. Appl.*, vol. 61, no. 5, pp. 7903–7915, Sept./Oct. 2025.
[36] H. W. Dommel, "Digital computer solution of electromagnetic transients in single-and multiphase networks," *IEEE Trans. Power App. Syst.*, vol. PAS-88, no. 4, pp. 388–399, Apr. 1969.
[37] M. McGranaghan, D. Mueller, and M. Samotyj, "Voltage sags in industrial systems," in *Proc. Conf. Rec. Ind. Commercial Power Syst. Tech. Conf.*, 1991, pp. 18–24.
[38] J. Pedra, L. Sainz, F. Corcoles, and L. Guasch, "Symmetrical and unsymmetrical voltage sag effects on three-phase transformers," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 1683–1691, Apr. 2005.
[39] M. T. Aung and J. V. Milanovic, "The influence of transformer winding connections on the propagation of voltage sags," *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 262–269, Jan. 2006.

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