# A Novel Hybrid Circuit Breaker Architecture With Built-in Current Limiting Capability – I: Semiconductor Design

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***Abstract*—Fault interruption in high-power dc distribution applications is challenging owing to the fast rate of rise of short circuit currents and the lack of a natural zero crossing in the current. A hybrid dc circuit breaker (HCB) has emerged as a promising solution that synthesizes the fast interruption speed of solid-state breakers with the low ON-state losses of mechanical circuit breakers. This work introduces a novel concept of current-limiting (CL) HCB capable of actively clamping the fault current for a few hundred microseconds, thereby ensuring the downstream CB acts first in case of a fault event. This protection coordination scheme guarantees selectivity and prevents loss of coordination. The proof-of-concept prototype is developed using a pair of series-connected IGBTs connected in parallel to varistors as a CL branch. This work carried out a successful CL function of 4.5 kA for 100 $\mu$s and subsequent current interruption within 180 $\mu$s for a di/dt ranging from 4 A/$\mu$s to 40 A/$\mu$s. The article also provides a comprehensive discussion on the selection of semiconductor devices, surge current conduction capability, and current turn-OFF characteristics based on experimental evaluation of multiple commercially available packages. Analytic calculations of clamping device viability are also analyzed to assess suitability for practical implementation.**

***Index Terms*—Current limiting, datacenters, dc fault isolation, dc microgrid, fault current interruption time, hybrid circuit breaker (HCB), IGBT, IGBT turn-OFF capability, surge current conduction.**

## I. Introduction

DC MICROGRIDS are becoming popular because of their industry leading benefits like minimized losses, optimized efficiency, absence of reactive power, and their potential of directly connecting renewable energy sources. One of the greatest difficulties of the dc grids is the interruption of fault currents due to a lack of zero current crossing. DC grids offer much lower impedance, which leads to a 5–10 times faster rate of rise of fault currents in dc systems compared to ac systems [1], [2], [3], [4]. Conventional mechanical circuit breakers (MCBs) cannot manage such rapidly rising fault currents in case they are required to be interrupted rapidly [5]. Alternatively, the recently developed solid-state circuit breakers (SSCB) offer a solution using power semiconductor devices that can interrupt fault currents within a few hundred microseconds. However, in SSCBs, power semiconductor devices are responsible for carrying nominal, overload currents as well as interrupting fault currents. As a result, they exhibit high conduction losses and need a large heat dissipation system. Additionally, they need a galvanic isolation switch and are susceptible to transient overvoltage and sensitive to overcurrent [6], [7]. To address the drawbacks of MCB and SSCB, the integration of a mechanical switch and semiconductor switch is investigated, commonly known as a hybrid dc circuit breaker (HCB), and is widely acknowledged among researchers.

HCBs can interrupt fault current rapidly by diverting it to the solid-state branch from the mechanical branch before interrupting it completely. HCBs are a promising solution offering high efficiency, reliability, and admissible response time ($\sim$ 600 $\mu$s) [8]. Once the mechanical switch in the HCB is commanded to open, we must wait for a certain amount of time before any voltage can be applied across the mechanical switch. This creates a separate problem for HCBs due to the specific nature of dc networks, wherein a short circuit current is only restrained by a tiny fault resistance. The rate of rise of the short-circuit current itself is only limited by the fault inductance. Thus, the semiconductor branch of a conventional HCB must keep conducting an ever increasing short-circuit current until the mechanical switch is capable of fully blocking the dc bus voltage, at which point, the semiconductor switch can be turned OFF to commutate the current into the voltage clamping circuit. The voltage clamping circuit generates counter-voltage on the fault inductance and eventually interrupts the fault current. In such a situation, the required current rating of the semiconductor branch can increase significantly as it is required to carry the short-circuit current for an extended amount of time. In this article, we focus on pursuing an alternate strategy to limit the short-circuit current for hundreds of microseconds after a period of conduction and then interrupting it completely.

The literature review of this article is aligned towards cost-effective, reliable, and high-performance CL topologies for HCB. The literature consists of various ways to limit the fault

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TABLE I
COMPARISON OF THE PROPOSED HCB WITH SIMILAR APPROACHES

| Topology | CL technology | Features | Limitations | Complexity | CL time | Scalability |
|---|---|---|---|---|---|---|
| [7] | Resistor + mechanical switch (MS) | ✓ No MOV needed | × Bulky and lossy as large resistance is needed,<br>× Lifetime limitations of MS | Medium | Not reported | Moderate |
| [9] | Fuse + IGBT | ✓ Fast fault current interruption | × Single use<br>× Limited repetitive capability<br>× Coordination complexity | High | Not reported | Low |
| [11], [12], [17] | Superconducting coil, [17]-liquid metal limiter | ✓ promising for high power | × Requires cryogenics<br>× Requires thermal management | Medium | Not reported | Difficult |
| [13], [14], [15], [16], [18], [19] | Thyristor based resonant CL and turn-off, [19]-di/dt limiter | ✓ Precharging of the capacitor helps reduce voltage overshoot and shape the fault current | × Involves multiple circuits<br>× Needs coordination<br>× Lossy and bulky<br>× Requires precharged Cap. | High | ~ 400 μs to 500 μs | Moderate to high |
| Proposed Topology | IGBT module and MOVs | ✓ Faster current interruption<br>✓ Lower device count<br>✓ Guarantees selectivity for protection and coordination<br>✓ No capacitor or aux circuits | × Additional MOVs may be needed in parallel to optimize lifetime of HCB over an extended operation | Low | 100 μs | Highly Modular |

current, such as using CL fuses [9], [10] and superconductors [11], [12]. The study in [9] develops a novel CL hybrid DCCB based on a fuse and an IGBT module to avoid operation delay associated with mechanical contacts, with a CL performance limited to 1 kA fault current interruption.

Fuses enable fast fault clearing, high interruption capability, but are inflexible to different trip thresholds, require manual replacement after one use, and coordination [10].

Some literature works [11], [12] study HCB based on superconducting material, offering potential to open at low current. But superconductors entail high cost and require special attention to maintain cryogenic temperature. These solutions are inadequate for current interruption under severe current interrupting conditions. Analysis in [13] and [14] verified CL concepts that exploit inductors to limit the rate of rise of fault current using simulations, although no hardware validation of this novel topology is reported. Additionally, inductors are bulky, lossy, higher form factor as well as expensive. Wang et al. [15] introduced a novel HCB with additional passive components to reduce the rate of rise of fault current as it assists in reducing the stress on semiconductor devices but their main focus is on overall cost reduction of HCB. A low loss branch and current commutation switch with additional CL and precharge circuit is proposed in [16] to improve current limitation and energy dissipation capability. However, multiple circuits necessitate coordination and increase complexity, potentially limiting its application. Nonetheless, Yin et al. [17] outlined a use of liquid metal device to limit the fault current but this necessitates maintenance challenges, integration, and cause reliability issues, limiting its application to compact SSCB. Lulu et al. [18] proposed a fast CL HVdc CB consisting of multiple submodules to improve interruption speed, but at the cost of increased system size for MV dc applications. A novel CL dc HCB in [19] utilizes a combinatorial electronic power switch in addition to a CL circuit to reduce the number of series-connected power electronic devices and suppress fault current rise. However, this solution is complex and difficult to deploy for adapting to high voltage dc system. Literature does not provide an HCB solution that has built-in CL capabilities using a fewer semiconductor device and has a capability to clear fault faster. Table I summarizes the features and limitations of existing CL HCB topologies available in literature. It is to be noted that this table only focusses on CL technology of HCBs. Although almost every topology involves MS and surge arrestors common to most designs for carrying nominal current and, hence, not compared. Compared to the works proposed in literature, this article provides a simplified solution that explores the concepts of CL and current interruption, where the fault current is held at a constant level for a few microseconds, preventing its uncontrolled rise, until the mechanical switch is ready to block the full source voltage. Semiconductor devices of the proposed HCB concept bear surge current for a few milliseconds and need to turn OFF the peak surge current safely. Besides, the built in CL feature ensures selectivity and improves overall fault handling of CBs in dc distribution system. Furthermore, this article proposes a solution that is modular to implement for MVdc industrial or shipboard dc grids applications. This topology uses fewer semiconductor devices to limit the fault current, which reduces electrical and thermal stress on the switching devices, especially during turn-OFF, thereby extending their operational lifespan and minimizing derating requirements. Also, the control and coordination effort needed to turn ON and OFF the devices are minimum and with no additional circuitry needed.

The proposed concept is validated experimentally using semiconductor devices, each for the CL and current interruption stage. This brings additional challenges that require comprehensive investigation. The rest of this article is organized as follows. Section II explains the novel concept of the proposed topology and its CL feature, which enables coordinated protection of radially connected circuit breakers. In Section III, an analysis of the selection of semiconductor devices and the selection of blocking voltage rating with different module packages is reported. This section also contains the analysis about the selection of metal oxide varistor (MOV), the mechanical assembly adopted to build the prototype, and the custom-made gate driver design. Section IV demonstrates the details of the experimental

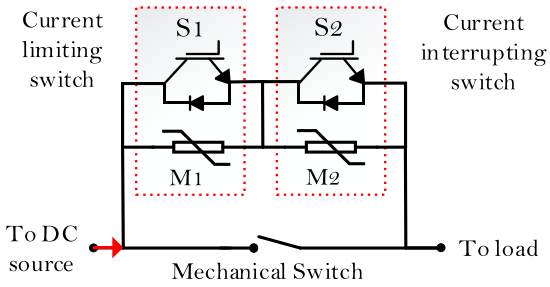


Fig. 1. Semiconductor based circuit topology of HCB.

TABLE II
TARGET SPECIFICATIONS OF THE PROPOSED HCB

| Parameter | Requirement Value |
|---|---|
| Nominal dc voltage | 1.5 kV |
| Nominal current | 250 A |
| Interrupting and limiting current level | 4.5 kA |
| Current limiting duration | 40 µs – 120 µs |
| Current interruption duration | 20 µs – 30 µs |
| Current commutation duration | 200 µs – 500 µs |
| MOV clamping voltage | 1 kV – 2 kV |

setup used to validate the novel HCB. In Section V, the results are demonstrated with relevant waveforms. Finally, Section VI concludes this article.

## II. CONCEPT OF PROPOSED TOPOLOGY

### A. Working Principle of Proposed Topology

Fig. 1 shows that the HCB topology employs a combination of semiconductor switch pairs connected in parallel with clamping devices, such as MOV, along with a mechanical switch (MS) to enable rapid and efficient current interruption. During normal operation, the MS carries the current with low ohmic losses, and semiconductor switches are kept OFF. Upon the detection of the fault, the MS is commanded to open, and the semiconductor switches are turned ON following a sequence to carry the fault current and interrupt it gradually. When semiconductor switches are turned OFF, the fault current commutates to the MOV. The MOV absorbs the transient energy stored in the system's inductance and generates a counter voltage that causes the fault current to decay to zero. During this time, the MS cannot block the full voltage instantaneously when commanded to open, as the opening distance is insufficient and the gas in the gap is too conductive; hence, semiconductor switches are operated to carry the fault current for a few milliseconds. Although the article focuses on a unidirectional current flow from the dc source to the load and semiconductor branch, the proposed design can also be extended to bidirectional HCBs.

The following Table II shows the key parameters considered to develop the prototype of the HCB topology.

### B. Operation Principle of Proposed Topology

Fig. 2 illustrates the timing sequence of HCB, while Fig. 3 reveals the operation modes for the proposed HCB.

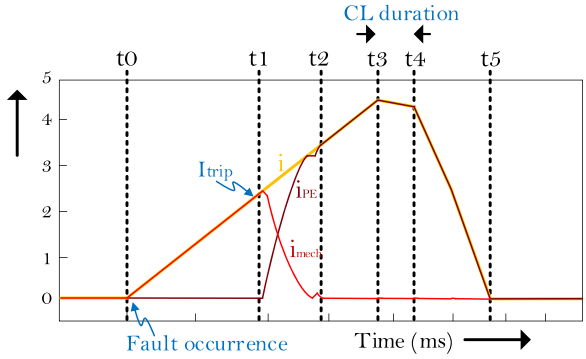


Fig. 2. Timing sequence upon fault occurrence of HCB.

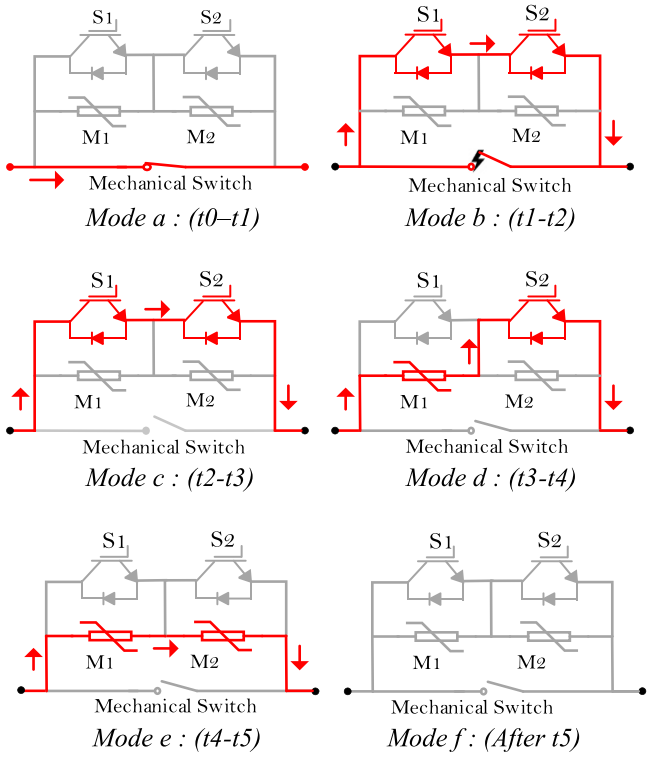


Fig. 3. Operation modes of the proposed HCB topology.

*Mode a (t0–t1):* Under normal operation, the nominal current flows through the MS, and semiconductor switches remain OFF. The fault occurs at time *t0*, and the nominal current starts to rise rapidly, as seen in Fig. 2.

*Mode b (t1–t2):* Somewhat before *t1,* when the fault current reaches $I_{trip}$, the semiconductor switches are turned ON and the MS begins to open *t1*. As the MS contact begins to separate, an arc is formed, and arcing voltage increases. This arcing voltage results in gradual current reduction flowing through MS, $i_{mech}$ and current starts to commute to devices. It is essential to point out that even if the semiconductor switches are turned ON, they do not conduct instantaneously because the voltage across MS is initially minimal. Each IGBT exhibits a forward voltage; accordingly, the MS must develop a voltage exceeding the total forward voltage of each IGBT before current can begin commutating to the IGBTs.

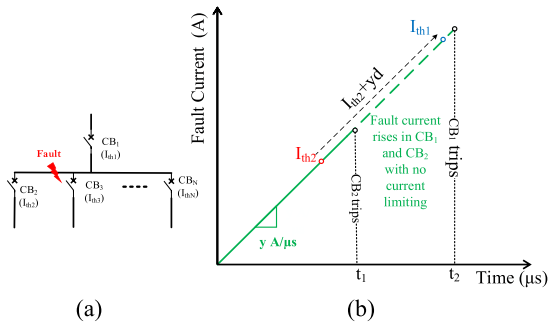


Fig. 4. (a) Radially connected CBs in a DC distribution system. (b) Trip sequence indicating coordination failure.

*Mode c (t2–t3):* At time *t2*, the commutation is over, and dielectric recovery starts, where the full fault current is carried by semiconductor switches $i_{PE}$. Even during this time, the full voltage cannot be applied to MS, as the arc could reignite.

*Mode d (t3–t4):* At time *t3*, the "*Current limiting switch*" S1 is turned OFF, causing the fault current to commutate to MOV M1. Subsequently, M1 begins to dissipate the system's energy as its impedance decreases, and this leads to a voltage rise across switch S1. During this time, the MS can withstand the partial voltage rise corresponding to the MOV M1, but not the full voltage of two MOVs. The time between *t3-t4* represents the "*Current limiting time*". During the CL mode, MOV1 or MOV2 can be used alternatively to achieve a balanced lifetime between them.

*Mode e (t4–t5):* By time *t4*, the MS has achieved sufficient separation and is capable of withstanding the total voltage of MOVs M1 and M2; thus, "*Current interrupting switch*" S2 is turned OFF, and the fault current transfers to M2. The time between *t4-t5* is called "*Current interruption time*".

*Mode f (After t5):* After time *t5*, the fault current is finally interrupted, blocking the full dc source voltage.

The proposed topology can be extended to higher voltage levels or with a high number of MOVs in series. The number of MOVs can be selectively determined during the CL mode.

### C. Protection and Coordination of CL HCBs

The general strategy of breaker coordination is that the "downstream" breaker should trip first for clearing the fault, and the "upstream" breaker (CB) acts as a backup with a time-delayed protection setting. Fig. 4(a) represents a radial dc distribution system (or dc microgrid) with multiple circuit breakers (CBs) arranged in a selective protection hierarchy. $CB_1$ is the upstream breaker while $CB_2$,.., $CB_N$ are the downstream breakers. For illustration, consider $CB_2$ detects the fault and issues a trip command as fault current reaches its trip threshold $I_{th2}$. During this interval, $CB_1$, being the upstream breaker, also conducts the same fault current. Because of the inherently high di/dt associated with dc faults and total system delay d, the fault current continues to rise rapidly [see green trajectory of Fig. 4(a)].

This uncontrolled increase places the HCBs component under excessive thermal and electrical stress. Eventually, the fault current reaches the trip threshold $I_{th1}$ of $CB_1$ as well, causing $CB_1$ to operate unintentionally. This lack of selectivity underlines the challenge of protection coordination of dc breakers under fast faults. The protection coordination is lost if both the breakers trip; then the selectivity and survivability of the system are compromised. Therefore, the aim is to limit the fault current and ensure that only the downstream CB clears the fault while the upstream CB remains closed, maintaining the system stability for high di/dt fault scenarios.

TABLE III
COMPARISON OF DIFFERENT SEMICONDUCTOR DEVICES

| Parameters | SiC MOSFET | IGCT | SCR (forced commutation) | IGBT |
|---|---|---|---|---|
| **Thermal capacitance** | Low | High | Very High | Medium |
| **Conduction loss** | Medium | Low | Very Low | High |
| **Switching loss** | Low | High | Very High | Medium |
| **Paralleling capability** | High | Low | Low | Medium |
| **Gate driver complexity** | Low | High | High | Low |
| **Cost** | High | Medium | Low | Medium |
| **Reliability** | Medium | High | Very High | High |

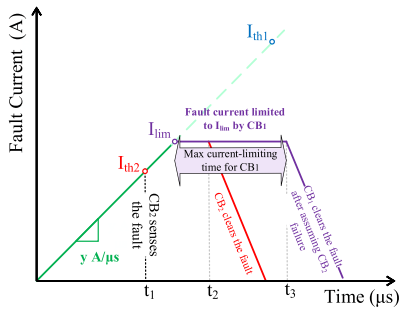


Fig. 5. Trip coordination sequence between $CB_1$ and $CB_2$ using CL mode.

This section focuses on a protection coordination strategy using the built-in CL feature of the proposed HCB topology. This challenge is addressed by actively limiting the fault current for a short duration ($\sim 100\,\mu s$) without further stressing semiconductor devices. This controlled delay allows the upstream CB to trip without relying on high fault current levels. The HCB uses a fast-switching IGBT and energy-absorbing components to limit the fault current during this brief window, effectively decoupling fault current magnitude from trip timing. This ensures that the following conditions hold.

1) Fault current is contained within safe limits, reducing stress on devices.
2) Selective tripping is maintained, improving system reliability.
3) The upstream CB can trip promptly and safely if the downstream CB fails.

Fig. 5 demonstrates the coordinated sequence between $CB_1$ and $CB_2$, where $CB_1$ incorporates an active CL feature. At time $t_1$, $CB_2$ detects the fault current and prepares to trip. Before $CB_2$ trips, $CB_1$ enters CL mode, preventing the fault current from

rising further and limiting it to $I_{lim}$. $CB_2$ subsequently clears the fault as planned, shown by the red trajectory in Fig. 5. The key novelty of the CL feature becomes apparent if $CB_2$ fails to trip. In this case, $CB_1$ maintains CL mode until its maximum allowable CL duration is reached, after which $CB_1$ clears the fault at time $t_3$ shown by the purple trajectory of Fig. 5. Evidently, the allowable CL duration is determined by the thermal limits of MOVs. This controlled action provides adequate time for the downstream breaker $CB_2$ to clear the fault first. If $CB_2$ fails, $CB_1$ serves as an automatic backup and clears the fault once its maximum CL duration has elapsed. This approach ensures proper coordination, enhances system reliability, and reduces electrical and thermal stress on devices during fault conditions.

## III. Selection of Semiconductors

Semiconductor switches are turned ON for an order of a few milliseconds, during which the fault current can rise to several kA. The CL level and current interruption level for the proposed topology are targeted at 4.5 kA; consequently, careful selection of semiconductors is performed and summarized in the following sections.

### A. Selection of Semiconductor Devices

Several semiconductor technologies can be exploited in HCB applications, including majority charge carrier devices such as MOSFET, junction field-effect transistor (JFET), and minority charge carrier devices like thyristors, IGBT, and IGCT. The latter devices guarantee better surge current capability (lower conductor voltage drop at high current level) due to the conductivity modulation, while the majority charge carrier device demonstrates resistive conduction characteristics and can be paralleled to reduce the conduction resistances. These devices are available in different packaging technologies, discrete and power modules with multiple chips.

Table III summarizes four tabulated semiconductor technologies, accounting for key parameters to draw a significant conclusion among them for the HCB application. SCRs are highly reliable with very high thermal capacitance and low conduction losses, but incur the highest switching losses among the considered semiconductor technologies. Besides, they possess a slow current turn-OFF speed, require controlled commutation, and suffer from poor controllability, high gate driver complexity, and being difficult to parallel. Alternatively, SiC MOSFET exhibits superior conduction performance and lower switching losses when compared to Si counterpart devices, but at a higher cost. For the proposed topology, conduction loss and switching loss play a minimal role as the semiconductor switches are ON only after a fault occurrence for a very short duration (a few milliseconds). Therefore, accounting for high cost, low reliability, and low thermal capacitance, SiC devices are not a good fit for HCB applications. The reverse blocking IGCT (RB-IGCT) could be a suitable candidate for high current circuit breakers due to their bidirectional voltage blocking capability [20], but they require complex current-driven gate drivers. In addition, the turn-OFF capability of IGCT is lower due to stray inductance in the gate commutation loop. Although robust and reliable, due to their limited switching speed, they are less suitable for fast fault interruption and offer poor paralleling capability. The rating and package availability of RB-IGCT are also limited in the market compared to IGBTs. In contrast, IGBTs offer fast turn-OFF speed, simple gate driver design, good current conduction capability, and low cost compared to other semiconductor power devices. Although IGBT has a higher conduction voltage drop but for this topology, switches are turned ON for a few milliseconds; hence, the conduction power losses would be minimal. IGBTs are highly reliable, cost-effective, and practical solutions for medium- to high-power HCB applications. Furthermore, IGBTs are easy to acquire commercially in wide current ratings, at a lower cost compared to other devices.

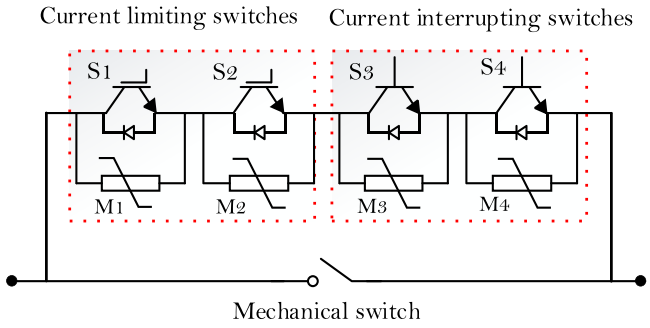


Fig. 6. 1.2 kV IGBT-based HCB topology.

### B. Device Blocking Voltage Selection

After finalizing the selection of semiconductor technology, the right blocking voltage rating for the IGBT devices needs to be determined. The target dc-link voltage of the HCB is 1.5 kV as listed previously in Table I. Considering device reliability over its desired lifetime, the nominal voltage rating of the IGBT assembly must be approximately 2 kV. During the current interruption, a transient overvoltage is applied across the semiconductor switches due to the voltage clamping components, MOVs. Depending on the selection of MOV, typically, the ratio between the transient overvoltage and the rated operation voltage (2 kV) is ∼2, which implies that the IGBTs need to withstand a transient voltage around $2 \times 2\,\text{kV} = 4\,\text{kV}$. The proposed topology comprises a series connection of a CL switch and a current interruption switch to share the transient overvoltage; hence, both the switches must withstand ∼2 kV each. Based on the package availability of IGBT voltage ratings, 1.2 kV and 3.3 kV devices are considered for the evaluation.

*1) 1.2 kV IGBT-Based Design:* The objective is to achieve the 2 kV rated voltage for the CL and the current interruption for each stage. Accordingly, two 1.2 kV IGBTs connected in series for the CL stage, and two 1.2 kV IGBTs connected in series for the current interruption stage, as shown in Fig. 6, should suffice for the target withstand voltage.

*2) 3.3 kV IGBT-Based Design:* Using 3.3 kV devices, the proposed topology is realized by connecting one CL switch and one current interruption switch for each stage, as shown in Fig. 1. The key advantage of using 3.3 kV IGBT-based design is lower voltage drop during current commutation, and employment of

fewer semiconductor devices. Fewer devices require fewer gate drivers and auxiliary circuits, resulting in a smaller form factor. On the other hand, this design has a few drawbacks, such as voltage overdesign and cost compared to a 1.2 kV-based design.

For instance, if the dc-link voltage is to be scaled to 8 kV, considering a typical ratio of ∼2 between transient overvoltage and rated operation, current interruption and limiting stages must withstand a total voltage of 16 kV. The 1.2 kV-based design would need seven series-connected switches for each stage, with a total of 8.4 kV of voltage withstand capacity per stage. On the other hand, with a 3.3 kV-based design, three such devices are required per stage, which totals a withstanding capacity of 9.9 kV per stage. The latter approach will needlessly exceed the target requirement of 8 kV by 23%. This brief analysis certainly supports the idea that employing 1.2 kV IGBT devices has more flexibility to adapt to dc bus voltages by connecting a greater number of switches in series. Moreover, 1.2 kV IGBTs are easy to acquire commercially in different current ratings, at a lower cost compared to other packages. Although a 1.2 kV IGBT-based design needs more isolated power supplies and gate drivers contributing to a larger form factor compared to 3.3 kV, for this application, form factor is not a prime concern. After comparing both the designs, the 1.2 kV IGBT is chosen to develop the prototype due to high surge current capability, economy, and several commercially available device options. Besides, the 1.2 kV IGBT device is closer to the target blocking voltage and is manufactured by a wide range of vendors.

### C. Selection of 1.2 kV IGBT Modules

To select a suitable module, three major manufacturers and their various package types are tested. The surge current conduction capability and current turn-OFF capability tests on each of the devices are carried out, and the resulting I-V characteristics are plotted. The current conduction test is performed by increasing the current gradually for 1 ms from 0 to the target peak turn-OFF current ($I_c$). The losses during a transient current increase prominently as the device enters desaturation. This test helps to determine the desaturation region of each device. The current turn-OFF test is conducted by ramping the current from 0 to the target turn-OFF current ($I_c$) throughout 1 ms and interrupting this current with the device under test. During this interruption, the peak collector-emitter voltage ($V_{CE(peak)}$) is measured across the device and recorded. If the device successfully reaches the $V_{CE(peak)}$ of 1200 V with the target turn-OFF current of approximately 4.5 kA, then the test is said to be complete. More details on the test are provided in section IV. Usually, the arbitrary surge current pulse capability is limited by current saturation characteristics [21]. The current in the IGBT is the sum of pnp transistor collector current and the channel current. Hence, the saturation current ($I_{CE(sat)}$) can be written as [22]

$$I_{CE(sat)} = \frac{1}{1-\alpha_{pnp}} * \frac{W * \mu_n * C_{ox}}{L} * (V_{GE} - V_{th})^2 \quad (1)$$

where $\alpha_{pnp}$ is the bipolar current gain, $V_{GE}$ is the gate voltage, and $V_{th}$ is the threshold voltage of the IGBT, $W$ is the width of the channel, $\mu_n$ is the mobility of electrons, $C_{ox}$ is oxide capacitance, and L is the length of the channel. Equation (1) shows that enhancing the gate voltage $V_{GE}$ can boost the current-carrying capability of the IGBT, concurrently offering lower conduction voltage $V_{CE(sat)}$ during conduction. The IGBT's conduction voltage drop, $V_{CE(sat)}$ is essential in determining the IGBT's conduction losses and the current commutation time between the mechanical switch and the semiconductor switch for HCB. However, a potentially higher gate voltage could damage the gate oxide layer of the device if operated for a long time. Investigation in [23] employed a higher gate voltage for a short duration and verified no adverse effects under high temperature. Therefore, the gate drive voltage is increased to 18 V from the conventional 15 V to perform the current conduction and current turn-OFF test. By extracting voltage and current data of the IGBT, the I-V curve is obtained, as shown in Fig. 7. The IGBT manufacturer's datasheet provides the conduction characteristics (I-V curves); however, it is usually tested up to 2x the rated current, which is not enough in this investigation. The limit of the IGBT's current conduction in a short period (∼ milliseconds), of the order 4x–6x of the rated current, has been explored, and no failures were observed for any of the devices. It is evident that initially the current increased linearly, but then most of the IGBT saturate at ∼6x of the rated current.

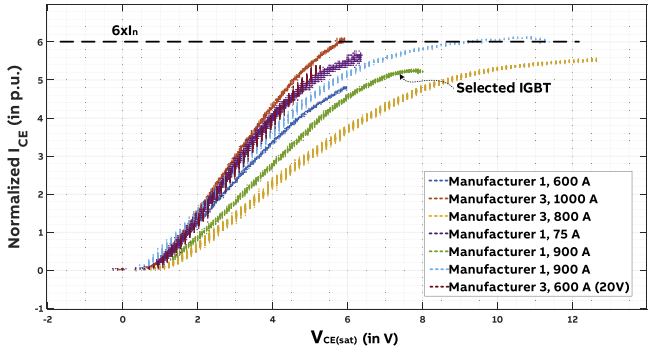


Fig. 7. IGBT I-V curve with $V_{GE} = 18$ V at room temperature.

This study evaluates IGBT modules of current ratings ranging from 600 A to 1000 A, each of which is tested to determine if it can reach 4.5 kA of peak turn-OFF current. Table IV summarizes the results of the current turn-OFF tests performed on the different IGBT modules, and a comparison is made based on target peak turn-OFF current (4.5 kA), nominal current conduction, and the peak turn-OFF voltage (1200 V) of the device. The IGBTs can successfully turn OFF between five to six times the nominal current rating of the device being tested. Furthermore, devices are scrutinized based on peak turn-OFF voltage $V_{CE(peak)}$, being close to 1200 V, and based on lower conduction voltage drop $V_{CE(sat)}$. Some of the modules are referred to as "Econodual," which is a trademark of Infineon. However, due to the widespread adoption of this form factor, we use "Econodual" as a general label to describe that package style.

Discrete IGBTs from Manufacturer 1, 75 A and Manufacturer 2, 120 A are also included for an evaluation. However, multiple switches must be connected in parallel to reach the desired current interruption level [24]. The paralleling of devices not

TABLE IV
SUMMARY OF TESTS FOR THE MODULE EVALUATION

| IGBT Manufacturer | Type of package | Peak turn-off current IC (A) | Nominal current (A) | Multiple of nominal current | Peak turn off voltage VCE(peak) (V) |
|---|---|---|---|---|---|
| Manufacturer 1 | TO247 | 434 A | 75 A | 5.79x | 1116 V |
| | 62 mm, Half bridge | 3640 A | 600 A | 6.06x | 1152 V |
| | 62 mm, Single IGBT | 4428 A | 900 A | 4.92x | 1176 V |
| | **Econodual** | **4536 A** | **900 A** | **5.04x** | **1240 V** |
| Manufacturer 2 | TO264 | 675 A | 120 A | 5.63x | 1122 V |
| Manufacturer 3 | Econodual | 2980 A | 600 A | 4.97x | 1168 V |
| | Econodual | 4464 A | 800 A | 5.58x | 1128 V |
| | Econodual | 6000 A | 1000 A | 6x | 1110 V |

only increases the circuit complexity, but also requires careful design to share the transient current among them in addition to contributing to a larger form factor. Upon testing, the device from Manufacturer 2, 120 A, demonstrated large voltage oscillations on the gate voltage during the turn-OFF process. The peak voltage measured across the gate exceeded the maximum gate voltage of 24 V. This led to a miller turn-ON of the IGBT, which subsequently destroyed the device. Therefore, they are disregarded for further analysis. Manufacturer 3, 600 A showed promising results during the surge current conduction tests as it was able to conduct up to 4.5 kA for about 1 ms. This device was then tested for interrupting fault currents; however, the performance of this device did not reach the same fault current levels as reached in the current conduction tests. The device did not perform as expected, and several changes were needed to the gate driver circuit, such as increasing the gate voltage to 20 V from 18 V to reduce the conduction voltage drop, increasing turn-OFF voltage to 0 V from −4 V to reduce the turn-OFF di/dt, and increasing the gate resistance to 80 Ω compared to other devices. However, after all modifications, it is observed that the device is able to reach only 2980 A with the peak voltage $V_{CE(peak)}$ of 1168 V, which clearly states that this device is unable to turn OFF the target peak fault current of 4.5 kA. Tests at higher current led to the destruction of the device. A module from manufacturer 3800 A was tested; it entered in desaturation region at 4400 A at a $V_{CE(sat)}$ of 13 V, as seen in Fig. 6. The objective is to keep the voltage that develops across the four IGBTs minimal, so that the voltage required across the MS is reduced. Thus, this device is not the best among available devices.

On validating the performance of the Manufacturer 3, 1000 A module, results are found to be impressive; however, the rating of that device is significantly higher than the target fault current interruption capability. Additionally, the 1000 A IGBT module is a custom package that has a larger form factor as compared to the popular Econodual package. Manufacturer 1, 900 A, 62 mm single IGBT module could have proved to be a suitable candidate, but four modules are required as compared to a half-bridge module, leading to increased form factor compared to others.

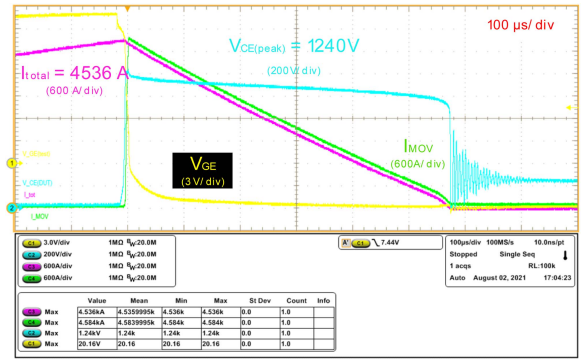


Fig. 8. Current turn-OFF capability test for Manufacturer 1, 900 A, at c, −5 V, $R_G = 50\ \Omega$.

Furthermore, the peak turn-OFF current is slightly less when compared to Econodual and the desired current target.

The final candidate from manufacturer 1, 900 A, was tested, and it showed promising results during the conduction test, as it can conduct 4.5 kA for 1 ms, and the voltage drop remained almost linear over the entire current range, i.e., it does not enter desaturation. The IGBT turn-OFF current is 4536 A, and the peak voltage measured across the IGBT, $V_{CE(peak)}$, is 1240 V, which is slightly above the nominal rating of the device. However, the overvoltage across the IGBT lasts only for a few microseconds, unlike the continuous operating voltage. No failures of the IGBTs were observed during the short circuit testing due to this transient overvoltage. Therefore, the module from manufacturer 1, 900 A (highlighted in bold in Table III) is considered the best choice to be employed as a semiconductor branch for the proposed topology. This module requires 8 V of $V_{CE(sat)}$ to reach 4.5 kA compared to other devices, which benefit from the voltage developed across four IGBTs. Eventually, developing less voltage across the MS can help commutate current from MS to semiconductor devices faster. The peak turn-OFF current of the device is at least 4500 A and is within the margin. Additionally, the form factor of the module is suitable for a compact design with the MOV seated on top of it, reducing overall stray inductance between the MOV and the IGBT. As discussed before, all the selected devices of Table III were tested for current conduction and current turn-OFF, but only the test results of the chosen IGBT are shown in Fig. 8. The details of the test setup are discussed in the subsequent section. $I_{total}$ is the total current carried by a device and MOV. $V_{CE(peak)}$ is the peak voltage across the collector and emitter of the switch when the device is turned off. $V_{GE}$ is the gate voltage applied to turn ON and OFF the switch. $I_{MOV}$ is the current flowing through the MOV. The peak turn-OFF voltage of the MOV at a target fault current of 4.5 kA is found to be nearly 1240 V, meeting target requirements. A commercially available gate driver was modified to conduct this test before the custom-made gate driver was designed.

### D. Selection of MOV

The MOV is selected to absorb a certain amount of energy in joules for each turn-OFF event of the semiconductor device,

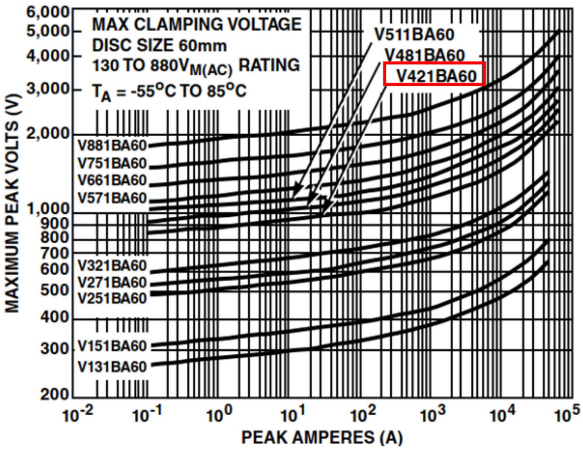


Fig. 9. Maximum clamping voltage of BA series, source: [25].

and the MOV that is used for the CL mode must expend this energy "budget" by splitting it between the CL mode as well as the current interruption mode. Therefore, the primary limiting factor in increasing the CL mode time is the thermal rating of the MOV. The MOV must be chosen carefully such that it does not conduct during normal operation and limits overvoltage during fault interruption. For the prototype development target dc voltage is 1.5 kV, and each MOV needs to withstand 375 V continuously. V421BA60 from Littelfuse [25] is chosen (highlighted in red in Fig. 9), since the continuous operation dc voltage of this MOV is 560 V, higher than the required, and the clamping voltage is 1255 V at 4.5 kA. It is observed from the datasheet that this MOV is the most suitable candidate for the target application among others in the datasheet. Additionally, through sheer coincidence, the BA series perfectly meets the mechanical assembly requirements for the proposed topology.

By applying KVL to the system inductance voltage drop, applied dc bus voltage, and voltage across MOVs, equation can be written as

$$V_{dc} \ - \ 2V_{\text{MOV}} = L_{sys} \ \frac{dt_{ic(\text{peak})}}{dt_{int}} \tag{2}$$

where $V_{\text{dc}}$ is applied dc bus voltage, $V_{\text{MOV}}$ is instantaneous MOV voltage, $L_{\text{sys}}$ is total system inductance seen by the fault current, $i_{c(\text{peak})}$ is the peak fault current, tint is an interruption time. Both MOVs are identical, hence, voltage across MOVs is considered as 2 $V_{\text{MOV}}$. From the available measurement data, the MOV clamping voltage (see Fig. 8) approximated using a linear curve fitting and relationship can be established as, $V_{\text{MOV}}(t) = -kt+V_m$, where $V_m$ is maximum MOV voltage obtained from the fitted curve, k is slope of the fitted line, t is time in seconds. Substituting $V_{\text{MOV}}$ into (2) and integrating w.r.t. time and current, quadratic expression of the interruption time can be written as

$$kt_{int}^2 + (V_{\text{dc}} \ - \ 2V_M)t_{int} + L_{sys} * \ i_{c(\text{peak})} \ = \ 0.$$

Finding roots of the quadratic expression and solving with the help of L'Hôpital's rule, the current interruption mode time can

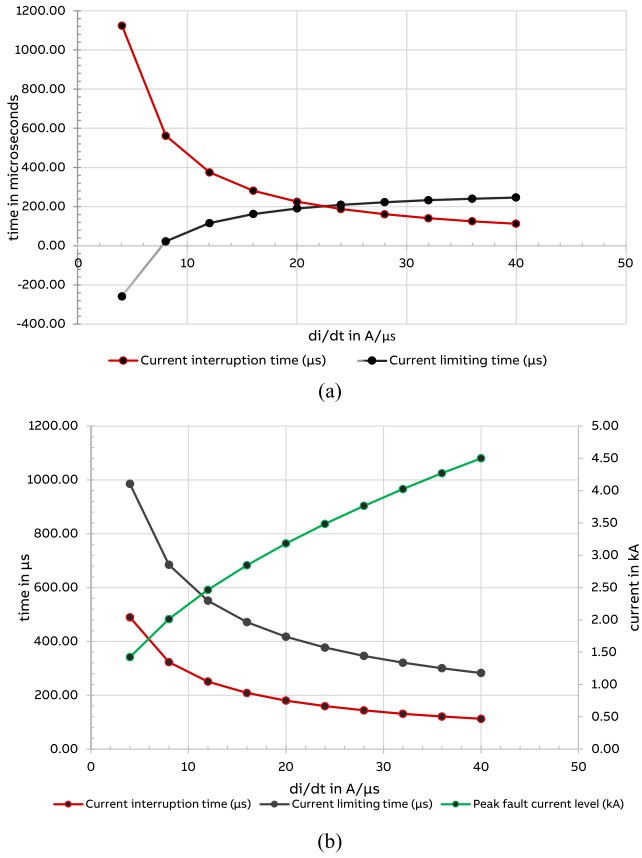


Fig. 10. (a) CL mode time and Current interruption mode time calculation. (b) CL mode time and Current interruption mode time calculation for variable fault current.

be calculated as

$$t_{int} \approx \frac{I_{C\ (\text{peak})} L_{sys}}{2V_{\text{MOV}} - V_{\text{dc}}} \tag{3}$$

where, $I_{C(\text{peak})}$ is the peak of the fault current at the beginning of $t_{lim}$, $L_{sys}$ is the system inductance, $V_{\text{MOV}}$ is the average voltage across the MOV during the current interruption mode, and $V_{\text{dc}}$ is the voltage rating of the dc grid. Equation (3) shows that the system inductance determines the current interruption time if the HCB needs to trip at a specified peak fault current level, in this case, 4.5 kA. The CL mode time is then calculated as

$$t_{lim} = \frac{E_{\text{MOV}} - P_{\text{MOV}(int)} t_{int}}{P_{\text{MOV}(lim)}} \tag{4}$$

where $E_{\text{MOV}}$ is the energy "budget" or the maximum energy dissipation capacity of each MOV, $P_{\text{MOV(int)}}$ and $P_{\text{MOV(lim)}}$ are the average power dissipated in the MOV during the current interruption mode and the CL mode, respectively. The relationships between the CL mode time and the current interruption mode time are plotted as a function of di/dt in Fig. 10(a) for a constant value of peak fault current $I_c = 4.5$ kA. It can be said from Fig. 10(a) that for low values of di/dt (i.e., high system inductance), the CL time may become negative for a di/dt less than 8 A/$\mu$s, indicating that MOVs do not have enough energy "budget" to dissipate energy stored in the fault inductance, $L_{f,}$

during a dc fault interruption event. The energy stored in the fault inductance is given by

$$E_{Lf} = \frac{1}{2} * L_f I_c^2. \tag{5}$$

Assuming that the source capacitance is large enough, it can be considered that the dc source voltage, $V_{dc}$ does not decrease during the fault. Then, the fault inductance is given by

$$L_f = \frac{V_{dc}}{\frac{dI_c}{dt}}. \tag{6}$$

Substituting the value of (6) into (5), we get

$$E_{Lf} = \frac{1}{2} * (V_{dc}/(dI_c/dt)) * I_c^2. \tag{7}$$

It can be seen from (7) that, if all quantities are constant, then the energy stored in the inductor $E_{Lf}$ is inversely proportional to $dI_c/dt$. In our analysis, the highest $dI_c/dt$ is at the lowest inductor energy of 40 A/$\mu$s, so to solve the MOV energy dissipation issue, $E_{Lf}$ can be kept constant over the entire range of $dI_c/dt$, while changing $I_c$ with $dI_c/dt$. Let $E_{Lf\_40}$ be the energy in the inductor at 40 A/$\mu$s and let the peak current, $I_c$ at 40 A/$\mu$s be the 4500 A, then

$$E_{Lf_{40}} = (V_{dc}/2) * 4500^{\,2}/40. \tag{8}$$

As mentioned earlier, energy is kept constant; therefore, evaluating inductor energy $E_{Lf}$ at any arbitrary $dI_c/dt$ as

$$E_{Lf} = E_{Lf_{40}} \tag{9}$$

$$\frac{1}{2} * (V_{dc}/(dI_c/dt)) * I_c^2 = (V_{dc}/2) * 4500^{\,2}/40.$$

Simplifying the abovementioned equation, we obtain

$$I_C = 4500\sqrt{\frac{dI_C/dt}{40}}\text{A}. \tag{10}$$

It can be concluded that the energy stored in the system inductance keeps increasing at lower di/dt levels. Correspondingly, the current interruption mode time reduces as we compare both the red curves of Fig. 10(a) and (b). The reduction in this time interval increases the energy dissipation capacity available in the MOV for the CL mode, which is inferred by comparing the black curves of Fig. 10(a) and (b).

The CL time in this situation is not only positive, as seen in Fig. 10(b), but it steadily increases to up to a millisecond as the low di/dt limit of 4 A/$\mu$s is approached. This adjustment shows the viability of the selected MOV in this design.

Fig. 11 shows the repetitive surge capability of the V421BA60 MOV, where the impulse current magnitude and the number of MOV operations at that current magnitude are plotted against the impulse duration. In the proposed configuration, the MOV can perform between two to ten CL and interruption operations for a total of 260 $\mu$s, including CL and interruption at peak impulse current of 2256 A. Adding another MOV in parallel to the existing MOV would improve the reliability and lifetime by an order of magnitude, as shown by the pink point in Fig. 11.

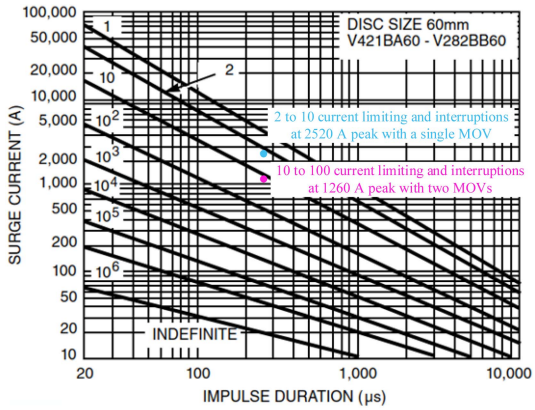


Fig. 11. Repetitive Surge Capability of BA Series, source: [25].

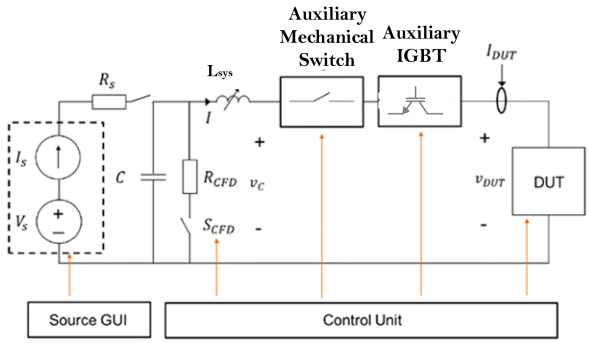


Fig. 12. Schematic of the test setup for the IGBT conduction voltage drop test and current interruption capability test.

## IV. Experimental Validation

### A. Test Setup and Procedure

A test setup schematic is shown in Fig. 12 to perform the current conduction test and the current turn-OFF test. The auxiliary IGBT and auxiliary mechanical switch (AMS) are solely used to initiate the test and turn OFF the test but are not part of the device under test (DUT) (IGBT module to be evaluated). Inductor *L* is adjusted to achieve the desired di/dt for the fault current, and the capacitor *C* is charged to a predetermined voltage to achieve the desired peak fault current. To perform the test, the short circuit is initiated in the test setup by turning on the prototype for 1 ms, and the fault is cleared by turning OFF either the prototype first or the protection IGBT first, depending on the test being conducted. The IGBTs were turned ON with gate drive voltage $V_{GE}$ of 18 V with an external fiber optic signal for the duration of the test. An AMS and DUT are kept in on state during the current conduction test, and the auxiliary IGBT is turned ON and then OFF after $\sim$1 ms to create the high current pulse through DUT. Only an auxiliary IGBT is used to turn OFF once the test is complete. In the current turn-OFF test, the DUT is coordinated to turn ON 65.5 ms after the command to turn ON the AMS, accounting for the delay in closing the AMS. The ON-state pulse width is set to 1 ms for the turn-OFF capability tests, and the IGBT under test (DUT) itself is used to turn OFF the test current.

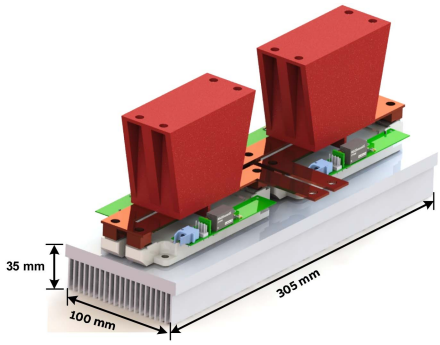


Fig. 13. Mechanical design of 4.5 kA prototype assembly.

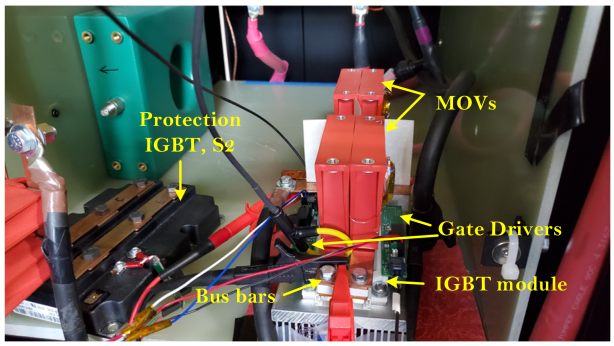


Fig. 14. Test setup for the proposed prototype inside the short-circuit test setup.

### B. Prototype Assembly

To minimize the peak overvoltage at current interruptions due to stray inductance between IGBTs and MOVs, the MOVs are mounted in an upside-down position above the IGBT module. This helps to reduce the switching loop and, hence, reduces stray inductance. Short busbars are used to connect MOV power terminals with IGBT emitter/collector terminals. There are two IGBTs packed in the same Econodual 3 packaging so that two MOVs are mounted in the single IGBT module assembly. Noteworthy to mention that the prototyped mechanical designs are adapted based on low-cost machining, easy assembly, while maintaining minimum stray inductance.

The complete prototype is assembled, as illustrated in Fig. 13, both IGBTs are bolted on top of an aluminum heatsink to provide mechanical support to the module. Fig. 14 shows the test setup of the proposed HCB topology, set up in series with the protection IGBT inside the short circuit test setup, as outlined in Fig. 12. As discussed in the above section, the upper space above the IGBT module is occupied by MOVs; therefore, gate drivers are uniquely designed to fit at the edge of the module. The gate drive is designed to provide gate voltage, $V_{GE}$ of +18 V and -2.5 V. The gate drive circuit is powered with a 24 V dc power supply. In switching applications, it is advantageous to implement a slower turn-OFF of power switches to effectively control the voltage across the MOV. A slower turn-OFF can be achieved by reducing the di/dt during the switching event. To this end, the gate resistance is optimized to 50 Ω, which limits the transient overshoot voltage $V_{CE(peak)}$ and ensures it remains within the rated voltage of the switch. The optimized gate resistance slows down the turn-OFF of the IGBT, which reduces the voltage overshoot but increases the turn-OFF switching loss dissipated in the device.

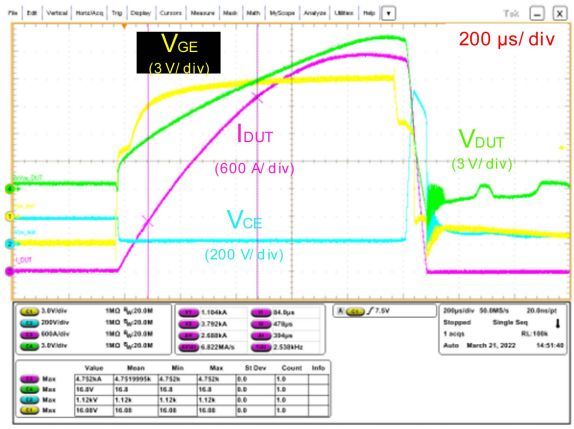


Fig. 15. Current conduction test for two IGBTs in series, $I_{Cpeak} = 4752$ A, $V_{GE} = 18$ V.

## V. Results and Discussion

### A. Current Conduction Mode Test

All four IGBTs in the proposed prototype are assessed individually for conducting 4.5 kA with the designed gate driver board. All the IGBTs in the prototype conducted 4.5 kA successfully. Two IGBTs are then evaluated to conduct current in series to measure the voltage drop across them, and the results of the tests can be seen in Fig. 15. The conduction voltage drops $V_{DUT}$ across the two IGBTs are measured to be 13.7 V at $I_{DUT} =$ 4.5 kA. $V_{CE}$ is the voltage measured across switch S2 of the schematic (outlined in Fig. 12).

### B. Dual Device Turn-off Test

Current conduction and turn-OFF tests are initially conducted on individual IGBTs to validate the custom-designed gate driver and the experimental setup. Subsequently, turn-OFF testing is performed on two IGBTs connected in series. This has been set as an intermediate step towards eventually derisking the CL mode by applying twice the rated transient voltage (∼2.2 kV) onto the prototype as well as onto the test system. Two sets of tests were performed, one on each pair of IGBTs for the proposed HCB prototype, but test results for one of the tests are presented in Fig. 16. Both pairs of IGBTs successfully turned OFF at the peak fault current, $I_{DUT}$ of 4.5 kA, after a current conduction time of 1 ms. The peak voltage across both IGBTs $V_{CE\_IGBT1}$ and $V_{CE\_IGBT2}$ is almost equal and below the nominal voltage rating of the two devices, i.e., 1200 V. It is seen from the result that once the IGBT turns OFF, the MOV carries the fault current $I_{M2}$.

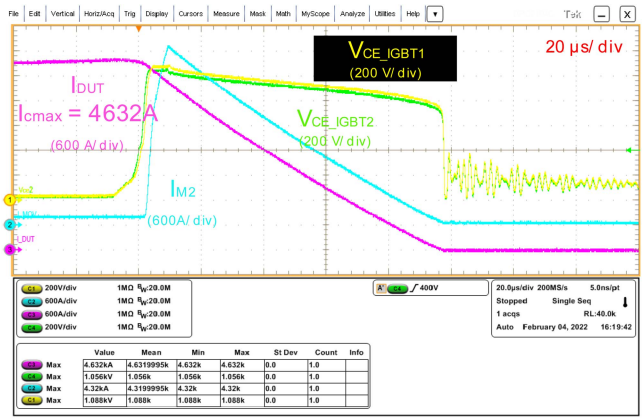


Fig. 16. Two IGBTs in series turned OFF at $I_{Cpeak} = 4632$ A, $V_{GE} = 18$ V.

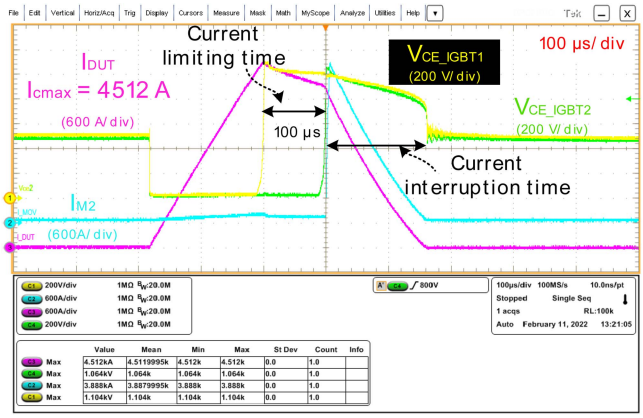


Fig. 17. CL mode test at $I_{Cpeak} = 4512$ A and limiting time $= 100$ $\mu$s.

### C. Current Limiting Mode Test

The previous set of tests de-risked the creepage and clearance of the prototype while turning OFF two IGBTs. The purpose of this test is to demonstrate the CL mode and determine the "CL mode" time interval. The limiting time is determined by the thermal capacity of the MOVs used in the prototype, the inductive energy of the fault to be transferred, the voltage rating of the dc system, and the amplitude of the fault current.

Due to the unavailability of high voltage in the lab, this test is conducted with one IGBT half-bridge module only, i.e., IGBT1 as the CL switch, while IGBT2 of the same module is the current interrupting switch. The fiber optic commands to the two IGBTs are set up in such a way that IGBT1 turns OFF in a controllable interval before IGBT2. The test was performed with the dc bus voltage of 1000 V, which is about half of the target voltage rating for the full prototype. When IGBT1 is turned OFF, the voltage $V_{CE\_IGBT1}$ that develops across MOV1 is slightly more than 1000 V (1104 V), and this imposes a small negative voltage across the system inductance. This causes the di/dt to remain close to zero (slightly negative for this test), resulting in the current being limited close to its peak value. Fig. 17 shows the test result for a CL mode, demonstrating a time interval of 100 $\mu$s and a peak fault current of 4512 A. After 100 $\mu$s, IGBT2 is turned OFF, and this causes M2 to impose an additional negative voltage of 1064 V across the system inductance, and this causes the fault current to rapidly decay to zero. Fig. 17 demonstrates time intervals for the CL mode and the current interruption mode.

## VI. Conclusion

This article investigates a novel concept of CL HCB topology based on semiconductor devices and evaluates the feasibility of the proposed HCB. Several IGBT modules from 3 different manufacturers are assessed for surge current conduction and surge current interruption capabilities up to their ~6 times rated nominal current. Based on their performance, cost, and commercial availability, the best suitable IGBT module is selected for the test device to develop the proposed topology. All the tests on the test device were performed for a peak surge current of 4.5 kA; relevant experimental results are presented, indicating the feasibility of the proposed topology. In summary, we demonstrated an HCB with built-in CL capability, capable of limiting fault current for up to 100 $\mu$s and fully interrupting it within 180 $\mu$s following the CL phase. These results highlight the HCB's ability to respond rapidly and effectively during fault conditions. Furthermore, a protection strategy for radially connected CBs is presented to prevent coordination loss and improve overall system reliability of dc applications. Moreover, successful CL and interruption are achieved for a di/dt range of 4 A/$\mu$s to 40 A/$\mu$s. The proposed topology can be extended to higher voltage levels or by selectively determining the number of MOVs in series during the CL mode. The future work is intended to integrate a mechanical commutation switch with semiconductor devices.

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