A Novel Deadbeat Sliding Mode Predictive Control for T-Type Three-Phase Four-Leg Three-Level Voltage-Source Inverters

Zijian Zhao, Yong Yang, *Senior Member, IEEE*, Rong Chen, Jiefeng Hu, *Senior Member, IEEE*, Hui Yang, *Senior Member, IEEE*, Huiqing Wen, *Senior Member, IEEE*, Yiwang Wang, *Member, IEEE*, and Jose Rodriguez, *Life Fellow, IEEE*

***Abstract*—This article proposes a novel deadbeat sliding mode predictive control (DB-SMPC) strategy for T-type three-phase four-leg three-level voltage source inverters. Developed in the $\alpha\beta\gamma$ frame, the control strategy integrates the advantages of traditional sliding mode control (SMC) and deadbeat predictive control (DBPC), offering enhanced robustness, stability, and superior dynamic and steady-state performance. It outperforms traditional SMC and DBPC in terms of voltage regulation and dynamic response under varying load conditions. This strategy also reduces system chattering, ensures a fixed switching frequency, thereby simplifying the design of *LC*-filters. The four-leg inverter topology effectively addresses unbalanced and nonlinear loads. When integrated with the proposed DB-SMPC strategy, it enables robust system performance under such conditions. In addition, it significantly reduces total harmonic distortion for nonlinear loads and improves the dynamic and steady-state performance of balancing neutral-point voltage under unbalanced load conditions. Experimental results verify the effectiveness of the proposed strategy.**

Received 16 April 2025; revised 17 August 2025, 10 November 2025, and 17 December 2025; accepted 25 December 2025. Date of publication 31 December 2025; date of current version 20 March 2026. This work was supported in part by the National Natural Science Foundation of China under Grant 52377195, in part by the Transformation of Scientific and Technological Achievements in Suzhou (Carbon Peak Carbon Neutral Project) under Grant ST202303, in part by Suzhou Key Laboratory of Smart Energy Technology, in part by Science and Technology Planning Project of Suzhou City under Grant SZS2022015, in part by Natural Science Foundation of the Jiangsu Higher Education Institutions of China under Grant 25KJA470007, in part by "Qing-Lan Project"of Colleges and Universities in Jiangsu Province, and in part by the ANID through Project CIA250006. Recommended for publication by Associate Editor A. Safaee. *(Corresponding authors: Yong Yang; Rong chen.)*

Zijian Zhao, Yong Yang, and Rong Chen are with the School of Rail Transportation, Soochow University, Suzhou 215131, China, and also with the Intelligent Urban Rail Engineering Research Center of Jiangsu Province, Suzhou 215131, China (e-mail: 20234246014@stu.suda.edu.cn; yangy1981@suda.edu.cn; chrong@suda.edu.cn).

Jiefeng Hu is with the Centre for New Energy Transition Research, Australia, and also with the Institute of Innovation, Science and Sustainability, Federation University Australia, Mount Helen, VIC 3353, Australia (e-mail: j.hu@federation.edu.au).

Hui Yang is with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing 210096, China (e-mail: yang.hui@nuaa.edu.cn).

Huiqing Wen is with Xi'an Jiaotong-Liverpool University, Suzhou 215123, China (e-mail: huiqing.wen@xjtlu.edu.cn).

Yiwang Wang is with Suzhou Polytechnic University, Suzhou 211106, China (e-mail: wyw@jssvc.edu.cn).

Jose Rodriguez is with the Faculty of Engineering, Universidad San Sebastian Santiago, Santiago 8370146, Chile (e-mail: jose.rodriguezp@uss.cl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3649546.

Digital Object Identifier 10.1109/TPEL.2025.3649546

***Index Terms*—Balancing neutral-point voltage, deadbeat sliding mode predictive control (DB-SMPC), fixed switching frequency, three-phase four-leg three-level voltage source inverters (3P-4L-3L-VSIs).**

I. Introduction

THE renewable energy industry is growing under the framework of sustainable development policies. Inverters, as a crucial component of this industry, play a key role in ensuring system reliability and power quality. They must remain stable and respond rapidly under varying operating conditions. As a result, their topologies and control strategies have emerged as key research focuses in the field of power electronics [1], [2], [3].

Voltage source inverters (VSIs) are essential components in modern power systems, facilitating efficient energy conversion and management. In recent years, three-phase three-leg inverters [4] and three-phase four-wire inverters [5] have been widely adopted to ensure reliable operation under varying conditions. However, to mitigate issues such as zero-sequence currents, three-phase four-leg inverters provide a more effective solution [6], [7], [8]. In particular, T-type 3P-4L-3L-VSIs allow precise control of the neutral point voltage through the fourth leg [9], [10], [11], enabling them to handle unbalanced and nonlinear loads while ensuring stable output voltage.

Inverter control strategies are also fundamental for managing the operation of VSIs, ensuring efficient energy conversion and maintaining system stability. Traditional linear control strategies, such as proportional-integral (PI) control [12], proportional-resonant (PR) control [13], repetitive control [14], [15] and deadbeat control [16] are widely used due to their simplicity and effectiveness. However, traditional linear control strategies may struggle with system nonlinearities, external disturbances and parameter variations, leading to performance degradation.

In recent years, several nonlinear control strategies have been developed, each with unique advantages in addressing specific challenges. Model predictive control (MPC) [17], [18], [19] has emerged as a powerful control strategy for three-phase inverters, offering notable benefits over traditional methods. Yang et al. [20] and Zhu et al. [21] proposed a novel continuous

control set model predictive control (CCS-MPC) strategy that utilizes a dynamic system model to predict system behavior and optimize control actions. Xue et al. [22], [23] proposed a finite control set model predictive control strategy, designing a cost function to regulate system trajectories and ensure a simple controller structure with fewer tuning parameters. Kakosimos and Abu-Rub [24] and Bekhoucha et al. [25] proposed a deadbeat predictive control (DBPC), a subset of MPC, which directly computes the optimal voltage vector to eliminate the current error at the next sampling instant, achieving fast dynamic response with reduced complexity. Compared with traditional MPC, DBPC simplifies computation by using a one-step prediction model to directly calculate the control input that drives the system to its reference in the next sampling instant. This approach enables faster response, lower computational cost, and easier real-time implementation. However, DBPC is sensitive to model inaccuracies and parameter variations, and its variable switching frequency may lead to higher switching losses and limited flexibility, which can reduce robustness under complex operating conditions.

Sliding mode control (SMC) [26], [27] has also gained attention in power electronics due to its robustness, simple structure, and adaptability. Jung and Tzou [28] proposed a discrete SMC with feedforward compensation (DFSMC), enhancing tracking accuracy and reducing total harmonic distortion (THD). For four-leg inverters, Nalla et al. [29] proposed a novel sliding mode variable that embeds NP voltage for decoupled control, achieving stability under voltage sags and swells. To mitigate chattering, Pichan and Rastegar [30] introduced a fixed-switching-frequency SMC, ensuring stability at 15 kHz and low THD.

Recently, some researchers have integrated SMC with DBPC to enhance control performance. Zhang et al. [31] introduced a sliding-mode-based deadbeat predictive current control (DPCC) using a variable-speed reaching law for both speed and current control. Without relying on observers, the method improves robustness to parameter variations and maintains strong performance under mismatched conditions. For permanent magnet synchronous motor drives, Xu et al. [32] introduced an integral SMC-based DPCC, incorporating disturbance rejection terms to address parameter mismatches and time delays. Wang et al. [33] proposed an extended sliding-mode predictive control, optimizing output performance while significantly enhancing robustness and computational efficiency.

These studies highlight how hybrid SMC-DBPC strategies combine SMC's robustness with MPC's trajectory optimization capabilities, addressing challenges such as parameter sensitivity, disturbance rejection, and multiobjective tradeoffs. However, these strategies cannot be directly applied to three-phase four-leg inverters due to the additional neutral-leg current path and complex coupling between phase voltages, which make conventional control laws ineffective for maintaining neutral-point balance and system stability. Further research is therefore needed to address these challenges in multileg topologies. Therefore, this article focuses on T-type 3P-4L-3L-VSIs and adopts the DB-SMPC strategy. In this DB-SMPC strategy, to construct a predictive sliding surface in the $\alpha\beta\gamma$ reference frame, the predicted value at time step $k+2$ is obtained through discretization and parameter adaptation is performed via real-time sampling. Afterward, by incorporating a saturation function, the output voltage equations are derived. To handle nonlinear and unbalanced loads, an offset voltage calculation is performed. Finally, the phase opposition disposition pulsewidth modulation (POD-PWM) modulator enables stable operation of the inverters [34]. The performance of the DB-SMPC strategy is compared with traditional PI, SMC, and MPC strategies in terms of THD, recovery time, and control accuracy. The inverter operates stably under unbalanced and nonlinear loads, producing output voltage waveforms of a certain quality.

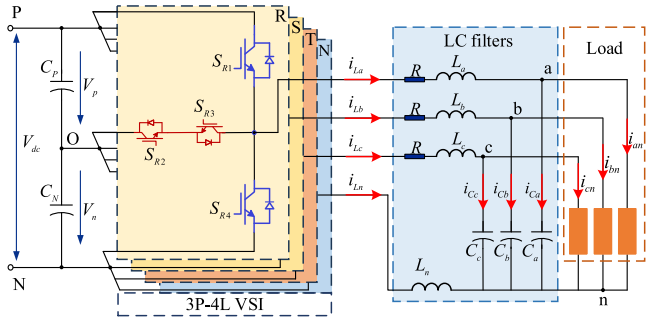

Fig. 1. Topology of the T-type 3P-4L-3L-VSI.

TABLE I
COMBINATIONS OF DIFFERENT SWITCHING STATES

S_{X1}	S_{X2}	S_{X3}	S_{X4}	V_{XO}
1	1	0	0	$V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

The rest of this article is organized as follows: Section II presents the topology and mathematical model of 3P-4L-3L-VSIs. In Section III, the principle of the proposed DB–SMPC is detailed. After that, comparative experimental results are presented in Section IV. Finally, Section V concludes this article.

II. Topology and System Modeling

The T-type 3P-4L-3L-VSI is a commonly used power electronic converter. Its topology is shown in Fig. 1. The typical characteristic of the inverter is the addition of a neutral leg N and a smoothing inductor L_n which provides a path for zero-sequence current while meeting the requirements of electrical equipment for the neutral line [6].

In Fig. 1, C_P and C_N are dc-link capacitors, $V_{\rm dc}$ is the dc bus voltage, V_p and V_n are the voltages of the upper dc-link capacitor and the lower dc-link capacitor. $i_{La}, i_{Lb}, i_{Lc}, i_{Ln}$ are output currents, i_{Ca}, i_{Cb}, i_{Cc} are capacitor currents, i_{an}, i_{bn}, i_{cn} are load currents, L_a, L_b, L_c and C_a, C_b, C_c are filter inductors and capacitors, L_n is the smoothing inductor. S_R, S_S, S_T, S_N represent 16 power switches, on the output side of the inverter, three-phase voltages can be generated by adjusting the power switches.

Table I presents the switching states, where "1" indicates ON switch and "0" denotes OFF.

We concern $L = L_a = L_b = L_c$ and $C = C_a = C_b = C_c$. V_{an}, V_{bn}, V_{cn} represent load voltages (equal to filter capacitor voltages). The relationship between the output voltages V_{RN}, V_{SN}, V_{TN} and currents $i_{La}, i_{Lb}, i_{Lc}, i_{Ln}$ can be obtained from Fig. 1, which are expressed as

$$\begin{bmatrix} V_{RN} \\ V_{SN} \\ V_{TN} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + R\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} - L_n\frac{d}{dt}\begin{bmatrix} i_{Ln} \\ i_{Ln} \\ i_{Ln} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} = C\frac{d}{dt}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}. \tag{2}$$

By applying Kirchhoff's law, (3) can be derived as

$$\begin{cases} i_{La} + i_{Lb} + i_{Lc} + i_{Ln} = 0 \\ V_{RN} + V_{SN} + V_{TN} = 0 \\ V_{an} + V_{bn} + V_{cn} = 0 \end{cases}. \tag{3}$$

Combining (1) and (3), the system state space equation can be expressed as

$$\begin{bmatrix} V_{RN} \\ V_{SN} \\ V_{TN} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} - R\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \begin{bmatrix} L+L_n & L_n & L_n \\ L_n & L+L_n & L_n \\ L_n & L_n & L+L_n \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}. \tag{4}$$

The Clarke transform simplifies the representation of three-phase signals by converting them from the *ABC* frame to the $\alpha\beta\gamma$ frame. Analyzing and controlling three-phase systems in the $\alpha\beta\gamma$ frame is more efficient than in the traditional *ABC* frame [6]. The transformation matrix is given by

$$T = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{5}$$

Subsequently, (2) and (4) can be converted into the following form using the Clarke transform

$$\frac{d}{dt}\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L\gamma} \end{bmatrix} = \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L+3L_n \end{bmatrix} \begin{bmatrix} V_{\alpha N} - V_{\alpha n} - i_{L\alpha}R \\ V_{\beta N} - V_{\beta n} - i_{L\beta}R \\ V_{\gamma N} - V_{\gamma n} - i_{L\gamma}R \end{bmatrix} \tag{6}$$

$$\frac{d}{dt}\begin{bmatrix} V_{\alpha n} \\ V_{\beta n} \\ V_{\gamma n} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} i_{L\alpha} - i_{\alpha n} \\ i_{L\beta} - i_{\beta n} \\ i_{L\gamma} - i_{\gamma n} \end{bmatrix} \tag{7}$$

where $i_{L\alpha}, i_{L\beta}, i_{L\gamma}$ and $i_{\alpha n}, i_{\beta n}, i_{\gamma n}$ are output currents and load currents in the $\alpha\beta\gamma$ reference frame, $V_{\alpha N}, V_{\beta N}, V_{\gamma N}$ and $V_{\alpha n}, V_{\beta n}, V_{\gamma n}$ are output voltages and load voltages in the $\alpha\beta\gamma$ reference frame.

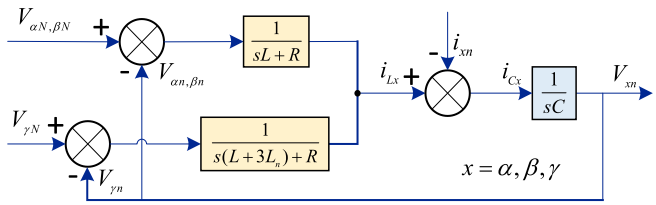

Fig. 2. Block diagram in s-domain.

Based on (6) and (7), the block diagram in s-domain is depicted in Fig. 2.

III. Proposed DB–SMPC Algorithms

Multileg systems face challenges such as complex decoupling, sensitivity to reaching law parameters, and the need for multiobjective optimization. The development of inverter control strategies reflects an ongoing effort to balance stability, simplicity, robustness, and computational efficiency. Traditional PI controllers are easy to implement but may lack robustness against system uncertainties. Traditional PI controllers are typically designed based on an ideal linear model, assuming that the parameters of the inverter remain constant. In practice, however, component parameters, such as resistance, inductance, and capacitance may vary, and factors like load changes, temperature effects, delays, or nonlinearities cause discrepancies between the actual system and the design model. Because the PI controller has a fixed structure and limited bandwidth, it lacks built-in mechanisms to compensate for these uncertainties or to adapt to parameter changes. As a result, its performance may degrade and, in severe cases, the system may oscillate or even become unstable.

DBPC [24] and SMC [30] are well-known nonlinear control strategies featuring significant advantages. Fig. 3 shows the block diagrams of these two strategies. DBPC improves dynamic response by predicting future system states but is computationally demanding. SMC enhances robustness but can suffer from chattering. Integrating SMC and DBPC into SMPC offers a promising approach, leveraging the strengths of both strategies to enhance inverter control performance.

A. Principle of DB-SMPC

In the ABC frame, the reference load voltages $V_{an}^*, V_{bn}^*, V_{cn}^*$ are given by

$$\begin{cases} V_{an}^*(t) = V_m \cos(\omega_{\text{ref}} t) \\ V_{bn}^*(t) = V_m \cos(\omega_{\text{ref}} t - 2\pi/3) \\ V_{cn}^*(t) = V_m \cos(\omega_{\text{ref}} t + 2\pi/3) \end{cases}. \tag{8}$$

Converted to the $\alpha\beta\gamma$ frame, the reference load voltages $V_{\alpha n}^*, V_{\beta n}^*, V_{\gamma n}^*$ are expressed as

$$\begin{cases} V_{\alpha n}^*(t) = V_m \cos(\omega_{\text{ref}} t) \\ V_{\beta n}^*(t) = V_m \sin(\omega_{\text{ref}} t) \\ V_{\gamma n}^*(t) = 0 \end{cases}. \tag{9}$$

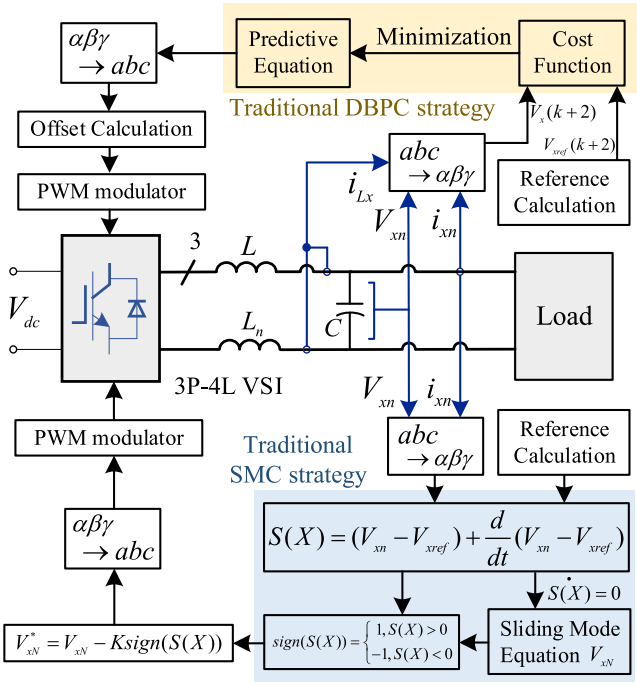

Fig. 3. Block diagrams of the traditional DBPC and SMC strategies.

The traditional sliding surface is constructed as follows, where λ is the weight coefficient of the sliding surface

$$S(X(k)) = \lambda \left(V_{xn}(k) - V_{xn}^*(k)\right) + \frac{d}{dt}\left(V_{xn}(k) - V_{xn}^*(k)\right) \quad x = \alpha, \beta, \gamma. \tag{10}$$

To track the voltage references stably and rapidly, the predictive sliding surface is constructed as the core of the DBPC cost function, where λ_1 and λ_2 are the adaptive weight coefficients of the sliding surface

$$S(X(k+2)) = \lambda_1 \left(V_{xn}(k+2) - V_{xn}^*(k+2)\right) + \lambda_2 \frac{d}{dt}\left(V_{xn}(k+2) - V_{xn}^*(k+2)\right) x = \alpha, \beta, \gamma. \tag{11}$$

To minimize the cost function, $S(X(\dot{k}+2))$ must be expressed. Inverter output voltages $V_{\alpha N}, V_{\beta N}, V_{\gamma N}$ are obtained through solving the following equation:

$$S(X(\dot{k}+2)) = \lambda_1 \left(V_{xn}(\dot{k}+2) - V_{xn}^*(\dot{k}+2)\right) + \lambda_2 \left(V_{xn}(\ddot{k}+2) - V_{xn}^*(\ddot{k}+2)\right) = 0 x = \alpha, \beta, \gamma. \tag{12}$$

To solve (12), we need to express the first-order and second-order derivatives of $V_{xn}(k+2)$ and $V_{xn}^*(k+2)$. By infinite approximation of (6) and (7), we obtain the discretized equation of the system, where $L_\alpha = L_\beta = L, L_\gamma = L + 3L_n$

$$\begin{cases} i_{Lx}(k+1) = i_{Lx}(k) + \frac{T_s}{L_x}\left(V_{xN}(k) - V_{xn}(k) - i_{Lx}(k)R\right) \\ V_{xn}(k+1) = V_{xn}(k) + \frac{T_s}{C}\left(i_{Lx}(k) - i_{xn}(k)\right) x = \alpha, \beta, \gamma \end{cases}. \tag{13}$$

Due to the high sampling frequency, we can assume that the load current remains constant within one sampling period

$$i_{xn}(k+1) \approx i_{xn}(k), (x = \alpha, \beta, \gamma). \tag{14}$$

By combining (13) and (14), $V_{xn}(k+2)$ can be predicted as

$$\begin{aligned} V_{xn}(k+2) &= V_{xn}(k+1) + \frac{T_s}{C}\left(i_{Lx}(k+1) - i_{xn}(k+1)\right) \\ &= V_{xn}(k) + \frac{{T_s}^2}{CL_x}\left(V_{xN}(k) - V_{xn}(k) - i_{Lx}(k)R\right) \\ &\quad + \frac{2T_s}{C}\left(i_{Lx}(k) - i_{xn}(k)\right) x = \alpha, \beta, \gamma. \end{aligned} \tag{15}$$

Since the control period T_s is much smaller than the dominant time constants of the inverter system, the variation of the state variables within one sampling interval is negligible. Therefore, the backward Euler form is approximated by the forward Euler form for simplicity, and the first-order derivative of (15) is expressed as

$$\begin{aligned} V_{xn}(\dot{k}+2) &= V_{xn}(\dot{k}+1) + \frac{T_s}{C}\left(i_{Lx}(\dot{k}+1) - i_{xn}(\dot{k}+1)\right) \\ &= \frac{1}{C}\left(i_{Lx}(k) - i_{xn}(k)\right) + \frac{T_s}{CL_x}\left(V_{xN}(k) - V_{xn}(k) - i_{Lx}(k)R\right) \\ &\quad x = \alpha, \beta, \gamma. \end{aligned} \tag{16}$$

The second-order derivative of (15) is given by

$$\begin{aligned} V_{xn}(\ddot{k}+2) &= \frac{1}{T_s}\left(V_{xn}(\dot{k}+2) - V_{xn}(\dot{k}+1)\right) \\ &= \frac{1}{{T_s}^2}\left(V_{xn}(k+2) + V_{xn}(k)\right) - \frac{2}{{T_s}^2}V_{xn}(k+1) \\ &= \frac{2}{{T_s}^2}V_{xn}(k) + \frac{1}{CL_x}\left(V_{xN}(k) - V_{xn}(k) - i_{Lx}(k)R\right) \\ &\quad + \frac{2}{CT_s}\left(i_{Lx}(k) - i_{xn}(k)\right) - \frac{2}{{T_s}^2}V_{xn}(k+1) x = \alpha, \beta, \gamma. \end{aligned} \tag{17}$$

Given that the past state is known, we can obtain $V_{xn}^*(k+2)$ by linear interpolation theory

$$V_{xn}^*(k+1) = 3V_{xn}^*(k) - 3V_{xn}^*(k-1) + V_{xn}^*(k-2) \tag{18}$$

$$V_{xn}^*(k+2) = 3V_{xn}^*(k+1) - 3V_{xn}^*(k) + V_{xn}^*(k-1) \tag{19}$$

$$V_{xn}^*(k+2) = 6V_{xn}^*(k) - 8V_{xn}^*(k-1) + 3V_{xn}^*(k-2). \tag{20}$$

The first-order and second-order derivatives of (20) are expressed as

$$\begin{aligned} V_{xn}^*(\dot{k}+2) &= \frac{V_{xn}^*(k+2) - V_{xn}^*(k+1)}{T_s} \\ &= \frac{3V_{xn}^*(k) - 5V_{xn}^*(k-1) + 2V_{xn}^*(k-2)}{T_s} x = \alpha, \beta, \gamma \end{aligned} \tag{21}$$

$$V_{xn}^*(\ddot{k}+2) = \frac{V_{xn}^*(k+2) + V_{xn}^*(k)}{{T_s}^2} - \frac{2}{{T_s}^2}V_{xn}^*(k+1)$$

$$= \frac{7V^*_{xn}(k) - 8V^*_{xn}(k-1) + 3V^*_{xn}(k-2)}{{T_s}^2} - \frac{2}{{T_s}^2} V^*_{xn}(k+1)$$

$$x = \alpha, \beta, \gamma. \tag{22}$$

Considering that the second derivative of the linear interpolation is zero and given the slow variation of the reference trajectory within the sampling interval and the fast dynamic response of the system, the predicted reference value can be reasonably approximated by the predicted system state to simplify the controller design and improve computational efficiency. The value at time step $k+1$ is therefore approximated as follows:

$$V^*_{xn}(k+1) \approx V_{xn}(k+1). \tag{23}$$

Substituting (16), (17), (21), (22), (23) into the first-order derivative of the predictive sliding surface (12), we obtain (24) shown at the bottom of this page, where **A** is the abbreviation for the reference load voltage.

By solving $S(X(\dot{k}+2)) = 0$, we obtain

$$\begin{aligned} V_{xN}(k) = {} & V_{xn}(k) + i_{Lx}(k)R \qquad x = \alpha, \beta, \gamma \\ & + \frac{CL_x}{\lambda_1 T_s + \lambda_2} \left(-A - \frac{2\lambda_2}{{T_s}^2} V_{xn}(k) \right. \\ & \left. - \frac{\lambda_1 T_s + 2\lambda_2}{CT_s} \left(i_{Lx}(k) - i_{xn}(k) \right) \right). \end{aligned} \tag{25}$$

The saturation function plays a crucial role in mitigating chattering while ensuring robust system performance. To get the saturation function of step $k+2$, the predictive sliding surface should be expressed by combining (11), (15), (16), (20), (21), and (25)

$$\begin{aligned} S(X(k+2)) = {} & \frac{\lambda_1 T_s - 2\lambda_2}{T_s} V_{xn}(k) + \frac{-3\lambda_1 T_s + 4\lambda_2}{T_s} V^*_{xn}(k) \\ & + \frac{3\lambda_1 T_s - 3\lambda_2}{T_s} V^*_{xn}(k-1) + \frac{-\lambda_1 T_s + \lambda_2}{T_s} V^*_{xn}(k-2) \\ & + \frac{\lambda_1 T_s - \lambda_2}{C} \left(i_{Lx}(k) - i_{xn}(k) \right) x = \alpha, \beta, \gamma. \end{aligned} \tag{26}$$

The saturation function is expressed as follows, where ϕ is the boundary of sliding surface

$$\text{sat}(S(X(k+2))) = \begin{cases} +1, & S(X(k+2)) > \phi \\ S(X(k+2))/\phi, & |S(X(k+2))| < \phi \\ -1, & S(X(k+2)) < -\phi \end{cases}. \tag{27}$$

Finally, the proposed DB-SMPC law is given as

$$V^*_{xN}(k) = V_{xN}(k) - K\text{sat}(S(X(k+2)))x = \alpha, \beta, \gamma \tag{28}$$

where K is the saturation function gain. Fig. 4 shows the block diagram of the proposed DB-SMPC strategy.

B. Parameters Adaptation

In the saturation function of DB-SMPC, the gain K directly affects the system's stability, convergence speed, and chattering characteristics. Meanwhile, λ_1 and λ_2 also influence the system's dynamic and steady-state performance. A reasonable value for K, λ_1, and λ_2 are necessary.

Selecting a relatively large value for the weighting factor λ is generally advantageous for enhancing control performance and improving tracking dynamics. However, the dynamic response of the inverter is inherently constrained by its switching frequency, thereby imposing an upper bound on λ, such that $\lambda_{\max} = f_{\text{switching}}$. Considering a maximum switching frequency of 20 kHz and reserving sufficient control margin to avoid potential instability, the upper limit of λ is conservatively set to 16 kHz. Based on these considerations and empirical tuning, an initial value of $\lambda_0 = 8000$ is adopted in this article.

After introducing the system perturbation ρ, $V^*_{xN}(k)$ can be expressed as

$$V^*_{xN}(k) = V_{xN}(k) - K\text{sat}(S(X(k+2))) + \rho\text{sat}(S(X(k+2))). \tag{29}$$

Therefore, the derivative of the predicted sliding surface can be expressed as

$$S^*(X(\dot{k}+2)) = -\frac{\lambda_1 T_s + \lambda_2}{CL_x} \cdot (K - \rho)\text{sat}(S(X(k+2))). \tag{30}$$

To ensure that ξ is absolutely positive, we can obtain that

$$K > \rho_{\max}. \tag{31}$$

The typical range of ρ is from 1 to 5. Considering system disturbances and stability margin, and based on simulation studies and experimental tuning, the final decision was to set the value of K_0 to 6.

To mitigate system chattering, the sigmoid function is applied, and the final expression for K is given by

$$K = 2K_0\text{sigmoid}(\|S(X(k+2))\|) = K_0 \frac{2}{1 + e^{-\|S(X(k+2))\|}}. \tag{32}$$

To determine λ_1 and λ_2, system error needs to be expressed

$$e(k) = V_{xn}(k) - V^*_{xn}(k) x = \alpha, \beta, \gamma. \tag{33}$$

To achieve better dynamic and steady-state performance of the system, the sigmoid function is applied, and the final expression

$$\begin{aligned} S(X(\dot{k}+2)) = {} & \frac{2\lambda_2}{{T_s}^2} V_{xn}(k) + \frac{\lambda_1 T_s + 2\lambda_2}{CT_s} \left(i_{Lx}(k) - i_{xn}(k) \right) \\ & + \frac{\lambda_1 T_s + \lambda_2}{CL_x} \left(V_{xN}(k) - V_{xn}(k) - i_{Lx}(k)R \right) x = \alpha, \beta, \gamma \\ & \underbrace{- \frac{3\lambda_1 T_s + 7\lambda_2}{{T_s}^2} V^*_{xn}(k) + \frac{5\lambda_1 T_s + 8\lambda_2}{{T_s}^2} V^*_{xn}(k-1) - \frac{2\lambda_1 T_s + 3\lambda_2}{{T_s}^2} V^*_{xn}(k-2)}_{A}. \end{aligned} \tag{24}$$

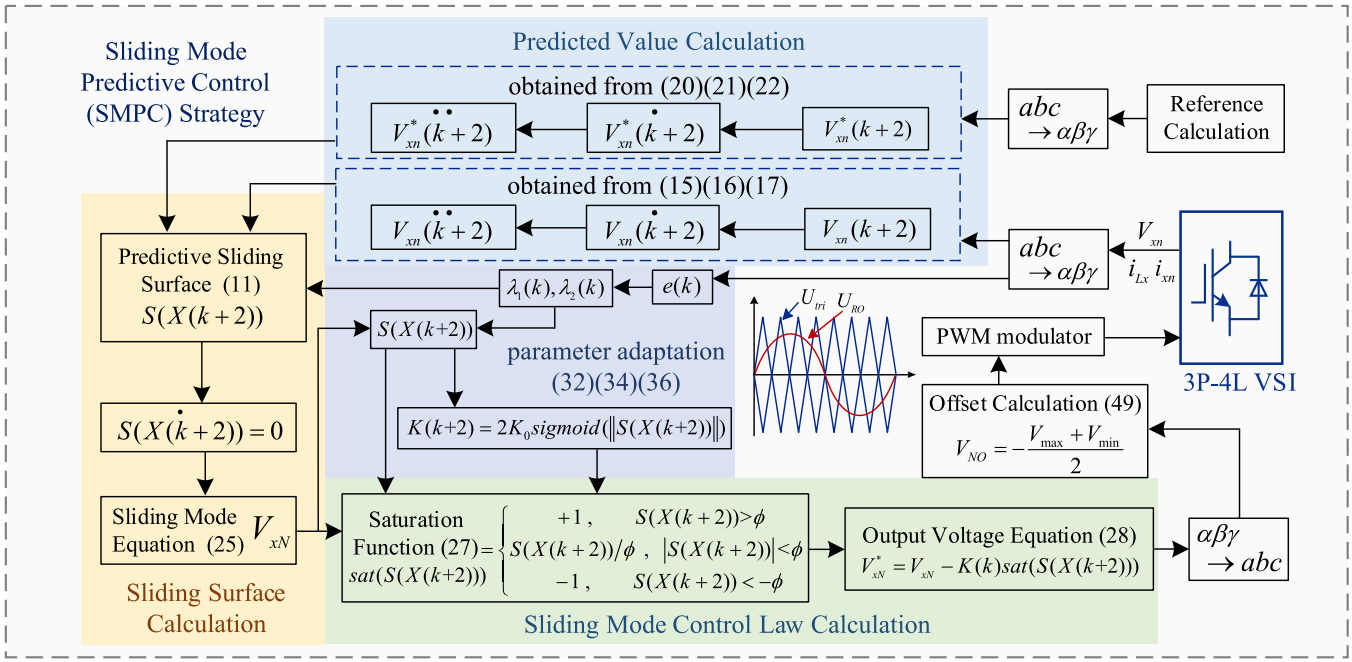

Fig. 4. Block diagram of the proposed DB-SMPC strategy.

for λ_1 is given by

$$\lambda_1 = 2\lambda_0 \text{sigmoid}(\|e(k)\|) = \lambda_0 \frac{2}{1+e^{-\|e(k)\|}}. \quad (34)$$

To make sure the coefficient of V_{xn} in (25) is positive, (35) needs to be satisfied

$$1 - \frac{CL}{\lambda_1 T_s + \lambda_2} \cdot \frac{2\lambda_2}{{T_s}^2} > 0 \Rightarrow 0 < \lambda_2 < \frac{\lambda_1 T_s^3}{2CL - T_s^2}. \quad (35)$$

Typically, the value of (35) is set to 1/2, which gives the value of λ_2

$$1 - \frac{CL}{\lambda_1 T_s + \lambda_2} \cdot \frac{2\lambda_2}{{T_s}^2} = \frac{1}{2} \Rightarrow \lambda_2 = \frac{\lambda_1 T_s^3}{4CL - T_s^2}. \quad (36)$$

C. Stability Analysis

Lyapunov's second method [30] is a technique used to determine the stability of an equilibrium point of a dynamical system without explicitly solving the system equations. It involves constructing a Lyapunov function E, which is positive definite and has a negative definite derivative along the system trajectories.

The deadbeat sliding mode predictive control law is defined in (28), by substituting the control law into the system and introducing system perturbations ρ, we obtain (30).

We choose the Lyapunov function E as

$$E = \frac{1}{2} S^2(X(k+2)) \quad (37)$$

which is positive definite.

Derivative of the Lyapunov function can be expressed as

$$\dot{E} = S(X(k+2))\, S^*(\dot{X}(k+2)). \quad (38)$$

Outside the boundary layer ($|S| > \phi$), the saturation function can be considered equal to the sign function

$$\text{sat}(S(X(k+2))) = \text{sign}(S(X(k+2))). \quad (39)$$

Thus,

$$\begin{aligned} \dot{E} &= S(X(k+2))\, S^*(\dot{X}(k+2)) \\ &= -\frac{\lambda_1 T_s + \lambda_2}{CL_x} \cdot (K - \rho)\, |S(X(k+2))| \end{aligned} \quad (40)$$

where

$$\begin{cases} \lambda_1 = \lambda_0 \frac{2}{1+e^{-\|e(k)\|}}, \lambda_{1\min} = \lambda_0 \\ \lambda_2 = \frac{\lambda_1 T_s^3}{4CL_x - T_s^2}, \lambda_{2\min} = \frac{\lambda_0 T_s^3}{4CL_x - T_s^2} \\ K = K_0 \frac{2}{1+e^{-\|S(X(k+2))\|}}, K_{\min} = K_0, K_0 > \rho_{\max} \end{cases}. \quad (41)$$

By substituting the minimum value of λ_1, λ_2, K, the range of the Lyapunov function can be obtained as

$$\begin{cases} \dot{E} < -\frac{4\lambda_0 T_s}{4CL_x - T_s^2} \cdot (K_0 - \rho_{\max})\, |S(X(k+2))| \le 0 \\ \dot{E} = 0 \text{if and only if} S(X(k+2)) = 0 \end{cases}. \quad (42)$$

This guarantees finite-time reachability of the sliding surface.

Within the boundary layer ($|S| \le \phi$), $S^*(\dot{X}(k+2))$ can be expressed as

$$S^*(\dot{X}(k+2)) = -\frac{\lambda_1 T_s + \lambda_2}{CL_x} \cdot \frac{(K-\rho)}{\phi} S(X(k+2)). \quad (43)$$

Thus,

$$\begin{aligned} \dot{E} &= S(X(k+2))\, S^*(\dot{X}(k+2)) \\ &= -\frac{\lambda_1 T_s + \lambda_2}{CL_x} \cdot \frac{(K-\rho)}{\phi} S^2(X(k+2)). \end{aligned} \quad (44)$$

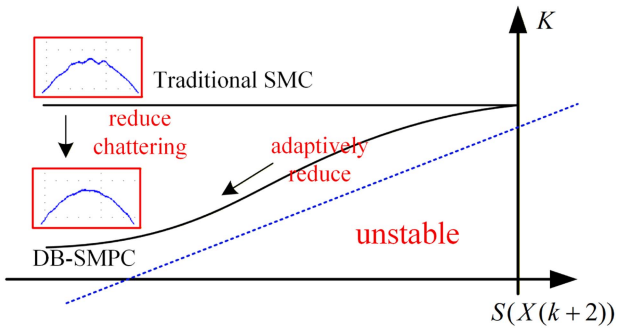

Fig. 5. Variation of the coefficient K.

By substituting the minimum value of λ_1, λ_2, K, the range of the Lyapunov function can be obtained as

$$\begin{cases} \dot{E} < -\frac{4\lambda_0 T_s}{4CL_x - T_s^2} \cdot \frac{(K_0 - \rho_{\max})}{\phi} \cdot S^2(X(k+2)) < 0 \\ \dot{E} = 0 \text{if and only if} S(X(k+2)) = 0 \end{cases}. \quad (45)$$

As a result, the Lyapunov condition is satisfied, which implies the asymptotic stability of the proposed DB-SMPC strategy globally.

Compared with the traditional PI controller, the DB-SMPC integrates a predictive sliding surface and deadbeat compensation, allowing it to actively anticipate system evolution and counteract parameter perturbations in each sampling period. The Lyapunov inequality ensures that all uncertain terms and external disturbances are confined within a finite range, thereby providing superior robustness compared with the traditional PI control strategy, whose performance is affected by parameter variations.

To guarantee Lyapunov global asymptotic stability, the coefficient K in the traditional SMC control law must always be greater than the upper bound of the disturbance [30], which results in significant chattering in the steady state. In the DB-SMPC strategy, since the predictive value of the sliding surface can be expressed, the introduction of a saturation or sigmoid function in (32) allows the DB-SMPC to effectively reduce chattering while maintaining convergence, thereby achieving adaptive disturbance suppression. Fig. 5 illustrates the variation of the coefficient K under the two control laws. Consequently, even under nonlinear or unbalanced load conditions, the proposed strategy sustains low THD, rapid dynamic recovery, and stable neutral-point voltage, theoretically superior to the traditional SMC.

D. Balancing the NP Voltage

As can be seen in Fig. 1, V_{RN}, V_{SN}, V_{TN} are output voltages obtained from $V_{\alpha N}^*, V_{\beta N}^*, V_{\gamma N}^*$ through the Clarke inverse transformation, where N is connected to the middle point of the additional leg. V_{RO}, V_{SO}, V_{TO} are pole voltages, V_{NO} is offset voltage. Their relationship can be written as

$$\begin{cases} V_{RO} = V_{RN} + V_{NO} \\ V_{SO} = V_{SN} + V_{NO} \\ V_{TO} = V_{TN} + V_{NO} \end{cases}. \quad (46)$$

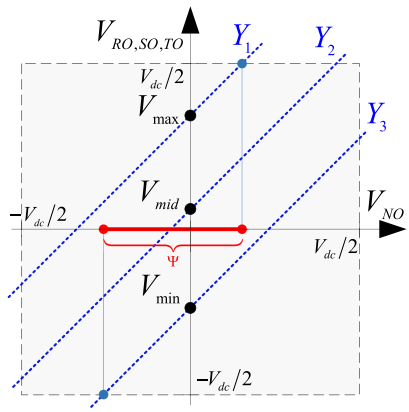

Fig. 6. Voltage range of $V_{RO}, V_{SO}, V_{TO}, V_{NO}$.

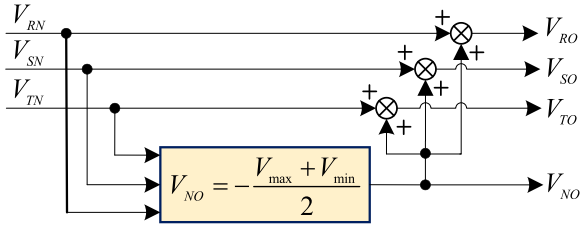

Fig. 7. Reference voltages $V_{RO}, V_{SO}, V_{TO}, V_{NO}$ calculation.

Fig. 6 shows the range of pole voltages and offset voltage caused by the dc-bus voltage limit

$$\begin{cases} -\frac{V_{\rm dc}}{2} \le V_{RO}, V_{SO}, V_{TO} \le \frac{V_{\rm dc}}{2} \\ -\frac{V_{\rm dc}}{2} \le V_{NO} \le \frac{V_{\rm dc}}{2} \end{cases}. \quad (47)$$

In Fig. 6, $V_{\max}, V_{\rm mid}, V_{\min}$ represent the maximum, middle, and minimum voltages of V_{RN}, V_{SN}, V_{TN}, respectively. Y_1, Y_2, Y_3 are the maximum, middle, and minimum voltages of V_{RO}, V_{SO}, V_{TO} [9]. Considering the range given in (47), V_{NO} falls within the range of ψ, which is expressed as

$$-\frac{V_{dc}}{2} - V_{\min} \le V_{NO} \le \frac{V_{\rm dc}}{2} - V_{\max}. \quad (48)$$

It is clear that $V_{\min}$ is negative and $V_{\max}$ is positive. Therefore, V_{NO} can be expressed as

$$V_{NO} = -\frac{V_{\max} + V_{\min}}{2}. \quad (49)$$

After calculating the offset voltage, we can obtain all the pole voltages by (46), as shown in Fig. 7. Finally, the POD-PWM scheme [34] is used to control the status of all 16 switches. Fig. 8 shows the states of the four switches in leg R.

IV. Experimental Results

Experiments were carried out to verify the superiority and adaptability of the proposed DB-SMPC strategy in terms of overall efficiency, robustness, neutral-point voltage balancing, THD, current tracking accuracy, voltage regulation, and transient response speed under various load conditions. As shown in Fig. 9, a T-type 3P-3L VSI experiment platform was developed

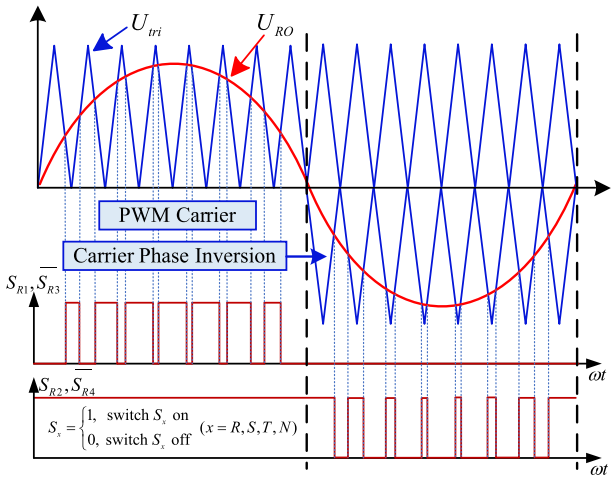

Fig. 8. POD-PWM scheme for T-type 3P-4L-3L-VSI.

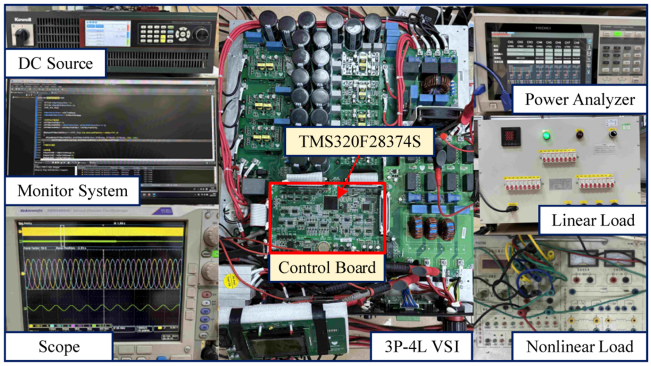

Fig. 9. System experiment platform.

TABLE II
ESSENTIAL PARAMETERS

Parameter	Description	Value
V_{dc}	dc voltage	600 V
$C_{P,N}$	dc-link capacitors	2340 μF
$L_{a,b,c,n}$	Filter inductors	960 μH
$C_{a,b,c}$	Filter capacitors	4.4 μF
T_s	Sampling and control period	50 μs
f_s	Switching frequency	20 kHz
V_{ref}	Reference value of voltage	282.8 V
ω_{ref}	Reference value of frequency	50 Hz
λ_0	Sliding mode control parameter	8000
K_0	Saturation function gain	6
ϕ	Saturation function boundary	1e5

using a TI DSP chip (TMS320F28374S). The inductor current $i_{La}, i_{Lb}, i_{Lc}, i_{Ln}$ and output current i_{an}, i_{bn}, i_{cn} are sampled by VAC current sensors, while the load voltages V_{an}, V_{bn}, V_{cn} are measured using LEM voltage sensors. The DSP executed the control strategy. Essential parameters are given in Table II.

Three traditional control strategies—Double closed-loop PI control, SMC [30], and CCS-MPC [21] are implemented and compared with the proposed DB-SMPC strategy on the experimental platform.

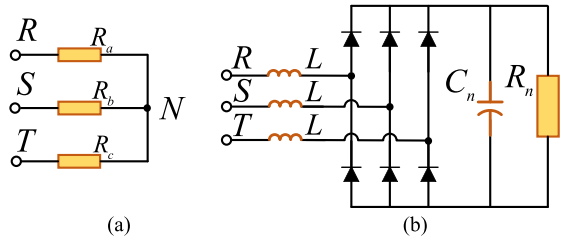

Fig. 10. Three-phase loads. (a) Linear load. (b) Nonlinear load.

TABLE III
ANALYSIS OF PARAMETERS SENSITIVITY

Mismatch	PI	MPC	SMC	SMPC
—	1.16%	1.55%	1.23%	0.97%
$\Delta L = 0\%,\ \Delta C = -50\%$	2.54%	1.88%	1.65%	1.32%
$\Delta L = 0\%,\ \Delta C = 50\%$	1.27%	1.49%	1.22%	1.02%
$\Delta L = -50\%,\ \Delta C = 0\%$	5.43%	2.64%	2.19%	1.88%
$\Delta L = 50\%,\ \Delta C = 0\%$	1.09%	1.28%	1.20%	0.95%

TABLE IV
ANALYSIS OF UNBALANCED PARAMETERS SENSITIVITY

Mismatch	R	S	T
—	0.97%	1.06%	1.14%
$\Delta L = 0\%,\ \Delta C = -50\%$	1.58%	1.16%	1.21%
$\Delta L = 0\%,\ \Delta C = 50\%$	0.95%	1.18%	1.26%
$\Delta L = -50\%,\ \Delta C = 0\%$	2.47%	1.87%	1.68%
$\Delta L = 50\%,\ \Delta C = 0\%$	0.92%	1.14%	1.17%

The inverter is tested under linear, nonlinear, and unbalanced load conditions, as illustrated in Fig. 10. The comparison focuses on computational time, efficiency, parameter adaptability, robustness, and both dynamic and steady-state performance.

All claimed improvements over PI, MPC, SMC and DB-SMPC have been quantified in Table V.

A. Comparative Analysis of System Performance Metrics

Fig. 11 presents the adaptive parameter values under three different conditions. The results indicate that, compared with using the traditional sign function, employing the saturation function with the adaptive parameter results in the lowest THD, which is reduced to 0.97%.

To analyze the system efficiency, four strategies are compared under different operating conditions. The system efficiency η is defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\% \tag{50}$$

where P_{out} represents the output power on the ac side, and P_{in} represents the input power on the dc side.

TABLE V
QUANTIFIED IMPROVEMENTS OVER PI, MPC, SMC, AND DB-SMPC

		PI	MPC	SMC	DB-SMPC
Efficiency	Case1	95.02%	96.90%	97.56%	97.17%
	Case2	90.70%	94.38%	95.31%	95.90%
	Case3	90.20%	92.60%	90.60%	91.90%
Execution time (μs)		37.5	41.8	38.9	38.3
THD	Linear loads	1.16%	1.55%	1.23%	0.97%
	Nonlinear loads	3.86%	3.18%	3.23%	2.71%
Dynamic response under reference voltage and load variations		Chattering	Mild Chattering	Mild Chattering	Smooth
Voltage sag under unbalanced load (V)		5	14.9	13.7	1.4
Bus voltage dip (V)	Linear loads	42	30	28	28
	Nonlinear loads	12	10	14	10
	Unbalanced loads	25	12	20	12
Recovery time (ms)	Linear loads	1700	150	160	150
	Nonlinear loads	>2000	110	140	110
	Unbalanced loads	>2000	160	150	150

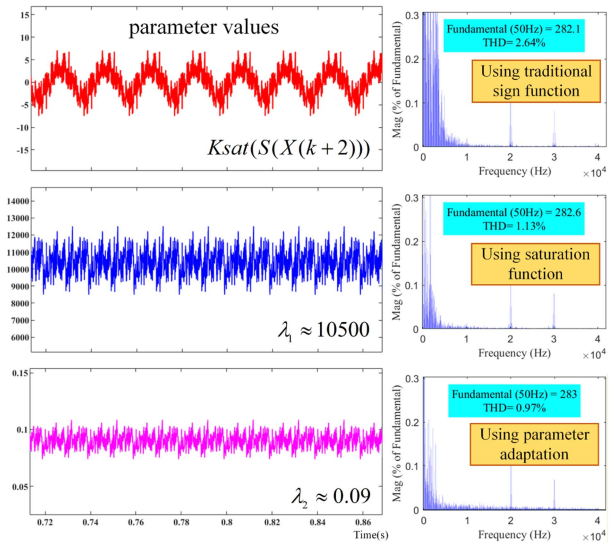

Fig. 11. Adaptive parameter values.

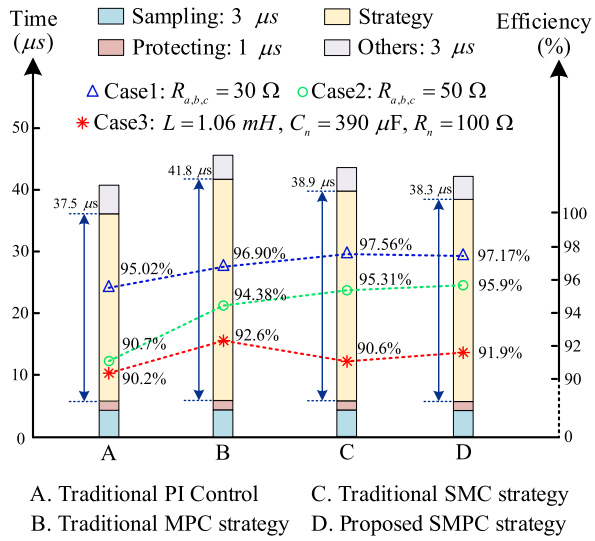

Fig. 12. Comparison of four strategies.

Three different working conditions are defined to compare the efficiency of the four strategies.

1) *Case 1:* Linear loads with $R_{a,b,c} = 30\ \Omega$.
2) *Case 2:* Linear loads with $R_{a,b,c} = 50\ \Omega$.
3) *Case 3:* Nonlinear loads $L = 1.06$ mH, $C_n = 390\ \mu$F, $R_n = 100\ \Omega$.

In Fig. 12, the execution time of the control algorithm is measured through the high and low logic levels of a hardware GPIO pin. When the control loop starts, the GPIO pin is set high, and it is set low when the loop ends. The total control cycle is 50 μs, and the high-level duration represents the execution time of the control strategy. The remaining sampling time and other processes are kept identical. The input power P_{in} is set by the dc power supply, while the output power P_{out} is measured using a power analyzer. The efficiencies of the DB-SMPC strategy and the SMC strategy are comparable and superior to PI control and they also outperform the MPC strategy under linear load conditions. Under nonlinear conditions, the proposed DB-SMPC strategy is slightly lower than the MPC strategy but outperforms the SMC strategy. As a result, the system efficiency of the proposed DB-SMPC strategy in this article is noteworthy.

Fig. 12 also shows the execution times for the four strategies, where the DB-SMPC strategy is only slightly higher than traditional PI control.

In practical applications, model parameter mismatches are inevitable due to various disturbances. The parameter sensitivity of four strategies are evaluated by varying the inductance $L$and

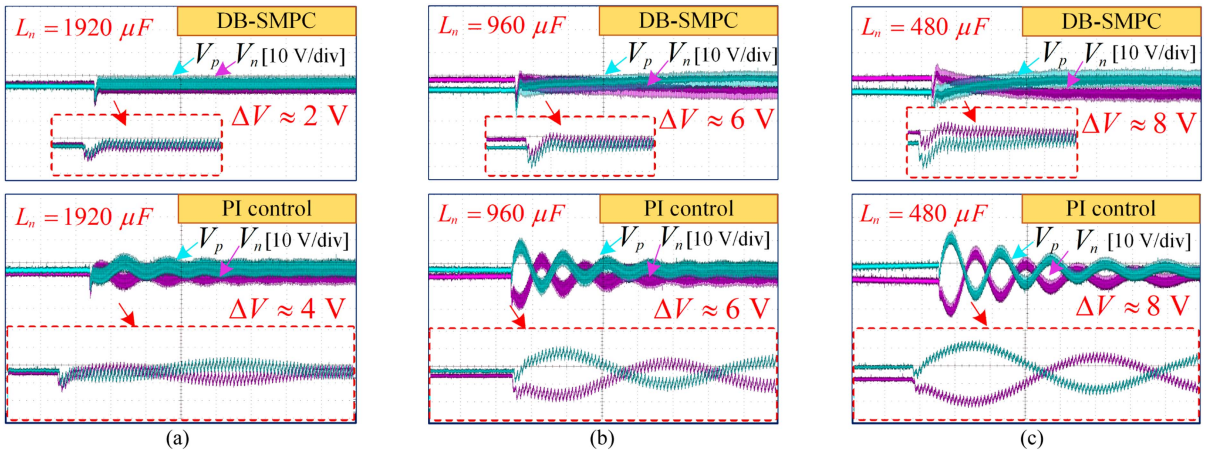

Fig. 13. NP voltages under variations in L_n. (a) $L_n = 1920\ \mu$F. (b) $L_n = 960\ \mu$F. (c) $L_n = 480\ \mu$F.

capacitance C, where the change rate ΔL and ΔC are

$$\begin{cases} \Delta L = \left(\widetilde{L} - L_f\right) \Big/ L_f \times 100\% \\ \Delta C = \left(\widetilde{C} - C_f\right) \Big/ C_f \times 100\% \end{cases} \tag{51}$$

where L_f and C_f represent the inductance and capacitance values used in the experiments, while $\widetilde{L}$ and $\widetilde{C}$ are the real filter inductance and capacitance values of the hardware.

The experimental results in Table III indicate that the double closed-loop PI control exhibits the poorest capability in handling model mismatches among all four strategies. Among the three nonlinear strategies, traditional MPC shows the weakest ability to handle model mismatches compared to SMC and the proposed DB-SMPC. Despite parameter mismatches, the proposed DB-SMPC achieves the lowest THD, proving its superior robustness.

Under the DB-SMPC strategy, experiments were conducted by varying only the filter parameters L and C of phase-A, while the other two phases remained unchanged. As given in Table IV, the THD of phase-A remains low under most parameter variations, demonstrating the strong robustness of the proposed control method. The results reveal that THD is more sensitive to reductions in inductance than to changes in capacitance, with a 50% decrease in L causing the largest performance degradation. Even in this worst-case scenario, the DB-SMPC strategy effectively limits the THD increase, highlighting its superior capability to maintain high power quality under unbalanced parameter conditions.

Fig. 13 compares the NP voltage performance of the DB-SMPC and PI control strategies under variations in the filter inductance L_n of the fourth leg. When $L_n = 1920\ \mu$F, DB-SMPC maintains a small NP voltage fluctuation of approximately 2 V, while PI control exhibits larger oscillations around 4 V. As L_n decreases to 960 μF, the fluctuation amplitude for DB-SMPC increases to about 6 V, but remains comparable to PI control at the same inductance. With a further reduction to 480 μF, both methods experience significant NP voltage deviations of about 8 V, however, DB-SMPC still demonstrates better damping and a faster settling time compared to PI control. These results indicate that DB-SMPC exhibits superior NP voltage regulation capability, especially under large inductance conditions, and maintains stability as inductance decreases.

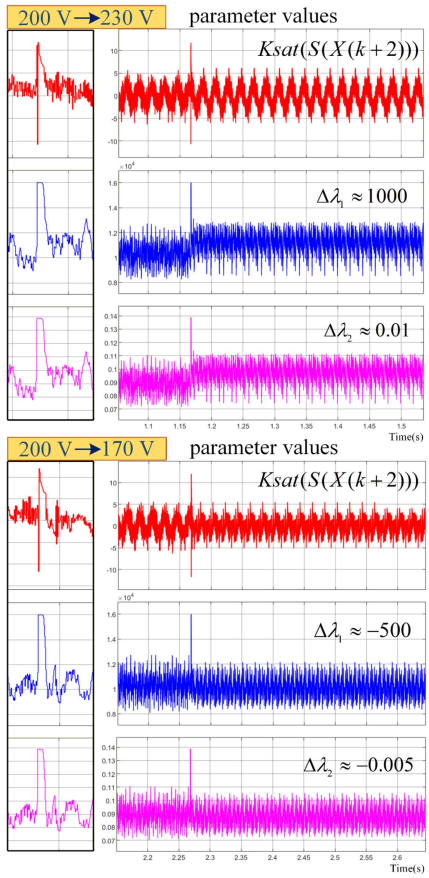

Fig. 14. Parameter adaptation under step changes in the load voltage reference.

B. Results for Step Changes of the Load Voltage Reference

To evaluate the transient performance under reference variations, the experimental results of step changes in the load voltage reference for four control strategies are presented in Fig. 15. These include the upper capacitor voltage V_p, lower

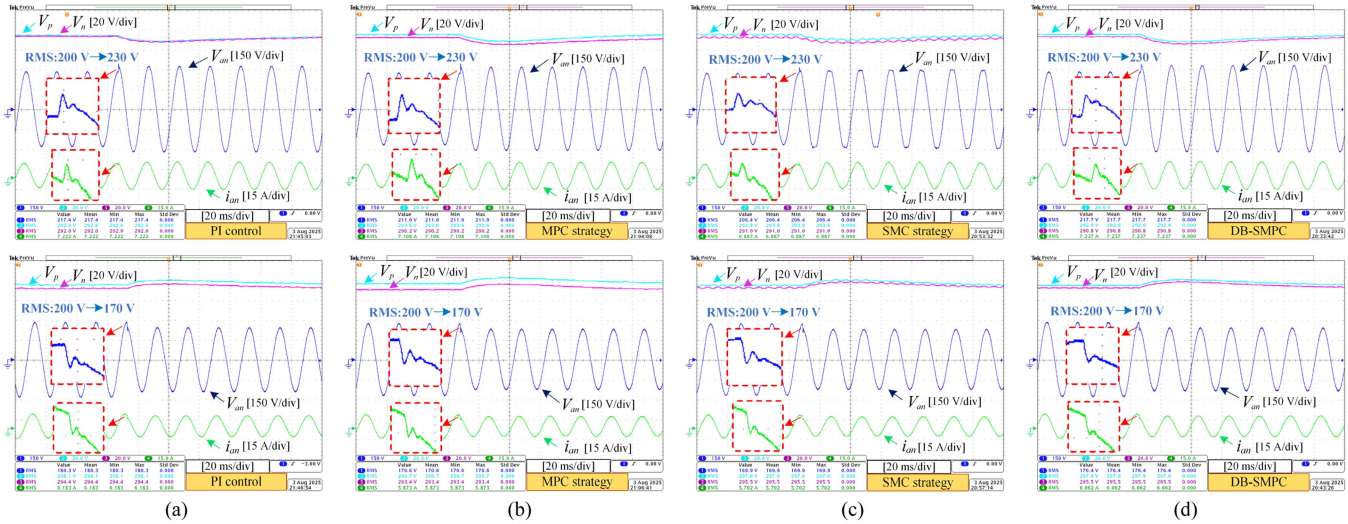

Fig. 15. Dynamic responses under step changes in load voltage reference. (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

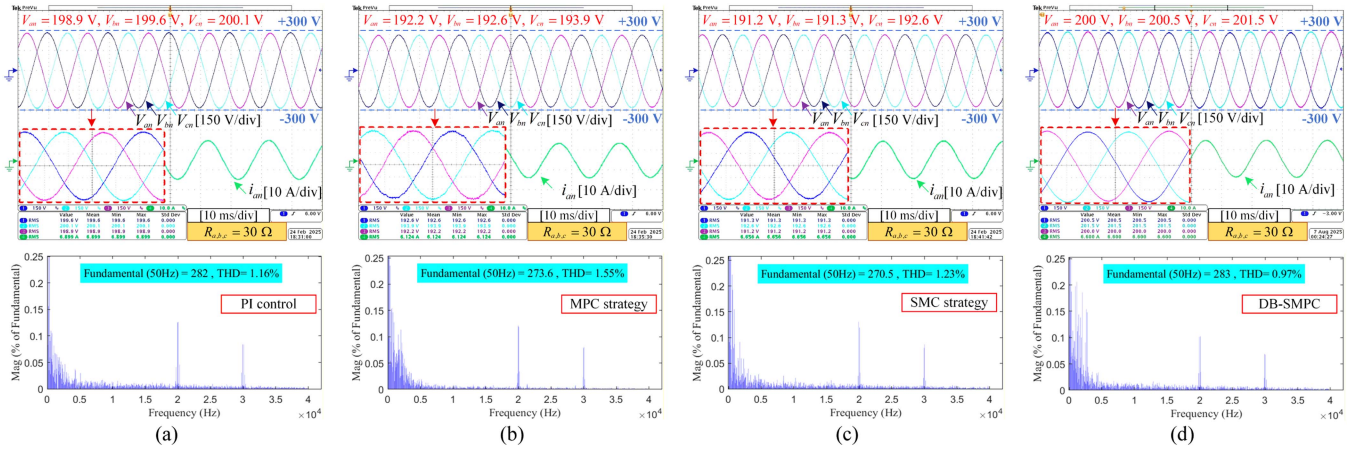

Fig. 16. Steady-state experimental waveforms with linear loads (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

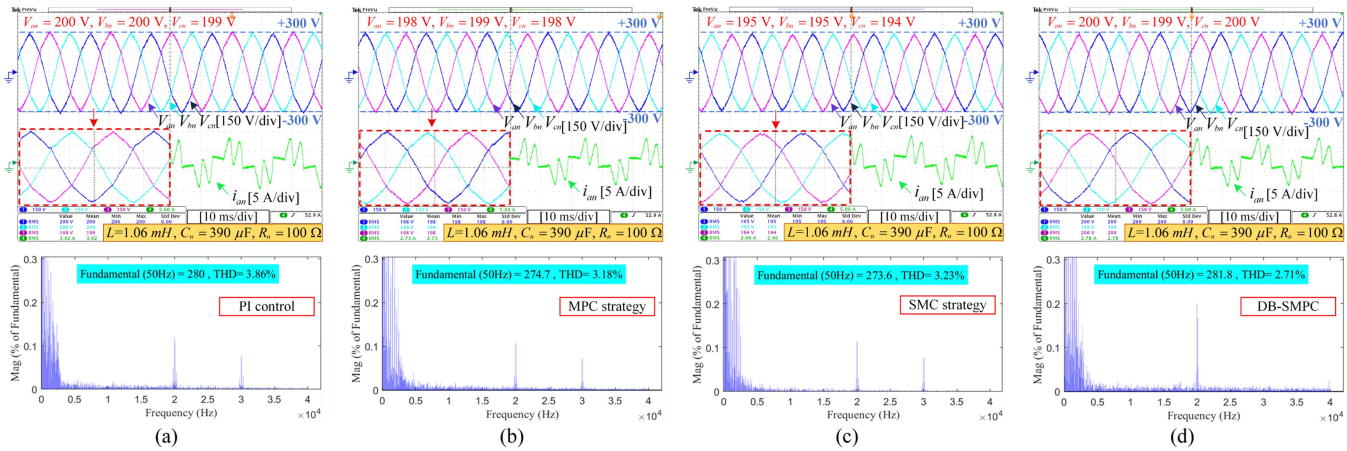

Fig. 17. Steady-state experimental waveforms with nonlinear loads (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

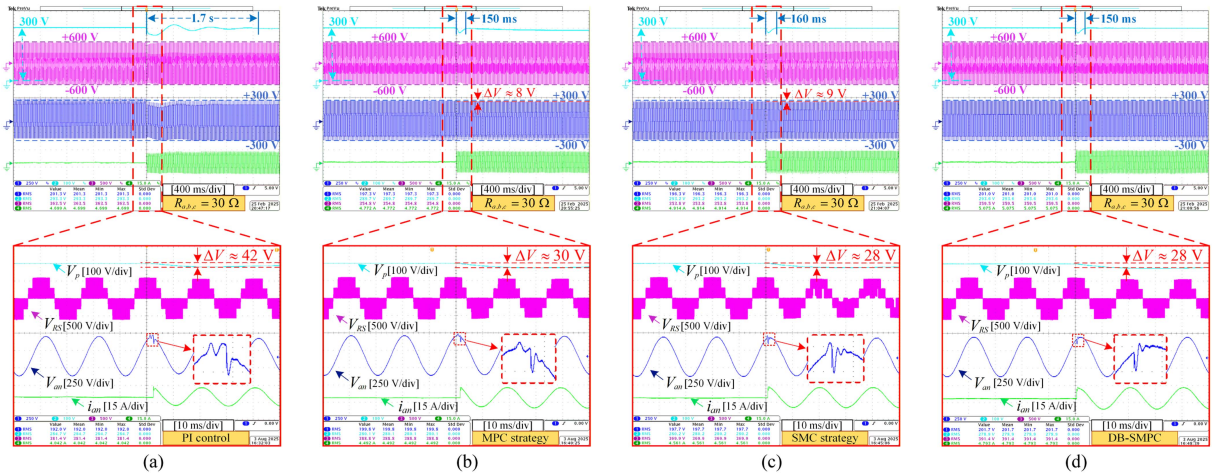

Fig. 18. Dynamic experimental waveforms with linear loads. (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

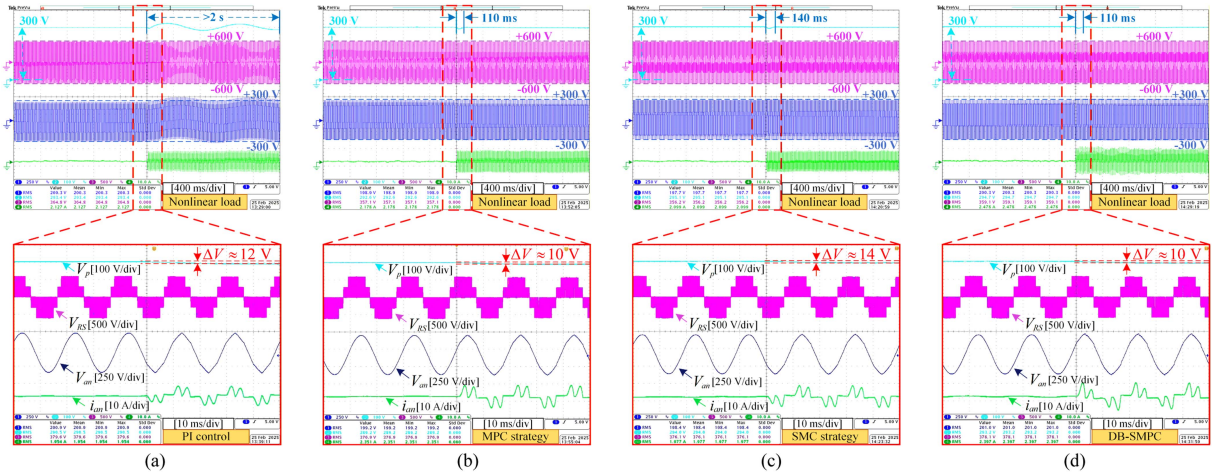

Fig. 19. Dynamic experimental waveforms with nonlinear loads. (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

capacitor voltage V_n, phase-A load voltage V_{an}, and phase-A output current i_{an}.

The experimental results under step changes in the load voltage reference demonstrate the transient performance of different control strategies.

When the RMS voltage steps from 200 to 230 V or from 200 to 170 V, the proposed DB-SMPC strategy exhibits the smoothest waveform and the fastest recovery among all tested methods.

SMC exhibits the worst steady-state voltage waveform, while PI and MPC provide improved performance but still lag behind DB-SMPC.

Parameter adaptation curves in Fig. 14 reveal that DB-SMPC adjusts its control gains promptly to compensate for load reference changes, ensuring minimal THD growth and stable operation throughout the transition.

C. Steady-State Experimental Results

Figs. 16 and 17 show the experimental steady-state waveforms of four strategies for both linear and nonlinear load conditions. The three-phase load voltage (V_{an}, V_{bn}, V_{cn}) and load current (i_{an}, i_{bn}, i_{cn}) are presented. Notably, the proposed DB-SMPC strategy achieves a THD below 1% and a steady-state voltage error of 1.7 V for linear load. For nonlinear load conditions, its load voltage maintains a THD of 2.71% and achieves a steady-state voltage error of 1.3 V. Figs. 16 and 17 also present the harmonic spectra of the output voltage, reconstructed in MATLAB/Simulink using experimental data acquired from the oscilloscope.

The experimental results indicate that, regardless of linear or nonlinear loads, the DB-SMPC strategy mitigates the steady-state voltage error observed in SMC and MPC while achieving the lowest THD among the four strategies, demonstrating its effectiveness in both conditions.

D. Dynamic Experimental Results

To analyze the dynamic performance of the proposed DB-SMPC strategy, the experimental dynamic response waveforms of four strategies under sudden load addition are shown in Figs. 18 and 19. These include the upper capacitor voltage V_p,

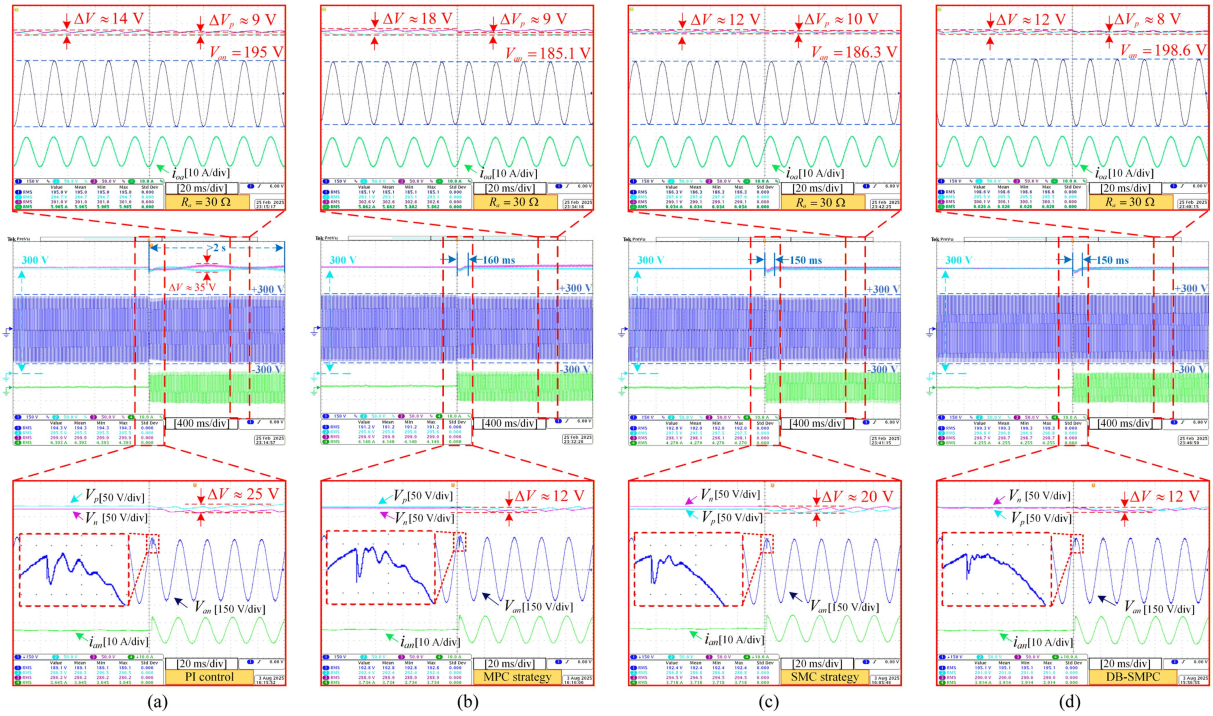

Fig. 20. Dynamic and steady-state experimental waveforms with unbalanced loads. (a) PI control. (b) MPC strategy. (c) SMC strategy. (d) Proposed DB-SMPC strategy.

inverter output line voltage V_{RS}, phase-A load voltage V_{an} and phase-A output current i_{an}.

Fig. 18 shows that under linear load conditions, the DB-SMPC strategy achieves the smallest bus voltage dip, the least oscillation and the smoothest waveform, demonstrating its superior voltage regulation capability. In terms of recovery time, the DB-SMPC strategy and MPC restore the voltage in 150 ms, which is comparable to SMC (160 ms) but significantly faster than PI control, which takes 1.7 s. Moreover, the DB-SMPC strategy and MPC exhibit the smallest voltage spike of 50 V, while PI control and SMC experience larger spikes of 100 V. Fig. 19 shows the results under nonlinear load conditions. Similar to the results under linear load conditions, the DB-SMPC strategy combines the advantages of SMC and MPC, demonstrating outstanding dynamic performance.

Under both linear and nonlinear load conditions, the DB-SMPC strategy exhibits the smallest bus voltage dip and the fastest recovery time, which are comparable to those of MPC and SMC, significantly outperforming PI control. Meanwhile, under linear load conditions, its voltage spike is the smallest among the four strategies, demonstrating its superior dynamic performance.

E. Results Under Unbalanced Load Conditions

Under unbalanced load conditions, NP balance is a crucial control indicator. Thus, the upper capacitor voltage V_p, the lower capacitor voltage V_n, phase-A load voltage V_{an} and phase-A output current i_{an} are presented in Fig. 20.

As shown in Fig. 20, the proposed DB-SMPC strategy, which combines the advantages of SMC and MPC, achieves the fastest NP balance recovery time of 150 ms, the smallest NP error in the steady state at 12 V, and the lowest NP voltage fluctuation of 8 V, significantly outperforming traditional PI control in NP balance performance. Furthermore, under sudden load addition, the proposed DB-SMPC strategy exhibits smaller voltage spike compared to traditional MPC and SMC, while its steady-state voltage error is significantly lower than that of MPC and SMC. These results indicate that the proposed strategy effectively integrates the advantages of traditional control methods, making it highly valuable for practical applications.

V. Conclusion

A novel DB-SMPC strategy is proposed in this article for T-type 3P-4L-3L-VSIs and is experimentally evaluated. The results demonstrate that the DB-SMPC strategy leverages the advantages of both SMC and MPC, resulting in enhanced system performance. By integrating the predictive capabilities of MPC with the robustness of SMC, the DB-SMPC strategy achieves fast response times, zero steady-state error, and strong robustness. Some conclusions are summarized as follows.

1) It achieves low THD under both linear and nonlinear load conditions, ensuring high power quality and stable output voltages.
2) It exhibits minimal bus voltage dip and fast dynamic response under sudden load changes, effectively enhancing system stability and transient performance.
3) It has strong robustness against parameter mismatches and external disturbances, maintaining reliable operation in uncertain conditions.

4) Under unbalanced load conditions, it ensures superior NP voltage balance with rapid recovery time and minimal NP voltage fluctuations.

These advantages make the DB-SMPC strategy an ideal choice for real-time control applications.

REFERENCES

[1] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[2] P. C. Loh and D. G. Holmes, "Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 644–654, Mar./Apr. 2005.

[3] G. He, M. Chen, W. Yu, N. He, and D. Xu, "Design and analysis of multiloop controllers with DC suppression loop for paralleled UPS inverter system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6494–6506, Dec. 2014.

[4] Y. Yang, H. Wen, M. Fan, M. Xie, and R. Chen, "Fast finite-switching-state model predictive control method without weighting factors for T-type three-level three-phase inverters," *IEEE Trans. Ind. Informat.*, vol. 15, no. 3, pp. 1298–1310, Mar. 2019.

[5] H. Xiong and C. Wu, "Control strategy of three-phase four-wire three-leg inverters," in *Proc. IEEE 10th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2019, pp. 75–78.

[6] F. Rojas et al., "An overview of four-leg converters: Topologies, modulations, control and applications," *IEEE Access*, vol. 10, pp. 61277–61325, 2022.

[7] I. Vechiu, H. Camblong, G. Tapia, B. Dakyo, and O. Curea, "Control of four leg inverter for hybrid power system applications with unbalanced load," *Energy Convers. Manag.*, vol. 48, no. 7, pp. 2119–2128, Jul. 2007.

[8] I. Vechiu, O. Curea, and H. Camblong, "Transient operation of a four-leg inverter for autonomous applications with unbalanced load," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 399–407, Feb. 2010.

[9] J.-H. Kim and S.-K. Sul, "A carrier-based PWM method for three-phase four-leg voltage source converters," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 66–75, Jan. 2004.

[10] I. Lopez et al., "Generalized PWM-based method for multiphase neutral-point-clamped converters with capacitor voltage balance capability," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4878–4890, Jun. 2017.

[11] I. Lopez et al., "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 928–941, Feb. 2016.

[12] X. He, "Hybrid ADRC and PI controller design for three-phase inverter with nonlinear loads," *IEEE Access*, vol. 12, pp. 130857–130864, 2024.

[13] M. Parvez, M. F. M. Elias, N. A. Rahim, F. Blaabjerg, D. Abbott, and S. F. Al-Sarawi, "Comparative study of discrete PI and PR controls for single-phase UPS inverter," *IEEE Access*, vol. 8, pp. 45584–45595, 2020.

[14] Q. Meng and Z. Hou, "Active disturbance rejection based repetitive learning control with applications in power inverters," *IEEE Trans. Control Syst. Technol.*, vol. 29, no. 5, pp. 2038–2048, Sep. 2021.

[15] B. Zhang, D. Wang, K. Zhou, and Y. Wang, "Linear phase lead compensation repetitive control of a CVCF PWM inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1595–1602, Apr. 2008.

[16] M. Pichan, H. Rastegar, and M. Monfared, "Deadbeat control of the stand-alone four-leg inverter considering the effect of the neutral line inductor," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2592–2601, Apr. 2017.

[17] J. Xu et al., "Carrier-based modulated model predictive control strategy for three-phase two-level VSIs," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1673–1687, Sep. 2021.

[18] C. Xue, D. Zhou, and Y. Li, "Hybrid model predictive current and voltage control for LCL-filtered grid-connected inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 5, pp. 5747–5760, Oct. 2021.

[19] S. Bayhan, H. Abu-Rub, and R. S. Balog, "Model predictive control of quasi-Z-source four-leg inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4506–4516, Jul. 2016.

[20] Y. Yang et al., "A novel continuous control set model predictive control for *LC* -filtered three-phase four-wire three-level voltage-source inverter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4572–4584, Apr. 2023.

[21] Y. Zhu et al., "Decoupled continuous control set model predictive control for T-type three-phase four-leg three-level inverters driving constant power loads," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7002–7015, Jun. 2024.

[22] C. Xue, W. Song, X. Wu, and X. Feng, "A constant switching frequency finite-control-set predictive current control scheme of a five-phase inverter with duty-ratio optimization," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3583–3594, Apr. 2018.

[23] C. Xue, D. Zhou, and Y. Li, "Finite-control-set model predictive control for three-level NPC inverter-fed PMSM drives with *LC* filter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 11980–11991, Dec. 2021.

[24] P. Kakosimos and H. Abu-Rub, "Deadbeat predictive control for PMSM drives with 3-L NPC inverter accounting for saturation effects," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 4, pp. 1671–1680, Dec. 2018.

[25] N. Bekhoucha, M. Kermadi, N. Mesbahi, and S. Mekhilef, "Performance investigation of deadbeat predictive controllers for three-level neutral point clamped inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 1, pp. 1165–1177, Feb. 2022.

[26] H. Esmaeili and M. Asadi, "A sliding mode controller based on robust model reference adaptive proportional-integral control for stand-alone three-phase inverter," *J. Modern Power Syst. Clean Energy*, vol. 9, no. 3, pp. 668–678, 2021.

[27] L. Zheng, F. Jiang, J. Song, Y. Gao, and M. Tian, "A discrete-time repetitive sliding mode control for voltage source inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 3, pp. 1553–1566, Sep. 2018.

[28] S.-L. Jung and Y.-Y. Tzou, "Discrete sliding-mode control of a PWM inverter for sinusoidal output waveform synthesis with optimal sliding curve," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 567–577, Jul. 1996.

[29] L. Nalla, M. K. Mishra, and A. Ghosh, "Sliding mode control of a four-leg dynamic voltage restorer in a natural reference frame," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 4, no. 3, pp. 919–927, Jul. 2023.

[30] M. Pichan and H. Rastegar, "Sliding-mode control of four-leg inverter with fixed switching frequency for uninterruptible power supply applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6805–6814, Aug. 2017.

[31] X. Zhang, Z. Wang, and H. Bai, "Sliding-mode-based deadbeat predictive current control for PMSM drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 11, no. 1, pp. 962–969, Feb. 2023.

[32] Y. Xu, S. Li, and J. Zou, "Integral sliding mode control based deadbeat predictive current control for PMSM drives with disturbance rejection," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2845–2856, Mar. 2022.

[33] Y. Wang et al., "A novel extended sliding-mode predictive control with dynamic optimization and virtual voltage vectors," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 10976–10988, Sep. 2024.

[34] E. H. Al-Fatlawi and T. H. M. Al-Mhana, "Comparison between 3-level single phase NPC and SI-NPC multilevel inverter based on PD PWM & POD PWM techniques for photovoltaic applications," in *Proc. 2nd Int. Conf. Adv. Eng. Sci. Technol.*, 2022, pp. 639–644.

Zijian Zhao received the B.S. degree in electrical engineering from Soochow University, Suzhou, China, in 2023, where he is currently working toward the M.S. degree in engineering with the School of Rai Transportation, Soochow University, Suzhou, China.

His research interests include modeling predictive control and stability analysis of power electronic inverters.

Yong Yang (Senior Member, IEEE) received the B.S. degree in automation from Xiangtan University, Xiangtan, China, in 2003, the M.S. degree in electrical engineering from Guizhou University, Guiyang, China, in 2006, and the Ph.D. degree in electrical engineering from Shanghai University, Shanghai, China, in 2010.

He is currently a Full Professor with the School of Rail Transportation, Soochow University. From December 2017 to December 2018, he was a Visiting Scholar with Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. He has authored or co-authored more than 80 IEEE Transactions papers and is the holder of more than 60 patents in these areas. His current research interests include model predictive control in power electronic converters, distributed energy resource interfacing and high-performance motor drive control.

Rong Chen was born in Jiangsu, China, in 1983. She received the B.S. degree in communication engineering, the M.S. degree in communication and information system, and the Ph.D. degree in signal and information processing from Soochow University in 2006, 2009, and 2013, respectively.

She is currently an Associate Professor with the School of Rail Transportation, Soochow University. Her research interests include signal processing and synchronous phasor measuring.

Jiefeng Hu (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Technology Sydney, Ultimo, NSW, Australia, in 2013.

He participated in the research of minigrids in Commonwealth Scientific and Industrial Research Organization. He was an Assistant Professor with The Hong Kong Polytechnic University, Hong Kong. He is currently an Associate Professor and a Program Coordinator of Electrical Engineering with Federation University Australia, Ballarat, VIC, Australia, where he is also the Stream Leader of Centre for New Energy Transition Research. His research interests include power electronics, renewable energy, and smart microgrids.

Dr. Hu is an Associate Editor for IET Renewable Power Generation, an Editor for IEEE TRANSACTIONS ON ENERGY CONVERSION, an Associate Editor for IEEE ACCESS, and was a Guest Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS for a Special Issue "Applications of Predictive Control in Microgrids."

Hui Yang (Senior Member, IEEE) received the B.Eng. degree from Dalian University of Technology, Dalian, China, in 2011, and the Ph.D. degree from Southeast University, Nanjing, China, in 2016, respectively, all in electrical engineering.

From 2014 to 2015, he was supported by the China Scholarship Council through a one-year joint Ph.D. studentship at The University of Sheffield, Sheffield, U.K. From 2019 to 2020, he was a Postdoctoral Fellow with the School of Electrical Engineering, The Hong Kong Polytechnic University. From 2016 to 2024, he was with Southeast University, China, and he is currently a Full Professor with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. He has authored or co-authored over 120 IEEE Transactions papers and is the holder of more than 40 patents in these areas. His research interests include novel permanent-magnet machines and drives with particular reference to variable-flux machines for electric vehicles, robotics, and renewable energy applications.

Dr. Yang is currently an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON ENERGY CONVERSION, and an Editor of WEVJ. He was the Organizing Committee Chair of iSPEC 2021 and CIEEC 2022.

Huiqing Wen (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2006, respectively, and the Ph.D. degree in electrical engineering from the Chinese Academy of Sciences, Beijing, China, in 2009.

From 2009 to 2010, he was an Electrical Engineer working with the Research and Development Center, GE (China) Company, Ltd., Shanghai, China. From 2010 to 2011, he was an Engineer with the China Coal Research Institute, Beijing, China. From 2011 to 2012, he was a Postdoctoral Fellow with the Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates. He is currently a Full Professor with Xi'an Jiaotong-Liverpool University, Suzhou, China. His current research interests include bidirectional dc–dc converters, power electronics in flexible AC transmission applications, electrical vehicles, and high-power, three-level electrical driving systems.

Yiwang Wang (Member, IEEE) received the B.S. degree in electrical engineering and automation from the Kunming University of Science and Technology, Kunming, China, in 2005, and the Ph.D. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2020.

He is currently a Professor with the Collaborative Innovation Center of Smart Energy Equipment and Power Conversion, Suzhou Polytechnic University, Suzhou, China. He is also the Director of Suzhou Key Laboratory of Smart Energy Technology and Jiangsu Engineering Research Center for PV Generation. His research interests include power electronics intelligent control, and the applications of power electronics and renewable energy.

Jose Rodriguez (Life Fellow, IEEE) received the Engineer degree in electrical engineering from the Universidad Tecnica Federico Santa Maria, Valparaiso, Chile, in 1977, and the Dr.-Ing. degree in electrical engineering from the University of Erlangen, Erlangen, Germany, in 1985.

Since 1977, he has been with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, where he was a Full Professor and the President. From 2015 to 2019, he was the President of Universidad Andres Bello in Santiago, Chile. From 2022 to 2023, he was the President of Universidad San Sebastian, Santiago, Chile. He is currently the Director of the Center for Energy Transition, Universidad San Sebastian. He has coauthored two books, several book chapters and more than 1000 journal and conference papers. From 2014 to 2024, he has been included in the list of Highly Cited Researchers published by Web of Science. His main research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives.

Dr. Rodriguez was the recipient of a number of best paper awards from journals of the IEEE. Dr. Rodriguez is member of the Chilean Academy of Engineering, the National Award of Applied Sciences and Technology from the government of Chile, in 2014, and the Eugene Mittelmann Award from the Industrial Electronics Society of the IEEE, in 2015.