A Dual-Perspective Analysis of IGBT Open-Circuit Faults in Hybrid Modular Multilevel Converters: Unified Characteristics and Diagnoses

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***Abstract*—The hybrid modular multilevel converter (HMMC) comprising both full-bridge submodules (SMs) and half-bridge SMs has drawn extensive attention for its cost-effective dc fault ride-through capability. However, insulated gate bipolar transistor (IGBT) open-circuit fault (OCF) diagnosis—a prerequisite for fault isolation and fault reconfiguration—is critical to the reliability of HMMCs, while relevant research remains scarce. Furthermore, varied OCF scenarios within HMMC further complicate fault diagnosis. To fill this gap, this article first conducts a dual-perspective analysis of IGBT OCFs in HMMCs, covering single and multiple OCF scenarios in an SM. Two unified characteristics are yielded: first, Unified Characteristic I, derived from the mode-type perspective, reveals that IGBT OCFs cause specific mode-type conversions of the faulty SM, and second, Unified Characteristic II, derived from the switching-function perspective, indicates that the faulty SM maintains a specific switching function. Therefore, a unified characteristics-driven strategy is proposed, including a detection stage and a localization stage. In the detection stage, the suspected faulty SM is selected via Unified Characteristic II and its status is then ascertained using Unified Characteristic I. Upon the identification of a fault, other suspected faulty SMs are screened, with their statuses determined in the ensuing localization stage. Hardware-in-the-loop experiments validate the effectiveness of the proposed strategy.**

***Index Terms*—Hybrid modular multilevel converters (HMMCs), mode type, open-circuit fault (OCF), switching function, unified-characteristics-driven strategy.**

I. Introduction

MODULAR multilevel converters (MMCs) possess outstanding modularity, high efficiency, and superior scalability, which have been applied in diverse high-voltage scenarios, especially in flexible-high voltage direct current (flexible-HVdc) [1], [2], [3].

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As the cost is much lower than that of underground cables, overhead lines are extensively applied in long-distance flexible HVdc systems [4]. However, dc short-circuit faults (SCFs) have a higher likelihood of occurrence in the overhigh-line scenario [5]. Thus, the capability of handling dc SCFs requires attention in long-distance flexible HVdc systems [6]. Unfortunately, the most widely used half-bridge MMC (HBMMC) does not have the dc fault handling capability due to the freewheeling effect of diodes in the half-bridge submodule (HBSM) [7]. The introduction of the full-bridge submodule (FBSM) can remedy the deficiency of the dc fault handling capability [8]. Nevertheless, its cost is far higher than that of HBSM. Hence, the hybrid MMC (HMMC) composed of both FBSMs and HBSMs is proposed in [9]. HMMCs integrate the merits of both HBSMs and FBSMs, which have been applied in the Kunliulong Project in Southwestern China [4]. Meanwhile, compared to the HBMMC of the same voltage level, the HMMC consists of more power devices, and its reliability requires more attention.

According to pertinent statistics, power devices, such as insulated gate bipolar transistors (IGBTs), are the most fragile components in power electronic converters [10], [11]. There are two typical fault types of IGBT: the SCF and the open-circuit fault (OCF) [12]. IGBT SCFs can be caused by various factors, such as incorrect gate voltage, overvoltage, avalanche stress, and temperature overshoot [13]. IGBT SCFs can lead to abnormal overcurrent, thereby causing severe damage to other components in a short amount of time [14]. Therefore, the majority of SCF detection and protection methods are implemented based on hardware circuits to ensure sufficiently rapid response speeds, and these technical approaches have achieved a high degree of maturity. With regard to IGBT OCFs, those induced by the lift-off, rupture of bond wires, or the absence of the gate drive signal may not have strong short-term destructiveness [15], [16]. However, they can trigger faults in other normal components and deteriorate the normal operation of MMCs [12], [17]. Therefore, dedicated diagnostic strategies are required to diagnose the IGBT OCF.

Upon completion of the diagnosis, fault isolation and fault reconfiguration are activated to enable the converter to continue normal operation. This is achieved by closing the bypass switch in the faulty SM and utilizing hardware or software redundancy, respectively [18]. Furthermore, the intricate fault characteristics of IGBT OCFs render their diagnosis more

challenging. Therefore, this article focuses on the diagnosis of IGBT OCFs in HMMCs.

In the past few years, numerous IGBT OCF diagnostic strategies have been successively advanced, which can be broadly categorized into three categories: hardware-based strategies, artificial intelligence (AI)-based strategies, and model-based strategies. However, the vast majority of them only regard the HBSMs within the HBMMC as the research subject [19]. For instance, strategies in [20] and [21] employ hardware-based methodologies to diagnose IGBT OCFs in HBMMCs. In [20], a rearranged bleeding resistor-based circuit is utilized to diagnose IGBT OCFs of HBMMCs in light-load conditions. The installation positions of the SM voltage sensors are adjusted to measure output voltages of SMs [21]. However, the introduction of additional hardware or the adjustment of existing hardware will increase system costs. To avoid reliance on hardware, the strategies outlined in [22] and [23] diagnose IGBT OCFs by leveraging powerful AI tools. In [22], the faulty SM is accurately identified via cluster classification outputs. In [23], a feature reconstruction-recurrent neural network is employed to achieve fault diagnosis. This approach enables direct fault localization with no detection stage or diagnostic delay. Except for the two aforementioned categories of strategies, there exists another category of model-based diagnostic strategies. A scheme based on a signal synthesis technique is proposed, which is capable of detecting and locating the OCF simultaneously [24]. In [25], the error accumulation impact of numerical calculation on the diagnosis of IGBT OCFs is first unveiled. Subsequently, a fault diagnosis method with error elimination is proposed. Relying on the periodicity of the capacitor voltage deviations, a repetitive signal generator-based approach is proposed to confirm the malfunctioning arm [26]. In [27], a novel diagnostic strategy is proposed by utilizing a modified switching function and constructing a mathematical model of the faulty SM.

All the strategies mentioned above focus on HBMMCs but overlook other cases. The strategy in [28] considers the case of IGBT OCFs in full-bridge MMC (FBMMC). However, due to the limitations of the switching method, it ignores some fault types. The strategy in [29] employs a multilayer long short-term memory (LSTM) network to deeply extract the fault characteristics of FBMMCs. However, the aforementioned diagnostic strategies for MMCs containing only a single type of SMs cannot be directly generalized to HMMC scenarios. This is primarily attributed to the fact that the operation of FBSMs and HBSMs in HMMCs is not completely symmetrical, causing some research conclusions applicable to HBMMCs or FBMMCs to no longer be valid for HMMCs. To address this issue, an improved switching method-based strategy is proposed in [30], which can diagnose all types of IGBT OCFs in HMMCs. However, this study does not cover scenarios in which multiple IGBT OCFs occur simultaneously within a single SM. Furthermore, owing to the lack of sufficient in-depth analysis of fault characteristics, this method needs to be implemented separately for FBSMs and HBSMs. This exacerbates the complexity of the diagnostic strategy and also makes the setting of parameters more complicated. However, actually, because of the topological similarity of HBSMs and FBSMs, the fault characteristics of IGBT OCFs in them also show similarity, providing the theoretical possibility for a unified diagnosis. Therefore, it is necessary to conduct in-depth research on IGBT OCFs in HMMCs to reveal the commonalities in different types of IGBT OCFs.

Toward this end, a dual-perspective analysis of IGBT OCFs in HMMCs is first conducted in this article. By analyzing from the perspective of the impact on the operating modes of SMs, it is revealed that different scenarios of IGBT OCFs share certain unified characteristics from such a perspective. These characteristics are named Unified Characteristic I, indicating that an IGBT OCF causes a conversion of the affected bypassed-type mode from the bypassed type to the charging type and a conversion of the affected discharging type from the discharging type to the bypassed type or the charging type. Based on Unified Characteristic I, Unified Characteristic II is further summarized from the perspective of the impact on the switching function of SMs. Unified Characteristic II uncovers that two causal loops arise due to the conflict between the goal of the voltage balancing strategy (VBS) and the type conversion of the affected mode. These two causal loops force the faulty SM to remain in a specific function. Relying on these two unified characteristics, a unified characteristics-driven strategy is proposed, which consists of a detection stage and a localization stage. In the detection stage, the suspected faulty SM is first selected according to its switching-function characteristics. Subsequently, its status is further ascertained by its mode-type characteristic. Once an IGBT OCF has been detected in the detection stage, other potentially faulty SMs are screened by the switching-function characteristic. In the subsequent localization stage, the statuses of these SMs are determined by their mode-type characteristics. Immediately upon completion of diagnosis, fault isolation and fault reconfiguration are initiated. There are three main contributions in this article, which are enumerated as follows.

1) The dual-perspective analysis conducted in this article comprehensively uncovers the commonalities in diverse scenarios of IGBT OCFs within HMMCs, remedying the deficiencies of existing research.
2) Two unified characteristics summarized herein indicate that diverse scenarios of IGBT OCFs in HMMCs possess certain unified characteristics from the mode-type perspective and the switching-function perspective, offering a theoretical foundation for a unified diagnosis.
3) The unified characteristics-driven strategy proposed in this article integrates two unified characteristics and is capable of diagnosing all scenarios of IGBT OCFs within HMMCs in a unified and straightforward manner, facilitating application.

The rest of this article is organized as follows. Section II introduces the configurations and controls of HMMCs. Sections III and IV, respectively, analyze the unified characteristics of diverse types of IGBT OCFs within HMMC from the mode-type perspective and the switching-function perspective. The unified-characteristics-driven strategy is proposed in Section V. Further discussions of the proposed diagnostic strategy are given in Section VI. Section VII presents a comprehensive comparison between the proposed diagnostic strategy and existing ones. Section VIII offers the hardware-in-the-loop

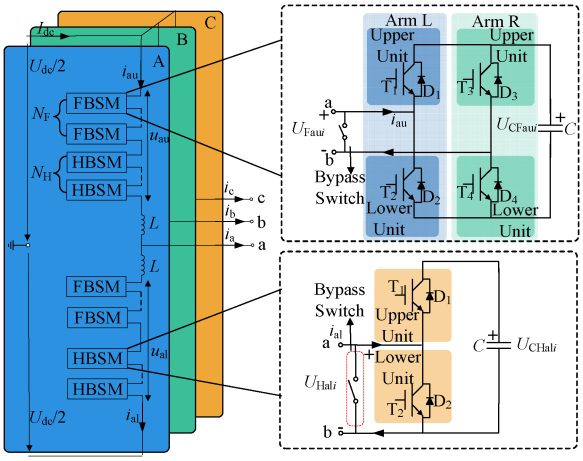

Fig. 1. Topology of an HMMC.

(HIL) experimental results under various scenarios. Finally, Section IX concludes this article.

II. Configurations and Controls of HMMCs

A. Configurations of HMMCs

The configuration of a three-phase six-arm HMMC is shown in Fig. 1. Each arm is composed of N_{F} FBSMs, N_{H} HBSMs, and an arm inductor L. U_{dc} and I_{dc} denote the dc voltage and current, respectively. i_{au} and i_{al} represent the upper arm current and the lower arm current of phase A, respectively. u_{au} and u_{al} are the output voltages of all SMs in the upper arm and the output voltages of all SMs in the lower arm of phase A, respectively. To differentiate between parameters corresponding to FBSMs and HBSMs, this article employs the "F" and "H" in the subscripts of parameters that correspond to FBSMs and HBSMs, respectively. Moreover, the "i" used in the subscripts corresponds to the sequence number of SMs.

The configurations of the FBSM and the HBSM are also shown in Fig. 1. Both the FBSM and the HBSM are equipped with bypassed switches for the purpose of fault isolation [31]. The FBSM comprises four fundamental units and a capacitor C. Each fundamental unit consists of an IGBT and an antiparallel diode. During normal operation, the IGBT drive signals of the upper and lower units in the same arm are complementary. Therefore, there are four switching combinations for the FBSM, which can be expressed as follows.

$$(\mathrm{T}_1, \mathrm{T}_2, \mathrm{T}_3, \mathrm{T}_4)_i = \begin{cases} (1,0,0,1) \\ (0,1,1,0) \\ (1,0,1,0) \\ (0,1,0,1). \end{cases} \tag{1}$$

The combination of two flow directions of the arm current and four switching combinations results in a total of eight modes for the FBSM, as illustrated in Table I. $S_{\mathrm{F}i}$ represents the switching function of the FBSM. i_{arm} represents the arm current. $u_{\mathrm{CF}i}$ represents the capacitor voltage of the FBSM. During normal operation, the VBS regulates the switching state of the FBSM via the switching function as follows:

$$S_{\mathrm{F}i} = \begin{cases} 1, & \text{positive - inserted state} \\ 0, & \text{bypassed state} \\ -1, & \text{negative - inserted state.} \end{cases} \tag{2}$$

Furthermore, the output voltage of the FBSM is controlled by the switching function as follows:

$$u_{\mathrm{F}i} = S_{\mathrm{F}i} u_{\mathrm{CF}i} \tag{3}$$

where $u_{\mathrm{F}i}$ represents the output voltage of the FBSM.

The HBSM comprises two fundamental units and a capacitor C. Similar to the FBSM, the IGBT drive signals of the upper and lower units are also complementary in the HBSM. Therefore, there are two switching combinations for the HBSM, which can be expressed as follows:

$$(\mathrm{T}_1, \mathrm{T}_2)_i = \begin{cases} (1,0) \\ (0,1). \end{cases} \tag{4}$$

The combination of two flow directions of the arm current and two switching combinations results in a total of four modes for the HBSM, as illustrated in Table II. $S_{\mathrm{H}i}$ represents the switching function of the HBSM. $u_{\mathrm{CH}i}$ represents the capacitor voltage of the HBSM. During normal operation, the VBS regulates the switching state of the HBSM via the switching function as follows:

$$S_{\mathrm{H}i} = \begin{cases} 1, & \text{positive - inserted state} \\ 0, & \text{bypassed state.} \end{cases} \tag{5}$$

Furthermore, the output voltage of the HBSM is controlled by the switching function as follows:

$$u_{\mathrm{H}i} = S_{\mathrm{H}i} u_{\mathrm{CH}i} \tag{6}$$

where $u_{\mathrm{H}i}$ represents the output voltage of the HBSM.

TABLE I
FBSM Operating Modes in Normal State

Mode	i_{arm}	Switching combination	$S_{\mathrm{F}i}$	Flow path	$u_{\mathrm{CF}i}$	Type
$\mathrm{I_F}$	≥0	(1,0,0,1)	1	$\mathrm{D_1}$, $\mathrm{D_4}$	↑	C
$\mathrm{II_F}$		(0,1,1,0)	-1	$\mathrm{T_2}$, $\mathrm{T_3}$	↓	D
$\mathrm{III_F}$		(1,0,1,0)	0	$\mathrm{D_1}$, $\mathrm{T_3}$	—	B
$\mathrm{IV_F}$		(0,1,0,1)	0	$\mathrm{T_2}$, $\mathrm{D_4}$	—	B
$\mathrm{V_F}$	<0	(1,0,0,1)	1	$\mathrm{T_1}$, $\mathrm{T_4}$	↓	D
$\mathrm{VI_F}$		(0,1,1,0)	-1	$\mathrm{D_2}$, $\mathrm{D_3}$	↑	C
$\mathrm{VII_F}$		(1,0,1,0)	0	$\mathrm{T_1}$, $\mathrm{D_3}$	—	B
$\mathrm{VIII_F}$		(0,1,0,1)	0	$\mathrm{D_2}$, $\mathrm{T_4}$	—	B

TABLE II
HBSM Operating Modes in Normal State

Mode	i_{arm}	Switching combination	$S_{\mathrm{H}i}$	Flow path	$u_{\mathrm{CH}i}$	Type
$\mathrm{I_H}$	≥0	(1,0)	1	$\mathrm{D_1}$	↑	C
$\mathrm{II_H}$		(0,1)	0	$\mathrm{T_2}$	—	B
$\mathrm{III_H}$	<0	(1,0)	1	$\mathrm{T_1}$	↓	D
$\mathrm{IV_H}$		(0,1)	0	$\mathrm{D_2}$	—	B

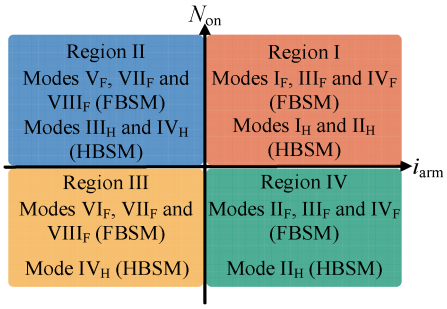

Fig. 2. Modes utilized in four regions.

B. Controls of HMMCs

According to papers [9] and [31], the modulation index of the HMMC can be expressed as

$$m = \frac{U_{\mathrm{m}}}{0.5U_{\mathrm{dc}}} \tag{7}$$

where m represents the modulation index of the HMMC. U_{m} represents the amplitude of the output ac voltage. According to the paper [31], the range of u_{au} and u_{al} can be expressed as

$$0.5U_{\mathrm{dc}}(1-m) \le \{u_{\mathrm{au}}, u_{\mathrm{al}}\} \le 0.5U_{\mathrm{dc}}(1+m). \tag{8}$$

Since u_{au} and u_{al} have equivalent ranges, this article exclusively analyzes u_{au}. Given that u_{au} is the output voltage of all SMs in the upper arm of phase A, it can be expressed as

$$u_{\mathrm{au}} = \sum_{i=1}^{N_{\mathrm{F}}} u_{\mathrm{Fau}i} + \sum_{i=1}^{N_{\mathrm{H}}} u_{\mathrm{Hau}i} = \sum_{i=1}^{N_{\mathrm{F}}} S_{\mathrm{Fau}i} u_{\mathrm{CFau}i} + \sum_{i=1}^{N_{\mathrm{H}}} S_{\mathrm{Hau}i} u_{\mathrm{CHau}i}. \tag{9}$$

In the event of m being less than 1, it can be obtained from (8) that the lower limit of u_{au} is positive. Therefore, the arm does not necessitate the generation of negative voltage, and the negatively inserted state of the FBSM is not employed.

In the event of m being greater than 1, it can be obtained from (8) that the lower limit of u_{au} is negative. Therefore, the negatively inserted state of the FBSM is employed to generate a negative voltage. In such a scenario, the HMMC is capable of outputting the rated ac voltage under the low dc voltage or outputting the boosted ac voltage under the rated dc voltage, a feat that is not attainable with the HBMMC.

C. VBS Adopted in HMMCs

To better illustrate the objectives of the VBS, four regions are defined based on the polarity of the arm current and the number of inserted SMs, as shown in Fig. 2.

In each region, the control logic of the VBS is presented in Table III to ensure the balance of SM capacitor voltages within the arm. In this table, "N_{on}" represents the number of inserted SMs in the current control period.

In Regions I and II, the VBS does not distinguish between FBSMs and HBSMs, but its operational logic is reversed. Specifically, in Region I, the VBS prioritizes the positive insertion of SMs with lower capacitor voltages to charge them; in contrast, in Region II, it prioritizes the positive insertion of SMs with higher capacitor voltages to discharge them.

In Regions III and IV, the VBS exclusively activates FBSMs, with reversed operational logic between the two regions as well. Specifically, in Region III, the VBS prioritizes charging FBSMs with lower voltages under negative insert conditions; in Region IV, by contrast, it prioritizes discharging FBSMs with higher capacitor voltages under negative insert conditions.

Moreover, the improved switching method proposed in [30] is employed in this article to ensure that the characteristics of IGBT OCFs are fully captured.

TABLE III
CONTROL LOGIC OF THE VBS IN FOUR REGIONS

Region	Operational logic for FBSMs	Operational logic for HBSMs
I	Follow the same logic: SMs with higher capacitor voltages are assigned higher priority for positive insertion.	
II	Follow the same logic: SMs with lower capacitor voltages are assigned higher priority for positive insertion.	
III	FBSMs with lower capacitor voltages are assigned higher priority for negative insertion.	All are bypassed
IV	FBSMs with higher capacitor voltages are assigned higher priority for negative insertion.	All are bypassed

TABLE IV
THREE TYPES OF OPERATING MODES OF THE SM

Type	The state of the SM capacitor
B	Bypassed
C	Charged
D	Discharged

TABLE V
TWO DIRECTIONS OF THE ARM CURRENT

Polarity	The ports that the arm current flows into and out of the SM
Positive	Flows into the SM through port a and out through port b
Negative	Flows into the SM through port b and out through port a

III. UNIFIED CHARACTERISTICS FROM THE MODE-TYPE PERSPECTIVE

To facilitate subsequent analysis, several key concepts are first defined. Based on the state of the SM capacitor, the operating modes of the SM can be classified into three different types, as illustrated in Table IV. When the SM operates in a Type B operating mode, its capacitor is bypassed. In the cases of the SM operating in a Type C mode or a Type D mode, its capacitor is charged or discharged, respectively.

In both HBSMs and FBSMs, two directions of the arm current are defined in Table V. When the arm current is positive, it flows into the SM through port a and then out through port b. Conversely, when the arm current is negative, it flows into the SM through port b and out through port a.

This section classifies analysis scenarios by the number of faulty IGBTs in an SM and conducts separate analyses for two scenarios: a single IGBT OCF and multiple IGBT OCFs.

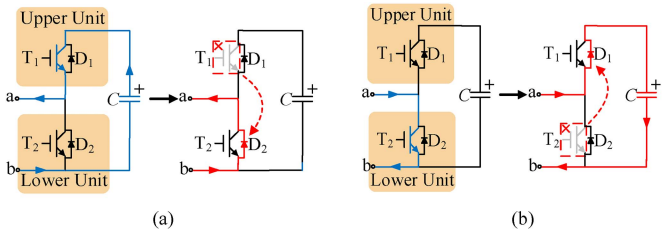

Fig. 3. Affected modes caused by IGBT OCFs in HBSMs. (a) Affected Mode III_H by a Position T_{1H} fault. (b) Affected Mode II_H by a Position T_{2H} fault.

A. Characteristics of Single IGBT OCF in an SM From the Mode-Type Perspective

1) Analysis of a Single IGBT OCF in an HBSM: Corresponding to the two IGBTs in the HBSM, IGBT OCFs in the HBSM are likely to arise at two positions. These are designated as Position T_{1H} fault and Position T_{2H} fault, which correspond to open-circuited T_1 fault and open-circuited T_2 fault, respectively. As indicated in Table II, only the flow path of Mode III_H contains the T_1. Since the impact of IGBT OCFs is confined to the operating modes whose flow paths encompass the corresponding faulty IGBT, a Position T_{1H} fault only affects Mode III_H. Furthermore, as demonstrated in Table II, the arm current is required to flow either via the diode of the lower unit or the IGBT of the upper unit when the arm current is negative.

Therefore, the arm current flows via D_2 in lieu of the open-circuited T_1 in affected Mode III_H, as shown in Fig. 3(a). Due to the modification of the flow path, the affected Mode III_H is converted to Mode IV_H. As illustrated in Table II, when the arm current is negative, the flow path of a Type D mode encompasses an IGBT, and the flow path of a Type B mode contains a diode. Therefore, Position T_{1H} fault causes the type of the affected Type D mode to undergo a conversion from Type D to Type B.

As indicated in Table II, only the flow path of the Mode II_H contains the T_2. Since the impact of IGBT OCFs is confined to the modes whose flow paths encompass the corresponding faulty IGBT, a Position T_{2H} fault only affects Mode II_H. Furthermore, as demonstrated in Table II, the arm current is required to flow either via the diode of the upper unit or the IGBT of the lower unit when the arm current is positive. Therefore, the arm current flows via D_1 instead of the open-circuited T_2 in affected Mode II_H, as shown in Fig. 3(b). Due to the modification of the flow path, the affected Mode II_H is converted to Mode I_H. As illustrated in Table II, when the arm current is positive, the flow path of a Type B mode encompasses an IGBT, and the flow path of a Type C mode contains a diode. Therefore, Position T_{2H} fault causes the type of the affected Type B mode to undergo a conversion from Type B to Type C.

2) Analysis of a Single IGBT OCF in an FBSM: Corresponding to the four IGBTs in the FBSM, IGBT OCFs in the FBSM are likely to arise at four positions. These are designated as Position T_{1F} fault, Position T_{2F} fault, Position T_{3F} fault, and Position T_{4F} fault, which correspond to open-circuited T_1 fault, open-circuited T_2 fault, open-circuited T_3 fault, and open-circuited T_4 fault, respectively.

TABLE VI
CHARACTERISTICS OF SINGLE IGBT OCFS IN AN HBSM OR AN FBSM FROM THE MODE-TYPE PERSPECTIVE

Position	Polarity of the arm current	Affected mode	Mode type
T_{1H}	Negative	$III_H \rightarrow IV_H$	D→B
T_{2H}	Positive	$II_H \rightarrow I_H$	B→C
T_{1F}	Negative	$V_F \rightarrow VIII_F$	D→B
		$VII_F \rightarrow VI_F$	B→C
T_{2F}	Positive	$II_F \rightarrow III_F$	D→B
		$IV_F \rightarrow I_F$	B→C
T_{3F}	Positive	$II_F \rightarrow IV_F$	D→B
		$III_F \rightarrow I_F$	B→C
T_{4F}	Negative	$V_F \rightarrow VII_F$	D→B
		$VIII_F \rightarrow VI_F$	B→C

As indicated in Table I, only the flow paths of Mode V_F and Mode VII_F contain the T_1. Since the impact of IGBT OCFs is confined to the modes whose flow paths encompass the corresponding faulty IGBT, a Position T_{1F} fault affects Modes V_F and VII_F. Moreover, as illustrated in Tables I and IV, when the arm current is negative, it flows into the SM through port b and out through port a. This current must flow either via the diode of the lower unit in the Arm L or the IGBT of the upper unit in the Arm L. Therefore, the arm current flows via D_2 in lieu of the open-circuited T_1 in both affected modes, as shown in Fig. 4(a) and (b). Due to alterations to the flow paths, the affected Mode V_F is converted to Mode $VIII_F$, and the affected Mode VII_F is converted to Mode VI_F. As illustrated in Table I, when the arm current is negative, the flow path of a Type B mode incorporates an IGBT and a diode, the flow path of a Type C mode comprises two diodes, and the flow path of a Type D mode encompasses two IGBTs. Consequently, the Position T_{1F} fault results in a conversion of the affected Mode V_F from Type D to Type B, and a conversion of the affected Mode VII_F from Type B to Type C.

The analyses of Positions T_{2F}, T_{3F}, and T_{4F} faults are similar to the previously conducted analysis of Position T_{1F} fault; thus, they are not repeated here. The impacts in the flow paths corresponding to Positions T_{2F}, T_{3F}, and T_{4F} faults are also shown in other subgraphs of Fig. 4.

In light of the analysis conducted in Section III-A, the characteristics of a single IGBT OCF in an HBSM or an FBSM from the mode-type perspective can be summarized as presented in Table VI.

B. Characteristics of Multiple IGBT OCFs in an SM From the Mode-Type Perspective

As demonstrated in Section III-A, the polarity of the arm current corresponding to a single IGBT OCF in an HBSM or an FBSM is illustrated in Table VI. Based on the polarity of the arm current, the scenarios of multiple IGBT OCFs in an HBSM or an FBSM are classified into three categories, each of which will be analyzed in this section. In addition, given that an HBSM comprises two IGBTs and an FBSM comprises four IGBTs, the number of IGBTs subjected to simultaneous OCFs within an SM is constrained to two to streamline the analysis.

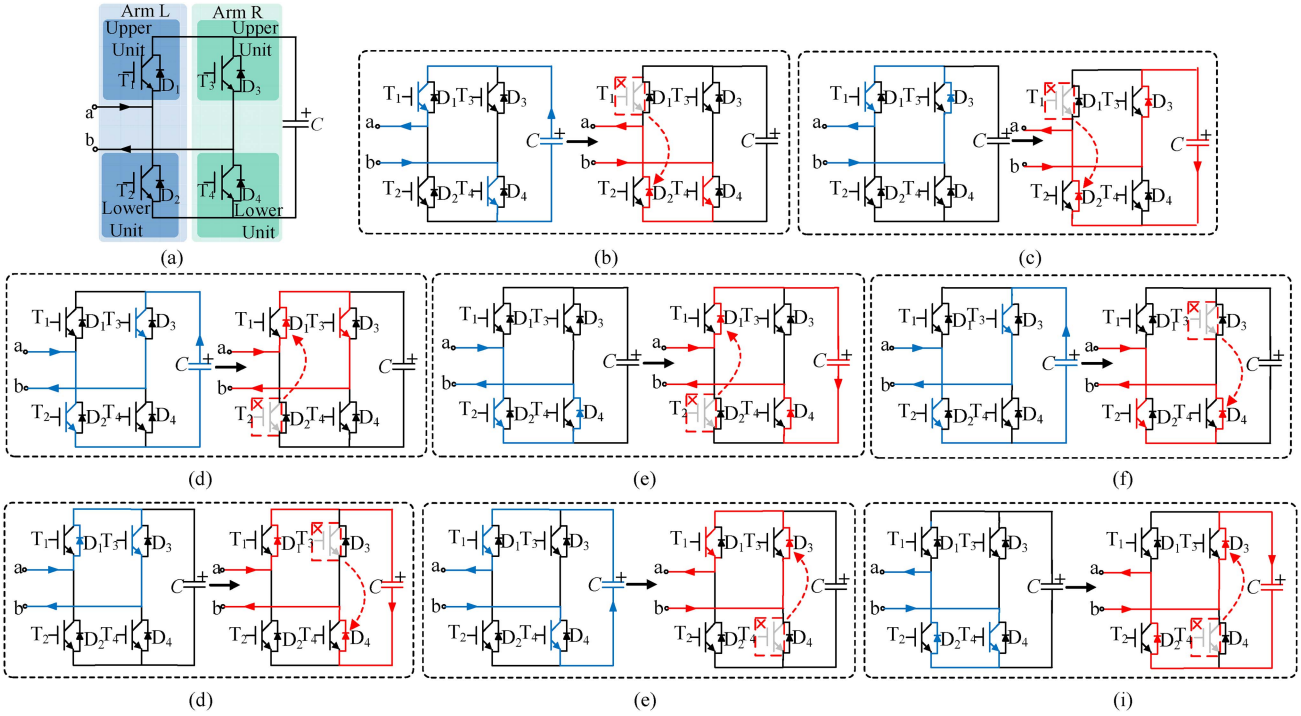

Fig. 4. Configuration of FBSMs and affected modes caused by IGBT OCFs in FBSMs. (a) Configuration. (b) Affected Mode V_F by a Position T_{1F} fault. (c) Affected Mode VII_F by a Position T_{1F} fault. (d) Affected Mode II_F by a Position T_{2F} fault. (e) Affected Mode IV_F by a Position T_{2F} fault. (f) Affected Mode II_F by a Position T_{3F} fault. (g) Affected Mode III_F by a Position T_{3F} fault. (h) Affected Mode V_F by a Position T_{4F} fault. (i) Affected Mode $VIII_F$ by a Position T_{4F} fault.

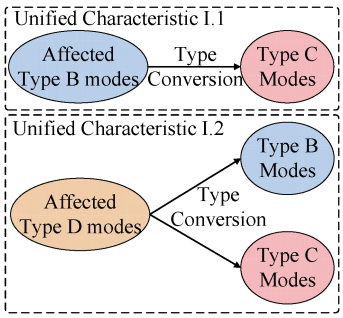

Fig. 5. Unified characteristics of IGBT OCFs from the mode-type perspective.

1) Corresponding Arm Current Polarity: Positive Only: As listed in Table VI, the only feasible combination of simultaneously occurring IGBT OCFs within an SM is the Position T_{2F} fault and the Position T_{3F} fault. As illustrated in Table I, the flow paths of Modes II_F, III_F, and IV_F each include at least one of the T_2 or the T_3. Consistent with the scenario where the faults occur individually, the arm current flows via D_1 instead of the open-circuited T_2 in affected Modes II_F and IV_F, and the arm current flows via D_4 instead of the open-circuited T_3 in affected Modes II_F and III_F. Due to the modification of the flow path, all three affected modes are converted to Mode I_F. Consequently, the combination of Position T_{2F} fault and Position T_{3F} fault results in a conversion of the affected Mode II_F from Type D to Type C, and a conversion of the affected Modes III_F and IV_F from Type B to Type C.

2) Corresponding Arm Current Polarity: Negative Only: As listed in Table VI, the only feasible combination of simultaneously occurring IGBT OCFs within an SM is the Position T_{1F} fault and the Position T_{4F} fault. The analysis of this fault combination is analogous to the prior analysis of the analysis conducted on the combination of the Position T_{2F} fault and the Position T_{3F} fault. Due to the modification of the flow path, Modes V_F, VII_F, and $VIII_F$ are all converted to Mode VI_F. Consequently, the combination of Position T_{1F} fault and Position T_{4F} fault results in a conversion of the affected Mode V_F from Type D to Type C, and a conversion of the affected Modes VII_F and $VIII_F$ from Type B to Type C.

3) Corresponding Arm Current Polarity: Positive and Negative: As listed in Table VI, under this scenario, there are five feasible combinations of simultaneously occurring IGBT OCFs within an SM, specifically: Position T_{1H} fault and Position T_{2H} fault, Position T_{1F} fault and Position T_{2F} fault, Position T_{1F} fault and Position T_{3F} fault, Position T_{2F} fault and Position T_{4F} fault, and Position T_{3F} fault and Position T_{4F} fault. In these five combinations, the arm current corresponding to one IGBT OCF exhibits a positive polarity, while that corresponding to the other IGBT OCF exhibits a negative polarity. This indicates that no fault coupling occurs between the two IGBT OCFs. Consequently, the composite fault characteristics when these two faults occur simultaneously are the direct superposition of their respective individual fault characteristics.

In light of the analysis conducted in Section III-B, the characteristics of multiple IGBT OCFs in an HBSM or an FBSM from

TABLE VII
CHARACTERISTICS OF MULTIPLE IGBT OCFS IN AN HBSM OR AN FBSM FROM THE MODE-TYPE PERSPECTIVE

Combination	Polarity of the arm current	Affected mode	Mode type
T_{2F} and T_{3F}	Positive only	$II_F \rightarrow I_F$	D→C
		$III_F \rightarrow I_F$	B→C
		$IV_F \rightarrow I_F$	
T_{1F} and T_{4F}	Negative only	$V_F \rightarrow VI_F$	D→C
		$VII_F \rightarrow VI_F$	B→C
		$VIII_F \rightarrow VI_F$	

the mode-type perspective can be summarized as presented in Table VII.

C. Unified Characteristics of IGBT OCFs From the Mode-Type Perspective

According to Tables VI and VII, a unified characteristic can be summarized from the mode-type perspective, as shown in Fig. 5. Unified Characteristic I can be described as follows:

1) *Unified Characteristic I. 1:* For the affected Type B mode, the IGBT OCF causes its type to convert from B to C.
2) *Unified Characteristic I. 2:* For the affected Type D mode, the IGBT OCF causes its type to convert from D to B or C.

Unified characteristic I is applicable to all scenarios presented in Sections III-A and III-B.

IV. UNIFIED CHARACTERISTICS FROM THE SWITCHING-FUNCTION PERSPECTIVE

To offer a more lucid description of the impacts resulting from IGBT OCFs from the switching-function perspective, the characteristics of the switching function in normal SMs are initially introduced in this section.

A. Characteristics of Normal SMs From the Switching-Function Perspective

1) Regions I and III: In Region I, the SMs with relatively lower capacitor voltages are regulated to operate in Type C mode, whereas the SMs with relatively higher capacitor voltages are regulated to operate in Type B mode. During operation in Type C mode, the capacitor voltage of the SM increases. After a period of time, this SM becomes the one with a relatively higher capacitor voltage in the arm and is regulated to operate in Type B mode under the control of VBS. During the operation in Type B mode, the capacitor voltage of this SM remains unaltered. Once the SM becomes the one with relatively lower capacitor voltages in the arm, the SM is then regulated to operate in Type C mode. Therefore, the mode of a normal SM alternates between Type B mode and Type C mode in Region I, as illustrated in Fig. 6. Furthermore, the switching function of a normal SM also alternates between the switching functions that correspond to Type B mode and Type C mode in Region I.

In Region III, all HBSMs are bypassed, and only FBSMs are regulated under the control of the VBS. Therefore, the FBSMs with relatively lower capacitor voltages are regulated to operate in Type C mode, while the FBSMs with relatively higher capacitor voltages are regulated to operate in Type B mode in Region III. Similar to the analysis of Region I, the mode of a normal FBSM alternates between Type B mode and Type C mode in Region III, as illustrated in Fig. 6. Furthermore, the switching function of a normal FBSM also alternates between the switching functions that correspond to Type B mode and Type C mode in Region III.

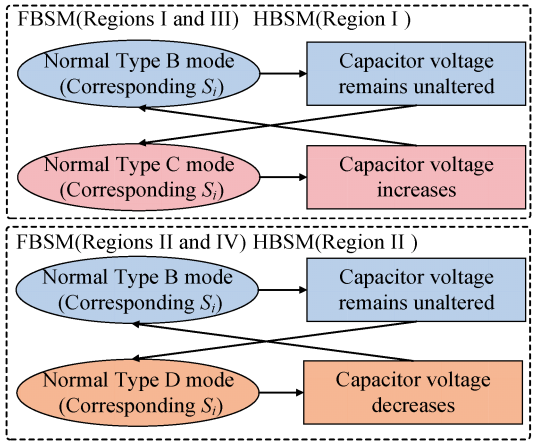

Fig. 6. Switching-function characteristics of normal SMs.

2) Regions II and IV: In Region II, the SMs with relatively higher capacitor voltages are regulated to operate in Type D mode, whereas the SMs with relatively lower capacitor voltages are regulated to operate in Type B mode. In Region IV, all HBSMs are bypassed, and only FBSMs are regulated under the control of the VBS.

Similar to the phenomena in Regions I and III, the mode of a normal FBSM alternates between Type B mode and Type D mode in Regions II and IV, as illustrated in Fig. 6. Furthermore, the switching function of a normal FBSM also alternates between the switching functions that correspond to Type B mode and Type D mode in Regions II and IV. Concerning the normal HBSM, its mode also undergoes a similar alternation between Type B mode and Type D mode during Region II, resulting in the switching function of a normal HBSM also alternating between the switching functions that correspond to Type B mode and Type D mode in Region II.

B. Characteristics of Single IGBT OCFs in an SM From the Switching-Function Perspective

1) Analysis of a Single IGBT OCF in an HBSM: As shown in Fig. 2, Mode III_H is only employed in Region II, which implies that the Position T_{1H} fault only exhibits fault characteristics in this particular region. Accordingly, the analysis of the characteristics of Position T_{1H} fault from the switching-function perspective is conducted in Region II. In the case of a Position T_{1H} faulty SM that initially operates in Mode IV_H, the faulty SM will be regulated to operate in Mode III_H after a period of time. This regulation occurs once the faulty SM attains a relatively higher capacitor voltage in the arm. Nevertheless, the

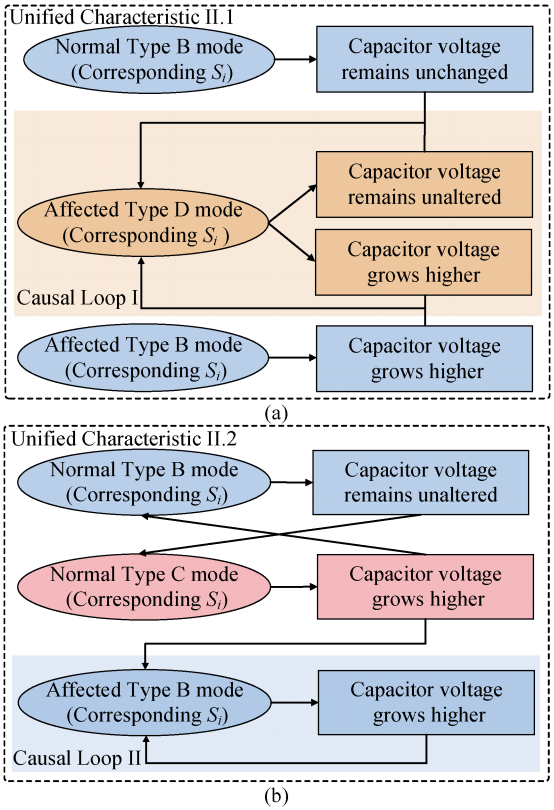

Fig. 7. Two causal loops in IGBT OCFs. (a) Causal Loop I. (b) Causal Loop II.

type conversion of the affected Mode III_H leads to the capacitor voltage of the faulty SM remaining unaltered, instead of decreasing as would be anticipated in the normal Mode III_H. Therefore, the capacitor voltage of the faulty SM remains relatively higher, thereby maintaining its operation in Mode III_H under the control of the VBS. Finally, a causal loop emerges as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Type D mode, as shown in Fig. 7(a). This causal loop compels the Position T_{1H} faulty SM to remain in the switching function corresponding to Mode III_H in Region II.

As shown in Fig. 2, Mode II_H is employed in Regions I and IV, indicating that the Position T_{2H} fault exhibits fault characteristics in these two regions. However, all HBSMs are compelled to operate in Mode II_H continuously in Region IV. Therefore, the analysis of the characteristics of the Position T_{2H} fault from the switching-function perspective is only conducted in Region I. In the case of a Position T_{2H} faulty SM that initially operates in Mode I_H, the faulty SM will be regulated to operate in Mode II_H after a period of time. This regulation occurs once the faulty SM attains a relatively higher capacitor voltage in the arm. Nevertheless, the type conversion of the affected Mode II_H leads to the capacitor voltage of the faulty SM increasing, instead of remaining unaltered as would be anticipated in the normal Mode II_H. Therefore, the capacitor voltage of the faulty SM remains relatively higher, thereby maintaining its operation in Mode II_H under the control of the VBS. Finally, a causal loop emerges as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Type B mode, as shown in Fig. 7(b). This causal loop compels the Position T_{2H} faulty SM to remain in the switching function corresponding to Mode II_H in Region I.

2) Analysis of a Single IGBT OCF in an FBSM: As shown in Fig. 2, Mode V_F is utilized in Region II, while Mode VII_F is utilized in Regions II and III. Thus, Position T_{1F} fault exhibits fault characteristics in Regions II and III. In the case of Region II, the Type Position T_{1F} faulty SM is invariably regulated to Mode V_F after a period of time, irrespective of the initial mode of the faulty SM, as illustrated in Fig. 7(a). This occurs when the faulty SM becomes the one with the relatively higher capacitor voltage in the arm. As with Position T_{1H} fault, Causal Loop I is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Mode V_F, as shown in Fig. 7(a). Causal Loop I compels the Type A_F faulty SM to remain in the switching function corresponding to Mode V_F in Region II. With respect to Region III, Position T_{1F} fault only affects Mode VII_F in this region. As illustrated in Fig. 7(b), the Position T_{1F} faulty SM is invariably regulated to Mode VII_F after a period of time, irrespective of the initial mode of the faulty SM. This occurs when the faulty SM becomes the one with the relatively higher capacitor voltage in the arm. As with the Type Position T_{2H} fault, Causal Loop II is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Mode VII_F, as shown in Fig. 7(b). Causal Loop II compels the Position T_{1F} faulty SM to remain in the switching function corresponding to Mode VII_F in Region III.

The analyses of Positions T_{2F}, T_{3F}, and T_{4F} faults are analogous to the previously conducted analysis of Position T_{1F} fault; thus, they are not repeated here. The characteristics of a single IGBT OCF in an FBSM from the switching-function perspective can be summarized, as presented in Table VII.

C. Characteristics of Multiple IGBT OCFs in an SM From the Switching-Function Perspective

1) Corresponding Arm Current Polarity: Positive: As shown in Fig. 2, Mode II_F is utilized in Region IV, while Modes III_F and IV_F are utilized in Region I and Region IV. Thus, the combination of Position T_2 fault and Position T_3 fault exhibits fault characteristics in Regions I and IV. In the case of Region I, both Modes III_F and IV_F are converted to Mode I_F. This indicates that the capacitor of the faulty SM can only be charged, which inevitably leads to its capacitor voltage being higher than that of the capacitor in a normal SM. As a result, the VBS controls the faulty SM to operate continuously in either Mode III_F or Mode IV_F. Specifically, which of these two modes the faulty SM operates continuously depends on the mode it initially entered. It is worth noting that this does not affect the conclusions of subsequent analyses, as the switching functions corresponding to the two modes are identical. As with the single Position T_{2H} fault, Causal Loop II is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Modes III_F and IV_F, as shown in

TABLE VIII
CHARACTERISTICS OF SINGLE IGBT OCFS IN AN HBSM OR AN FBSM FROM THE SWITCHING-FUNCTION PERSPECTIVE

Position	Region	Remaining mode	Causal loop	Switching function
T_{1H}	II	III_H	I	1
T_{2H}	I	II_H	II	0
T_{1F}	II	V_F	I	1
	III	VII_F	II	0
T_{2F}	I	IV_F	II	0
	IV	II_F	I	-1
T_{3F}	I	III_F	II	0
	IV	II_F	I	-1
T_{4F}	II	V_F	I	1
	III	$VIII_F$	II	0

Fig. 7(b). Causal Loop II compels the faulty SM with Position T_2 fault and Position T_3 fault to remain at 0 in Region I.

With respect to Region IV, Modes II_F, III_F, and IV_F are converted to Mode I_F. This indicates that the capacitor of the faulty SM can only be charged, which inevitably leads to its capacitor voltage being higher than that of the capacitor in a normal SM. As a result, the VBS controls the faulty SM to operate continuously in Mode II_F. As with the single Position T_{1H} fault, Causal Loop I is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Mode II_F, as shown in Fig. 7(a). Causal Loop I compels the faulty SM with Position T_2 fault and Position T_3 fault to remain in the switching function corresponding to Mode II_F in Region IV.

2) Corresponding Arm Current Polarity: Negative: As shown in Fig. 2, Mode V_F is utilized in Region II, while Modes VII_F and $VIII_F$ are utilized in Regions II and III. Thus, the combination of the Position T_{1F} fault and the Position T_{4F} fault exhibits fault characteristics in Regions II and III. In the case of Region II, Modes V_F, VII_F, and $VIII_F$ are all converted to Mode VI_F. As with the Position T_{2F} fault and the Position T_{3F} fault in Region IV, Causal Loop I is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Mode V_F, as shown in Fig. 7(a). Causal Loop I compels the faulty SM with the Position T_{1F} fault and the Position T_{4F} fault to remain in the switching function corresponding to Mode V_F in Region IV.

With respect to Region III, Modes VII_F and $VIII_F$ are both converted to Mode VI_F. As with the Position T_{2F} fault and the Position T_{3F} fault in Region I, Causal Loop II is generated as a consequence of a conflict between the operational logic of the VBS and the type conversion of the affected Modes VII_F and $VIII_F$, as shown in Fig. 7(b). Causal Loop II compels the faulty SM with the Position T_{1F} fault and the Position T_{4F} fault to remain at 0 in Region III.

3) Corresponding Arm Current Polarity: Positive and Negative: Based on the analysis in Section III-B, the fault characteristics presented for these five combinations under this scenario can be directly derived by superimposing the individual fault characteristics presented in Table VIII. As such, they are not elaborated upon further here.

TABLE IX
CHARACTERISTICS OF MULTIPLE IGBT OCFS IN AN HBSM OR AN FBSM FROM THE SWITCHING-FUNCTION PERSPECTIVE

Combination	Region	Remaining mode	Causal loop	Switching function
T_{2F} and T_{3F}	I	III_F/IV_F	II	0
	IV	II_F	I	-1
T_{1F} and T_{4F}	II	V_F	I	1
	III	$VII_F/VIII_F$	II	0

D. Unified Characteristics of IGBT OCFs From the Switching-Function Perspective

According to Tables VIII and IX, a unified characteristic can be summarized from the switching-function perspective, as shown in Fig. 7. Unified Characteristic II can be described as follows.

1) *Unified Characteristic II. 1:* In Regions II and IV, Causal Loop I is generated as a result of a conflict between the objective of the VBS and the type conversion of the affected Type D mode. Causal Loop I forces the malfunctioning SM to remain in the switching function corresponding to the affected Type D mode.
2) *Unified Characteristic II. 2:* In Regions I and III, Causal Loop II is generated as a result of a conflict between the objective of the VBS and the type conversion of the affected Type B mode. Causal Loop II forces the malfunctioning SM to remain in the switching function corresponding to the affected Type B mode.

Unified characteristic II is applicable to all scenarios presented in Section III-A and III-B.

V. UNIFIED CHARACTERISTICS-DRIVEN STRATEGY FOR DIAGNOSING IGBT OCFS IN HMMCS

In light of the summaries of Sections III-C and IV-D, it can be demonstrated that all scenarios of IGBT OCFs in HMMCs share some unified characteristics in terms of mode type and switching function, which provide a reliable theoretical basis for a unified diagnosis. Therefore, a unified characteristics-driven diagnostic strategy is proposed in this section. A detailed elaboration on its implementation and threshold selection is provided hereinafter.

A. Implementation of the Proposed Diagnostic Strategy

As demonstrated in Section IV, there are significant differences between the normal SM and the faulty SM when viewed from the switching-function perspective. Moreover, as can be observed from Tables VIII and IX, Regions I and II encompass all scenarios in which one or multiple IGBT OCFs occur in an HBSM or an FBSM. Therefore, the diagnosis only requires implementation in Regions I and II. In Region I, the switching function of a normal SM alternates between 0 and 1. In contrast, for a faulty HBSM with a Position T_{2H} fault, a faulty FBSM with at least one fault at either Position T_{2F} or Position T_{3F}, their switching functions remain at 0 in Region I. Furthermore, in the interval when its switching function remains at 0 in Region I, the capacitor voltage of the faulty SM increases due to the conversion of the mode type.

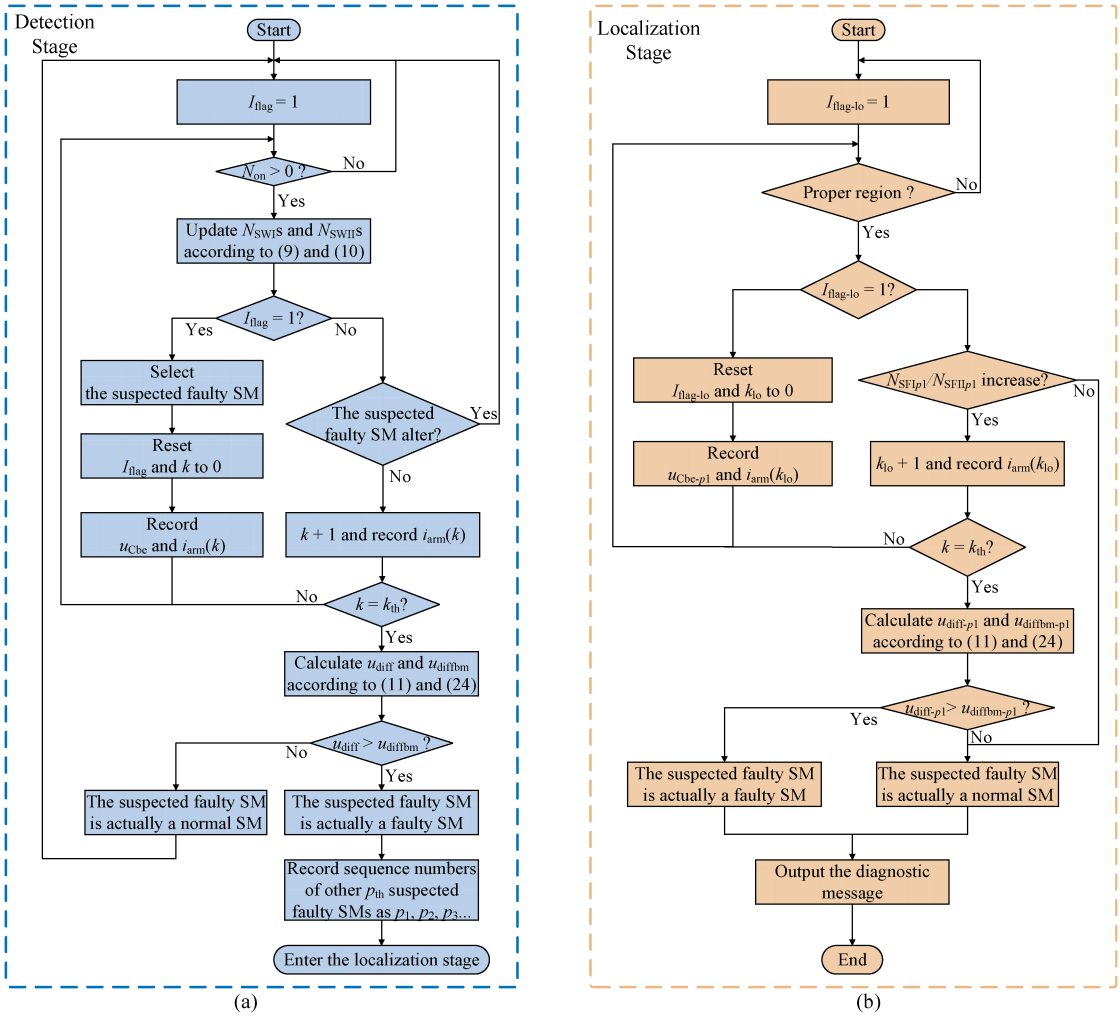

Fig. 8. Unified characteristics-driven diagnostic strategy proposed in this article. (a) Detection stage. (b) Localization stage.

In Region II, the switching function of a normal SM also alternates between 0 and 1. In contrast, for a faulty HBSM with a Position T_{1H} fault or a faulty FBSM with at least one fault at either Position T_{1F} or Position T_{4F}, their switching functions remain at 1 in Region II. Furthermore, in the period when its switching function remains at 1 in Region II, the capacitor voltage of the faulty SM increases or remains unaltered due to the conversion of the mode type.

Therefore, a unified characteristics-driven strategy can be proposed. The flowchart of this strategy is depicted in Fig. 8, where $N_{\mathrm{SFI}i}$ is defined as the number of control periods in which the switching function of the SM remains at 0 in Region I. Meanwhile, $N_{\mathrm{SFII}i}$ is defined as the number of control periods during which the switching function of the SM remains at 1 in Region II. The updates of $N_{\mathrm{SFI}i}$ and $N_{\mathrm{SFII}i}$ comply with the following two equations:

$$N_{\mathrm{SFI}i} = \begin{cases} N_{\mathrm{SFI}i} + 1, \ S_i = 0 \text{ in Region I} \\ 0, \ \text{other cases} \end{cases} \tag{10}$$

$$N_{\mathrm{SFII}i} = \begin{cases} N_{\mathrm{SFII}i} + 1, \ S_i = 1 \text{ in Region II} \\ 0, \ \text{other cases.} \end{cases} \tag{11}$$

I_{flag} denotes the initial flag. k and k_{th} represent the counting flag and the corresponding threshold, respectively. u_{diff} represents the actual difference in the capacitor voltage of the suspected faulty SM before and after its switching function remains at a specific value in a specific region for kth control periods, while u_{diffbm} represents the corresponding benchmark. p_{th} represents the number of suspected faulty SMs screened after the detection stage detects an IGBT OCF. The subscript of "lo" is used to distinguish variables with the same meaning utilized in the detection stage and the localization stage.

As shown in Fig. 8, the proposed strategy is divided into a detection stage and a localization stage. Given that the implementations of the proposed strategy are near-identical in Regions I and II, the implementation in Region I is chosen as an example to clarify how the proposed strategy works.

The implementation of the detection stage is shown in Fig. 8(a). When I_{flag} equals 1, the SM corresponding to N_{SFImax} is selected as the suspected faulty SM. Here, N_{SFImax} represents the maximum values of N_{SFI}s in the arm. Subsequently, both

k and I_{flag} are reset to 0. Meanwhile, the capacitor voltage of the suspected faulty SM and the arm current are recorded. The initialization process is not re-executed unless k attains kth or the suspected faulty SM alters. The assessment of whether the suspected faulty SM has been altered can be accomplished by judging whether there is an increase in N_{SFImax}.

If the suspected faulty SM is actually a normal SM, then its capacitor will remain in a bypassed state during the period when its switching function remains at 0. Accordingly, the capacitor voltage of the suspected SM will remain unaltered during the process of k reaching k_{th}. Therefore, u_{diff} will equal 0. However, if the suspected faulty SM is indeed a faulty SM, then its capacitor will remain in a charging state due to the type conversion during the period when its switching function remains at 0. Accordingly, the capacitor voltage of the suspected SM will increase continuously during the process of k reaching k_{th}. Therefore, u_{diff} will be larger than that in the case where the suspected faulty SM is normal and exceeds the selected value of u_{diffbm}. Once a suspected faulty SM is confirmed as a faulty SM in the detection stage, SMs with the 2nd to (p_{th}+1)th largest $N_{\text{SFI}i}$ are selected as other p_{th} suspected faulty SMs. The basis for such selection is that SMs with larger $N_{\text{SFI}i}$ are more likely to be faulty SMs. Subsequently, the localization stage is activated to determine the status of the recorded other suspected faulty SMs.

The implementation of the localization stage is shown in Fig. 8(b). Since the IGBT OCF has been detected in Region I during the detection stage, the objective of the localization stage is to determine whether the p_{th} other suspected faulty SMs have included Positions T_{2H}, T_{2F}, or T_{3F} faults. The principle for determination is analogous to that of the detection stage. A suspected SM is confirmed as a faulty SM only if its switching function remains at 0 for the $k_{\text{th-lo}}$ control periods and the alternation in its capacitor voltage exceeds the threshold during the duration. Otherwise, the suspected SM is confirmed as a normal SM. The determination of the p_{th} suspected faulty SMs is carried out in parallel in the localization stage. Therefore, it takes at most $k_{\text{th-lo}}$ control periods to complete the judgement of all p_{th} suspected faulty SMs.

In addition, it should be noted that the proposed diagnostic strategy remains effective when two IGBT OCFs with opposite current polarities occur simultaneously in a single SM, as described in Sections III-B and IV-B. A typical scenario is the concurrent occurrence of Position T_{1H} fault and Position T_{2H} fault in an HBSM. Specifically, due to their opposite current polarities, only one fault manifests its fault characteristic at any given moment. Thus, if the system first enters Region I after the fault occurs, then the diagnostic process is consistent with that of an individual Position T_{2H} fault; while if the system first enters Region II, then the diagnostic process aligns with that of an individual Position T_{1H} fault.

As demonstrated in the preceding analysis, it is evident that the proposed diagnostic strategy has the capacity to identify up to (p_{th}+1) faulty SMs during a complete execution process. This capability enables the strategy to manage scenarios in which multiple SMs occur IGBT OCFs concurrently.

B. Threshold Selection of the Proposed Diagnostic Strategy

As shown in Fig. 8, the implementation of the proposed diagnostic strategy involves three distinct thresholds. These three thresholds are k_{th}, u_{diffbm}, and p_{th}. The following section elucidates the selections of these thresholds.

1) Selection of k_{th}: k_{th} denotes the duration of the suspected faulty SM determination process. For the convenience of the subsequent analysis, it is assumed that the accuracy level of the voltage sensor used in the SM is x%, and the true value of the capacitor voltage of the SM is u_{Creal} when k equals 0. Since the settings of the k_{th} are near-identical in Regions I and II, Region II is chosen as an example to clarify how to select the k_{th}.

If the suspected SM is actually a normal SM, then its capacitor will remain in a discharging state during the duration when its switching function remains at 1. Therefore, the true value of its capacitor voltage decreases Δu_{C}. The variation of the capacitor voltage during this duration can be expressed as the following equation:

$$u_{\text{diff}} = u_{\text{Caf}} - u_{\text{Cbe}} \tag{12}$$

where u_{Caf} and u_{Cbe} represent the measured values of the capacitor voltage of the suspected faulty SM when k equals k_{th} and 0, respectively.

After taking into account the influence of the sensor accuracy, the ranges of u_{Caf} and u_{Cbe} can be expressed as

$$u_{\text{Creal}}(1-x\%) \le u_{\text{Cbe}} \le u_{\text{Creal}}(1+x\%) \tag{13}$$

$$(u_{\text{Creal}} - \Delta u_{\text{C}})(1-x\%) \le u_{\text{Caf}} \le (u_{\text{Creal}} - \Delta u_{\text{C}})(1+x\%). \tag{14}$$

Considering the most extreme case, the maximum value of u_{diff} can be expressed as

$$u_{\text{diff - normax}} = -\Delta u_{\text{C}}(1+x\%) + 2u_{\text{Creal}}x\% \tag{15}$$

where $u_{\text{diff-normax}}$ represents the maximum value of u_{diff} when the suspected faulty SM is normal.

If the suspected SM is indeed faulty, then its capacitor will remain in a charging state or a bypassed state due to the type conversion during the duration when its switching function remains at 1. Therefore, the true value of its capacitor voltage increases Δu_{C} or remains unaltered. In this sense, the range of u_{Caf} can be expressed as

$$\begin{cases} u_{\text{Creal}}(1-x\%) \le u_{\text{Caf}} \le u_{\text{Creal}}(1+x\%), \text{bypassed} \\ (u_{\text{Creal}} + \Delta u_{\text{C}})(1-x\%) \le u_{\text{Caf}} \le (u_{\text{Creal}} + \Delta u_{\text{C}})(1+x\%), \text{charging} \end{cases}. \tag{16}$$

It is obvious that the minimum value in the bypassed state of u_{diff} is lower than that in the charging state, indicating that the bypassed state dominates the threshold setting. Subsequently, considering the most extreme case, the minimum value of u_{diff} can be expressed as follows:

$$u_{\text{diff - faumin}} = -2u_{\text{Creal}}x\% \tag{17}$$

where $u_{\text{diff-faumin}}$ represents the minimum value of u_{diff} when the suspected faulty SM is a faulty SM. To ensure that the proposed diagnostic strategy can correctly determine the status

of the suspected faulty SM, the following conditions need to be satisfied simultaneously:

$$\begin{cases}\text{Condition I: } u_{\text{diff - faumin}} > u_{\text{diff - normax}} \\ \text{Condition II:} u_{\text{diff - normax}} < u_{\text{diffbm}} < u_{\text{diff - faumin}}.\end{cases} \tag{18}$$

From (18), it can be seen that the smaller the $u_{\text{diff-normax}}$, the more favorable it is for meeting both conditions. Since Δu_{C} represents the decrease of the true value in the capacitor voltage, it can also be expressed as follows:

$$\Delta u_{\text{C}} = -\frac{1}{C}\int_0^{k_{\text{th}}T_{\text{c}}} i_{\text{arm}} dt \tag{19}$$

where C denotes the capacitance of the SM capacitor. T_{c} represents the control period. Combining (15) and (19), it can be observed that as k_{th} increases, $u_{\text{diff-normax}}$ decreases. Therefore, from the perspective of the proposed diagnostic strategy's effectiveness, the larger the value of k_{th}, the better it is. However, as k_{th} increases, the duration of the confirmation process also lengthens. Therefore, the final principle for the selection of k_{th} is to minimize it as much as possible while ensuring the effectiveness of the proposed diagnostic strategy.

As shown in (18), to facilitate the selection of u_{diffbm}, a certain margin should be maintained between its upper and lower limits. Accordingly, $u_{\text{diff-normax}}$ is set equal to twice the value of $u_{\text{diff-faumin}}$. According to (15) and (17), Δu_{C} can be expressed as

$$\Delta u_{\text{C}} = \frac{6u_{\text{Creal}}x\%}{1+x\%}. \tag{20}$$

To simplify the calculation, the instantaneous value of the arm current is replaced with its average value, and (19) can be simplified as follows:

$$\Delta u_{\text{C}} = -\frac{k_{\text{th}}T_{\text{c}}}{C} i_{\text{arm - ave}}. \tag{21}$$

Combining (20) and (21), k_{th} can be selected as follows:

$$k_{\text{th}} = -\frac{6u_{\text{Creal}}x\%C}{(1+x\%)T_{\text{C}}i_{\text{arm - ave}}}. \tag{22}$$

Given that the SM capacitor voltage generally fluctuates around its rated value, u_{Creal} in (22) can be replaced by the rated value of the SM capacitor voltage. Typically, $x\%$ is an extremely small value; therefore, $(1+x\%)$ can be approximated as 1. Moreover, k_{th} should be a positive integer. Therefore, (22) can be further simplified as follows:

$$k_{\text{th}} = \left\lfloor -\frac{6u_{\text{Crate}}x\%C}{T_{\text{C}}i_{\text{arm - ave}}} \right\rfloor + 1 \tag{23}$$

where u_{Crate} denotes the rated value of the SM capacitor voltage.

As demonstrated in (23), in scenarios where $i_{\text{arm-ave}}$ is substantial, the value of k_{th} is minimal. This phenomenon may result in the recurrent determination of the suspected faulty SM, thereby incurring unnecessary expenditures of resources. To avoid this phenomenon, a lower limit can be manually selected for k_{th}. Consequently, (23) can be finally optimized as follows:

$$k_{\text{th}} = \max\left(\left\lfloor -\frac{6u_{\text{Crate}}x\%C}{T_{\text{C}}i_{\text{arm - ave}}} \right\rfloor + 1, k_{\text{th - lowerlimit}}\right) \tag{24}$$

where $k_{\text{th-lowerlimit}}$ represents the lower limit for k_{th}. In (24), parameters, such as u_{Crate}, $x\%$, and T_{C}, are system-dependent and thus require reconfiguration when deployed in different systems.

2) Selection of u_{diffbm}: u_{diffbm} is employed to ascertain the status of the suspected faulty SM. According to Condition II and the above analysis, the feasible region of u_{diffbm} can be further expressed as

$$\frac{1}{3}\Delta u_{\text{C}} < u_{\text{diffbm}} < \frac{2}{3}\Delta u_{\text{C}}. \tag{25}$$

To ensure that u_{diffbm} lies within a reasonable margin relative to the upper and lower bounds in (25), u_{diffbm} is chosen as the midpoint of its feasible region, expressed as

$$u_{\text{diffbm}} = \frac{1}{2}\Delta u_{\text{C}} = \frac{1}{2C}\int_0^{k_{\text{th}}T_{\text{c}}} i_{\text{arm}} dt. \tag{26}$$

According to the trapezoidal integral formula, (26) can be further expressed as

$$u_{\text{diffbm}} = \frac{T_{\text{c}}}{2C}\sum_{m=0}^{m=k_{\text{th}}-1}\frac{i_{\text{arm}}(m)+i_{\text{arm}}(m+1)}{2}. \tag{27}$$

As shown in (27), only T_{C} is system-dependent. Thus, when the proposed diagnostic strategy is deployed to different systems, only T_{C} requires reconfiguration.

3) Selection of p_{th}: p_{th} represents the number of suspected faulty SMs that are selected after an IGBT OCF is detected during the detection stage. According to the analysis in Section V-A, during a complete implementation process of the proposed diagnostic strategy, at most $(p_{\text{th}}+1)$ faulty SMs can be handled. According to [12], [19], and [24], in practical applications, the number of SMs with simultaneous IGBT OCFs is related to the number of SMs in the arm and is typically not large. When the number of SMs in the arm is relatively large, p_{th} can be appropriately increased.

In this article, p_{th} is selected as three. In this sense, the proposed diagnostic strategy can diagnose a maximum of four faulty SMs in one complete execution.

VI. Further Discussion of the Proposed Diagnostic Strategy

A. Performance of the Proposed Diagnostic Strategy for Identifying the Specific Faulty IGBT Within Faulty SMs

After accounting for scenarios involving simultaneous multiple IGBT OCFs within a single SM, the proposed diagnostic strategy can only identify a subset of the faulty IGBTs, while remaining unable to identify other potentially faulty ones. The detailed analysis is as follows.

When the proposed diagnostic strategy localizes a faulty HBSM in Region I, the only obtainable information is that the T_2 of this HBSM has occurred an OCF. However, since Position T_{2H} fault does not exhibit fault characteristics in Region I and fault isolation is executed immediately upon completion of diagnosis, the status of the T_1 within the same HBSM cannot be further determined. Similarly, the information obtained from

TABLE X
INFORMATION OBTAINED FROM THE DIAGNOSTIC STRATEGY UNDER ALL SCENARIOS

SM Type	Region	Information	
HBSM	I	T_1 OCF	T_2 OCF
		Unknown	Certain
	II	T_1 OCF	T_2 OCF
		Certain	Unknown
FBSM	I	T_1 OCF/T_4 OCF	T_2 OCF/T_3 OCF
		Unknown	At least one
FBSM	II	T_1 OCF/T_4 OCF	T_2 OCF/T_3 OCF
		At least one	Unknown

the proposed diagnostic strategy under other scenarios can be derived through the same logic, as summarized in Table X.

It should be noted that both fault isolation and fault reconfiguration after fault diagnosis only require identification of the faulty SMs, without the need for precise localization to the specific faulty IGBT. Thus, identifying the exact faulty IGBT is not a primary or necessary objective of the existing diagnostic strategies [10], [11], [12], [13], [19], [22], [30]. In this sense, the focus is on detecting and localizing faulty SMs.

B. Performance of the Proposed Diagnostic Strategy Under Transient Conditions

1) Performance Under Load Changes: As indicated in Section V-A, the suspected faulty SM is selected based on the unified characteristics from a switching-function perspective. Subsequently, the status of the suspected faulty SM can be further determined based on the unified characteristics from the mode-type perspective.

As Section III shows, Unified Characteristics I derived from the mode-type perspective relate only to flow paths within the SM during the analysis. This means that the characteristics are established at the topological level of the SM and are independent of external operating conditions. This indicates that, even if a suspected faulty SM is selected during the detection stage, the proposed diagnostic strategy can correctly determine its status under load changes. Therefore, the proposed diagnostic strategy is immune to load changes.

2) Performance Under DC Faults: According to [4], [9], and [32], the HMMC has the ability to actively ride through dc faults and operates under conditions equivalent to zero dc voltage conditions during the ride-through process.

As is the case with the aforementioned analysis of load changes, the unified characteristics derived from the mode-type perspective also remain unaffected under load changes, as the flow paths within the SM do not change during dc faults. This finding indicates that under dc faults, even if selected as a suspected faulty SM during the detection stage, the proposed diagnostic strategy can correctly determine its status. Hence, the proposed diagnostic strategy has immunity to dc faults.

C. Impact of the IGBT Switching Frequency on the Performance of the Proposed Diagnostic Strategy

For an SM with an IGBT OCF that can be effectively diagnosed by the proposed diagnostic strategy, the entire process from fault occurrence to final diagnosis can be divided into three stages, as shown in Fig. 9. t_0, t_1, t_2, and t_3 denote the times at which the IGBT OCF occurs, the switching function of the faulty SM starts to remain at a specific value, the faulty SM is selected as a suspected faulty SM, and it is identified as a faulty SM by the proposed diagnostic strategy, respectively.

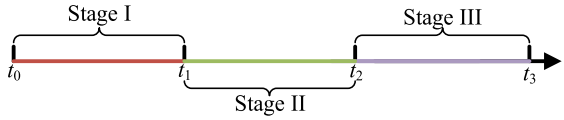

Fig. 9. Entire process from fault occurrence to final diagnosis.

The duration of Stage I is related to two factors: the initial operating mode of the faulty SM and the IGBT switching frequency. To make the analysis process more intuitive and understandable, the position T_{1H} fault is utilized as an example. When a Position T_{1H} fault occurs, if the initial operating mode of the faulty SM is Mode IV_H, it must switch to Mode III_H before exhibiting fault characteristics. As indicated in Section IV-A, the transition of the faulty SM's operating mode is inevitable. During this mode transition, T_1 switches from the OFF state to the ON state, which means that this IGBT is turned ON once. In MMC systems, the IGBT switching frequency is defined as the number of times an IGBT is turned ON per second [33]. Therefore, the duration of Stage I is influenced by the IGBT switching frequency as follows:

$$t_{\text{StageI}} = \frac{1}{f_{\text{sw}}} \tag{28}$$

where t_{StageI} represents the duration of Stage I. f_{sw} represents the IGBT switching frequency. According to (28), when the IGBT switching frequency is low, the duration of Stage I increases to some extent.

The effect of IGBT switching frequency on Stage II is similar to that on Stage I. As indicated in Section V-A, the proposed diagnostic strategy only selects this faulty SM as a suspected faulty SM once its $N_{\text{SWII}i}$ reaches the maximum value within the arm. For a normal SM, the maximum $N_{\text{SWII}i}$ can be expressed as follows:

$$N_{\text{SWII}i\text{ - normax}} = \frac{1}{f_{\text{sw}} T_{\text{C}}} \tag{29}$$

where T_{C} represents the control period. Therefore, the duration of Stage II can be expressed as

$$t_{\text{StageII}} = \frac{1}{f_{\text{sw}}}. \tag{30}$$

From (30), it is evident that when the IGBT switching frequency is low, the duration of Stage II increases to a certain extent. Furthermore, similar to Stage I, it is also inevitable that the $N_{\text{SWII}i}$ of the faulty SM becomes the maximum one in the arm.

As analyzed in Section V, the duration of Stage III solely depends on the values of k_{th} and $k_{\text{th-lo}}$, which are both independent of the IGBT switching frequency. Therefore, Stage III is not impacted by the IGBT switching frequency.

TABLE XI
COMPARISON WITH RECENT DIAGNOSTIC STRATEGIES

Literature	Category	Main method	Research object	Detection Accuracy	Diagnosis Time	Extra cost	IGBT OCFs in Multiple SMs	Multiple IGBT OCFs in an SM	Applicability
[20]	Hardware-based	Rearranged bleeding resistor circuit	HBMMC	Moderate	<20ms	Yes	Yes (in parallel)	No discussion	Direct
[21]		SM voltage sensor reconfiguration	HBMMC	Low	<20ms	Yes	Yes (in parallel)	Yes (HBSM only)	Direct
[22]	AI-based	Improved *K*-means algorithm	HBMMC	High	<20ms	No	Yes (in sequence)	No discussion	Readjustment
[29]		LSTM network	FBMMC	High	<20ms	No	Yes (in sequence)	No discussion	Readjustment
[19]	Model-based	Amending Kalman Filter	HBMMC	Moderate	<20ms	No	Yes (in parallel)	No discussion	Direct
[24]		Signal synthesis technique	HBMMC	Moderate	<20ms	No	Yes (in sequence)	No discussion	Readjustment
[25]		Forward Euler method	HBMMC	Moderate	<20ms	No	Yes (in parallel)	No discussion	Direct
[26]		Repetitive signal generator	HBMMC	Low	<20ms	No	No	No discussion	Readjustment
[30]		Switching sequence	HMMC (Separate)	Moderate	<20ms	No	Yes (in parallel)	No discussion	Direct
Proposed		**Mode-type and switching-function perspectives**	**HMMC (Unified)**	**Moderate**	**<20ms**	**No**	**Yes (in sequence)**	**Yes**	**Direct**

In summary, the IGBT switching frequency does not affect the effectiveness of the proposed diagnostic strategy, but it does influence the duration of Stages I and II, thereby affecting the diagnostic speed to some extent. Specifically, the lower the IGBT switching frequency, the longer the theoretical diagnostic time required for the faulty SM. Furthermore, when the theoretical duration of the entire diagnostic process approaches or exceeds that of either Region I or Region II, the proposed strategy may be unable to complete the diagnosis within a single power frequency period. Therefore, the proposed diagnostic strategy is not recommended for application in scenarios with excessively low IGBT switching frequencies, as with the diagnostic strategy proposed in [30].

TABLE XII
PARAMETERS OF THE HMMC

Parameters	Value
AC side voltage	290 kV
AC side voltage frequency	50 Hz
DC side voltage	400 kV
Rated active power	750 MW
N_F	160
N_H	84
Arm inductance	0.1 H
SM capacitance	8 mF

VII. COMPARISON BETWEEN THE PROPOSED DIAGNOSTIC STRATEGY AND EXISTING DIAGNOSTIC STRATEGIES

To demonstrate the superiority of the proposed diagnostic strategy and highlight the contributions of this article, several recent diagnostic strategies for IGBT OCFs of MMCs are selected as objects of comparison for the proposed diagnostic strategy. The comparison results are presented in Table XI .

Compared with the hardware-based strategies and the AI-based strategies, the model-based strategies not only do not need extra hardware circuits but also do not rely on complex AI algorithms, which are more appropriate for high-voltage scenarios.

The detection accuracy is qualitatively compared on three levels: high, moderate, and low. Although the proposed strategy exhibits lower detection accuracy than AI-based strategies, it has undergone thorough evaluation with nonideal factors considered during threshold selection, thereby achieving a relatively reliable option. Furthermore, the interpretability of deep learning-based diagnostic strategies is generally low, and the unified characteristics summarized in this article can partially offset this shortcoming. With regard to the time required for diagnosis, the performance of the proposed strategy is comparable to that of other strategies. It should be emphasized that the switching functions, arm currents, and capacitor voltages required by the proposed diagnostic strategy are all inherent to the existing control architectures of the MMC. Therefore, no additional measurement or hardware components are needed, thus incurring no extra costs. Moreover, the proposed diagnostic strategy is applicable to both scenarios where IGBT OCFs occur simultaneously across multiple SMs and scenarios where multiple IGBT OCFs occur simultaneously within a single SM. The performance characteristics of the latter have rarely been investigated in existing studies on the HBMMC. Furthermore, the proposed diagnostic strategy can be directly applied to various MMC operating conditions without readjustments, which

is attributed to the fact that the unified characteristics leveraged by the strategy are derived from the two SM topologies and the VBS control logic and are independent of specific MMC operating conditions.

The most significant distinction between the proposed diagnostic strategy and the existing ones pertains to the research objects. In the existing diagnostic strategies, the majority of their research objects are HBMMCs, and these strategies generally cannot be directly applied to the scenarios of HMMCs. There are mainly two restrictive factors.

The first restrictive factor is attributed to the differences in the topological structures between the FBSM and the HBSM, along with the resultant disparities in the characteristics of IGBT OCFs. As indicated in Table VI, compared with the HBSM, the characteristics of IGBT OCFs in the FBSM are much more complex. Due to the differences in fault characteristics, when the analysis of IGBT OCF characteristics in FBSMs is lacking, existing diagnostic strategies that take the HBMMC as the research object cannot be generalized to the HMMC. A typical case is that the diagnostic strategies in [19] and [25] require the influence of IGBT OCFs on the SM capacitor voltages. Unified Characteristic I derived from the mode-type perspective provides the possibility for applying these two strategies to the scenarios of HMMCs. In addition, these two strategies both need to be applied to all SMs in the arm. The analysis conclusions based on the switching-function perspective in this study can help to narrow down their diagnostic scopes.

The second restrictive factor is that in HMMCs, the operating principles of the FBSM and the HBSM are not symmetric. Consequently, certain conclusions derived from HBMMC may not be applicable to HMMC. For instance, in [22], [25], and [29], the localization of the faulty SM is based on the criterion that there is a significant deviation between the capacitor voltages of the normal SM and the faulty SM. However, a significant deviation can also occur between normal SMs in the HMMC. This phenomenon has been elaborated in detail in [34]. If this phenomenon is not given consideration, it can result in the erroneous diagnosis of existing strategies.

The strategy proposed in [30] necessitates being implemented separately for FBSMs and HBSMs, consequently engendering a relatively complex execution process and numerous threshold parameters. This can be avoided based on the dual-perspective analysis conducted in this article.

In summary, the diagnostic strategy proposed in this article boasts performance comparable to that of other existing diagnostic strategies. More importantly, it achieves a unified diagnosis of IGBT OCFs in HMMCs, which is a feat that existing strategies fail to accomplish. Furthermore, the two unified characteristics revealed through the dual-perspective analysis in this article can provide a theoretical foundation and opportunities to expand some existing strategies to the context of the HMMC, thereby further optimizing their performance.

VIII. Experimental Verification

To prove the effectiveness of the proposed unified characteristics-driven strategy, a HIL platform is constructed,

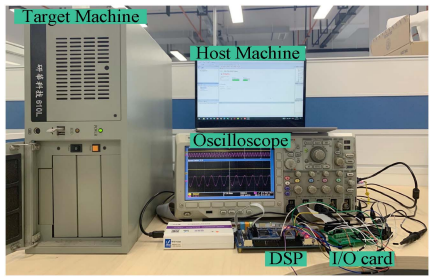

Fig. 10. Configurations of the HIL platform.

TABLE XIII
Experimental Scenarios

Scenario	Fault
I	IGBT OCFs occur simultaneously in three SMs: A Position T_{1H} fault occurs in $HBSM_1$, a Position T_{1F} fault occurs in $FBSM_1$, and a Position T_{4F} fault occurs in $FBSM_4$.
II	IGBT OCFs occur simultaneously in three SMs: A Position T_{2H} fault occurs in $HBSM_2$, a Position T_{2F} fault occurs in $FBSM_2$, and a Position T_{3F} fault occurs in $FBSM_3$.
III	IGBT OCFs occur simultaneously in an SM: A Position T_{1F} fault and a Position T_{4F} fault occur in $FBSM_4$
IV	IGBT OCFs occur simultaneously in an SM: A Position T_{2F} fault and a Position T_{3F} fault occur in $FBSM_2$

as shown in Fig. 10. Therein, the model of an HMMC in Fig. 1 is built and compiled on the host machine. Subsequently, it is downloaded to the target machine for real-time simulation. The conversion and communication of the signals between the target machine and the DSP control board are facilitated by an I/O card. The experimental waveforms can be observed in real time by the oscilloscope. Table IX lists the parameters of the HMMC.

A. Verification of the Proposed Diagnostic Strategy

To validate the effectiveness of the proposed diagnostic strategy, two typical scenarios are considered: one where simultaneous IGBT OCFs occur in multiple SMs, and the other where simultaneous multiple IGBT OCFs occur in a single SM. Therefore, four experimental scenarios are meticulously designed in accordance with Section IV, and the specific contents are listed in Table XIII. The $k_{\text{th-lowerlimit}}$ in (22) is selected as 10 in this article empirically. According to [12], [25], and [30], the $x\%$ is selected as 0.2% in this article, which is a mainstream for voltage sensors in practical applications.

1) Scenario I: Experimental waveforms of Scenario I are in Fig. 11. For a better display of the SM capacitor voltage in the oscilloscope, the dc bias U_{dc}/N is subtracted from the SM capacitor voltage. D_{flag} and D_{num} represent the flag of diagnostic completion and the number of faulty SMs, respectively. D_{SN1}, D_{SN2}, and D_{SN3} represent the sequence numbers of faulty SMs. To prevent confusion between the sequence numbers of FBSMs and HBSMs, 0.5 is added to the sequence number of the faulty SM if it is an HBSM.

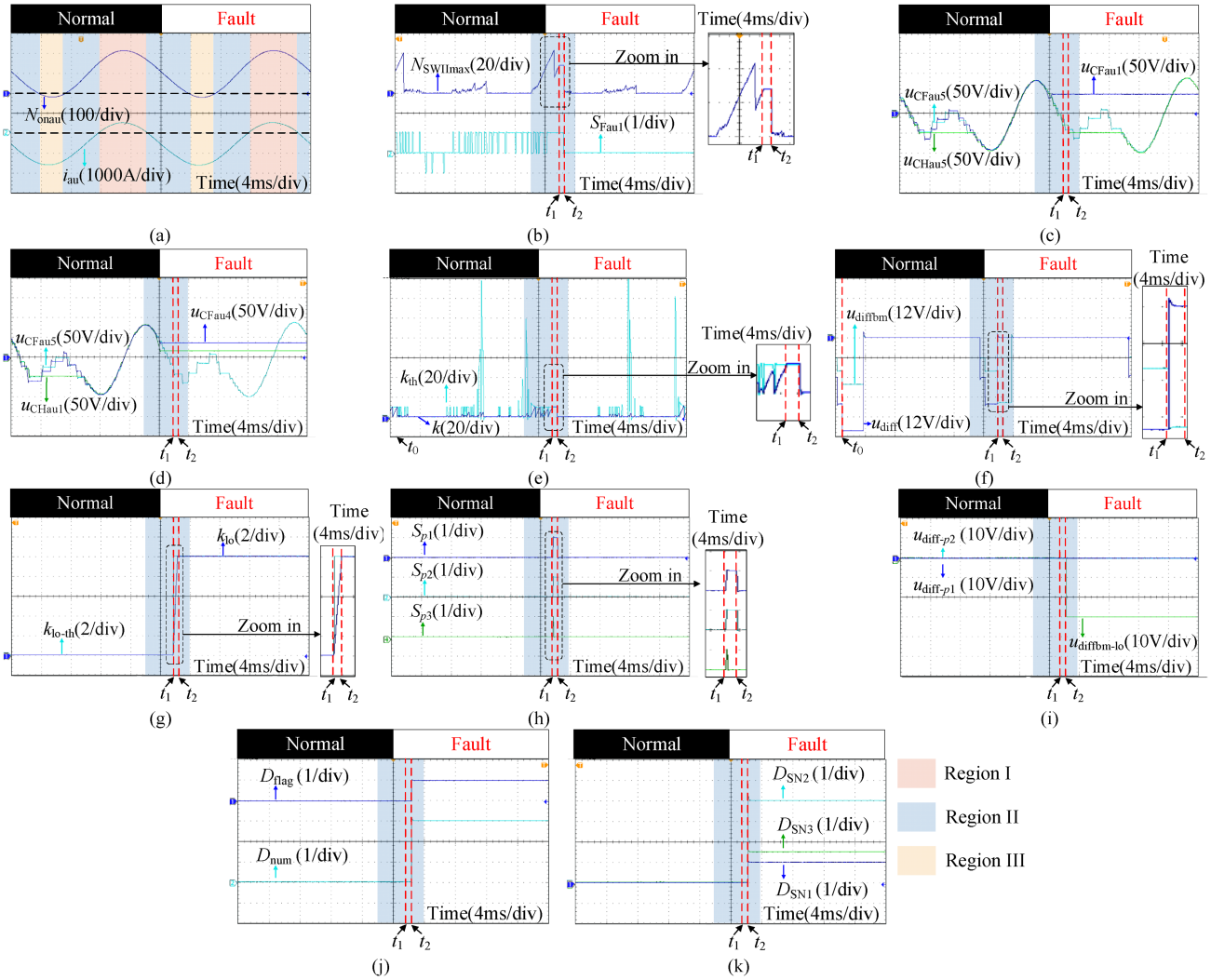

Fig. 11. Experimental waveforms of Scenario I. (a) Arm current and number of inserted SMs. (b) SM switching function and maximum value of N_{SFII}s. (c) SM capacitor voltages of FBSM_1, FBSM_5, and HBSM_5. (d) SM capacitor voltages of FBSM_4, FBSM_5, and HBSM_1. (e) Counting flag and corresponding threshold in the detection stage. (f) Alternation in the capacitor voltage and corresponding threshold in the detection stage. (g) Counting flag and corresponding threshold in the localization stage. (h) Switching functions of three potentially faulty SMs. (i) Alternation in the capacitor voltage and corresponding threshold in the localization stage. (j) Completion flag and number of faulty SMs. (k) Sequence numbers of faulty SMs.

At the moment t_0, k reaches k_{th} and u_{diff} is smaller than u_{diffbm}, indicating that the suspected faulty SM is actually a normal SM. This confirms that selecting thresholds according to the principles in Section V-B can effectively prevent misdiagnosis. As shown in Fig. 11(a), IGBT OCFs occur simultaneously in three SMs during Region II. Therefore, fault characteristics of Position $\mathrm{T}_{1\mathrm{H}}$, Position $\mathrm{T}_{1\mathrm{F}}$, and Position $\mathrm{T}_{4\mathrm{F}}$ faults can all be immediately exhibited. As shown in Fig. 11(b), the switching function of the faulty SM remains at 1 in Region II, which is consistent with the previous analysis in Section IV. Accordingly, N_{SFII} of the FBSM_1 continuously increases, quickly becomes the max N_{SFII}, and is then selected as the faulty SM. As shown in Fig. 11(b), N_{SFIImax} continuously increases, which implies that the suspected faulty SM does not alter. Moreover, due to the conversion of the mode type, the capacitor voltage of all three faulty SMs remains unaltered in the interval when its switching function remains at 1 in Region II, as shown in Fig. 11(c) and (d). At the moment t_1, k reaches k_{th} and u_{diff} exceeds u_{diffbm}, indicating the suspected faulty SM is indeed a faulty SM, as shown in Fig. 11(e) and (f). Then, SMs with the 2nd to 4th largest $N_{\mathrm{SFII}i}$ are selected as three suspected faulty SMs, whose statuses are determined in the following localization stage.

In the localization stage, k_{lo} increases and reaches $k_{\mathrm{lo\text{-}th}}$ at the moment t_2, as shown in Fig. 11(g). As shown in Fig. 11(h), during the duration from t_1 to t_2, S_{p3} does not remain at 1 consistently, indicating that it is a normal SM. However, S_{p1} and S_{p2} remain at 1 during this duration. As shown in Fig. 11(i), both $u_{\mathrm{diff\text{-}p1}}$ and $u_{\mathrm{diff\text{-}p2}}$ exceed $u_{\mathrm{diffbm\text{-}lo}}$ at the moment t_2, indicating these two suspected faulty SMs are indeed faulty SMs. As shown in Fig. 11(j) and (k), both the number of faulty SMs and the sequence numbers of the corresponding three faulty SMs can be output correctly. Subsequently, the bypass switches in the three faulty SMs are closed to complete the fault isolation, and their

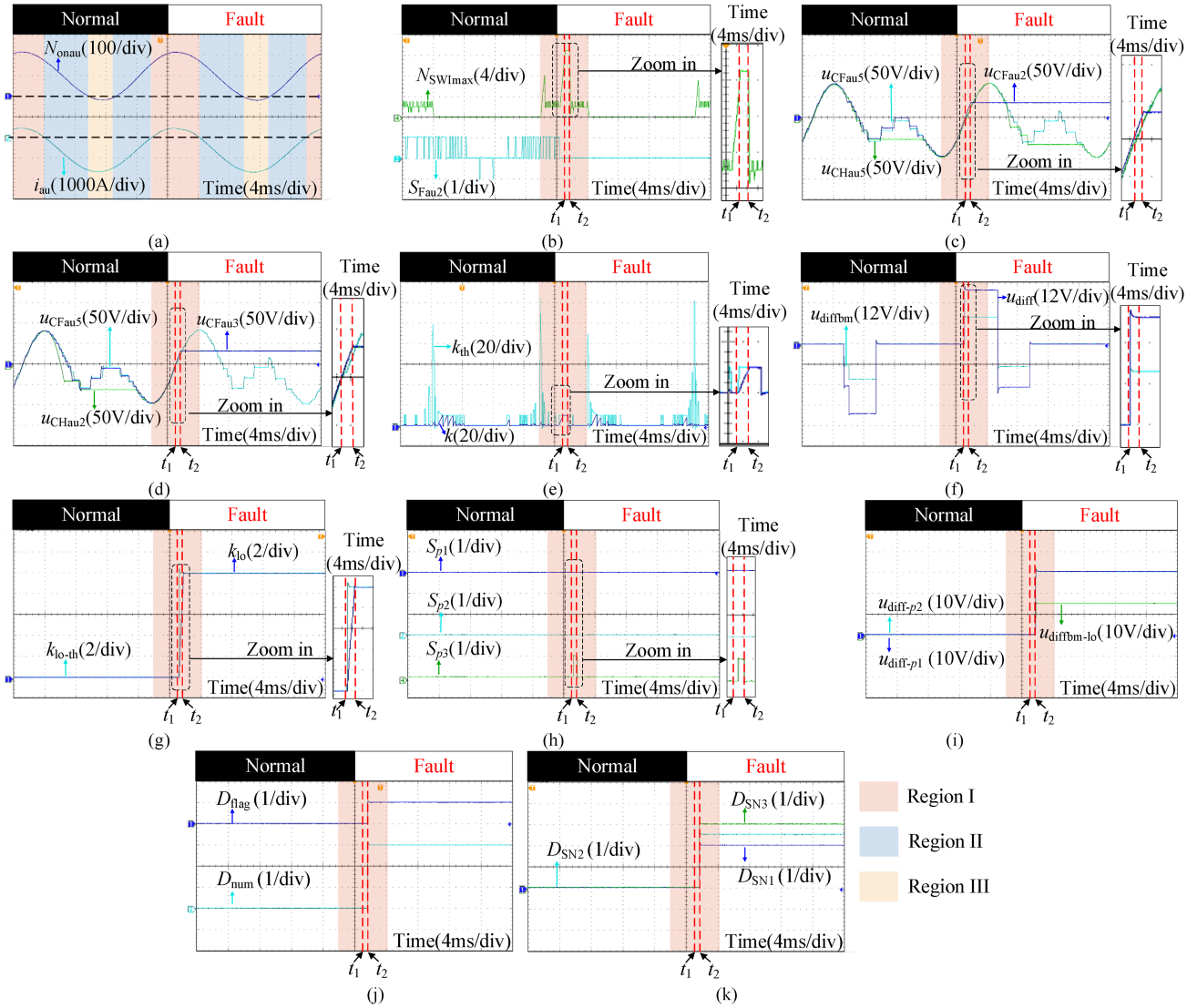

Fig. 12. Experimental waveforms of Scenario II. (a) Arm current and number of inserted SMs. (b) SM switching function and maximum value of N_{SFII}s. (c) SM capacitor voltages of FBSM_1, FBSM_5, and HBSM_5. (d) SM capacitor voltages of FBSM_4, FBSM_5, and HBSM_1. (e) Counting flag and corresponding threshold in the detection stage. (f) Alternation in the capacitor voltage and corresponding threshold in the detection stage. (g) Counting flag and corresponding threshold in the localization stage. (h) Switching functions of three potentially faulty SMs. (i) Alternation in the capacitor voltage and corresponding threshold in the localization stage. (j) Completion flag and number of faulty SMs. (k) Sequence numbers of faulty SMs.

capacitor voltages remain constant, as shown in Fig. 11(c) and (d). The whole diagnostic process takes 2.4 ms.

2) Scenario II: Experimental waveforms of Scenario II are shown in Fig. 12. As shown in Fig. 12(a), IGBT OCFs occur simultaneously in three SMs during Region I. Therefore, fault characteristics of Position $\mathrm{T}_{2\mathrm{H}}$, Position $\mathrm{T}_{2\mathrm{F}}$, and Position $\mathrm{T}_{3\mathrm{F}}$ faults can all be immediately exhibited. As shown in Fig. 12(b), the switching function of the faulty SM remains at 0 in Region I, which is consistent with the previous analysis in Section IV. Accordingly, N_{SFI} of the FBSM_2 continuously increases, quickly becomes the max N_{SFI}, and is then selected as the faulty SM. As shown in Fig. 12(b), N_{SFImax} continuously increases, which implies that the suspected faulty SM does not alter. Moreover, due to the conversion of the mode type, the capacitor voltages of all three faulty SMs continuously increase in the interval when their switching function remains at 0 in Region I, as shown in Fig. 12(c) and (d). At the moment t_1, k reaches k_{th} and u_{diff} exceeds u_{diffbm}, indicating the suspected faulty SM is indeed a faulty SM, as shown in Fig. 12(e) and (f). Then, SMs with the 2nd to 4th largest $N_{\mathrm{SFI}i}$ are selected as three suspected faulty SMs, whose statuses are determined in the following localization stage.

In the localization stage, k_{lo} increases and reaches $k_{\mathrm{lo\text{-}th}}$ at the moment t_2, as shown in Fig. 12(g). As shown in Fig. 12(h), during the duration from t_1 to t_2, S_{p3} does not remain at 0 consistently, indicating that it is a normal SM. However, S_{p1} and S_{p2} remain at 0 during this duration. As shown in Fig. 12(i), both $u_{\mathrm{diff\text{-}p1}}$ and $u_{\mathrm{diff\text{-}p2}}$ exceed $u_{\mathrm{diffbm\text{-}lo}}$ at the moment t_2, indicating these two suspected faulty SMs are indeed faulty SMs. As shown in Fig. 12(j) and (k), both the number of faulty SMs and the

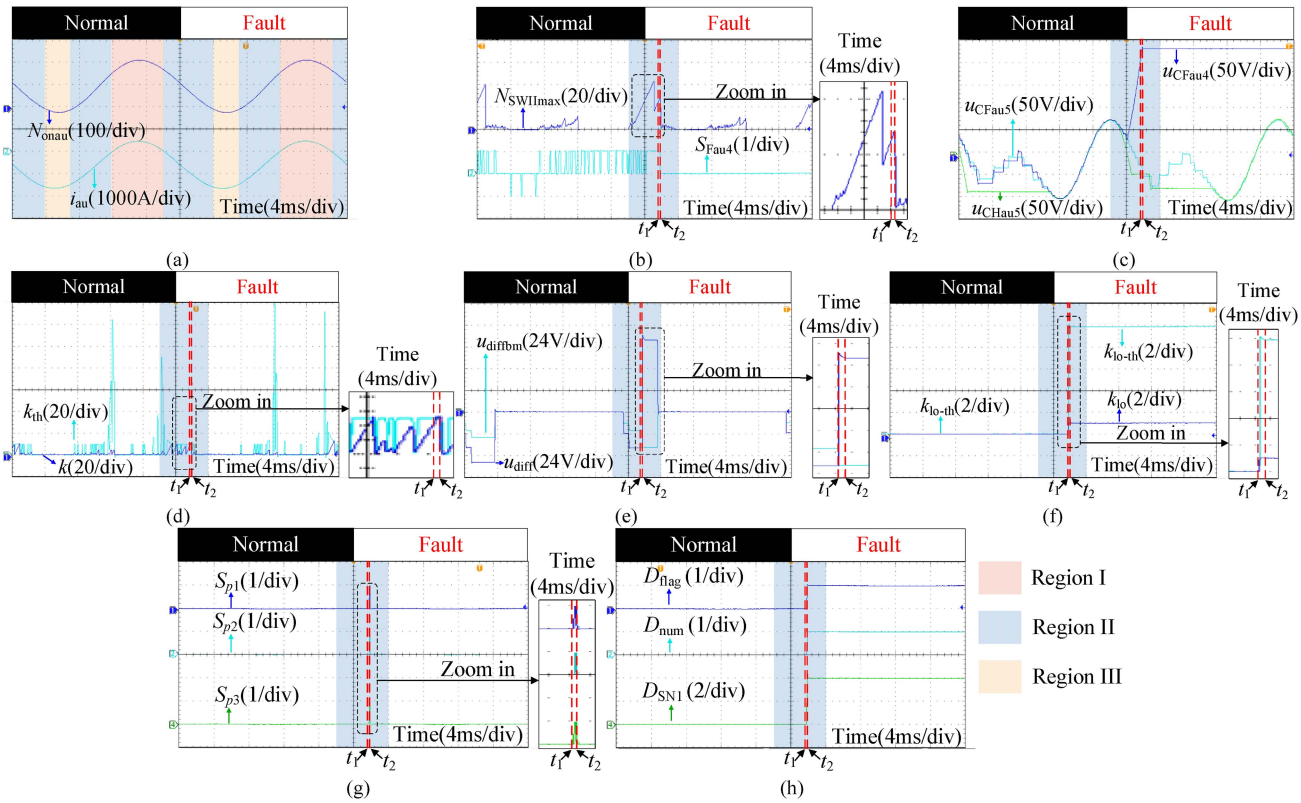

Fig. 13. Experimental waveforms of Scenario III. (a) Arm current and number of inserted SMs. (b) SM switching function and maximum value of N_{SFII}s. (c) SM capacitor voltages of FBSM_4, FBSM_5, and HBSM_5. (d) Counting flag and corresponding threshold in the detection stage. (e) Alternation in the capacitor voltage and corresponding threshold in the detection stage. (f) Counting flag and corresponding threshold in the localization stage. (g) Switching functions of three potentially faulty SMs. (h) Completion flag, number of faulty SMs, and sequence number of the faulty SM.

sequence numbers of the corresponding three faulty SMs can be output correctly. Subsequently, the bypass switches in the three faulty SMs are closed to complete the fault isolation, and their capacitor voltages remain constant, as shown in Fig. 12(c) and (d). The whole diagnostic process takes 1.8 ms.

3) Scenario III: Experimental waveforms of Scenario III are shown in Fig. 13. As shown in Fig. 13(a), both IGBT OCFs occur simultaneously in FBSM_4 during Region II. Therefore, the fault characteristics of Position $\mathrm{T}_{1\mathrm{F}}$ and Position $\mathrm{T}_{4\mathrm{F}}$ faults can all be immediately exhibited. As shown in Fig. 13(b), the switching function remains at 1 in Region II, which is consistent with the previous analysis in Section IV. Accordingly, N_{SFII} of FBSM_4 continuously increases, quickly becomes the maximum N_{SFII}, and is then selected as the faulty SM. As shown in Fig. 13(b), N_{SFIImax} continuously increases, which implies that the suspected faulty SM does not alter. Moreover, due to the conversion of the mode type, the capacitor voltage of the faulty SM continuously increases in the interval when its switching function remains at 1 in Region II, as shown in Fig. 13(c). This phenomenon differs from when the two IGBT OCFs occur independently in Scenarios I and II, which is consistent with the analysis in Section IV. The root cause of this phenomenon lies in the simultaneous OCFs of both IGBTs, which leads to a transition from Mode V_{F} to Mode VI_{F} instead of Mode $\mathrm{VII}_{\mathrm{F}}$ or Mode $\mathrm{VIII}_{\mathrm{F}}$. At the moment t_1, k reaches k_{th} and u_{diff} exceeds u_{diffbm}, indicating the suspected faulty SM is indeed a faulty SM, as shown in Fig. 13(d) and (e). Then, SMs with the 2nd to 4th largest $N_{\mathrm{SFI}\,i}$ are selected as three suspected faulty SMs, whose statuses are determined in the following localization stage.

In the localization stage, when k_{lo} does not reach its threshold $k_{\mathrm{lo\text{-}th}}$, S_{P1}, S_{P2}, and S_{P3} all switch to 0 and fail to remain consistently at 1, as shown in Fig. 13(f) and (g). This results in the termination of the localization stage and simultaneously indicates that all three suspected SMs are in a normal state. As shown in Fig. 13(h), both the number of faulty SMs and the sequence numbers of the corresponding three faulty SMs can be output correctly. Subsequently, the bypass switch in FBSM_4 is closed to complete the fault isolation, and its capacitor voltage remains constant, as shown in Fig. 13(c). The whole diagnostic process takes 1.8 ms.

4) Scenario IV: Experimental waveforms of Scenario IV are shown in Fig. 14. As shown in Fig. 14(a), both IGBT OCFs occur simultaneously in FBSM_2 during Region I. Therefore, the fault characteristics of Position $\mathrm{T}_{2\mathrm{F}}$ and Position $\mathrm{T}_{3\mathrm{F}}$ faults can all be immediately exhibited. As shown in Fig. 14(b), the switching function remains at 0 in Region I, which is consistent with the previous analysis in Section IV. Accordingly, N_{SFI} of FBSM_2 continuously increases, quickly becomes the maximum N_{SFI}, and is then selected as the faulty SM. As shown in Fig. 14(b), N_{SFImax} continuously increases, which implies that the suspected faulty SM does not alter. Moreover, due to the conversion of the mode type, the capacitor voltage of the faulty

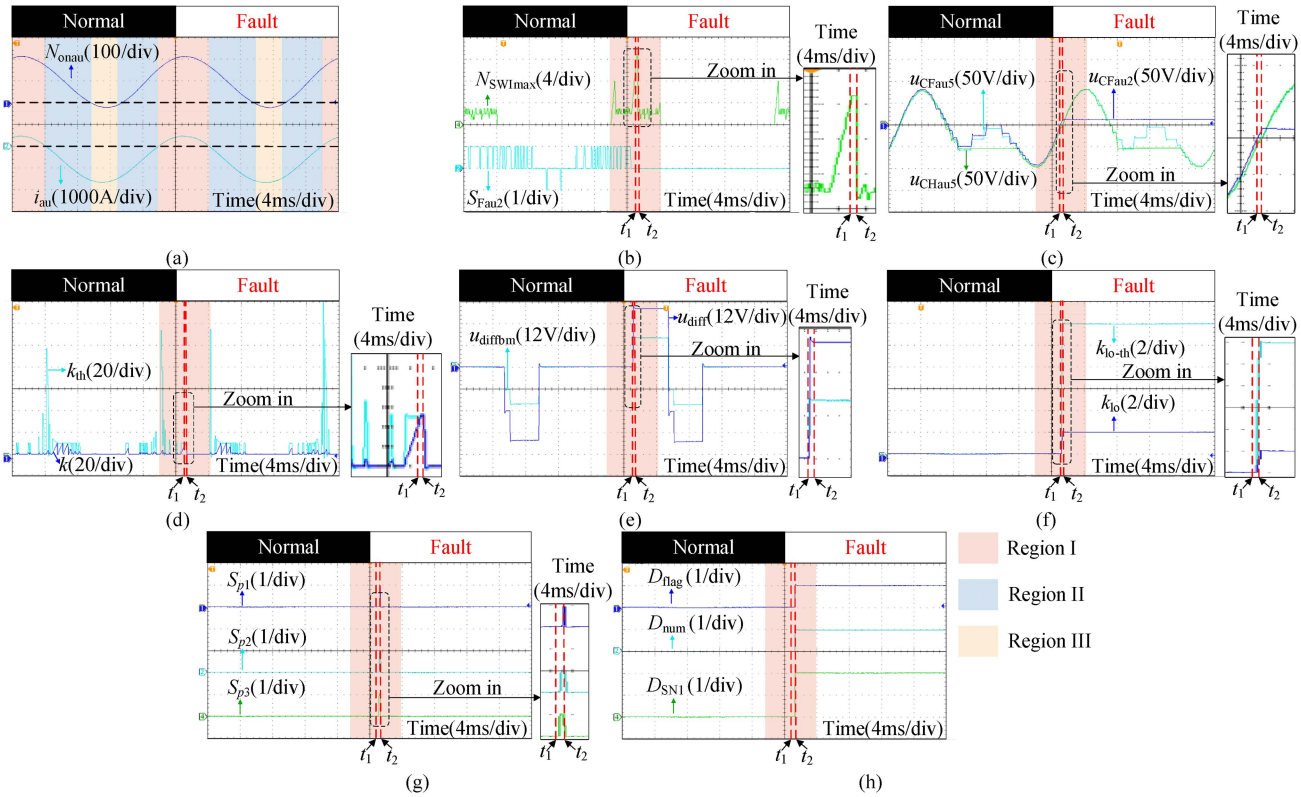

Fig. 14. Experimental waveforms of Scenario IV. (a) Arm current and number of inserted SMs. (b) SM switching function and maximum value of N_{SFIS}. (c) SM capacitor voltages of FBSM_2, FBSM_5, and HBSM_5. (d) Counting flag and corresponding threshold in the detection stage. (e) Alternation in the capacitor voltage and corresponding threshold in the detection stage. (f) Counting flag and corresponding threshold in the localization stage. (g) Switching functions of three potentially faulty SMs. (h) Completion flag, number of faulty SMs, and sequence number of the faulty SM.

SM continuously increases in the interval when its switching function remains at 0 in Region I, as shown in Fig. 14(c). At the moment t_1, k reaches k_{th} and u_{diff} exceeds u_{diffbm}, indicating the suspected faulty SM is indeed a faulty SM, as shown in Fig. 14(d) and (e). Then, SMs with the 2nd to 4th largest $N_{\mathrm{SFI}i}$ are selected as three suspected faulty SMs, whose statuses are determined in the following localization stage.

In the localization stage, when k_{lo} does not reach its threshold $k_{\mathrm{lo\text{-}th}}$, S_{P1}, S_{P2}, and S_{P3} all switch to 1 and fail to remain consistently at 0, as shown in Fig. 14(f) and (g). This results in the termination of the localization stage and simultaneously indicates that all three suspected SMs are in a normal state. As shown in Fig. 14(h), both the number and the sequencer number of the faulty SM can be output correctly. Subsequently, the bypass switch in FBSM_2 is closed to complete the fault isolation, and its capacitor voltage remains constant, as shown in Fig. 14(c). The whole diagnostic process takes 1.3 ms.

Validation results of Experimental Scenarios I and II further confirm that the proposed diagnostic strategy is applicable to the scenario of two IGBT OCFs with opposite current polarities occurring simultaneously in a single SM. These two scenarios correspond to the diagnostic processes in which the system first enters Region II and Region I, respectively.

Based on the above validations in Experimental Scenarios I–IV, it can be demonstrated that the proposed diagnostic strategy can effectively diagnose both scenarios where multiple SMs simultaneously occur IGBT OCFs and those where a single SM simultaneously occurs multiple IGBT OCFs.

B. Verification of the Performance of the Proposed Diagnostic Strategy Under Transient Conditions

1) Under Load Changes: To verify the performance of the proposed diagnostic strategy under load change, the experiment under the corresponding condition is done, whose experimental waveforms are shown in Fig. 15. To imitate load change, the active power dips from 1.0 to 0.8 per unit (p.u.) at t_0 [10], [26], [30].

As shown in Fig. 15(a), the active power dips from 1.0 to 0.8 p.u. at t_0. The waveforms of i_{au} and $N_{\mathrm{on\text{-}au}}$ are presented in Fig. 15(b). As shown in Fig. 15(c) and (d), the capacitor voltages of SMs are still well balanced during load change. As shown in Fig. 15(e)–(g), although some SMs are selected as suspected faulty SMs, no occurrence of u_{diff} exceeding u_{diffbm} is observed during load change. This is attributed to the fact that Unified Characteristic I relied upon in the determination process of suspected faulty SMs is based on the topological level of the SM and is therefore unaffected by external operating conditions. Therefore, it is demonstrated that the proposed diagnostic strategy is immune to load change. Furthermore, three IGBT OCFs are set to occur according to Scenario I at the moment t_1 to verify that the proposed diagnostic strategy can work effectively

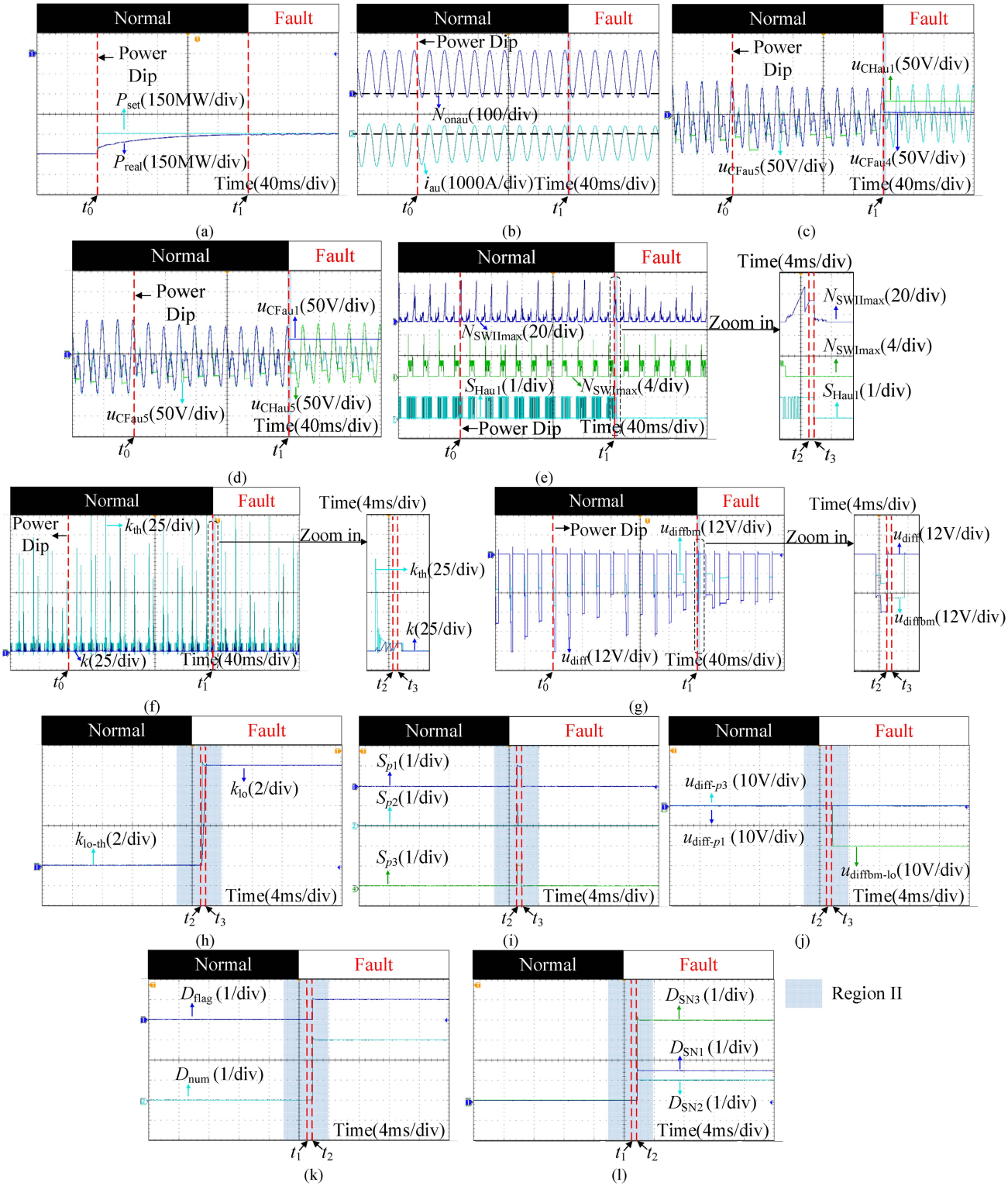

Fig. 15. Experimental waveforms under load change. (a) Set active power and real active power. (b) Arm current and number of inserted SMs. (c) SM capacitor voltages of $FBSM_4$, $FBSM_5$, and $HBSM_1$. (d) SM capacitor voltages of $FBSM_1$, $FBSM_5$, and $HBSM_5$. (e) SM switching function and maximum value of N_{SFI}s and N_{SFII}s. (f) Counting flag and corresponding threshold in the detection stage. (g) Alternation in the capacitor voltage and corresponding threshold in the detection stage. (h) Counting flag and corresponding threshold in the localization stage. (i) Switching functions of three potentially faulty SMs. (j) Alternation in the capacitor voltage and corresponding threshold in the localization stage. (k) Completion flag and number of faulty SMs. (l) Sequence numbers of faulty SMs.

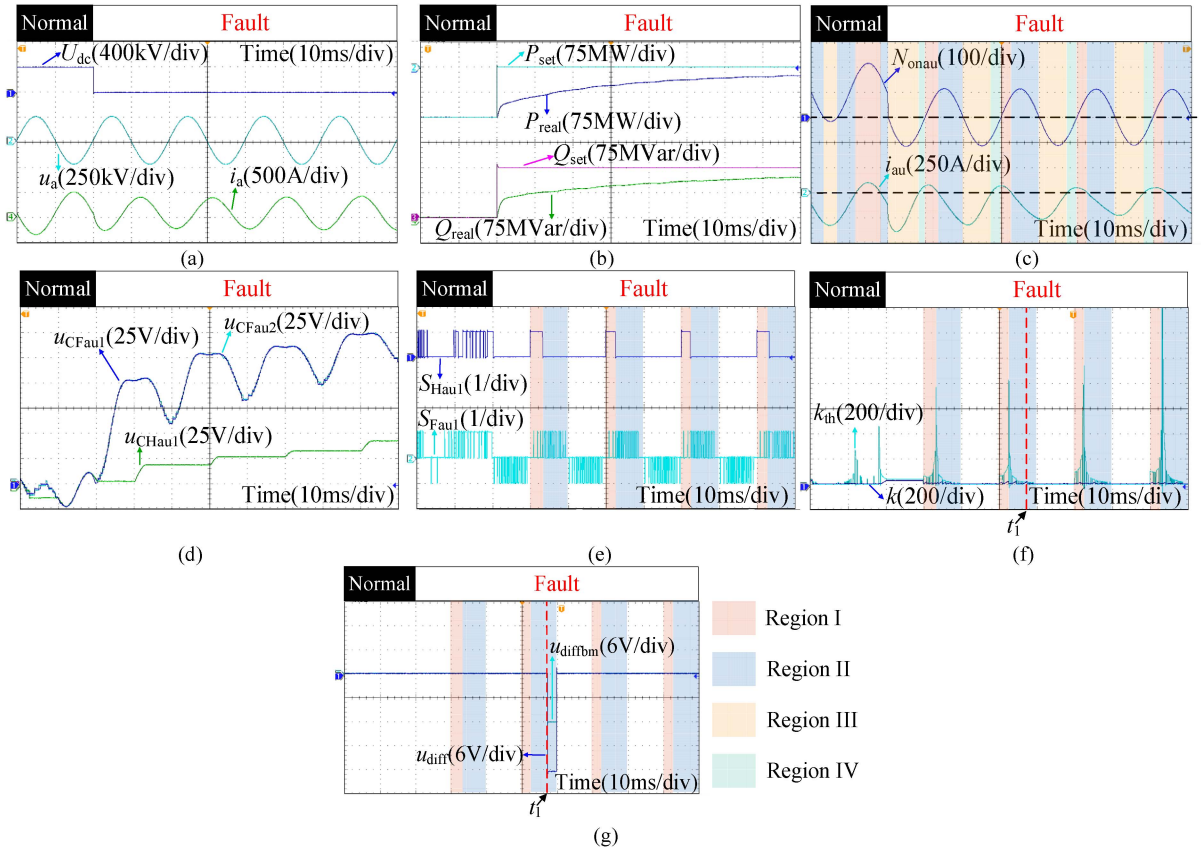

Fig. 16. Experimental waveforms under DC faults. (a) DC voltage, output voltage and output current. (b) Set active power, real active power, set reactive power and real reactive power. (c)Arm current and number of inserted SMs. (d) SM capacitor voltages of $FBSM_1$, $FBSM_2$, and $HBSM_1$. (e) Switching functions (f) Counting flag and corresponding threshold in the detection stage. (g) Alternation in the capacitor voltage and corresponding threshold in the detection stage.

under different loads. Since the diagnostic process is similar to that in scenario, it is not elaborated here. Through the diagnostic process presented in Fig. 15(f)–(l), the detection stage completes at the moment t_2 and the localization stage completes at the moment t_3. Subsequently, the bypass switches in the three faulty SMs are closed to complete the fault isolation, and their capacitor voltages remain constant, as shown in Fig. 15(k) and (l). The whole diagnostic process takes 1.7 ms.

2) Under DC Faults: To verify the performance of the proposed diagnostic strategy under dc faults, the experiment under corresponding condition is also carried out, whose experimental waveforms are shown in Fig. 16. The HMMC employs the fault ride-through (FRT) strategy proposed in [32], which enables it to operate under conditions equivalent to zero dc voltage during dc faults [30], [32]. As shown in Fig. 16(a), the output current and output voltage of the HMMC can still be output normally with the employed FRT strategy. As shown in Fig. 16(b), the set active power is decreased to 0 and the set reactive power is increased to 150 MVar when a dc fault occurs. The waveforms of i_{au} and $N_{on\text{-}au}$ are presented in Fig. 16(c). As shown in Fig. 16(d), a certain capacitor voltage difference occurs between the capacitor voltages of FBSMs and HBSMs. This phenomenon has been elaborated in detail in [30] and [34]. However, as described in Section VII-B, Unified Characteristic I is independent of external operating conditions. As a result, no occurrence of u_{diff} exceeding u_{diffbm} is observed during dc faults, as shown in Fig. 16(e)–(g). For example, at the moment t_1, although a normal SM is selected as a suspected faulty SM, u_{diff} does not exceed u_{diffbm}, indicating that the diagnostic strategy correctly determines its status. Therefore, it is demonstrated that the proposed diagnostic strategy has immunity to dc faults.

IX. Conclusion

In this article, two unified characteristics of IGBT OCFs in HMMCs from dual perspectives are revealed. Summarized from the mode-type perspective, Unified Characteristic I indicates that an OCF in one or multiple IGBTs of an SM causes conversions of the affected Type B mode from B to C and the affected Type D mode from D to B or C. Unified Characteristic II is summarized from the switching-function perspective, revealing that two causal loops are generated as a consequence of the conflict between the objective of the VBS and the type conversion of the affected mode in specific regions, which compels faulty SMs to be maintained in specific switching functions in specific regions. In this way, a unified characteristics-driven strategy is proposed. With the integration of two unified characteristics, the commonalities among diverse scenarios of IGBT OCFs in HMMCs can be fully utilized to achieve uniform and accurate diagnosis. In the detection stage, the suspected faulty SM is first

selected. Specifically, the SM for which the switching function remains at 0 for the longest duration is selected as the suspected faulty SM in Region I. Regarding Region II, the SM for which the switching function remains at 1 for the longest duration is chosen as the suspected faulty SM. Afterward, the status of the suspected faulty SM can be further judged by observing the alternation of capacitor voltage during a specific interval when the switching function remains at the corresponding value. Once a suspected faulty SM is confirmed as an indeed faulty SM in the detection stage, other suspected faulty SMs are first selected relying on identical characteristics utilized for selecting the first suspected SM. Subsequently, in the localization stage, the statuses of these suspected faulty SMs are ascertained via the detection-stage method. The HIL experimental results fully verify that the proposed diagnostic strategy can effectively diagnose all malfunctioning scenarios in HMMCs, including those where OCFs occur in multiple SMs and those where multiple OCFs occur in a single SM.

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