A 14.6× DR Output Power-Tracking CSCR SC Energy-Harvesting Interface Achieving 90.4%End-to-End Efficiency With Exponential DCO

Mingyu Kim, *Graduate Student Member, IEEE*, Minhyeok Jeong, *Graduate Student Member, IEEE*, Donguk Seo, *Graduate Student Member, IEEE*, Inhee Lee, *Senior Member, IEEE*, and Yoonmyung Lee, *Senior Member, IEEE*

***Abstract*—A novel energy-harvesting interface (EHI) circuit that employs a continuously scalable-conversion-ratio (CSCR) switched-capacitor dc–dc converter is introduced in this article. CSCR converters inherently sustain high power conversion efficiency across a wide voltage conversion ratio, making them well-suited for EHI applications. Realizing wide-range maximum-power-point tracking (MPPT) with a hill-climbing algorithm, however, demands accurate on-chip power estimation. Recent EHI works failed to provide such an estimation, neglecting the unit step voltages in the internal flying-capacitor network, hence constraining the attainable MPPT range. To overcome this limitation, a compact power monitor that explicitly accounts for the unit step voltages in the internal flying-capacitor network is introduced. The monitor employs a capacitive divider and is tightly coupled to an exponential digitally controlled oscillator, yielding precise power measurements over a broad frequency span. Fabricated in a 180 nm CMOS process, the prototype delivers up to 6.05 mW while achieving 90.4% end-to-end efficiency. It sustains ≥97% MPPT efficiency over a 14.6× dynamic-power range (130 μW–1.9 mW), 3.4× wider than previously reported CSCR-based harvesters. The proposed architecture thus offers an efficient and scalable solution for next-generation energy-harvesting systems.**

***Index Terms*—Continuously scalable-conversion-ratio (CSCR), digitally controlled oscillator (DCO), energy-harvesting interface (EHI), maximum-power-point tracking (MPPT), power monitoring, switched-capacitor (SC) dc–dc converter.**

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Mingyu Kim, Minhyeok Jeong, Donguk Seo, and Yoonmyung Lee are with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea (e-mail: yoonmyung@skku.edu).

Inhee Lee is with the Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15261 USA.

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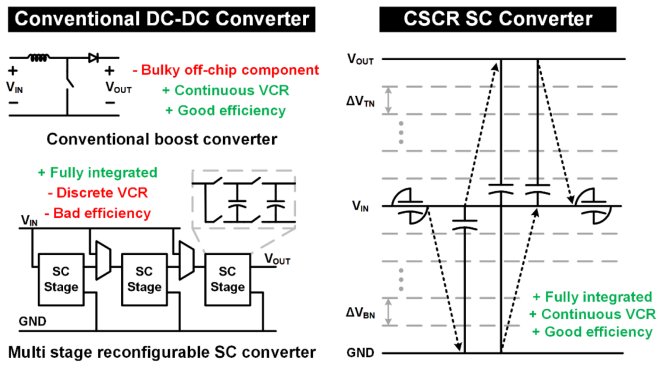

Fig. 1. Conventional DC–DC converter and CSCR SC converter.

I. Introduction

ENERGY harvesting (EH) presents numerous advantages for small-scale systems by extending battery life or directly providing power to the system. This capability makes EH an essential technology for enhancing the sustainability and independence of portable and remote devices [1], [2], [3], [4], [5], [6], [7]. Photovoltaic (PV) sources are particularly favored in many small-scale EH applications because they can generate considerable power from a compact area, supporting the movement toward more sustainable energy solutions [2], [8], [9]. Within an energy-harvesting interface (EHI), the dc–dc converter plays a critical role in transferring the energy generated from EH sources to batteries or loads, ensuring that the harvested energy is used efficiently according to the system's power requirements or charging demands. Ideally, these converters should minimize the use of bulky components, such as off-chip inductors, to facilitate broader application in a more compact form factor [1], [2], [10], [11]. Moreover, the ability to provide continuous voltage conversion ratios (VCRs) is highly desirable for handling a wide range of output voltages from EH sources while ensuring high efficiency in power delivery.

Fig. 1 highlights the distinctions between conventional dc–dc converters and continuously scalable-conversion-ratio (CSCR) switched-capacitor (SC) converters in energy-harvesting applications. Conventional inductor-based converters typically

require bulky off-chip components, making them less practical for compact systems [3], [4], [12], [13]. In a prior study [12], a peak power conversion efficiency (PCE) of 92.6% was achieved, but this relied on a large 10 μH off-chip inductor. While SC converters offer a more compact alternative, they are limited by discrete VCR options and often suffer from lower power transfer efficiency [10], [11], [14], [15], [16], [17], [18]. In contrast, CSCR SC converters [1], [2], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29] achieve higher efficiency by utilizing a continuous VCR and dividing the charging and discharging of the flying capacitor into multiple phases. This reduces the flying capacitor's voltage change ΔV per phase, minimizing charge-sharing loss. Additionally, it mitigates losses caused by parasitic capacitance on the flying capacitor, resulting in improved performance compared to conventional SC converters [19], [22].

Previous EHIs using CSCR SC converters have implemented SC-based Pulse Frequency Modulation (PFM) and hill-climbing techniques for maximum-power-point tracking (MPPT) [1], [2]. The SC-based PFM method is effective for specific types of energy-harvesting sources, e.g., thermoelectric generators (TEGs), but its applicability is limited for other sources due to its reliance on a constant ratio between the open-circuit voltage and optimal harvesting voltage [1]. On the other hand, the hill-climbing method, which requires precise power monitoring for effective MPPT, can be applied to a broader range of energy sources. However, its performance depends heavily on the accuracy of the power-monitoring implementation. Prior research employing the hill-climbing method encountered challenges with power monitoring approximation, which restricted the MPPT range and reduced the overall effectiveness [2].

To address these challenges, this article introduces a novel CSCR SC converter-based EHI that enhances MPPT efficiency across a wide power range through precise real-time output power monitoring. This is achieved by integrating an innovative power monitoring circuit with an exponential digitally controlled oscillator (DCO), ensuring highly efficient MPPT efficiency across diverse input conditions. This article is an extended version of a conference paper previously presented in [30]. This journal version provides a more in-depth analysis of the key building blocks, including detailed operational principles of the proposed power monitor and the exponential DCO. Furthermore, we have included comprehensive measurement results, such as MPPT performance with a TEG model, end-to-end efficiency under various conditions, dynamic MPPT operation, and a detailed power loss analysis to more thoroughly validate the proposed design.

The remainder of this article is organized as follows. Section II discusses the conventional and proposed MPPT methods for EHIs utilizing CSCR SC converters with a detailed explanation of the implementation and operation of the crucial power monitor block. Section III presents the overall EHI system architecture and describes the individual circuits. Section IV presents the measurement results, and Section V concludes this article.

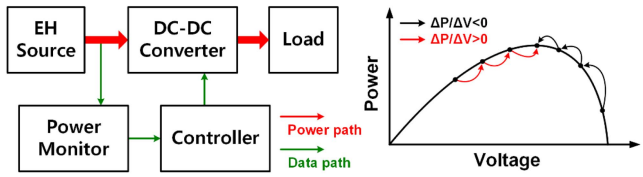

Fig. 2. EHI block diagram and hill-climbing algorithm.

TABLE I
LIST OF SYMBOLS AND DESCRIPTIONS

Symbol	Description
ΔV_{TN}, ΔV_{BN}	Unit voltage step at the top and bottom plates of the flying capacitor
C_{FLY}	Capacitance of a flying capacitor
M	Frequency multiplication factor for the exponential DCO (Coarse: 2, Fine: 1.06)
f_{clk}	Switching frequency of the SC converter
P_{IN}, P_{OUT}	Input power and output power of the energy harvesting interface
V_{IN}, V_{OUT}	Input voltage and output voltage
Q_{OUT}	Charge delivered to the output per switching cycle

II. MPPT With ΔV_{TN} Compensation for CSCR Converters

Fig. 2 illustrates the MPPT process of an EHI utilizing a hill-climbing algorithm. The energy harvested from the source is delivered to the load through a dc–dc converter. The controller, employing the hill-climbing method, dynamically adjusts the converter's operating conditions based on the harvested power, which is estimated by the power-monitoring circuit [2]. The adjustment of operating conditions involves measuring the power at a given point, modifying the circuit control signals (e.g., frequency), and evaluating the power at a neighboring operating point. By comparing the two power levels, the controller determines the next step: if the power has increased, the control signals are adjusted further in the same direction; if the power has decreased, the direction is reversed. Through this iterative process of comparing the power levels at successive points, the algorithm converges toward the MPP.

The key advantage of this method is its ability to perform MPPT in real-time, making it versatile and applicable to a wide range of EH sources. By continuously adapting to environmental changes, such as fluctuations in light source brightness, the algorithm ensures that the EHI operates at maximum efficiency, effectively optimizing power extraction under varying conditions. To aid in understanding the mathematical analysis and circuit operation discussed in the following subsections, the main symbols and their descriptions are summarized in Table I.

A. Prior MPPT With Approximated Power Estimation

Previous research employing the hill-climbing method for MPPT utilized a capacitive digital-to-analog converter (CDAC) for power monitoring [2]. In this approach, the resolution of the CDAC is crucial in determining the accuracy of MPPT. Achieving high-resolution power estimation requires a large number of capacitors, which can significantly increase the circuit area. To analyze the power estimation mechanism, we first define the key parameters of the CSCR converter. Let C_{FLY} represent

the flying capacitance. The voltage steps at the top and bottom nodes of the flying capacitors during charge transfer are denoted as ΔV_{TN} and ΔV_{BN}, respectively. Using these parameters, the steady-state input power of a CSCR SC converter can be mathematically represented as follows [20]:

$$P_{IN} = f_{clk} \times V_{IN} \times (V_{OUT} - -\Delta V_{TN} + \Delta V_{BN}) \times C_{FL} \tag{1}$$

where V_{IN} and V_{OUT} are the input and output voltages of the converter, respectively. In this equation, P_{IN} represents the input power monitored by the power monitoring circuit. The flying capacitance per stage is denoted by C_{FLY}, and f_{clk} is the switching frequency. The voltage step changes at the top and bottom nodes of C_{FLY}, represented by ΔV_{TN} and ΔV_{BN}, respectively, play a critical role in power estimation.

Assuming that $\Delta V_{TN} = \Delta V_{BN}$, the input power P_{IN} can be approximated as follows [2]:

$$P_{IN} \approx f_{clk} \times V_{IN} \times V_{OUT} \times C_{FLY}. \tag{2}$$

Since V_{OUT} and C_{FLY} remain constant during an MPPT cycle, P_{IN} can be further simplified to

$$P_{IN} \propto f_{clk} \times V_{IN}. \tag{3}$$

However, the assumption that $\Delta V_{TN} = \Delta V_{BN}$ does not hold for all V_{IN} values because both ΔV_{TN} and ΔV_{BN} are determined by V_{IN}, V_{OUT}, and the number of stages in the CSCR SC converter. This assumption leads to inaccuracies in input power estimation, thereby reducing the precision of MPPT.

Additionally, this method measures input power rather than directly monitoring the harvested output power, neglecting the power losses within the dc–dc converter. These losses can further exacerbate power estimation errors, especially under low input power conditions, thus diminishing the overall accuracy of the MPPT process. Fig. 3(c) illustrates the decline in the calculated accuracy resulting from the "ΔV_{TN}–ΔV_{BN}" error, which was previously assumed to be zero. A discrepancy of 100 mV leads to a significant 7% reduction in power monitoring accuracy at an output voltage of 1.5 V.

B. Proposed MPPT With C_{FLY} Unit Step Voltage (ΔV_{TN})

To address the limitations observed in previous research, a new MPPT technique is proposed. This method improves the accuracy of the harvested power estimation by explicitly accounting for the unit step voltage, ΔV_{TN}, of the top flying capacitor. According to [20], the charge delivered to the output per cycle (Q_{OUT}) depends on both the bottom and top plate voltage steps

$$Q_{OUT} = (M+1) \times \Delta V_{BN} \times C_{FLY} - \Delta V_{TN} \times C_{FLY}. \tag{4}$$

Since the total voltage increase at the bottom plate equals the input voltage in steady state, i.e., $(M+1) \times \Delta V_{BN} = V_{IN}$, the equation simplifies to

$$Q_{OUT} = (V_{IN} - \Delta V_{TN}) \times C_{FLY}. \tag{5}$$

Substituting this into the power equation $P_{OUT} = f_{clk} \times V_{OUT} \times Q_{OUT}$, the steady-state output power of a CSCR SC converter

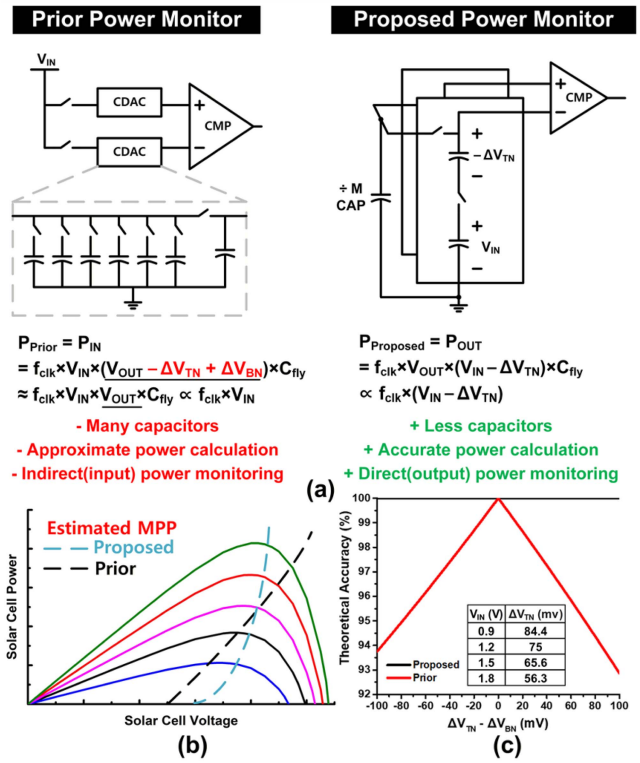

Fig. 3. (a) Prior and proposed power monitor for CSCR EHIs. (b) MPPT accuracy vs solar cell voltage from different light intensities. (c) Accuracy of power monitor across different ΔV_{TN}–ΔV_{BN}.

can be expressed as follows:

$$P_{OUT} = f_{clk} \times (V_{IN} - -\Delta V_{TN}) \times V_{OUT} \times C_{FLY}. \tag{6}$$

Assuming the output of the proposed EHI is connected to an energy storage element (i.e., a battery), V_{OUT} can be assumed to be constant, since the voltage of an energy storage device changes slowly relative to the power monitoring cycle, and C_{FLY} also does not change. Then, P_{OUT} can be simplified as follows:

$$P_{OUT} \propto f_{clk} \times (V_{IN} - -\Delta V_{TN}). \tag{7}$$

It is noteworthy that, while the input power estimation (1) requires considering both ΔV_{TN} and ΔV_{BN}, the proposed MPPT scheme focuses on the output power, which is determined by (6). Regarding output power delivery, the charge transfer depends on the voltage potential at the top plate relative to the input. Therefore, ΔV_{BN} does not directly affect the instantaneous output power estimation. Consequently, the proposed monitor only compensates for ΔV_{TN} to ensure accurate tracking of P_{OUT} while keeping the circuit complexity low. The proposed technique ensures a precise output power estimation, even under fluctuating V_{IN} conditions. Fig. 3(b) conceptually illustrates how this new estimation scheme improves the accuracy of MPPT compared to previous methods. Earlier power estimation techniques often failed to correctly identify the MPP under extreme brightness conditions—very dark (low light intensity) and very bright (high light intensity) environments—due to inaccuracies in power estimation. In contrast, the proposed monitoring scheme can accurately track the MPP by properly

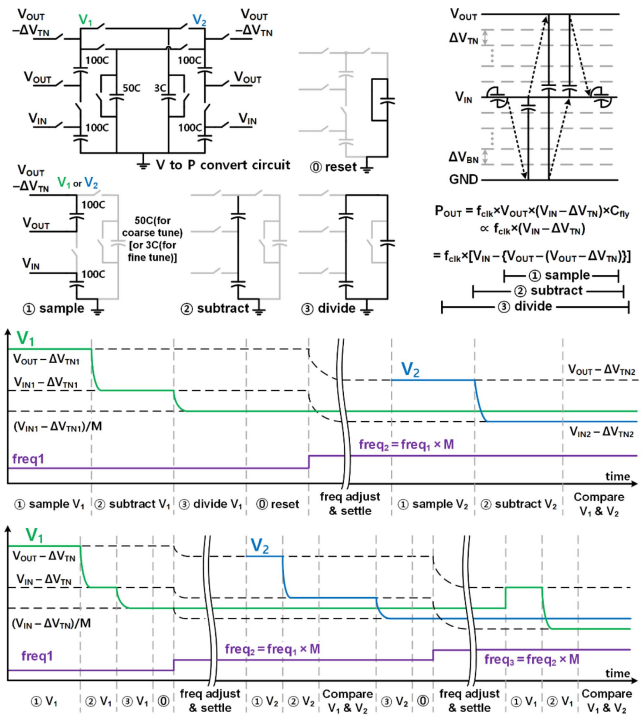

Fig. 4. Proposed power monitor circuit and its operation details.

accounting for the unit step voltage, ΔV_{TN}, of the top flying capacitor during output power estimation. This improvement enables more reliable and efficient MPPT performance, even under variable environmental conditions.

C. Circuit Implementation of Power Monitor

According to (7), the estimated powers with two different f_{clk} values can be expressed as follows:

$$P_{OUT,t_1} \propto f_{clk,t_1} \times \left(V_{IN,t_1} - -\Delta V_{TN,t_1}\right) \tag{8}$$

$$P_{OUT,t_2} \propto f_{clk,t_2} \times \left(V_{IN,t_2} - -\Delta V_{TN,t_2}\right) \tag{9}$$

where the subscripts $t1$ and $t2$ represent parameters corresponding to the initial and subsequent f_{clk} values, respectively. The proposed circuit adjusts f_{clk} using a constant multiplication factor M, defined as the exponential frequency scaling ratio, unlike previous methods that update it linearly. This constant M allows for direct comparison of harvested powers at different f_{clk} values without explicitly involving f_{clk} in the comparison. For example, if $M \times f_{clk,t1} = \mathrm{f_{clk,t2}}$, the circuit can compare $\mathrm{P_{OUT,t1}}$ and $\mathrm{P_{OUT,t2}}$ by evaluating "$V_{IN,t1}$–$\Delta V_{TN,t1}$" and "($V_{IN,t2}$–$\Delta V_{TN,t2}$)/M."

Fig. 4 illustrates the proposed power monitor circuit in detail. Since V_{IN}–ΔV_{TN} cannot be directly obtained from the CSCR SC converter, the circuit indirectly samples V_{IN}, V_{OUT}, and V_{OUT}–ΔV_{TN} and estimates P_{OUT} using the modified expression

$$P_{OUT} \propto f_{clk} \times \left[V_{IN} - -\{V_{OUT} - -(V_{OUT} - -\Delta V_{TN})\}\right]. \tag{10}$$

To clarify the indirect measurement mechanism shown in Fig. 4, the operation is divided into three phases. First, during the "Sample" phase, the circuit captures ΔV_{TN} indirectly by sampling the voltage difference between V_{OUT} and the top-plate node. Simultaneously, V_{IN} is sampled on a separate capacitor. Second, in the "Subtract" phase, these capacitors are connected in series to produce (V_{IN}–ΔV_{TN}). Finally, in the "Divide" phase, the voltage is scaled by M if needed. Furthermore, to improve the hill-climbing process, the monitor circuit uses an alternating "ping-pong" sampling scheme with two storage nodes, V_1 and V_2. Instead of refreshing both voltages each cycle, the system keeps the previous power value in one node (e.g., V_1) and updates only the other node (e.g., V_2) with the current power value. This alternating update reduces sampling overhead by half compared to fixed-assignment methods, increasing overall monitoring efficiency. The value of M is chosen based on the operation mode to optimize both tracking speed and accuracy. During initial coarse tuning, M is set to 2 to quickly sweep the frequency range. Then, for fine-tuning, M is lowered to about 1.06 to enable high-resolution tracking near the MPP. The specific implementation of these ratios using the exponential DCO is detailed in Section III-C. The inclusion of the "Subtract" phase noticeably increases the duration of a single power monitoring cycle by about 1.5 times compared to previous methods that only use "Sample" and "Divide" phases [2]. However, this slight rise in per-cycle latency is effectively offset by the system's overall tracking design. By employing the exponential DCO with a coarse tuning mode that doubles the frequency at each step, the system can cover the frequency range and reach the MPP vicinity with far fewer steps than linear stepping approaches. As a result, the total time to lock onto the MPP is similar to, or even faster than, previous linear methods, especially during wide-range sweeps.

In the middle of Fig. 4, the time progression of an example where f_{clk} increases is illustrated. Initially, the harvested power at f_{clk} (freq1) is estimated and stored as $\mathrm{V_1}$. Subsequently, the power harvested at a higher f_{clk} (freq2) is measured and stored as V_2. Comparing these voltages, if V_1 is greater than V_2, the system concludes that freq1 yields higher power and reverts the frequency back to freq1. Conversely, if V_2 is greater, the subsequent operation is shown at the bottom of Fig. 4. In this case, V_2 is divided by M, the frequency is again increased by a factor of M, the process of storing the voltage as was done for V_1 is repeated, and V_1 and V_2 are compared again.

In the process where the frequency decreases over time, the division step for V_1 is omitted. Instead, after subtracting V_2, V_2 is divided by M. This adjustment is necessary because during the frequency decrease, freq1 is higher than freq2, requiring V_2 to be divided by M rather than V_1. Following this adjustment, the subsequent steps mirror those in the increasing-frequency process. By continuously comparing the voltages on both sides, the EHI dynamically identifies the frequency that maximizes power harvesting, ensuring optimal MPPT performance.

III. System Architecture and Circuit Details

A. System Architecture

Fig. 5 presents the overall architecture of the proposed EHI. At the core of this design is a power comparison mechanism, which

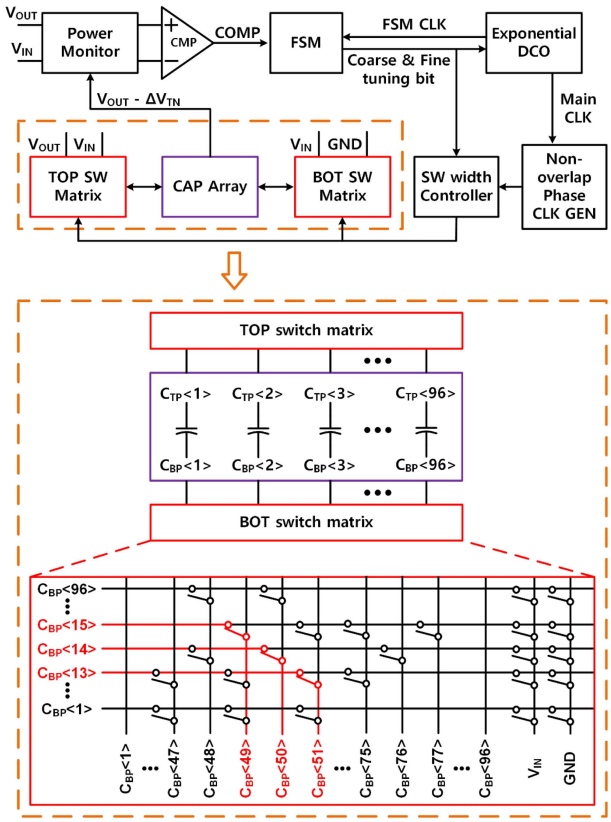

Fig. 5. Overall system diagram of the proposed EH system.

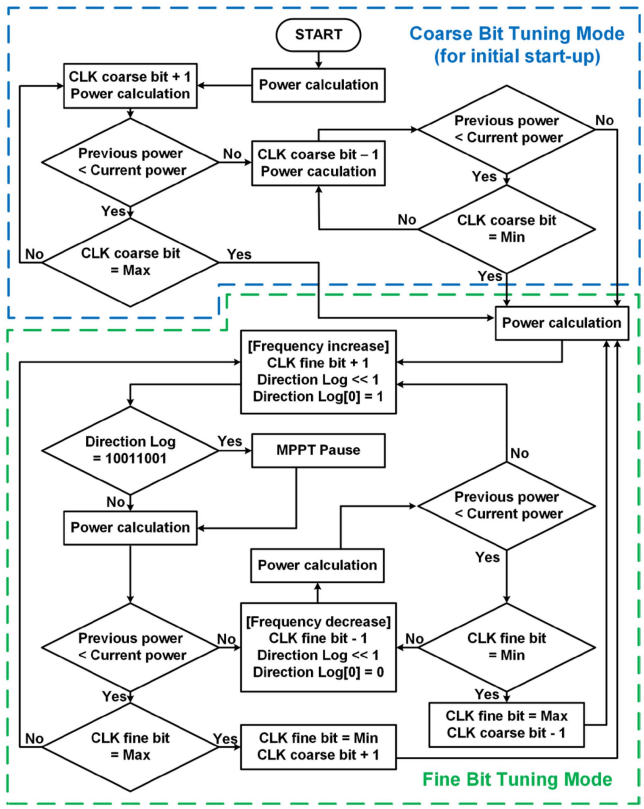

Fig. 6. Algorithm flowchart of FSM to control MPPT.

utilizes a power monitor block and a comparator to evaluate the harvested power at current and previous clock frequencies (f_{clk}). This comparator output (COMP) is processed by a finite state machine (FSM), which dynamically adjusts the frequency of the exponential DCO output, referred to as the Main CLK. The nonoverlap phase clock generator receives the Main CLK and produces 96 phase-shifted clock signals, each with a pulse width identical to that of the Main CLK. Instead of adding dedicated overlap-suppression logic, it simply treats the low portion of the Main CLK as the required dead time. Meanwhile, the switch-width controller taps the coarse-tuning bits that the FSM already forwards to the exponential DCO and uses them to scale the gate width of the power switches, providing a programmable drive-strength range of 12× between the minimum and maximum settings.

The proposed CSCR SC converter features a parallel capacitor array interconnected by a switch matrix. To maximize PCE, the capacitor array is optimized to provide 16 voltage steps between V_{IN} and GND and 32 steps between V_{OUT} and V_{IN}, resulting in a total of 96 capacitor arrays. The switch matrix and capacitor array design follow the methodology in [2], whose key improvement was reducing the two switches between capacitors to one, and this design likewise employs a single switch per capacitor pair. The streamlined configuration reduces power loss and enhances power transfer efficiency. As a result, the proposed architecture significantly boosts the power management and conversion capabilities, making it ideal for various EH applications.

B. FSM for Hill-Climbing MPPT

Fig. 6 illustrates the operational principles of the proposed MPPT mechanism, emphasizing the FSM's functional strategies. The FSM adjusts the operating frequency in multiplicative steps to efficiently locate the MPP. Larger multiplication factors allow for rapid MPP approximation but reduce precision, while smaller multiplication factors improve accuracy at the expense of speed.

To balance these trade-offs, the FSM employs a dual-mode approach. Initially, the Coarse-Bit Tuning Mode doubles the frequency for rapid MPP approximation. Once the coarse approximation is near complete, the FSM switches to the Fine-Bit Tuning Mode, refining the frequency with a precise multiplication factor of 1.06. If further adjustments are required after the fine bits reach their maximum, the FSM increments the coarse bit and resets the fine bit to its minimum. Conversely, when downward adjustments are needed, the fine bit decreases to its minimum value, triggering a decrement in the coarse bit. The fine-tuning is implemented with 4 bits, resulting in a 2.4× frequency range from its minimum to maximum setting. Since each coarse-tuning step involves a 2× frequency change, the 1.06× fine-tuning step offers adequate resolution and a 20% overlap between coarse steps. Because the proposed MPPT algorithm does not compare power across different coarse settings, having sufficient frequency overlap between neighboring coarse steps is essential to avoid dead zones at the transition points. This design choice ensures continuous tracking coverage even amid

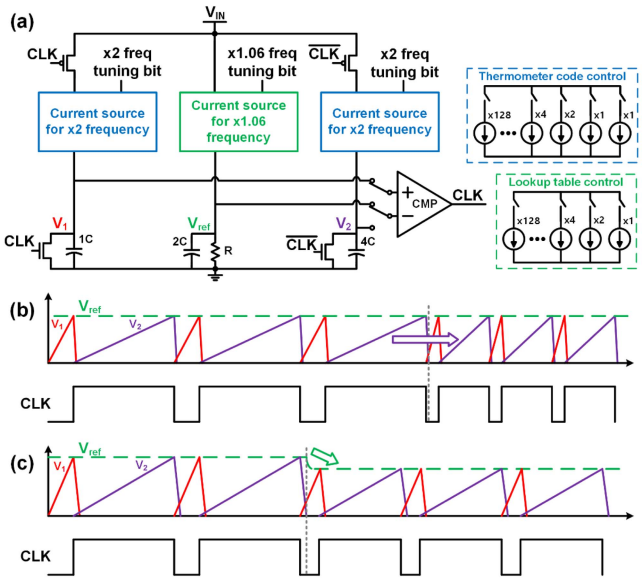

Fig. 7. (a) Proposed DCO to regulate frequency in multiples. (b) Increase frequency with coarse tuning. (c) Increase frequency with fine-tuning.

process, voltage, and temperature (PVT) variations. To maintain stability and prevent continuous oscillation around the MPP, the FSM uses a "Direction Log" mechanism. The direction of each frequency update during Fine Tuning is recorded in an 8-bit shift register ("1" for increase, "0" for decrease). The FSM constantly monitors this register for a specific pattern, 10011001, which indicates steady-state oscillation around the peak. When this pattern is detected, the system recognizes that the MPP has been reached and switches to the "MPPT Pause" (Lock) state, stopping the dither and reducing dynamic power consumption. This dual-mode approach ensures power comparisons are conducted only under identical coarse-bit configurations, optimizing the system's speed and precision in tracking the MPP.

C. Exponential DCO

Fig. 7(a) illustrates the proposed DCO, a key component of the power-monitoring system. The proposed DCO is designed based on a relaxation oscillator structure, where a capacitor is charged by a constant current and compared against a stable reference voltage. When the voltage of the capacitor exceeds the reference voltage, it discharges, restarting the cycle. To achieve precise frequency control, the proposed DCO incorporates separate sections for coarse tuning and fine tuning.

The coarse-tuning section, highlighted in blue in Fig. 7(a), adjusts the charging current of the capacitor using thermometer code control, enabling frequency doubling or halving. Fig. 7(b) illustrates this process, where doubling the charging current without altering the reference voltage increases the charging slopes of V_1 and V_2, leading to a doubled frequency. The capacitor sizes are intentionally asymmetrical to achieve an 80% duty cycle. Such a high duty cycle benefits the proposed CSCR SC converter because the capacitor array transfers charge through the switch matrix only when the main clock is high, thereby enhancing overall efficiency. Furthermore, when the clock is low, the entire switch matrix remains open, and no charge is transferred, so reducing the low-clock duration is advantageous to the converter's performance.

For fine-tuning, the frequency is adjusted by modifying the reference voltage (V_{ref}). A decrease in the reference voltage stored in the capacitor lowers the target voltage, resulting in a higher frequency for the same charging current. This adjustment is achieved using a preset look-up table (LUT) to generate the desired reference voltage. Fig. 7(c) shows this fine-tuning mechanism. As the reference voltage decreases without altering the charging slopes of V_1 and V_2, the time required for V_1 and V_2 to reach the reference voltage is reduced, resulting in a higher frequency.

The number of tuning bits was selected to optimize the trade-off between tracking performance and circuit area. Increasing the coarse bits would raise the maximum switching frequency, expanding the dynamic power range. Similarly, increasing the fine bits would enhance frequency resolution, reducing the gap between the discrete steps and the theoretical MPP, which helps prevent local drops in tracking efficiency. However, adding more bits requires an increased number of current mirror branches in the DCO, resulting in significant area overhead. Since the current resolution already achieves a tracking efficiency of over 97%, further expanding the bits offers minimal performance improvements relative to the area increase.

By combining these two control mechanisms—coarse tuning through current adjustment and fine tuning via reference voltage variation—the proposed DCO ensures a consistent and precise frequency scaling ratio across a wide operational range. Compared to the linear DCO in [2], which offers a 63× dynamic range (DR), the proposed design extends the range to 512×, representing an eight-fold increase. While the core structure for generating ramp voltages (V_1, V_2) resembles the linear DCO in [2], the proposed design fundamentally differs by introducing a variable $\mathrm{V_{ref}}$ control mechanism. In [2], $\mathrm{V_{ref}}$ is fixed, and the frequency is modulated solely by current, which would require a 256× larger current-mirror array to achieve the same dynamic range and resolution as this work. By combining current scaling (2× steps) with $\mathrm{V_{ref}}$ modulation (1.06× steps), the proposed DCO achieves an exponential frequency response to the control code. This multiplicative approach enables a wide dynamic range with high resolution while minimizing circuit area overhead.

Furthermore, the exponential DCO is a necessary part of the proposed output power monitoring scheme, which depends on multiplicative frequency scaling. While a traditional linear DCO combined with digital dividers or multipliers could be an option, it was considered unsuitable for this low-power application. Standard digital dividers support only integer ratios and cannot achieve the precise noninteger scaling of 1.06× needed for fine-tuning. On the other hand, frequency multiplication usually requires complex circuitry, such as a phase-locked loop (PLL), which would add significant area and design complexity. The proposed exponential DCO efficiently produces the necessary frequency steps through analog tuning, offering the best trade-off for the target system.

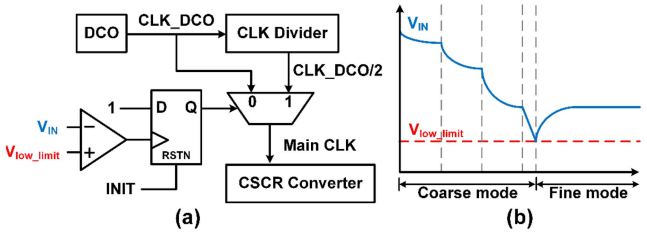

Fig. 8. (a) Proposed low-input voltage detector. (b) Operation of low input voltage detector.

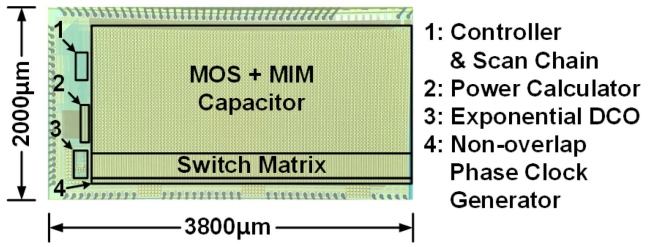

Fig. 9. Micrograph of the prototype chip.

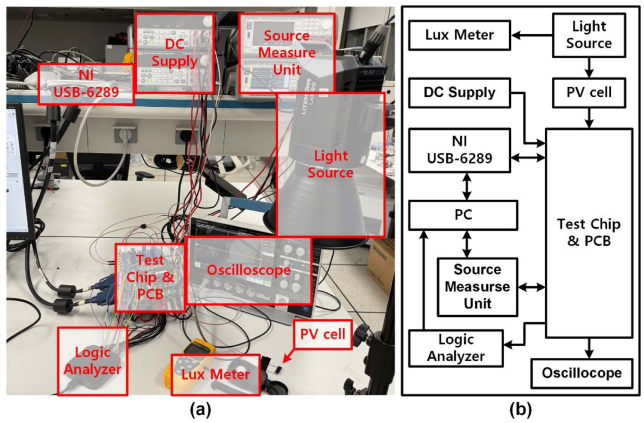

Fig. 10. (a) Measurement setup for PV EH. (b) Measurement setup block diagram.

Furthermore, the exponential DCO is crucial for the proposed output power monitoring scheme, which uses multiplicative frequency scaling to perform the hill-climbing algorithm. Using a traditional linear DCO would require a power-monitoring architecture similar to [2], where the dynamic range is limited by the resolution of the capacitor DAC (CDAC). To achieve the target 14.6× power range with a linear approach, the CDAC would need to be excessively large, resulting in a significant area penalty. Although the proposed exponential DCO adds a slight area overhead for the reference voltage generation circuitry, this is not significant considering that the capacitor arrays of the CSCR SC converter dominate the total chip area. Therefore, the exponential DCO is the most area-efficient solution for achieving high MPPT efficiency across a wide dynamic range.

D. Low Input Voltage Detector

Unlike systems relying on a fixed battery voltage, the proposed EHI dynamically up-converts varying input voltages. During the initial coarse-tuning phase of MPPT using the exponential DCO, the frequency is doubled in each step. However, excessively high frequency can lead to a significant drop in input voltage, potentially compromising the sub-block functionality. To prevent this, a low-input voltage detector is designed to ensure that the input voltage remains above a predefined threshold, maintaining system stability.

Fig. 8(a) illustrates the block diagram of the low-input voltage detector. This circuit consists of a comparator, a D flip-flop, a clock divider, and a multiplexer. Initially, the output of the D flip-flop is set to zero, aligning the main clock signal driving the CSCR SC converter with the DCO output (CLK_DCO). When the input voltage drops to the predefined threshold, $V_{\text{low\_limit}}$, the comparator output switches to high, setting the flip-flop output to transition from 0 to 1. As a result, the clock divider halves the CLK_DCO signal to produce CLK_DCO/2, which is then selected by the multiplexer to serve as the main clock. This step helps stabilize the lower input voltage. Once the frequency control mode shifts from coarse-tuning mode to fine-tuning mode, the coarse bit is decremented by one, and the INIT signal is driven low. This maintains a stable condition and allows the system to exit the inefficient scenario where the main clock remains divided.

In Fig. 8(b), the operational behavior of the input voltage adjustment under the low-input voltage detector is illustrated. Specifically, when the frequency doubling during coarse tuning causes excessive current and pulls V_{IN} below V_{low_limit}, the detector immediately switches to the divided clock (CLK_DCO/2) via the multiplexer. This halves the switching frequency, reducing input current and allowing V_{IN} to recover. Simultaneously, this event signals the FSM to end the coarse tuning sequence and automatically switch to fine tuning, ensuring continuous tracking stability.

IV. Measurement Results

The prototype chip, fabricated using a 180 nm CMOS process, is shown in Fig. 9. The design incorporates 96 flying capacitors, including both MOS and MIM capacitors, with a total capacitance of 204.8 pF. To evaluate the area overhead of the proposed control features, the active area is detailed as follows: the capacitor array occupies 4.45 mm^2, and the switch matrix with gate drivers covers 0.92 mm^2. These power stage components make up about 97.2% of the total active area (5.525 mm^2), ensuring high PCE. In comparison, the control and monitoring blocks are very compact; the digital controller (0.022 mm^2), scan chain (0.025 mm^2), power monitor (0.039 mm^2), exponential DCO (0.035 mm^2), and nonoverlap clock generator (0.034 mm^2) together occupy only around 2.8% of the total area. This demonstrates that the area overhead for the advanced MPPT features is minimal.

Fig. 10 illustrates the measurement setup used to verify the MPPT operation. Fig. 10(a) presents a photograph of the experimental environment, and Fig. 10(b) details the interconnection of the equipment in a block diagram. A commercial

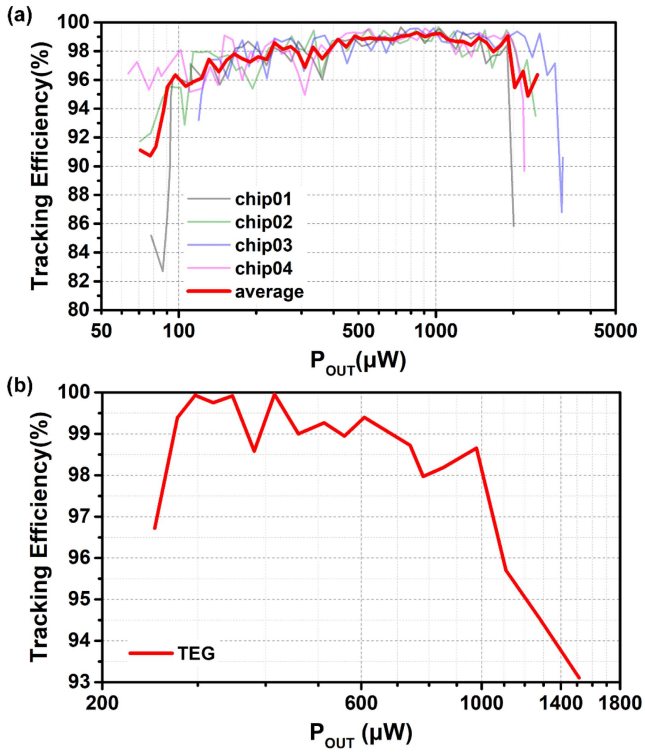

Fig. 11. Measured MPP tracking efficiency. (a) PV. (b) TEG.

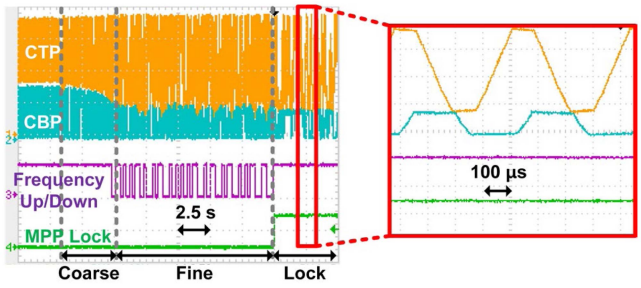

Fig. 12. MPP locking operation waveform of the proposed EHI.

millimeter-scale solar cell (KXOB25-03X4F-TR) is used as the energy-harvesting source. An adjustable light source (Godox Litemons LA150D) and a lux meter are employed to control and monitor the environmental conditions. A dedicated dc power supply provides all board-level powers; because the output stage is characterized as if it were charging a Li-ion battery, a regulated 3.6 V line from this supply is wired to the test chip's V_{OUT} pin. The chip is controlled, and the current values are measured using LabVIEW software, an NI-6289 data acquisition device, and a source measure unit. An oscilloscope probes multiple on-chip voltages in real time, and a logic analyzer captures the same signals for postprocessing on a PC. This comprehensive setup ensures precise and reliable testing of the proposed system under various lighting conditions.

Fig. 11(a) shows the measured MPP tracking efficiency. Here, the tracking efficiency is defined as the ratio of the measured output power with the proposed MPPT enabled ($P_{OUT,\ meas}$) to the maximum achievable output power ($P_{OUT,\ MAX}$). The $P_{OUT,\ MAX}$ is determined by manually sweeping the switching frequency and conversion ratios under fixed environmental conditions to find the absolute peak electrical power the converter can deliver. The measurements were conducted using four different chips, and the average tracking efficiency was calculated. The proposed system exhibits a fluctuating MPPT efficiency graph, attributed to resolution constraints from the digital frequency control. The DCO employs a 4-bit fine bit to transfer 8-bit binary values from the LUT, with each LUT value incrementing the frequency by a factor of 1.06 per step. These constraints prevent the MPPT circuit from achieving perfect alignment with the actual MPP, resulting in minor fluctuating errors due to discrepancies. Despite this, the peak efficiency achieved was 99.8%, underscoring the system's excellent performance. Compared to prior work [2], the range of harvested power achieving over 97% tracking efficiency has been expanded fourfold. This significant improvement is attributed to the enhanced power monitoring at the output, enabling more precise and efficient power harvesting. Fig. 11(b) illustrates the MPPT efficiency measured using a TEG model, with the open-circuit voltage fixed at 2 V while varying the resistance from 470 Ω to 3.3 k Ω. This approach demonstrates robust MPPT operation across a wider range of load conditions. Even with the TEG as the input power source instead of a solar cell, the proposed EHI demonstrated high MPPT efficiency. This showcases the proposed EHI's scalability and adaptability to diverse dc energy-harvesting sources.

Fig. 12 shows the operation waveform of the proposed EHI, highlighting a successful MPP locking sequence. The voltages at the top and bottom plates of the flying capacitor demonstrate the smooth soft-charging operation of the CSCR SC converter. When the frequency up/down signal is high, the frequency increases. Conversely, when the up/down signal is low, the frequency decreases. This dynamic adjustment allows the system to efficiently track the optimal frequency. Once the frequency up/down signal fluctuates around a specific configuration for a preset number of cycles, the system recognizes this operation point as the MPP and locks the frequency for a predetermined duration. This locking mechanism minimizes unnecessary frequency adjustments, conserving power and enhancing overall system efficiency.

Fig. 13 shows the PCE of the proposed EHI under different input voltage conditions with the output voltage fixed at 3.6 V. At an input voltage of 1.2 V, the PCE exceeds 85% within an output power range of 40–2450 μW. For an increased input voltage of 1.8 V, the PCE maintains 85% efficiency up to 5780 μW, reaching approximately 90% efficiency between 60 and 1000 μW. At a lower input voltage of 0.9 V, the PCE remains above 80% for an output power range of 30–770 μW.

Although the 1.2–3.6 V conversion might seem optimal due to the 32 top and 16 bottom voltage steps of the CSCR SC converter, the PCE is actually higher for the 1.8–3.6 V conversion. This is because the design uses MOS capacitors as part of the flying capacitors for high area efficiency. During the charge-sharing process within the converter, the capacitance of these MOS capacitors varies depending on the stored voltage.

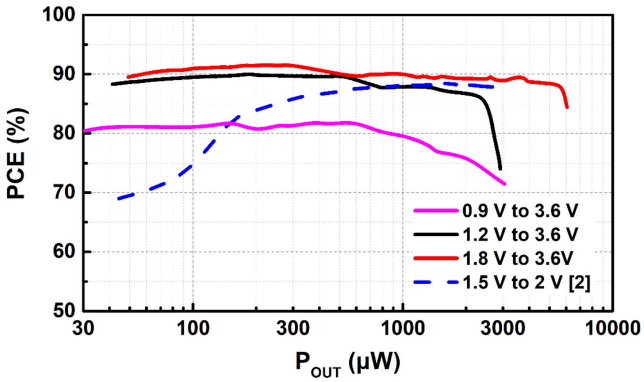

Fig. 13. Measured PCE.

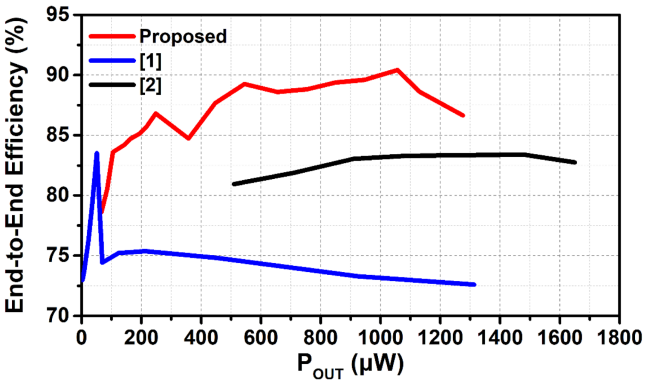

Fig. 14. Measured end-to-end efficiency.

This imbalance becomes more pronounced as the difference between the input and output voltage increases. Consequently, the 1.2–3.6 V conversion exhibits a lower PCE. These measurement results highlight the robust performance and adaptability of the proposed EHI across diverse input conditions.

Fig. 14 shows the end-to-end efficiency measurements of the proposed EHI. The end-to-end efficiency is calculated as the ratio of the MPPT output power to the maximum input power under varying conditions. Compared to prior works [1], [2], which leveraged a CSCR SC converter structure to perform MPPT by tracking the input power, the proposed EHI, which tracks the output power, exhibits mostly higher end-to-end efficiency. The results show that the efficiency exceeds 80% across a broader power range of 80–1000 μW. It is observed that there is a slight efficiency drop near the 360 μW output power region. This is attributed to the combined effects of local fluctuations in tracking efficiency, as shown in Fig. 11, and the reduced PCE of the SC converter. Since the 360 μW power point corresponds to a low-input-voltage condition, the converter operates in a region with lower PCE, as indicated in Fig. 13.

Fig. 15 illustrates the exponential DCO output frequency, effectively controlled from 41 kHz to 4.709 MHz. The proposed DCO is controlled with 3 coarse bits and 4 fine bits, where a coarse-bit change doubles the frequency, and a fine-bit change increases the frequency by a factor of 1.06. During the bit adjustments, the power monitor temporarily suspends power

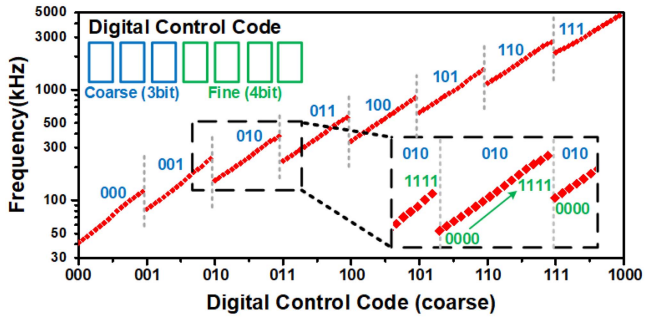

Fig. 15. Measured output frequency of exponential DCO.

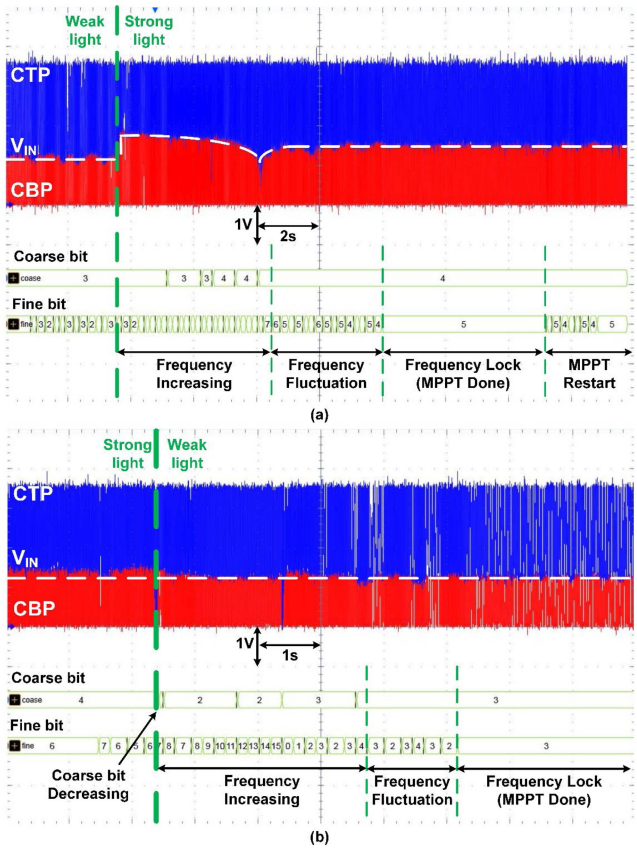

Fig. 16. MPPT operation under changing input conditions. (a) Weak to strong light. (b) Strong to weak light.

comparison to avoid inaccuracies, ensuring that precise frequency adjustments occur only during stable fine-bit intervals.

Fig. 16 shows the MPPT performance under varying input conditions. Specifically, these waveforms display the system dynamic response during fine-tuning after completing the initial coarse adjustment. As the lux level varies, the system continuously fine-tunes the DCO frequency code with high resolution to follow the new maximum power point (MPP). When lux levels increase, the DCO code rises, increasing the frequency, and when lux levels decrease, the DCO code decreases, reducing frequency. This demonstrates the system's adaptability to changing light conditions. The controller allows for adjustments in the timing of MPPT completion and frequency locking, providing flexibility to sustain optimal performance for diverse

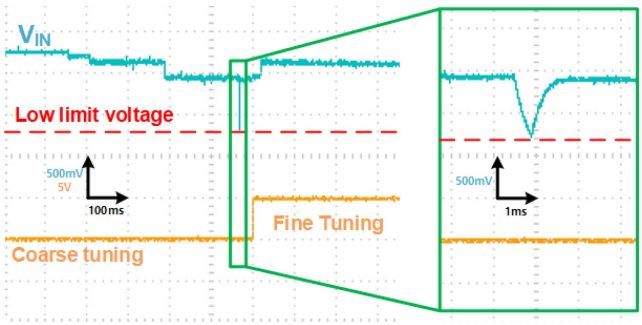

Fig. 17. Low input voltage detector operation waveform.

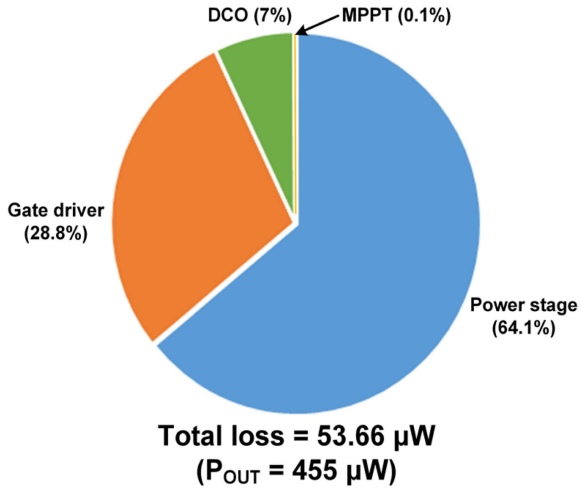

Fig. 18. Power conversion loss breakdown.

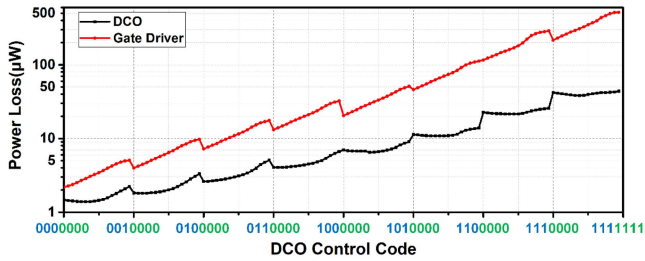

Fig. 19. DCO and gate driver loss.

energy sources and environments. However, when the input conditions change, the controller cannot re-enter the coarse-bit tuning mode. Instead, it continues operating in the fine-bit tuning mode, which may require up to approximately 36 s to complete retuning in the worst-case scenario. This worst-case timing occurs only under very large and abrupt changes in input power, which is an infrequent event for typical PV applications where sunlight conditions change gradually. Furthermore, the 36 s retuning time is based on a controller speed of 100 Hz; this time could be reduced to 3.6 s or lower by increasing the controller speed tenfold or higher, at the cost of a minor increase in monitoring power consumption. Therefore, this design choice is strategically optimized for indoor or stable EH scenarios where minimizing control overhead is essential, while still supporting applications that require faster transient responses, even if it means slightly higher power consumption.

Fig. 17 presents the operational waveform of the low-input voltage detector. During the coarse tuning mode, the frequency doubles at each step, eventually causing V_{IN} to drop to the low limit voltage due to excessive current draw. Upon detection, the circuit reverts the frequency back to half of its current value (i.e., the previous valid frequency). This reduction in current allows V_{IN} to recover to a stable level, and the FSM automatically switches to fine-tuning mode. This mechanism safeguards against the excessive input voltage drop below the critical level, ensuring stable operation of the sub-blocks within the EHI system.

Fig. 18 provides an analysis of the losses within each block during the MPPT process. At an output power of 455 μW, the power consumed by the proposed power monitor and FSM controller, which are combined and labeled as MPPT in the graph, accounts for only about 0.1% of the total power consumption. This minimal power overhead is mainly due to the low operating frequency of the FSM (100 Hz), which is far slower than the switching frequency of the power stage (up to MHz range). This demonstrates that the power overhead associated with the MPPT process is negligible. The power stage loss in Fig. 18 includes charge-sharing loss, bottom-plate parasitic loss, and switch conduction loss. The CSCR topology mainly reduces charge-sharing loss by lowering the voltage step across flying capacitors. This approach also reduces the per-cycle bottom-plate parasitic loss. At the measured point, the switch conduction loss and bottom-plate parasitic loss become the two main comparable loss components. While conduction loss dominates at high loads because of its I^2R dependence, parasitic loss becomes relatively more significant in this optimal efficiency range as conduction loss decreases quickly with the load.

Fig. 19 illustrates the power consumption in the DCO and the gate drivers as the DCO control bits vary. The power consumption of the gate driver steadily rises with increasing frequency. However, unlike that of the gate driver, the power consumption of the DCO does not strictly increase in proportion to the frequency. Instead, it repeatedly decreases and increases. Within the same coarse bit, as the fine bit increments, the reference voltage decreases while the frequency rises. This behavior reduces the power needed to generate the reference voltage, while the power consumed by the switches for capacitor charging and discharging, as well as by the comparator and clock buffer, increases. Consequently, as the fine bits increase within a single coarse bit, the overall DCO power consumption initially drops before rising again.

Table II presents a detailed comparison of the proposed EHI with prior-art EHIs. The proposed EHI demonstrates superior performance by accurately monitoring output power and efficiently tracking the maximum power delivered to the battery. Based on the characteristics of the utilized PV cell, the input voltage ranges from 0.9 to 1.8 V, while the output voltage is regulated at 3.6 V for a Li-ion battery. Unlike previous implementations [10], [11], it enables real-time power measurements, allowing continuous harvesting operation without interruptions.

TABLE II
PERFORMANCE COMPARISON OF SC CONVERTER BASED EH INTERFACES

	This work	JSSC 21 [1]	TCAS1 22 [2]	TCAS1 18 [10]	JSSC 16 [11]
Tech (nm)	**180**	180	28 (FD-SOI)	180	180
Converter type	**CSCR SC**	CSCR SC	CSCR SC	Reconfigure SC	Reconfigure SC
EH source	**PV/TEG**	TEG	PV	DC	DC
V_{IN} (V)	**0.9 – 1.8**	0.1 – 0.5	0.65 – 1.5	0.5 – 1.8	0.45 – 3
V_{OUT} (V)	**3.6**	0.75	< 2	1.2 1.8	3.3
VCR	**CSCR (2 – 4)**	CSCR (1.5 – 7.5)	CSCR (0.3 – 3)	1.0 – 4	1.3 – 8
MPPT scheme	**Hill-climbing**	PFM	Hill-climbing	Hill-climbing	Hill-climbing
Monitoring power	**P_{OUT}**	P_{IN}	P_{IN}	P_{OUT}	P_{OUT}
MPPT implementation	**ΔV_{TN} compensated power monitor & exponential DCO**	V_{IN} connected bias circuit	Frequency-mapped CDAC	V_{OUT} hysteretic control & DCO	Voltage sensor
Continuous MPPT	**Yes**	Yes	Yes	No	No
V_{MPP}/V_{OC} ratio	**Adaptable**	Fixed	Adaptable	Adaptable	Adaptable
P_{OUT} range for tracking efficiency 97% (μW)	**130 – 1900 (14.6×)**	N/A	510 – 2200 (4.3×)	N/A	N/A
Peak conv. efficiency (%)	**91.5**	85.4	88.9	72	81
Output power (μW)	**30 – 6056**	1 – 176	60 – 2794	1 – 35	1 – 50
Max. power density (μW/mm^2)	**797**	49	582	63	13
Peak end-to-end efficiency (%)	**90.4**	85.4	86.2	N/A	N/A
Freq range (kHz)	**41 – 4709**	15 – 67.1	54 – 3400	35 – 1370	20 –1000
Flying Capacitor (nF)	**19.66**	7.8	15	N/A	0.5
Area (mm^2)	**7.6**	3.56	4.8	0.552	4

Furthermore, the adoption of the hill-climbing method allows the EHI to adapt to different energy sources, as it does not rely on the fixed ratio of the MPP to open-circuit voltage. It is worth noting that the metric "P_{OUT} range for tracking efficiency >97%" is explicitly compared only with [2], since other listed works do not provide enough data on tracking efficiency versus output power to define this range. Compared to the previous study [2], the proposed EHI achieves a 3.4-fold increase (14.6 vs 4.31) in the dynamic range of output power with a tracking efficiency exceeding 97%. We identify this extended dynamic range as the main figure of merit (FoM) for the proposed MPPT interface. By enabling precise tracking over a broader power range, the system can fully utilize the high PCE of the CSCR topology. This leads to a superior peak end-to-end efficiency of 90.4% and maintains high efficiency (in the mid-to-high 80% range) across a wide operating region. The integrated CSCR SC converter also demonstrates a peak PCE of 91.5% and a maximum output of 6.05 mW. By performing MPPT based on output power rather than input power, as done in prior work [1], the proposed system achieves a 5% improvement in peak end-to-end efficiency, highlighting its enhanced performance and energy optimization capabilities.

The proposed design has an area of 7.6 mm^2 and delivers a maximum power density of 797 μW/mm^2, which remains competitive with the other EHIs in Table II.

V. CONCLUSION

This article presented a novel EHI structure that achieves high MPPT efficiency across a wide power range using a CSCR SC dc–dc converter. The proposed system incorporates an output power monitor circuit that accounts for the unit step voltage of the flying capacitor alongside a specially designed exponential DCO to enhance performance. A switch matrix-based CSCR SC dc–dc converter was also developed to achieve high PCE. As a result, the power range with MPPT efficiency exceeding 97% expanded by 3.4 times compared to prior work, and a peak end-to-end efficiency of 90.4% was achieved.

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