Regionalized Multiobjective Optimization of Pin-Fin Heatsink for Enhanced Thermal Uniformity in Automotive SiC Power Modules

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***Abstract*—Silicon carbide (SiC) power modules, with its advantages of high-voltage tolerance, high-temperature operation capability, high-switching frequency, and low power loss, are progressively replacing traditional silicon-based devices in applications such as new energy vehicles, renewable energy generation, and rail transportation. However, as the voltage and current ratings of SiC power modules increase, their power density escalates significantly, exacerbating thermal nonuniformity within the modules. This article proposes a regionalized multiobjective optimization method that explicitly addresses thermal nonuniformity, alongside module thermal resistance and pumping power. The methodology integrates a genetic algorithm with finite element analysis. Using the Pin-Fin heatsink of an automotive power module as a case study, an optimized design was developed and validated through a back-to-back test platform. Experimental results show that, compared to the traditional Pin-Fin heatsink, the optimized design achieves a 43.7% improvement in thermal uniformity, a 6.2% reduction in thermal resistance, and a 9.8% decrease in pumping power—without added costs.**

***Index Terms*—Back-to-back test platform, genetic algorithm (GA), pin-fin heatsink, silicon carbide (SiC) power modules, thermal uniformity.**

I. Introduction

Over the past three decades, SiC devices have undergone significant research and development advancements. Today, they play a critical role in electric vehicles and renewable energy systems, where their lower ON-state resistance and higher switching frequency make them highly suitable for high-power-density applications [1], [2]. Although SiC exhibits high-temperature tolerance, its practical operating temperature remains confined to 175 °C–200 °C due to limitations in packaging technology [3]. Moreover, the heat flux of SiC devices increases significantly with elevated voltage and current ratings. Consequently, thermal management in SiC power modules has emerged as a critical challenge [4].

Air cooling, the most conventional thermal management method, has shown notable advancements in power module applications. Investigated techniques include the integration of heat pipes into air-cooled heatsink [5], innovative air-cooled structures optimized through GA [6], and advanced packaging designs utilizing aluminum nitride ceramic substrates [7]. While these strategies lower thermal resistance compared to traditional air-cooled configurations, they are still limited by the inherent constraints of air's cooling capacity, which does not meet the high heat flux requirements of SiC power modules [8]. So, the majority of research efforts have been focused on the liquid cooling.

Research on liquid cooling has been extensive, covering a wide range of advanced heat dissipation structures, such as microchannel heatsink [9], various Pin-Fin configurations [10], ShowerPower heatsink [11], and irregular geometries heatsink obtained through topology optimization [12]. It also includes high thermal conductivity materials, for instance, Cu-Diamond composite heatsink [13] and multilayer graphene films grown via CVD on DBC surfaces [14]. Furthermore, significant progress has been made in advanced packaging techniques, including double-sided cooling [15], direct metal bonding without DBC [16], jet impingement cooling, and spray cooling approaches [14]. Practical implementations of microchannel heatsinks are limited by high flow resistance and vulnerability to clogging, while ShowerPower heatsink experience challenges similar to hydraulic impedance. Although topology-optimized designs are thermally efficient, they face issues related to algorithms and manufacturability. In addition, emerging materials and advanced packaging strategies continue to struggle with cost scalability and long-term reliability. As a result, Pin-Fin heatsinks remain the most widely adopted solution in industrial

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applications, offering a favorable balance of thermal efficiency and manufacturability.

Emerging cooling media, such as phase change cooling [17], [18] and nanofluids [19], have attracted considerable interest in the field of thermal management research. Existing studies on phase change cooling primarily focus on addressing transient overload conditions in power devices. This often needs a hybrid integration with conventional cooling methods to manage heat flow during normal operating conditions. Conversely, nanofluids face considerable challenges, including issues such as nanoparticle sedimentation, increased flow resistance, and cost-related barriers to practical implementation.

Among existing cooling solutions, the Pin–Fin heatsink stands out as the most well-established and widely adopted configuration for thermal management in power modules, and has consequently been the focus of extensive research. Various strategies have been developed to enhance its performance. For instance, a variable-density topology optimization method has been applied to refine the Pin–Fin structure, achieving a 12% reduction in junction-to-flow thermal resistance compared to traditional designs while simultaneously addressing hydraulic pressure drop [20]. In another approach, the integration of response surface methodology with topology optimization enabled synergistic improvement in thermal efficiency and flow resistance, leading to a 7.62% decrease in thermal resistance relative to commercial automotive power modules under both steady and dynamic operating conditions [21]. Further progress is made through the use of a parabolic thermal model combined with the teaching–learning-based optimization (TLBO) algorithm, which not only optimized the Pin–Fin heatsink but also reduced cooling system weight and increased the power density of the converter [22]. In addition, optimization of Pin–Fin dimensions and spacing via a lattice Boltzmann method integrated with a turbulence model has been shown to significantly boost the thermal performance of power modules [23]. However, these methodologies exhibit the following limitations.

1) Narrow optimization objectives primarily focus on thermal resistance and pressure drop, while giving insufficient attention to thermal uniformity across the module.
2) Absence of a comprehensive optimization framework that integrates cold plate design. While conventional designs often assume identical depths for the cold plate and Pin-Fin height, the depth can be optimized independently as a design parameter to change fluid flow distribution and thermal resistance.
3) Overreliance on numerical simulations without experimental validation in real-world high-power applications limits practical relevance and scalability.

Beyond these limits, temperature nonuniformity remains a critical challenge in multichip parallel power modules, with a thermal gradient reaching up to 15 °C between the minimum and maximum junction temperatures of paralleled chips under severe operating conditions [24]. According to the 10 °C rule (where the lifespan of electronic components is approximately halved with every 10 °C increase in operating temperature) [25], this significant thermal gradient severely compromises the reliability and operational lifetime of power modules.

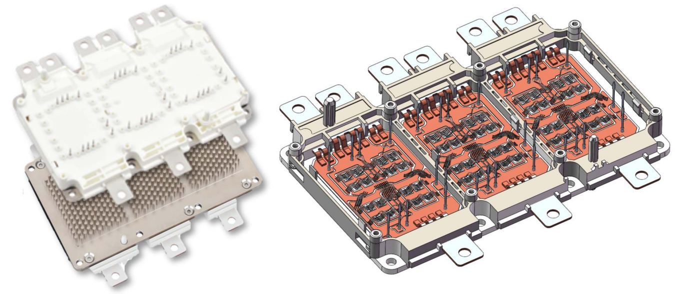


Fig. 1. 1200 V/640 A SiC power module packaging structure.

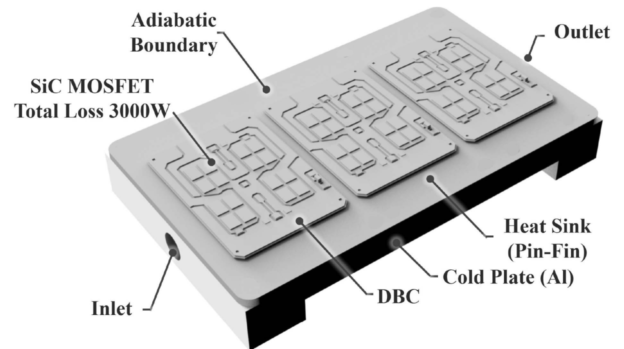


Fig. 2. Simplified thermal simulation model.

This article proposes a regionalized multiobjective optimization method that incorporates thermal uniformity as a critical design metric, partially mitigating temperature nonuniformity in multichip parallel power modules while simultaneously reducing the thermal resistance of the module and the pumping power. The rest of this article is organized as follows. Section II analyzes the root causes of thermal nonuniformity in power modules. Subsequently, a subregional heatsink optimization strategy to mitigate temperature gradients across power modules is proposed based on the thermal resistance decomposition of the junction-to-fluid in power modules. Furthermore, a GA-FEA automated co-optimization framework is introduced, detailing the workflow using an automotive-qualified power module with an integrated Pin-Fin heatsink as a case study. Section III presents the optimization of the Pin-Fin heatsink and validates the optimized structure's thermal performance through numerical simulations. Section IV describes the experimental validation of the optimized heatsink using a back-to-back test platform. Finally, Section V concludes this article.

II. Proposed Optimize Methodology

A. Thermal Nonuniformity in Power Modules

Fig. 1 illustrates the packaging structure of a 1200 V/640 A automotive-qualified SiC power module. Each phase leg consists of eight paralleled SiC MOSFET dies integrated with a Pin-Fin heatsink for direct liquid cooling. To enable efficient thermal finite element analysis (FEA) simulation, the geometric model is simplified by omitting aluminum bond wires, gate signal

TABLE I
MATERIAL PROPERTIES OF THE PACKAGING COMPONENTS AND COOLANT

	Material	k[W/(m·K)]	Size[mm]
Dies	SiC	490	5.36×4.44×0.13
Dies Solder Layer	SAC305	38	5.36×4.44×0.02
DBC Copper Layer	Cu	380	63.5×44.5×0.3
DBC Ceramic	Si_3N_4	70	63.5×44.5×0.32
Substrate Solder Layer	SAC305	38	63.5×44.5×0.15
Heatsink	Cu	380	152×92×3
Cold Plate	Al 6061	167	152×92×16
Coolant	50% Ethylene Glycol	0.406	——

pins, and the encapsulating housing. Fig. 2 shows the simplified thermal simulation model and its corresponding boundary conditions. Given the low thermal conductivity of the encapsulant and housing, all external surfaces were defined as adiabatic boundaries. Table I summarizes the material properties of the packaging components and coolant used in the FEA simulation. The coolant was modeled as an incompressible viscous fluid with an inlet temperature of 65 °C and a flow rate of 10 L/min. For quantitative analysis, the following metrics are established: Maximum junction-to-fluid thermal resistance R_{thjf}, thermal uniformity index Ψ, and pumping power P.

The maximum junction-to-fluid thermal resistance of the power module is defined as follows:

$$R_{\text{thjf}} = \frac{T\text{in}_{\text{jmax}}}{P_{\text{loss}}} \tag{1}$$

where T_{jmax} refers to the peak temperature at the junctions of the module's dies, and T_{in} indicates the temperature of the incoming cooling fluid. Meanwhile, P_{loss} refers to the total power loss of the power module. The junction-to-fluid thermal resistance plays a vital role in assessing the effectiveness of liquid cooling in power modules.

The thermal uniformity index is defined as follows:

$$\Psi = \frac{T_{\text{jmax}} - T_{\text{jmin}}}{T\text{in}_{\text{jmax}}} \tag{2}$$

where T_{jmin} corresponds to the minimum junction temperature observed across the semiconductor dies within the module. The higher this value, the worse the temperature uniformity across the chips in the module.

In addition, the pumping power P required for liquid cooling is also a key factor in evaluating the thermal performance of the cooling configuration as follows:

$$P = Q \cdot \Delta p \tag{3}$$

where Q is the inlet flow rate, Δp is the inlet pressure drop. Under identical conditions, a lower value of P indicates better cooling performance of the thermal management system.

Fig. 3 shows the COMSOL Multiphysics simulation results demonstrate that, under a power loss of 3000 W in the power module, the maximum junction temperature of the dies reaches 123.44 °C, while the minimum is 111.36 °C. This results in a temperature difference of 12.08 °C, corresponding to a 15.4% temperature nonuniformity across the dies.

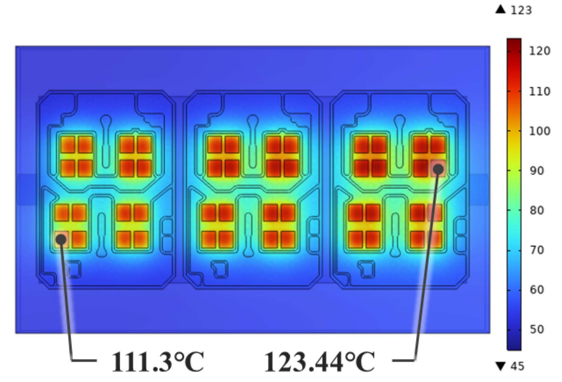


Fig. 3. Simulation results of the 1200 V/640 A SiC power module.

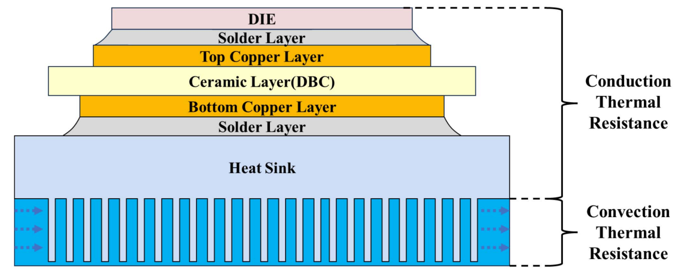


Fig. 4. Decomposition of the junction-to-fluid thermal resistance.

The temperature nonuniformity can be primarily attributed to following two factors.

1) As illustrated in Fig. 4, the junction-to-fluid thermal resistance primarily consists of two components: conduction thermal resistance and convection thermal resistance. Since each layer contributing to conduction thermal resistance has identical geometry and material properties, this aspect of thermal resistance remains consistent throughout the module. Moreover, convection thermal resistance is significantly influenced by flow velocity and contact area. In a traditional Pin-Fin heatsink, both the pin structures and flow velocity are uniform, resulting in nearly uniform convection thermal resistance across all regions.
2) The series configuration of the coolant pathways results in a progressive increase in the temperature of the downstream fluid. With a consistent junction-to-fluid thermal resistance, this phenomenon contributes to elevated junction temperatures in the downstream chips, as shown in Fig. 5.

Based on the two factors discussed above, there are two approaches to reducing the temperature nonuniformity within the module.

1) Keeping the package structure unchanged, which means the components of the junction-to-fluid thermal resistance remain the same. In this case, using parallel coolant pathways helps prevent the accumulation of heat in the coolant, thereby reducing the temperature gradient across the dies, as shown in Fig. 6(a).

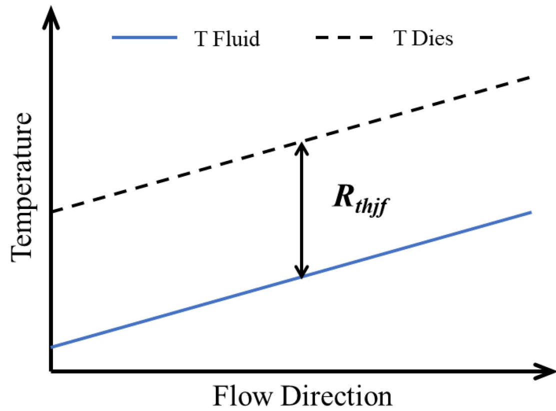
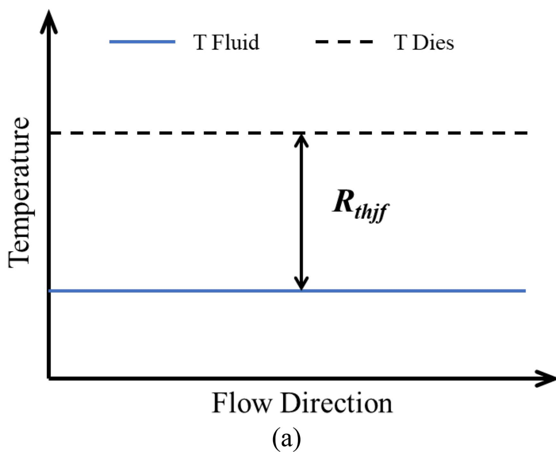


Fig. 5. Temperature nonuniformity in the traditional cooling configuration.



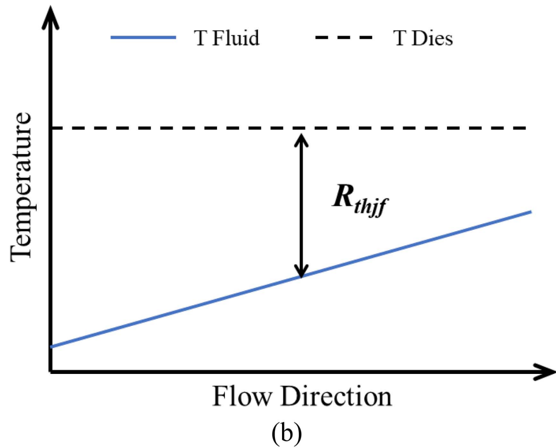


Fig. 6. (a) Thermal uniformity enhancement by using parallel coolant pathways. (b) Thermal uniformity enhancement with reduction of R_{thjf}.

2) Maintaining the series coolant pathway but altering the composition of the junction-to-fluid thermal resistance. Given the arrangement of the dies, insulation, and mechanical support, altering the conduction thermal resistance is quite challenging. Therefore, the emphasis should be placed on modifying the convection thermal resistance by adjusting the heatsink geometry positioned beneath the dies. The intended outcome, as shown in Fig. 6(b), is a progressive reduction in junction-to-fluid thermal resistance along the flow direction, with a particular focus on decreasing convection thermal resistance.

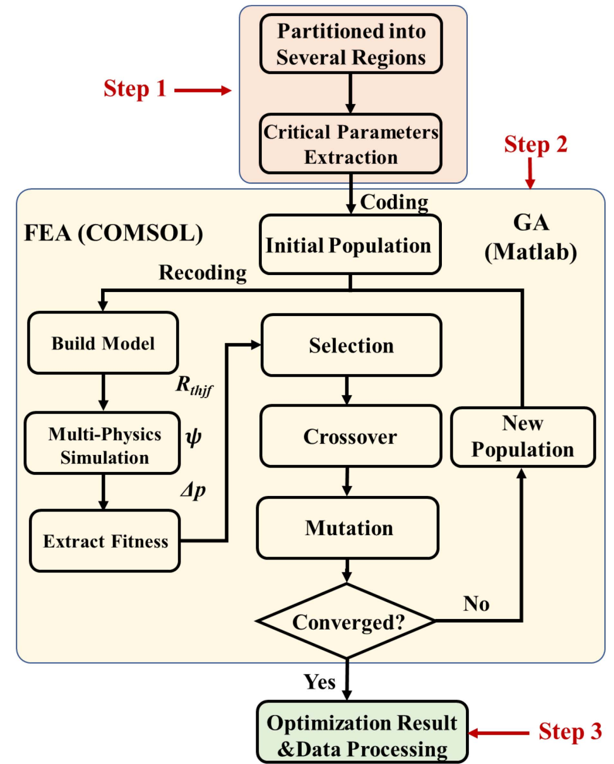


Fig. 7. Flowchart of the proposed multiobjective optimization method.

B. Optimize Methodology

Since parallel coolant pathways have higher resistance and a more complex structure, this article chooses the second method to resolve the temperature nonuniformity within the module.

The flowchart of this method is shown in Fig. 7, which can be divided into the following three steps.

1) *Step 1*: Based on the layout of the power module dies, the heatsink to be optimized is divided into several distinct optimization regions along the flow direction of the coolant. The key structural parameters of the corresponding heatsink are then extracted. Fig. 8 shows this process using a Pin-Fin heatsink as an example. The Pin-Fin heatsink is divided into three optimization regions along the coolant flow direction, and the key structural parameters are extracted: pin height H, pin pitch in the y direction D_y, pin pitch in the x-direction D_x, pin radius R, and the depth of the cooling plate C. A similar operation can be applied to other types of heatsinks.
2) *Step 2*: A regionalized multiobjective optimization algorithm coupled with FEA is employed to automate the design of region-specific heatsink structures. Taking the GA as an example, each individual in the GA represents a set of critical structural parameters of the heatsink. The optimization process initiates with coding to generate an initial population of sufficient size. The coded structural

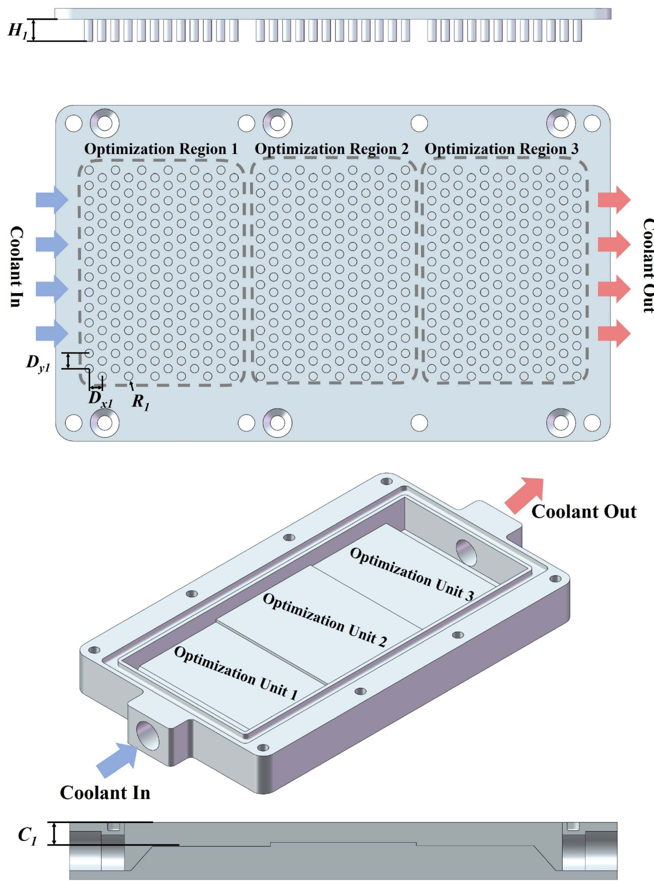


Fig. 8. Explanation of Step 1 using the Pin-Fin heatsink as an example.

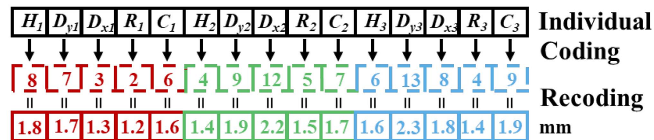


Fig. 9. Coding and recoding of the critical structural parameters.

parameters are then recoded to reconstruct the geometric model of the power module heatsink. Fig. 9 illustrates the coding and recoding process, where the structural parameters are constrained within a range of 1–3 mm with a step size of 0.1 mm. Subsequently, multiphysics simulations are conducted in FEA software to evaluate the fitness of each individual based on R_{thjf}, Ψ, and P. Individuals with higher fitness scores are chosen for the next iteration. During the generation of offspring, crossover and mutation operations are implemented. Crossover can take the form of single-point or multipoint variants: single-point crossover involves exchanging one structural parameter between two individuals, as shown in Fig. 10(a), whereas multipoint crossover swaps all structural parameters within two optimized regions, as shown in Fig. 10(b). Mutation injects stochastic variations into specific parameters of an individual based on a predefined probability, as illustrated in Fig. 11.

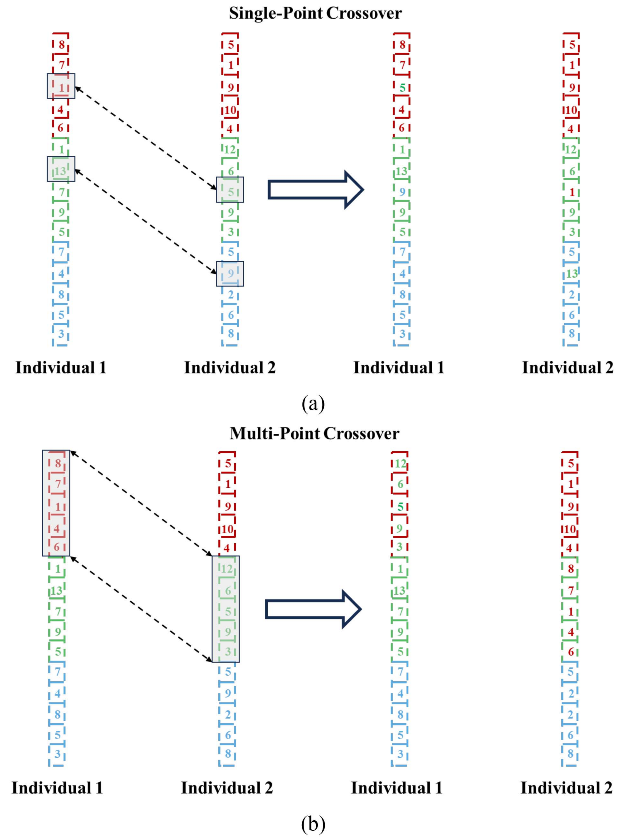


Fig. 10. (a) Single-point crossover. (b) Multipoint crossover.

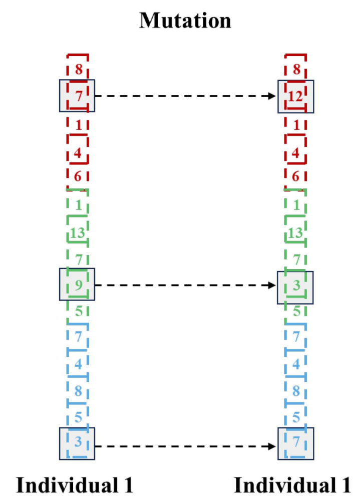


Fig. 11. Mutation of individuals.

3) *Step 3:* Once the convergence criteria have been met, the results from the optimization process undergo a systematic evaluation. Each individual is plotted within a coordinate system, with the optimization objectives as axes, resulting in the creation of a Pareto front. From this front, the optimal solution is then meticulously chosen based on the established optimization objectives, as illustrated in Fig. 12.

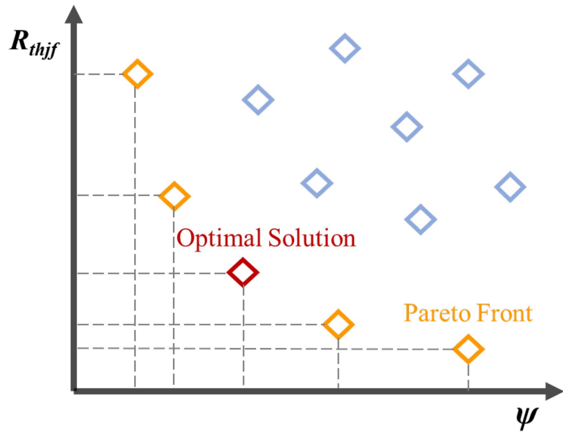


Fig. 12. Optimal solutions in the Pareto front.

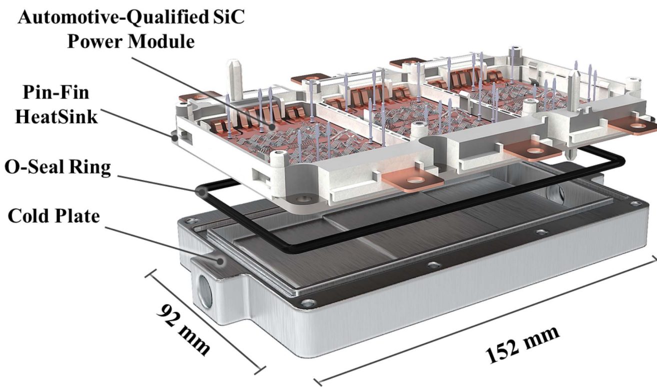


Fig. 13. Mechanical configuration of the automotive-qualified SiC power module.

In the described workflow, parameteric modeling and multiphysics simulations are conducted using COMSOL software, while the GA and data processing tasks are implemented in MATLAB. These two platforms are interconnected through COMSOL Multiphysics with MATLAB, enabling automated optimization.

III. Optimization of Traditional Pin-Fin Heatsink

A. Design of Automotive-Qualified SiC Power Module With Pin-Fin Heatsink

Based on the optimization methodology proposed in Section II, this section presents an enhanced design of a conventional Pin-Fin heatsink validated through multiphysics simulations. Drawing from the packaging architecture and layout of Infineon HybridPACK Drive CoolSiC automotive-qualified SiC power module, a direct liquid-cooled automotive-qualified SiC power module with a Pin-Fin heatsink was developed. As illustrated in Fig. 13, the mechanical configuration features three half-bridge substrates welded to a copper Pin-Fin heatsink. Each phase leg comprises eight parallel-connected SiC MOSFET dies, excluding antiparallel Schottky barrier diode integration. The module achieves liquid-cooling sealing via bolts and an O-seal ring interfaced with a water-cooling plate. The relevant material properties of the power module, water-cooling plate, and coolant are summarized in Table I.

In Fig. 8, the critical structural parameters of the Pin-Fin heatsink are detailed. To ensure the mechanical strength of the pins, a minimum pin radius, denoted as R_i, is set at 1.1 mm. Due to manufacturing constraints, the spacing between the pins in both the *x*- and *y*-directions, referred to as D_x and D_y, cannot be reduced below a minimum of 1.5 mm. In addition, excessively large or small structural dimensions can adversely affect the heat dissipation performance of the Pin-Fin heatsink. Therefore, the maximum limit for R_i is established at 2.5 mm, while the upper limits for D_x and D_y are set at 5 mm. A pin height that is too small negatively impacts heat dissipation, whereas excessively large heights are restricted by the dimensions of the cold plate. Consequently, the pin height, H, is specified to range from 3 mm to 8 mm. Furthermore, the depth, C, of the cold plate must exceed H by a margin of 0.2 mm to 1.5 mm. Since excessively small optimization step sizes have a negligible effect on the optimization results, the optimization step size for these parameters is set at 0.1 mm.

Considering the constraints of junction-to-fluid thermal resistance, thermal uniformity, and pumping power, the multi-objective optimization problem can therefore be formulated as follows:

$$\begin{cases} Min: R_{\text{thjf}},\ \Delta p,\ \psi \\ \text{s.t.}\quad 1.1\text{ mm} \le R_i \le 2.5\text{ mm}\ \ i = 1,2,3 \\ \quad 1.5\text{ mm} \le D_{yi} \le 5\text{ mm} \\ \quad 1.5\text{ mm} \le D_{xi} \le 5\text{ mm} \\ \quad 3\text{ mm} \le H_i \le 8\text{ mm} \\ \quad (H_i + 0.2\text{ mm}) \le C_i \le (H_i + 1.5\text{ mm}) \end{cases} \tag{4}$$

B. Optimization Result and Simulation Validation for the Optimized Heatsink

The optimization of the Pin-Fin heatsink for the SiC power module is conducted according to the optimization process described in Section II, following the constraints outlined in (4). Due to the necessity for multiphysics simulations for each individual, the power module is simplified as shown in Fig. 2. Moreover, the population size of the genetic algorithm (GA) is set to 50, with a maximum iteration limit of 10. The probabilities for crossover and mutation are defined as 0.7 and 0.05, respectively. After executing the optimization method detailed in Section II, the top 10 solutions from each generation are selected, resulting in a collection of 100 optimized solutions, as illustrated in Fig. 14. The blue points represent nonPareto solutions, while the red points indicate the Pareto frontier, and the stars denote the selected optimal solution. Given that the thermal management system prioritizes junction-to-fluid thermal resistance and thermal uniformity, greater emphasis is placed on these two factors during the selection of the optimal solution, which consequently leads to a higher pressure drop. Therefore, in subsequent simulations, the pressure drop is maintained at a consistent boundary condition to facilitate a comparative analysis of the thermal performance between the traditional Pin-Fin heatsink and the optimized heatsink.

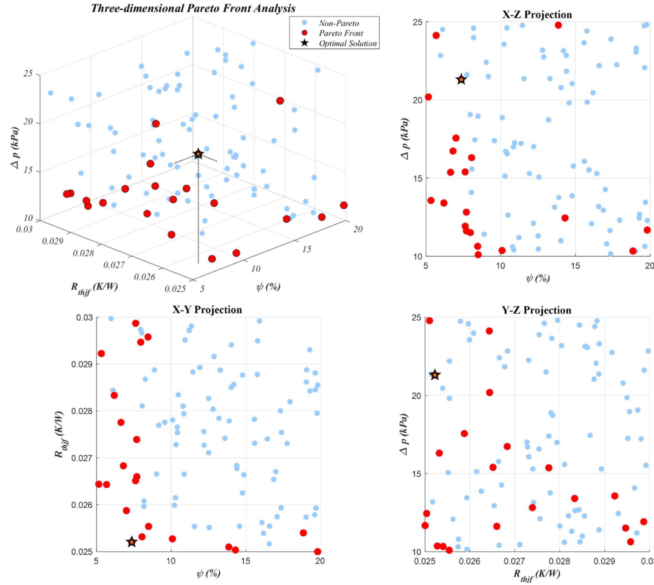


Fig. 14. Pareto optimal solution of R_{thjf}, Ψ, and Δp.

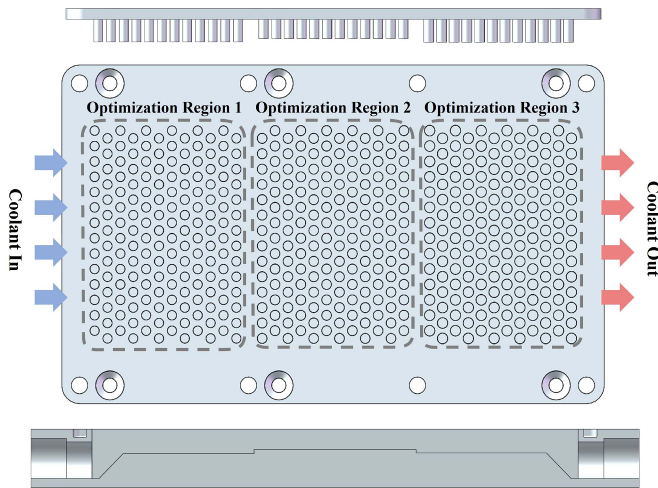


Fig. 15. Configuration of the optimal Pin-Fin heatsink.

TABLE II
PARAMETERS OF OPTIMAL PIN-FIN HEATSINK

	H(mm)	D_y(mm)	D_x(mm)	R(mm)	C(mm)
Region 1	6.2	4.18	3.61	1.28	6.7
Region 2	5.3	4.18	3.61	1.35	5.6
Region 3	6.3	4.18	3.61	1.44	6.5

Fig. 15 shows the configuration of the optimal Pin-Fin heatsink. The structural parameters for the selected optimal Pin-Fin heatsink and the traditional Pin-Fin heatsink are presented in Tables II and III. To improve the convergence of the solution, the D_x and D_y dimensions of all optimized regions have been treated as two identical optimization variables, due to the high number of factors involved in the optimization process.

TABLE III
PARAMETERS OF TRADITIONAL PIN-FIN HEATSINK

	H(mm)	D_y(mm)	D_x(mm)	R(mm)	C(mm)
Region 1	6.0	4.10	3.42	1.10	6.0
Region 2	6.0	4.10	3.42	1.10	6.0
Region 3	6.0	4.10	3.42	1.10	6.0

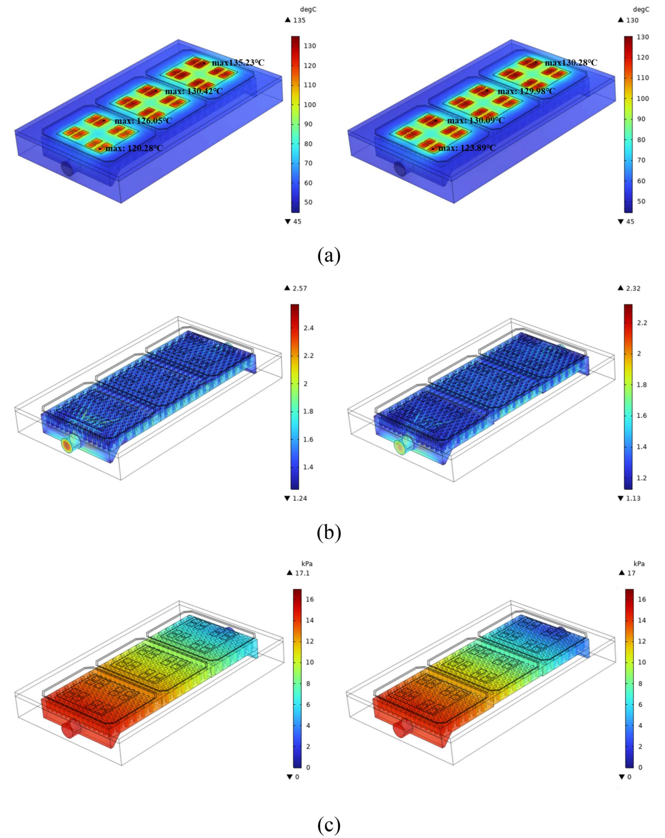


Fig. 16. Simulation results of power module with traditional Pin-Fin heatsink (left) and optimized Pin-Fin heatsink (right). (a) Temperature distribution diagram. (b) Fluid flow velocity diagram. (c) Fluid pressure drop diagram.

Thermal flow coupling simulations are conducted on the SiC power module integrated with both the traditional Pin-Fin heatsink and the optimized Pin-Fin heatsink, maintaining identical boundary conditions. The simulation results are illustrated in Fig. 16. With a 17 kPa inlet/outlet pressure drop and a total power loss of 3300 W, the maximum junction temperature of the traditional SiC power module is recorded at 135.23 °C, with a maximum temperature difference of 12.95 °C between the half-bridges. Following optimization, the maximum junction temperature decreased to 130.28 °C, and the maximum temperature difference between the half-bridges is reduced to 6.39 °C. In comparison, the optimized heatsink exhibited a 5.6% reduction in junction-to-fluid thermal resistance and a 50.7% improvement in thermal uniformity, resulting in a significant improvement in thermal performance. Moreover, compared to the traditional Pin-Fin heatsink, the pumping power is reduced by 10.5%.

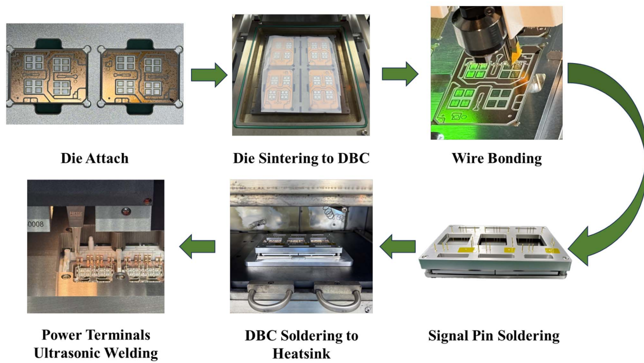


Fig. 17. Fabrication of automotive-qualified SiC power module.

IV. Experimental Verification

A. Fabrication of Automotive-Qualified SiC Power Module

To validate the effectiveness of the optimization method, the automotive-qualified SiC power module described in Section III is fabricated following the process shown in Fig. 17. First, the SiC dies are attached to the DBC substrates precoated with nano-silver paste. A protective polytetrafluoroethylene film is subsequently applied over the dies to prevent oxidation and contamination by isolating them from atmospheric oxygen, moisture, and impurities. Furthermore, the film's elastic properties facilitated uniform pressure distribution during sintering, resulting in a consistent bond-line thickness. Following die sintering, wire bonding is conducted using an automatic bonder to establish electrical connections between the dies and the DBC substrates, thereby completing both the power and driver circuitry. Next, signal pins and the heatsink are positioned using fixtures, and the driver terminals along with the heatsink are soldered to the DBC. Finally, ultrasonic welding is utilized to attach the power terminals to the DBC, and the housing is bolted to the heatsink for mechanical reinforcement. The fabricated power module is illustrated in Fig. 18(a). In addition, it should be noted that the module is intentionally left unencapsulated to enable precise temperature extraction from the semiconductor dies during subsequent thermal analysis characterization.

Simultaneously, both optimized and conventional Pin-Fin heatsinks, along with their corresponding water cold plates, are machined using CNC technology according to the specifications detailed in Tables II and III. The designs of these components are illustrated in Fig. 18(b). Furthermore, the processing techniques and procedures employed are identical, resulting in no additional processing costs. The module features STMicroelectronics' SCT130N120G3D8AG SiC MOSFETS (1200 V/16 mΩ), with the heatsink crafted from copper and the water-cooling plate constructed from aluminum.

B. Experimental Setup

To evaluate the thermal performance of the power module with an optimized heatsink, a back-to-back three-phase inverter test system with purely inductive loads is utilized, as shown in Fig. 19. This method alleviates the stringent requirements for high-capacity power supplies and load equipment typically

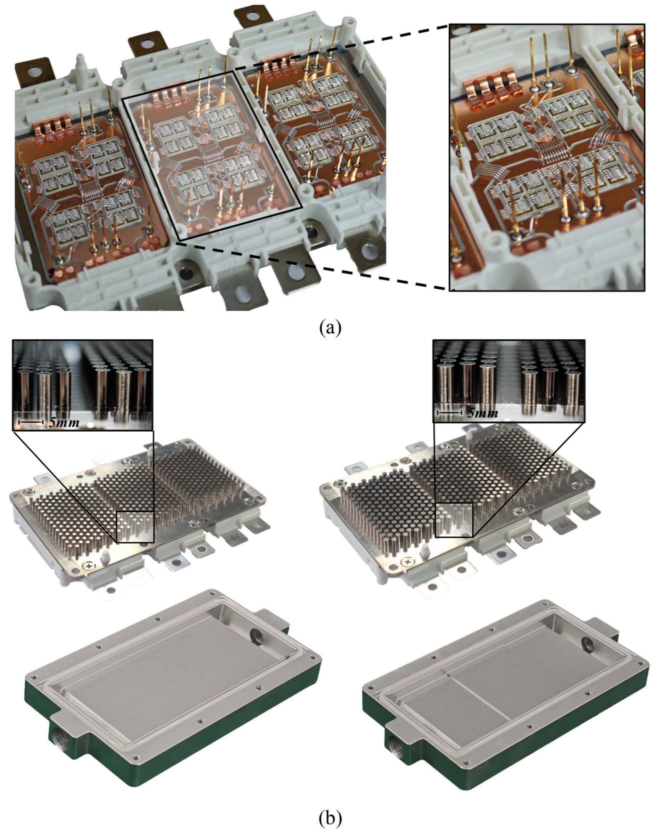


Fig. 18. (a) Fabricated power module. (b) Traditional Pin-Fin cooling configuration (left) and optimized Pin-Fin cooling configuration (right).

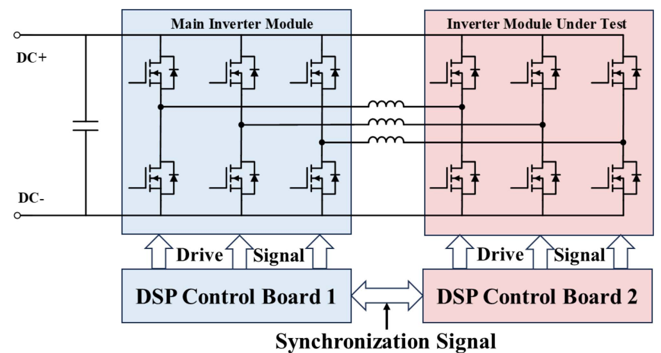


Fig. 19. Back-to-back three-phase inverter test system main circuit schematic.

associated with direct-drive full-power testing. By adjusting the phase difference between the output voltages of the paired inverters, the load current magnitude can be accurately controlled, thus reducing the demands on external testing infrastructure. In this setup, the main inverter module, the device-under-test (DUT) inverter module, and three purely inductive loads are interconnected in a back-to-back three-phase configuration. During testing, synchronized control signals are used to initiate the simultaneous startup of both inverters, generating three-phase sinusoidal fundamental voltages with identical frequency, phase, and amplitude. Under these conditions, the voltage differential across the inductors approached zero, resulting in a minimum

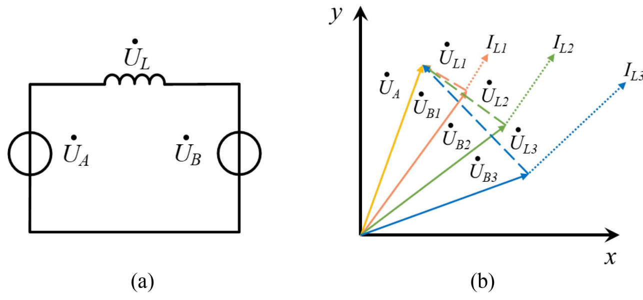


Fig. 20. (a) Test circuit principle. (b) Test circuit phase diagram.

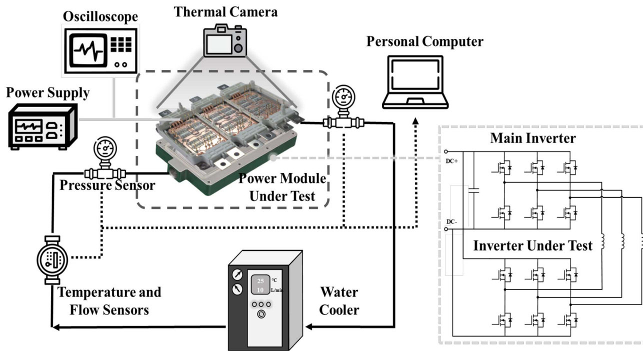


Fig. 21. Schematic of the thermal testing platform.

current flow. Once stabilized at the target voltage level, the output voltage phase of the DUT inverter is gradually shifted to introduce a controlled phase discrepancy between the inverters. This phase modulation progressively increased the three-phase current until the rated current is reached. The system maintained this operational state until thermal equilibrium is achieved in the power module, completing the thermal evaluation.

Due to three-phase symmetry, the test circuit can be equivalently simplified by a simplified single-phase schematic, as shown in Fig. 20(a). Fig. 20(b) illustrates the relationship between voltage phase difference and current magnitude.

A dedicated thermal test platform is constructed based on the three-phase back-to-back architecture, with its schematic shown in Fig. 21. The physical implementation (see Fig. 22) features independent liquid cooling configuration for both the main and DUT inverter modules, enabling precise monitoring of coolant temperature and flow rate. Deionized water, maintained at a constant inlet temperature of 45 °C, served as the coolant, with flow rate controlled via a valve positioned near the inlet. Pressure sensors (600 kPa range, 0.2% accuracy) are installed at the cold plate inlet and outlet to measure pressure drop, while downstream flow and temperature sensors (0.2% accuracy) quantified the coolant flow rate and temperature.

To improve the accuracy of temperature measurements, a uniform layer of black insulating paint is applied to the surface of the module, as illustrated in Fig. 23, thereby optimizing its emissivity for infrared thermography. Die temperatures are recorded using a Guide PS610 infrared thermal camera. At the same time, the rated voltage and rated current of the SiC power modules are measured using an oscilloscope to ensure that the

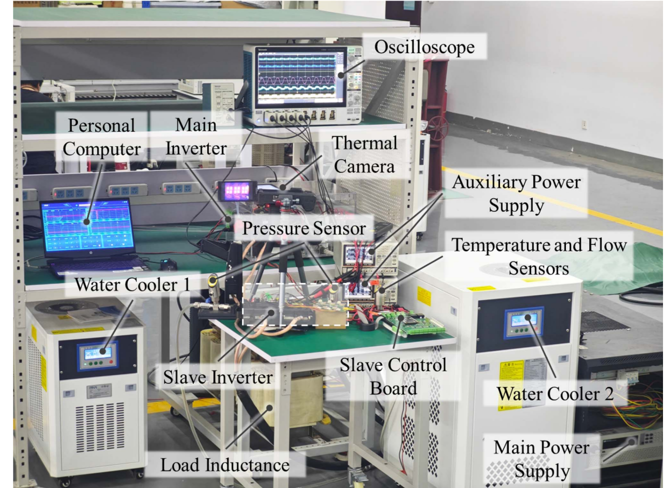


Fig. 22. Experimental setup for the SiC power module thermal test.

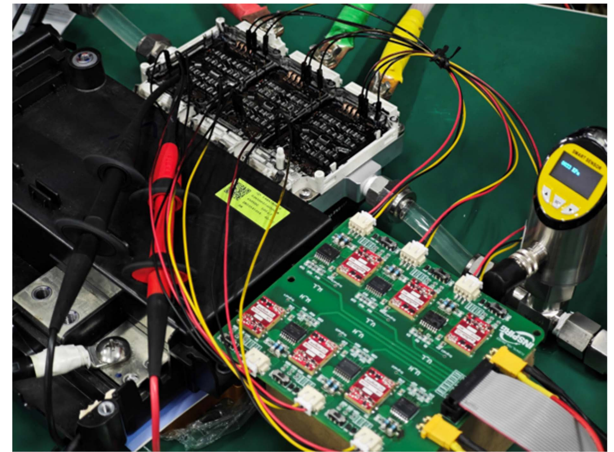


Fig. 23. SiC module sprayed with insulating black paint and driver board.

heat dissipation performance of the heatsink is evaluated under the same operating conditions.

C. Experimental Results

The coolant employed is deionized water. In automotive applications, the power module typically operates in a high-temperature environment, prompting the coolant inlet temperature to be set at 45 °C. A flow valve positioned near the inlet regulates the flow rate, ensuring a pressure drop of 17 kPa between the inlet and outlet. Given the lack of potting on the power module to prevent creepage, the bus input voltage is established at a fixed level of 350 V.

Fig. 24 displays infrared thermal images of the SiC power modules under rated currents of 220 A, 260 A, and 300 A. The data shows that as the rated current increases, the highest junction temperature of the power module equipped with a conventional Pin-Fin heatsink rises, leading to a greater maximum temperature difference among the three half-bridges. Conversely, while the peak junction temperature of the power module utilizing an optimized Pin-Fin heatsink also increases,

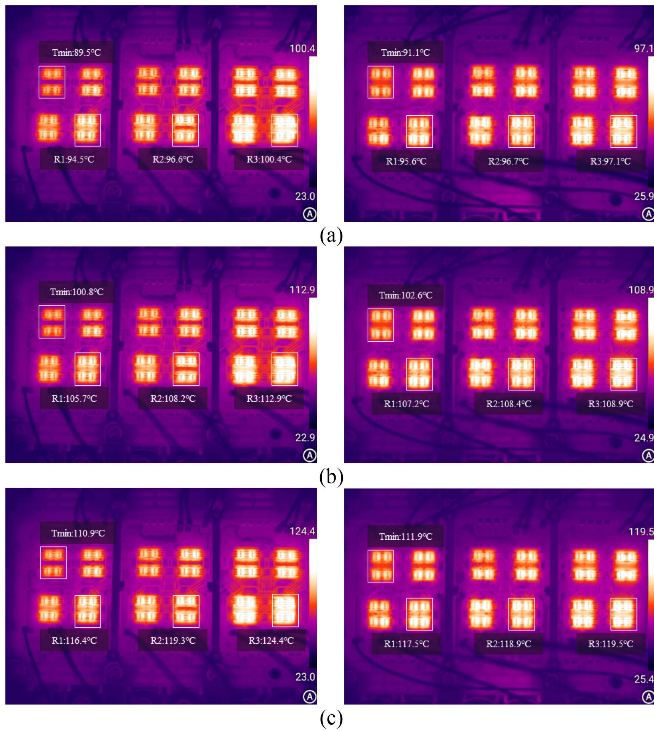


Fig. 24. Temperature distribution of the power module with traditional Pin-Fin heatsink (left) and optimized Pin-Fin heatsink (right) in an infrared thermal imaging camera at (a) rated current of 220 A, (b) rated current of 260 A, and (c) rated current of 300 A.

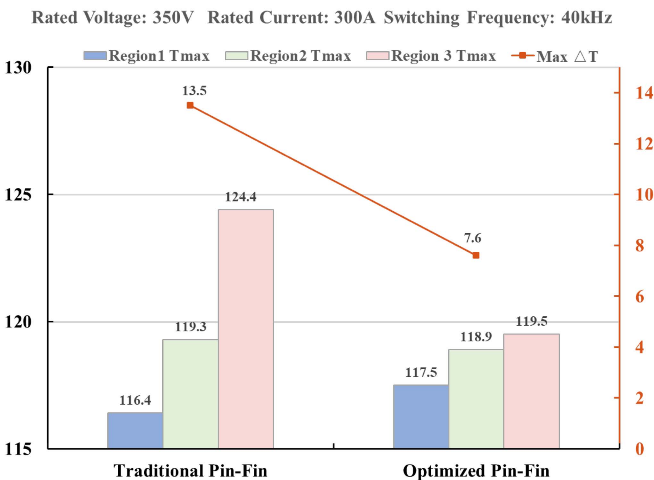


Fig. 25. Comparison of thermal performance between two heatsinks at rated current 300 A operating condition.

it remains significantly lower than that of the conventional heatsink, and the maximum temperature difference between the three half-bridges is notably reduced.

Fig. 25 shows the highest junction temperature in optimized regions and the maximum temperature difference between the dies in the entire module at rated current 300 A for both the power module with the traditional Pin-Fin heatsink and the optimized Pin-Fin heatsink. The optimized Pin-Fin heatsink significantly improves both the junction-to-fluid thermal resistance and the thermal uniformity of the SiC power module.

At a rated current of 300 A, the maximum junction temperature of the power module integrated with a conventional Pin-Fin heatsink reaches 124.4 °C, accompanied by a maximum temperature difference of 13.5 °C. In contrast, the power module paired with the optimized Pin-Fin heatsink displays a maximum junction temperature of 119.5 °C, with a maximum temperature difference of 7.6 °C. This data illustrates that the optimized Pin-Fin heatsink has successfully reduced the junction-to-fluid thermal resistance by 6.2% and enhanced thermal uniformity by 43.7%, ultimately contributing to the long-term reliability of the SiC power module. Furthermore, the optimized Pin-Fin heatsink demonstrates an improvement in pumping efficiency by 9.8%. The following factors contribute to these improvements:

1) Optimizing each region of the cold plate is essential. The height difference between the cold plate and the Pin-Fin structure enables the circular bottom surface of the pins to aid in heat dissipation, thereby increasing the heat dissipation area. In addition, variations in height in certain areas of the water-cooled plate leads to changes in the cross-sectional area of the fluid channel, which enhances fluid disturbance and improves heat dissipation.
2) Different regions of the heatsink have distinct structures and junction-to-fluid thermal resistances, compensating for heat accumulation in the fluid and improving the temperature uniformity of the module.
3) Compared to the traditional Pin-Fin heatsink, the section of the cold plate where the depth exceeds the pins' length releases some pressure drop due to the absence of pins, improving pumping efficiency.

V. Conclusion

This study introduces a regionalized multiobjective optimization methodology for Pin-Fin heatsink of SiC power modules that explicitly addresses thermal uniformity, effectively tackling issues related to high heat flux density and temperature nonuniformity present in high-capacity SiC power modules. The optimization approach is validated using the Pin-Fin heatsink, which is implemented in Infineon's HybridPACK Drive CoolSiC automotive-qualified SiC power module, serving as the design benchmark. Experimental results demonstrate that the optimized heatsink offers substantial performance improvements compared to the traditional Pin-Fin heatsink under the working conditions of rated voltage 350 V and rated current 300 A: a 6.2% reduction in peak junction-to-coolant thermal resistance, a 43.7% enhancement in thermal uniformity, and a 9.8% reduction in pumping power.

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