Optimal Switching Sequence Model Predictive Control for Modular Multilevel Converter With Low Computational Complexity

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***Abstract*—Model predictive control (MPC) has been widely adopted in modular multilevel converters (MMCs) due to its multiobjective capabilities and rapid dynamic response. However, it faces challenges such as significant computational burden, difficulty in adjusting weighting factors, and variable switching frequency. Additionally, the presence of numerous redundant switching states further complicates the application of space vector modulation in MMC. To address these issues, this article proposes an optimal switching sequence MPC (OSS-MPC) for MMC. First, a method for determining the candidate switching sequence is developed to identify specific switching states while minimizing computational complexity. Next, a predictive model based on the gradient of output current is introduced to reduce current ripple and improve tracking accuracy. Finally, circulating current suppression is achieved by integrating the predictive model of arm unbalanced voltage with the OSS. The proposed OSS-MPC exhibits excellent steady-state performance and a reduced computational burden while preserving the rapid response characteristic of MPC. Simulation and experimental results from a prototype with 24 submodules demonstrate the feasibility of the proposed method.**

***Index Terms*—Model predictive control (MPC), modular multilevel converter (MMC), optimal switching sequence, space vector modulation (SVM).**

I. INTRODUCTION

THE modular multilevel converter (MMC) has garnered considerable attention for medium/high-voltage power conversion in the past decade [1], [2], [3], [4]. Owing to its high modularity, excellent scalability, low switching frequency and superior harmonic performance, the MMC has found widespread application in flexible dc transmission [5], [6], [7], wind power generation [8], [9], power electronic transformers [10], high-power motor drives [11], [12], and traction power supply systems [13].

Compared with the complex cascading structure under the traditional linear control method [14], [15], model predictive control (MPC), as a typical multiobjective control algorithm, is well-suited for MMC control due to the ease of implementing multiobjective constraints, straightforward parameter adjustment, and fast dynamic response [16]. Various MPC methods and related optimization methods have been proposed, which can be classified into two categories: 1) finite control set (FCS)-MPC and 2) continuous control set (CCS)-MPC. For FCS-MPC, the traditional method in [17] requires evaluating all possible switching states to select the optimal one that minimizes the cost function, thereby achieving multiobjective control. However, as the number of submodules (SMs) in MMC increases, the computational burden associated with the rolling optimization becomes significant, making practical implementation challenging. Consequently, FCS-MPC that considers voltage levels is easier to implement in MMC [18], as it requires optimization over only $N+1$ voltage levels to minimize the cost function. Significant computation reduction can be achieved by modifying the rolling optimization and the formulation of the cost function in [19] and [20]. To effectively suppress the circulating current and eliminate the need for weight factors, a cascaded FCS-MPC is proposed for the first time in [21]. The effectiveness of this cascaded FCS-MPC has been verified through simulation and experimental results in [22] and [23]. Nevertheless, these optimized FCS-MPCs have varying switching frequencies and relatively poor steady-state performance due to the absence of modulators, leading to a wide distribution of harmonic spectrum and increasing the complexity of filter design.

On the other hand, to mitigate the inherent challenges of FCS-MPC, various CCS-MPCs have been applied to MMC. A modulated MPC is proposed in [24] that retains the original nonlinear control characteristics of FCS-MPC while improving steady-state performance. However, the rolling optimization is still required to select two specific voltage levels applied to the next control period. In [25], the MPC based on deadbeat control is proposed, which eliminates the need for rolling optimization and achieves a fixed switching frequency by introducing a modulator. A two-stage modulated MPC is proposed in [26] to control the output currents and the circulating currents separately, achieving good dynamic and steady-state performance through carrier-phase-shift (PS) modulation. Poblete et al. [27] enhanced the PS pulsewidth modulation (PS-PWM) scalability by decomposing CCS-MPC optimization into sequential subproblems, updating six modulation signals through a carrier synchronization mechanism. Arias-Esquivel et al. [28] first applied

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CCS-MPC to MMC drives. The method achieves suppression of SM capacitor voltage fluctuations and optimal control of circulating currents through online adjustment of weighting factors in the cost function. Furthermore, Rivero et al. [29] developed a long-horizon CCS-MPC based on the alternating direction method of multipliers. This strategy effectively suppresses low-frequency oscillations in capacitor voltages while maintaining minimal circulating current ripple. In [30], the effects of control delay, SM capacitor voltage fluctuation compensation, and model parameter mismatch under CCS-MPC are analyzed in detail, and the corresponding compensation control is carried out to enhance the steady-state performance and stability.

Among the various CCS-MPC methods, optimal switching sequence model predictive control (OSS-MPC) has been effectively implemented in two-level [31], [32] and three-level converters [33] due to its excellent steady-state performance. Its essence lies in selecting a fixed optimal combination of switching vectors within a single sampling period to reduce current ripple and maintain a constant switching frequency. Specifically, the duration of the switching sequence can be obtained based on the gradient of the currents [32], enabling accurate current tracking.

However, the implementation of OSS-MPC becomes challenging in real-time systems, particularly when applied to MMC, due to the significant computational burden associated with determining the OSS. Several simplified methods have been proposed to address this challenge, such as two-level-based space vector modulation (SVM) [34], 45-degree frame [35], 60° frame [36], and other equivalent methods [37]. In [34], the OSS selection is simplified to a two-level SVM by selecting the center vector of the reference vector and only considering the six sectors around it. However, the iterative operation and mapping relationship become more complicated in the *abc* frame as the voltage level increases. In the simplified method of transforming coordinate systems, the 60° frame is the most widely used. Huang et al. [36] analyzed the space vector distribution in a 60° frame using a seven-level MMC as an example, which provided a method for low-complexity location and calculation of multilevel OSS. Although the computational burden is not influenced by the number of levels, only a single space vector is performed in one period, which does not exploit the advantages of OSS. A space-vector-equalized MPC control is proposed in [37], which regards each arm as a whole. Although the calculational burden is reduced, the modulation part still needs to be realized by CPS-PWM, which is difficult to apply in the case of a large number of SMs. OSS-MPC is effectively introduced into multilevel converters in [38]. However, it still requires extensive rolling optimization calculations and look-up tables to determine the optimal switching sequence, leading to significant computational complexity. Although further reductions in computational burden are possible by limiting the rolling optimization range in [39], this comes at the cost of compromised dynamic performance. Furthermore, the method for determining the exact switching sequence remains unclear, leading to complex algorithms and excessive storage requirements. To the best of our knowledge, no reference has reported the OSS-MPC applied in MMC with low computational complexity and excellent performance.

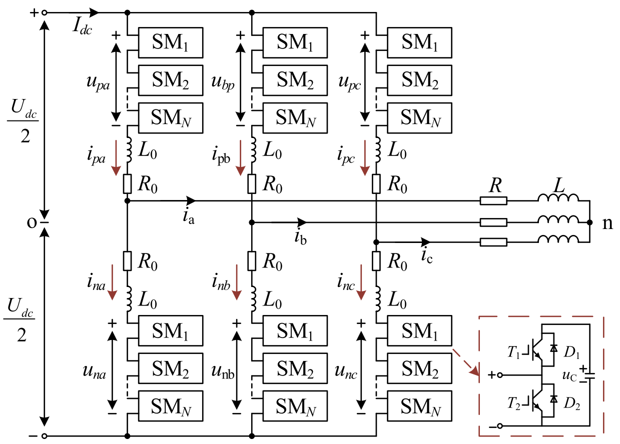


Fig. 1. Topology of the three-phase MMC and its submodule.

To address the issues mentioned above, this article proposes a novel MPC strategy with OSS for MMC. The main contributions of this article are summarized as follows.

1) A method for determining the candidate switching sequence with a fixed number of rolling optimization times is proposed. The method can be extended to any number of voltage levels without increasing the obvious computational burden.
2) A low-complexity OSS-MPC algorithm for MMC is proposed. Compared to existing FCS-MPC and CCS-MPC methods, the proposed method achieves reduced current ripple while providing enhanced system robustness.
3) By integrating with the seven-segment optimal switching sequence derived from space vectors, the proposed method achieves fixed switching frequency and improved dc-link voltage utilization.

The rest of this article is organized as follows. Section II provides a system description of MMC. Section III outlines the design and implementation of the OSS-MPC strategy. In Section IV, comparative simulation and experimental results are presented to verify the feasibility and effectiveness of the proposed methods. Finally, Section V concludes this article.

II. SYSTEM DESCRIPTION

A. *Working Principle and Control Objectives*

The topology of the MMC is shown in Fig. 1. Each arm is composed of N SMs and an arm inductor L_0 connected in series. The arm resistor R_0 represents the equivalent resistance of the parasitic parameters of the arm inductor and the associated losses within the arm. R and L denote the resistive-inductive load on the ac side. Each SM is formed by a half-bridge structure in parallel with a dc capacitor C_{SM}, containing two complementary power devices T_1 and T_2. Under normal operating conditions, the output voltage of the SM equals the capacitor voltage u_{s} when the SM is inserted and is zero when bypassed. Therefore, by adjusting the number of inserted SMs in the arm, the ac side output voltage can be controlled. If the capacitor voltages are well-balanced, the MMC can deliver $N+1$ or $2N+1$ voltage levels depending on the modulation strategy. In this article, the MMC operates with $N+1$ voltage levels.

B. Mathematical Model of the MMC

The basic mathematical model for MMCs has been extensively detailed in [12] and [27]. Combining the positive direction of the electrical quantities defined in Fig. 1, the following equations can be derived using Kirchhoff's laws:

$$\frac{U_{\mathrm{dc}}}{2} - u_{pj} - L_0\frac{di_{pj}}{dt} - R_0 i_{pj} - L\frac{di_j}{dt} - Ri_j = 0 \tag{1}$$

$$\frac{U_{\mathrm{dc}}}{2} - u_{nj} - L_0\frac{di_{pj}}{dt} - R_0 i_{pj} + L\frac{di_j}{dt} + Ri_j = 0 \tag{2}$$

$$i_j = i_{pj} - i_{nj} \tag{3}$$

$$i_{dj} = \frac{i_{pj} + i_{nj}}{2} = \frac{I_{dc}}{3} + i_{zj} \tag{4}$$

where U_{dc} denotes the dc bus voltage, subscript j ($j = a, b, c$) represents one of the three phases. u_{pj} and u_{nj} refer to the upper and lower arm voltages, respectively. i_{pj} and i_{nj} are the upper and lower arm currents, respectively. i_{dj} indicates the circulating currents in phase j, and i_{zj} is the ac component of the circulating currents. Based on (1)–(4), the dynamic equations of the ac currents and circulating currents can be obtained as

$$\frac{di_j}{dt} = \frac{2}{L_0 + 2L}u_j - \left(\frac{R_0 + 2R}{L_0 + 2L}\right) i_j \tag{5}$$

$$\frac{di_{dj}}{dt} = \frac{1}{2L_0}(U_{\mathrm{dc}} - u_{pj} - u_{nj}) - \frac{R_0}{L_0} i_{dj} \tag{6}$$

where the ac side phase voltage u_j is given by

$$u_j = \frac{u_{nj} - u_{pj}}{2}. \tag{7}$$

According to (5)–(7), the output currents and circulating currents can be controlled by adjusting the voltages of the upper and lower arms for each phase. Simultaneously, the dynamic characteristics of the SM capacitor voltage can be expressed as

$$\frac{du_{crji}}{dt} = \frac{i_{rj}}{C_{\mathrm{SM}}} \tag{8}$$

where the subscript r ($r = p, n$) hereinafter represents the upper and lower arm. u_{crji} denotes the SM capacitor voltage of the ith ($i = 1, 2, \ldots, N$) SM in the r arm of the phase j.

III. DESIGN OF THE OSS-MPC STRATEGY

The control objectives of MMC mainly include the following three aspects.

1) *Output Currents Tracking:* The output currents should accurately follow the given reference value.
2) *Circulating Currents Suppression:* The ac component of the circulating currents should be eliminated.
3) *Capacitor Voltage Balancing:* The capacitor voltage of the SMs should be effectively balanced.

An OSS-MPC strategy applied to MMC is proposed in this section, which consists of the following parts: reference voltage vector prediction, the candidate switching sequence determination, predictive model based on current gradient, circulating currents suppression (CCS), and SM capacitor voltage balancing. The specific design steps are as follows.

A. Discrete Predictive Model of Reference Voltage Vector

It is essential to rapidly determine the vector position by predicting the reference voltage vector, thereby eliminating the complex rolling optimization processes discussed in [38] and [39]. Based on the dynamic models in (5)–(8), the discrete mathematical model of the MMC is formulated using the forward Euler method as follows:

$$i_j(k+1) = \frac{2T_s}{L_0 + 2L}u_j(k+1) + \left(1 - \frac{R_0 + 2R}{L_0 + 2L}T_s\right) i_j(k) \tag{9}$$

$$\begin{aligned} i_{\mathrm{d}j}(k+1) = {} & \frac{T_s}{2L_0}\left(U_{\mathrm{dc}} - u_{pj}(k+1) - u_{nj}(k+1)\right) \\ & + \left(1 - \frac{R_0}{L_0}T_s\right) i_{\mathrm{d}j}(k) \end{aligned} \tag{10}$$

$$\begin{cases} u_{crji}(k+1) = \frac{T_s}{C_{\mathrm{SM}}} i_{rj}(k) + u_{crji}(k), S_{rji}(k) = 1 \\ u_{crji}(k+1) = u_{crji}(k), S_{rji}(k) = 0 \end{cases}. \tag{11}$$

The predictive model developed in this article adopts the cascaded control structure [12], which separately regulates the phase current and circulating current control objectives. To simplify the representation of a balanced three-phase MMC system, the amplitude-invariant Clarke transformation $\boldsymbol{T}_{\mathrm{Clarke}}$ is used to convert the output voltages and currents from the three-phase *abc* frame to the stationary α-β frame.

$$\begin{aligned} \boldsymbol{u} &= \boldsymbol{u}_\alpha + j\boldsymbol{u}_\beta = \boldsymbol{T}_{\mathrm{Clarke}}\begin{bmatrix} u_{an} & u_{bn} & u_{cn} \end{bmatrix}^T \\ \boldsymbol{i} &= \boldsymbol{i}_\alpha + j\boldsymbol{i}_\beta = \boldsymbol{T}_{\mathrm{Clarke}}\begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \end{aligned} \tag{12}$$

with the Clarke transformation as

$$\boldsymbol{T}_{\mathrm{Clarke}} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{13}$$

Based on (9) and (12), the discrete predictive model of the reference voltage vector at time instant $k+1$ can be expressed as

$$\begin{aligned} u_\alpha^*(k+1) &= \frac{L_0 + 2L}{2T_s}\left(i_\alpha^*(k+1) - i_\alpha(k)\right) + \frac{R_0 + 2R}{2}i_\alpha(k) \\ u_\beta^*(k+1) &= \frac{L_0 + 2L}{2T_s}\left(i_\beta^*(k+1) - i_\beta(k)\right) + \frac{R_0 + 2R}{2}i_\beta(k) \end{aligned} \tag{14}$$

where $\boldsymbol{i}(k+1)$ is replaced by $\boldsymbol{i}^*(k+1)$ to track the reference value of the output currents.

Thus, the optimal reference voltage vector $\boldsymbol{u}^*(k+1)$ at time instant $k+1$ can be obtained by this discrete predictive model.

B. Method of Determining Candidate Switching Sequences

Each voltage base vector of multilevel converters can be positioned distinctly in the *g-h* frame, also known as the 60° frame [36]. Compared with the *abc* frame in [34], the *g-h* frame

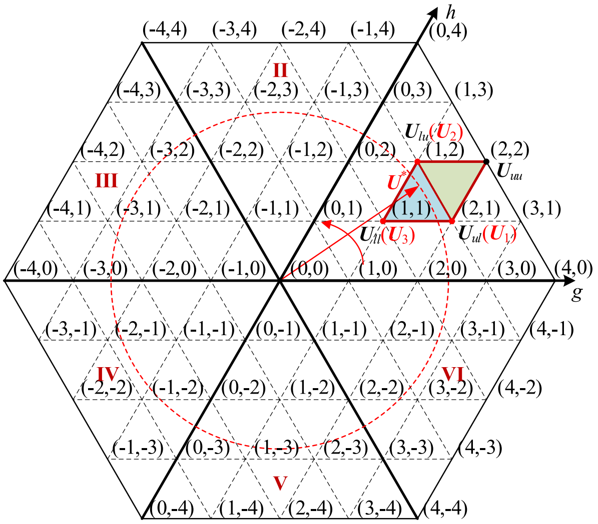


Fig. 2. Space vector diagram of MMC in the *g*-*h* frame.

eliminates the need for extensive trigonometric calculations, significantly reducing the computational burden associated with sector determination and coordinate calculations. The reference vector obtained by (14) is represented by (U^*_α, U^*_β), then the coordinates in the *g*-*h* frame can be expressed as

$$\begin{bmatrix} U^*_g \\ U^*_h \end{bmatrix} = \frac{1}{|U_{\min}|} \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} U^*_\alpha \\ U^*_\beta \end{bmatrix}, \ |U_{\min}| = \frac{2U_{\mathrm{dc}}}{3N} \tag{15}$$

where $|U_{\min}|$ denotes the magnitude of the smallest voltage base vector of MMC.

Since the coordinates of the base voltage vectors are all integers shown in Fig. 2, the four base voltage vectors closest to the prediction vector $\boldsymbol{U}^*$ can be obtained by rounding up and down (U^*_g, U^*_h), respectively, which can be expressed as

$$\boldsymbol{U}_{ul} = \begin{bmatrix} \overline{U^*_g} \\ \underline{U^*_h} \end{bmatrix}, \boldsymbol{U}_{lu} = \begin{bmatrix} \underline{U^*_g} \\ \overline{U^*_h} \end{bmatrix}, \boldsymbol{U}_{uu} = \begin{bmatrix} \overline{U^*_g} \\ \overline{U^*_h} \end{bmatrix}, \boldsymbol{U}_{ll} = \begin{bmatrix} \underline{U^*_g} \\ \underline{U^*_h} \end{bmatrix} \tag{16}$$

where the overline and underline symbols denote rounding the variable up and down, respectively.

The four base voltage vectors form a closed parallelogram around the reference voltage vector, as shown in Fig. 2. $\boldsymbol{U}_{ul}$ and $\boldsymbol{U}_{lu}$ always lie on the diagonals of this parallelogram and can serve as candidate vectors $\boldsymbol{U}_1$ and $\boldsymbol{U}_2$, respectively. Based on geometric relationships, the candidate vector $\boldsymbol{U}_3$ can be obtained by

$$\boldsymbol{U}_3 = \begin{cases} \boldsymbol{U}_{uu}, U^*_g + U^*_h - \overline{U^*_g} - \underline{U^*_h} \geq 0 \\ \boldsymbol{U}_{ll}, U^*_g + U^*_h - \overline{U^*_g} - \underline{U^*_h} < 0 \end{cases}. \tag{17}$$

Take a reference vector in Sector I as an example, as shown in Fig. 2, the coordinates of the selected vector $\{\boldsymbol{U}_1, \boldsymbol{U}_2, \boldsymbol{U}_3\}$ in the *g*-*h* frame can be determined according to (16) and (17) as {(21), (12), (11)}. The selected vector $\{\boldsymbol{U}_1, \boldsymbol{U}_2, \boldsymbol{U}_3\}$ may correspond to multiple switching states, known as redundant switching states [33]. It should be stated that the "switching states" described hereinafter refer to the number of inserted SMs in the lower arm of each phase of the MMC, represented by (S_{ax}, S_{bx}, S_{cx}).

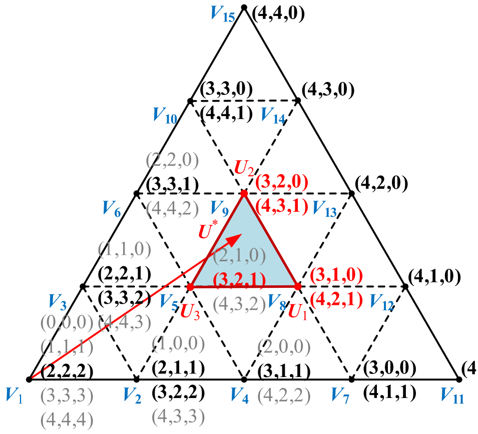


Fig. 3. Diagram of redundant switching states.

TABLE I
COMMON-MODE VOLTAGE FOR REDUNDANT SWITCHING STATES OF THE BASE VECTOR IN SECTOR I

Base vector	Switching state	CMV	Base vector	Switching state	CMV
V_1	(0,0,0)	-2*E*	V_6	(2,2,0)	-2*E*/3
	(1,1,1)	-*E*		(3,3,1)	0
	(2,2,2)	0		(4,4,2)	4*E*/3
	(3,3,3)	*E*	V_7	(3,0,0)	-*E*
	(4,4,4)	2*E*		(4,1,1)	0
V_2	(1,0,0)	-5*E*/3	V_8	(3,1,0)	-2*E*/3
	(2,1,1)	-2*E*/3		(4,2,1)	*E*/3
	(3,2,2)	*E*/3	V_9	(3,2,0)	-*E*/3
	(4,3,3)	4*E*/3		(4,3,1)	2*E*/3
V_3	(1,1,0)	-4*E*/3	V_{10}	(3,3,0)	0
	(2,2,1)	-*E*/3		(4,4,1)	*E*
	(3,3,2)	2*E*/3	V_{11}	(4,0,0)	-2*E*/3
	(4,4,3)	5*E*/3	V_{12}	(4,1,0)	-*E*/3
V_4	(2,0,0)	-4*E*/3	V_{13}	(4,2,0)	0
	(3,1,1)	*E*/3	V_{14}	(4,3,0)	*E*/3
	(4,2,2)	2*E*/3	V_{15}	(4,4,0)	2*E*/3
V_5	(2,1,0)	-*E*			
	(3,2,1)	0			
	(4,3,2)	*E*			

The relationship between these switching states and the *g*-*h* coordinates can be expressed as

$$\begin{cases} S_{ax} = i & 0 \leq i \leq N \\ S_{bx} = i - U_g & 0 \leq i - U_g \leq N \\ S_{cx} = i - U_g - U_h & 0 \leq i - U_g - U_h \leq N \end{cases} \tag{18}$$

where (U_g, U_h) represents the coordinates of the selected vector in the *g*-*h* frame.

Fig. 3 shows the redundant switching states corresponding to all base vectors in Sector I calculated according to (18). The relationship between different redundant states and corresponding common-mode voltage (CMV) is explicitly presented in [40]. In this article, the CMV corresponding to various redundant states in Sector I are listed, as shown in Table I, where *E* represents $U_{\mathrm{dc}}/2$. To minimize the CMV, the principle for selecting redundant switching states can be summarized as follows: base vectors with an even number of redundant states should retain the two central switching states, whereas base vectors with an odd number of redundant states should retain the one central switching state.

TABLE II
MAPPING RELATIONSHIP BETWEEN OTHER SECTORS AND SECTOR I

Sector number	Mapped coordinate values	
	U_{mg}	U_{mh}
II	U_g+U_h	$-U_g$
III	U_h	$-U_g-U_h$
IV	$-U_g$	$-U_h$
V	$-U_g-U_h$	U_g
VI	$-U_h$	U_g+U_h

Additionally, for a three-phase inverter, the minimum number of switching actions per switching cycle is three, thus requiring the application of four switching states within each cycle. When employing the three nearest voltage base vectors with seven-segment symmetric PWM, the first and fourth segments of the sequence must correspond to the same base vector. Consequently, all sequences initiate from base vectors possessing an even number of redundant switching states.

Based on the above selection principles, it is necessary to first determine the number of redundant switching states corresponding to the selected vector. In Sector I, it can be calculated by

$$X_R = N + 1 - (U_\mathrm{g} + U_\mathrm{h}) \tag{19}$$

where X_R represents the number of redundant switching states for the selected vector. To simplify the calculation of redundant switching states in other sectors, coordinates can be mapped to Sector I by Table II, where (U_{mg}, U_{mh}) denotes the coordinates after mapping.

To achieve symmetric seven-segment SVM, the initial switching state is selected from the base vector with an even number of redundant states, based on the terminal switching state of the previous sequence. Subsequently, the second and third switching states are chosen from the two remaining vectors, prioritizing those with the fewest switching transitions compared to the previous state. The number of switching actions is calculated by

$$Y = |S_{axk} - S_{aold}| + |S_{bxk} - S_{bold}| + |S_{cxk} - S_{cold}| \tag{20}$$

where $(S_{aold}, S_{bold}, S_{cold})$ refers to the previous switching state and $(S_{axk}, S_{bxk}, S_{cxk})$ denotes the candidate switching states.

Finally, the seven-segment switching sequence and the candidate set SS_can with the fewest switching transitions can be derived as

$$\begin{cases} SS_x = \{S_1, S_2, S_3, S_4, S_3, S_2, S_1\} \\ SS_\mathrm{can} = \{SS_1, SS_2, SS_3, SS_4, SS_5, SS_6\} \end{cases} \tag{21}$$

where S_i (i = 1,2,3) represent the candidate switching states corresponding to the selected vectors $\boldsymbol{U}_i$, whereas S_4 is another redundant state of the same base vector as S_1. SS_x (x = 1,2, …,6) represent the candidate switching sequence at time k+1.

For example, Fig. 4 shows the candidate switching sequence set SS_can. The switching states highlighted in bold are those that should be retained. Therefore, according to the position of $\boldsymbol{U}^*$, $\boldsymbol{U}_1$ corresponds to (3,1,0) and (4,2,1). $\boldsymbol{U}_2$ corresponds to (3,2,0) and (4,3,1). $\boldsymbol{U}_3$ corresponds to (3,2,1). Since both $\boldsymbol{U}_1$ and $\boldsymbol{U}_2$ have an even number of redundant switching states, any of the four switching states corresponding to $\boldsymbol{U}_1$ and $\boldsymbol{U}_2$ could potentially be the initial switching state. Assuming the switching state at time instant k is (3,0,0), the switch state (3,1,0) with the smallest Y value is selected according to (20) as the first switch state S_1, and the redundant switching state (4,2,1) corresponding to (3,1,0) is selected as the switching state S_4 for the fourth segment. Next, following the principle of minimizing the number of switching actions, the candidate switching sequence set SS_can can be obtained by (21). Similarly, the SS_can corresponding to the predicted value of any voltage vector can be calculated according to the algorithm shown in Fig. 5.

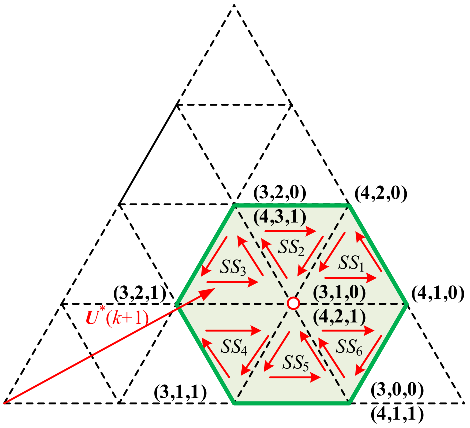


Fig. 4. Diagram of the candidate switching sequence set at time k+1 (taking a certain voltage vector as an example).

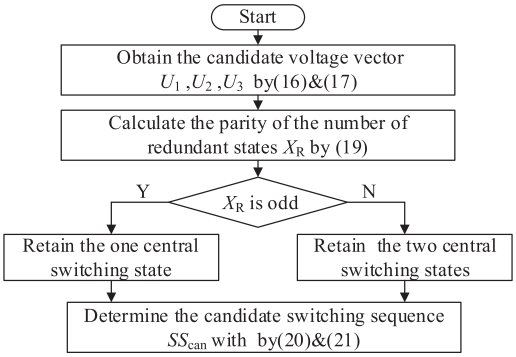


Fig. 5. Flowchart of the algorithm for determining SS_can.

According to the above analysis, the proposed SS_can determination method avoids the computational burden associated with unnecessary redundant vector states in [39]. The rolling optimization is confined to only six sequences within the green hexagon in Fig. 4, thereby significantly reducing computational burden. Furthermore, the CMV generated by the selected switching sequence is consistently minimized.

C. Predictive Model Based on Output Current Gradients

For voltage source inverters such as MMC, the output current change rate is directly related to the voltage vector. Based on the dynamic model of output currents (5), the current gradients for each voltage vector in the α-β coordinate system can be determined as

$$\begin{cases} K_{d\alpha n} = \frac{i_\alpha(k+1) - i_\alpha(k)}{T_s} = \frac{2}{L_0+2L} u_{\alpha n} - \frac{R_0+2R}{L_0+2L} i_\alpha(k) \\ K_{d\beta n} = \frac{i_\beta(k+1) - i_\beta(k)}{T_s} = \frac{2}{L_0+2L} u_{\beta n} - \frac{R_0+2R}{L_0+2L} i_\beta(k) \end{cases} \tag{22}$$

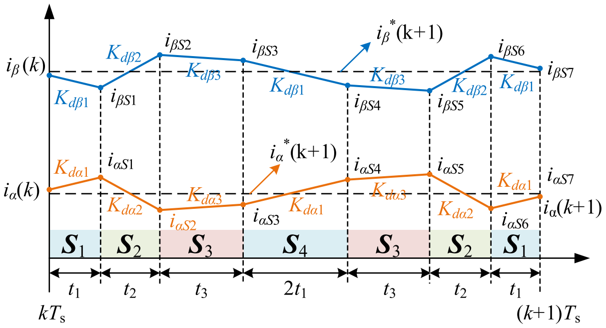


Fig. 6. Graphical description of the predicted output current trajectory of a symmetrical seven-segment vector switching sequence.

where $u_{\alpha n}$ and $u_{\beta n}$ represent the output voltage vectors corresponding to the switching state of the *n*th segment ($n = 1$–4). Since S_4 and S_1 correspond to the same voltage vector, the current gradients for both states are identical.

By integrating the switching sequence SS_{can} and the output current gradient derived from (22), the predictive current trajectory for one sampling period T_s is shown in Fig. 6. The output currents predictive model utilizing current gradients can be established as

$$\begin{cases} i_\alpha(k+1) = i_\alpha(k) + 2 \times (2K_{d\alpha 1}t_1 + K_{d\alpha 2}t_2 + K_{d\alpha 3}t_3) \\ i_\beta(k+1) = i_\beta(k) + 2 \times (2K_{d\beta 1}t_1 + K_{d\beta 2}t_2 + K_{d\beta 3}t_3) \\ 2t_1 + t_2 + t_3 = T_s/2 \end{cases} \tag{23}$$

where t_1, t_2, and t_3 represent the duration time of each vector segment, respectively.

To optimally track the current reference value within one T_s, the duration time of each switching state can be determined by minimizing the sum of squared current tracking errors in the following equation:

$$G(t_2, t_3) = \left(i_\alpha^*(k+1) - i_\alpha(k+1)\right)^2 + \left(i_\beta^*(k+1) - i_\beta(k+1)\right)^2. \tag{24}$$

The duration time of the switching sequences can be determined by solving the following constraint equations:

$$\begin{cases} \frac{\partial G(t_2,t_3)}{\partial t_2} = 0 \\ \frac{\partial G(t_2,t_3)}{\partial t_3} = 0 \end{cases}. \tag{25}$$

Based on (23)–(25), the analytic expression of the optimal time for t_2 and t_3 can be derived as

$$\begin{cases} t_{2o} = \frac{1}{K_{Den}} \\ \quad \times \begin{bmatrix} K_{d\beta 3} - K_{d\beta 1} \\ K_{d\alpha 1} - K_{d\alpha 3} \\ K_{d\alpha 3}K_{d\beta 1} - K_{d\alpha 1}K_{d\beta 3} \end{bmatrix}^{\boldsymbol{T}} \begin{bmatrix} i_\alpha^* - i_\alpha(k+1) \\ i_\beta^* - i_\beta(k+1) \\ T_s \end{bmatrix} \\ t_{3o} = \frac{1}{K_{Den}} \\ \quad \times \begin{bmatrix} K_{d\beta 1} - K_{d\beta 2} \\ K_{d\alpha 2} - K_{d\alpha 1} \\ K_{d\alpha 1}K_{d\beta 2} - K_{d\alpha 2}K_{d\beta 1} \end{bmatrix}^{\boldsymbol{T}} \begin{bmatrix} i_\alpha^* - i_\alpha(k+1) \\ i_\beta^* - i_\beta(k+1) \\ T_s \end{bmatrix} \end{cases} \tag{26}$$

with K_{Den} expressed as

$$K_{Den} = 2 \times (K_{d\alpha 1}K_{d\beta 2} - K_{d\alpha 2}K_{d\beta 1} - K_{d\alpha 1}K_{d\beta 3} + K_{d\alpha 3}K_{d\beta 1} + K_{d\alpha 2}K_{d\beta 3} - K_{d\alpha 3}K_{d\beta 2}). \tag{27}$$

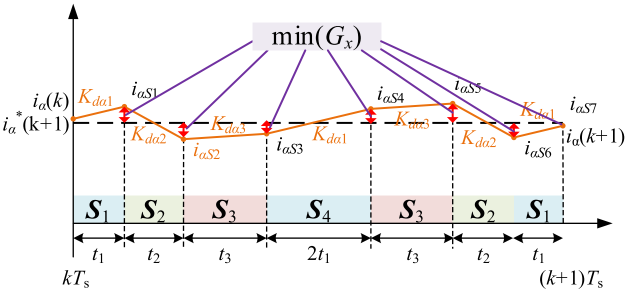


Fig. 7. Cost function minimization process of output current.

Based on (26), the optimal duration for each candidate switching sequence in set SS_{can} can be calculated. To minimize output current ripple, this article constructs a cost function G_x ($x = 1, 2, \ldots, 6$) by adopting the rolling optimization principle of FCS-MPC. This cost function accounts for current prediction errors during each time segment within one sampling period T_s under different switching vector combinations. The switching sequence SS_{opt} that minimizes G_x is selected from SS_{can} as the optimal switching sequence. G_x can be expressed as

$$G_x = \sum_{n=1}^{7} \left(i_\alpha^*(k+1) - i_{\alpha Sn}\right)^2 + \left(i_\beta^*(k+1) - i_{\beta Sn}\right)^2 \tag{28}$$

where $i_{\alpha Sn}$ and $i_{\beta Sn}$ represent the predicted current values after applying the *n*th switching state, which can be derived recursively through the following equation:

$$\begin{cases} i_{\alpha S(n+1)} = i_{\alpha Sn} + K_{d\alpha n}t_{nx} \\ i_{\beta S(n+1)} = i_{\beta Sn} + K_{d\beta n}t_{nx} \end{cases} \tag{29}$$

where $K_{\text{d}\alpha(\beta)n}$ and t_{nx} can be calculated from (22) and (26).

Moreover, the cost function minimization process of output current is shown in Fig. 7. Based on the gradient of output current, each segment of the vector switching sequence is considered by the proposed OSS-MPC. Hence, the current gradient is optimally adjusted, and the expected output current will be controlled closed to its reference.

Fig. 8 shows a sample diagram of the optimal duty ratio for an optimal switching sequence, where N_{j0} and N_{j1} represent the initial switching state and the fourth switch state of phase *j* in the optimal switching sequence, respectively.

Combined with the optimal duration time obtained from (26) and the action law of the switching sequence, the optimal duty ratio of the N_{j1} can be expressed as

$$\begin{cases} d_{ao} = \frac{2}{T_s}\left[(S_{a2} - S_{a1})t_{2o} + (S_{a3} - S_{a1})t_{3o} + 2(S_{a4} - S_{a1})t_{1o}\right] \\ d_{bo} = \frac{2}{T_s}\left[(S_{b2} - S_{b1})t_{2o} + (S_{b3} - S_{b1})t_{3o} + 2(S_{b4} - S_{b1})t_{1o}\right] \\ d_{co} = \frac{2}{T_s}\left[(S_{c2} - S_{c1})t_{2o} + (S_{c3} - S_{c1})t_{3o} + 2(S_{c4} - S_{c1})t_{1o}\right] \end{cases} \tag{30}$$

where S_{jn} represents the switching state of the *n*th segment of phase *j* in SS_{opt}.

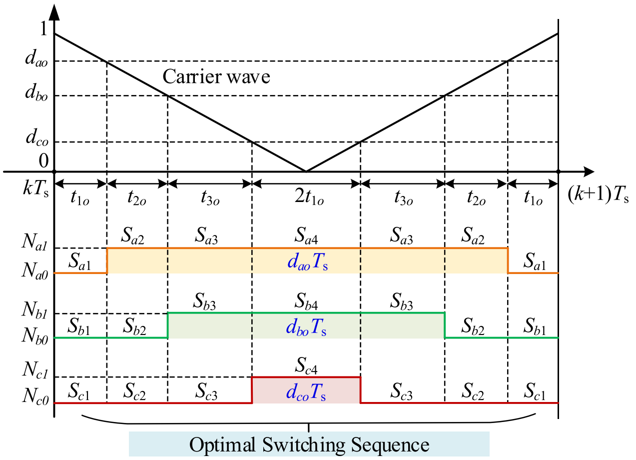


Fig. 8. Sample diagram of the optimal duty ratio.

D. Methods for Circulating Currents Suppression

The circulating current of the MMC flows exclusively within the upper and lower arms and does not impact the output currents. However, the ac component of the circulating currents increases the currents through power devices, leading to higher power loss and greater stress on the power devices. To improve the system efficiency and reliability, it is crucial to eliminate the ac component of the circulating currents.

Due to the capacitor voltage fluctuation of the SM, the sum of the upper and lower arm voltage of phase j cannot always equal U_{dc}. The unbalanced voltage acts on the inductance and resistance of the arm, resulting in the generation of the ac component in the circulating currents. Thus, the CCS can be achieved by adjusting the number of inserted SMs within the arm, which in turn modulates the arm voltage to eliminate the imbalance, which can be expressed as

$$u_{diffj} = 2u_{dj} = U_{dc} - (u_{pj} + u_{nj}). \tag{31}$$

If the upper and lower arms of phase j both bear half of the unbalanced voltage, represented by u_{dj} in (31), then according to (7), the ac side output will not be affected. By replacing $i_{dj}(k+1)$ in (10) with $I_{\text{dc}}/3$ as the reference value of the circulating currents, the predictive model of the reference arm unbalanced voltage can then be represented by

$$u^*_{dj}(k+1) = -\frac{L_0}{T_s}\left(i^*_{dj}(k+1) - i_{dj}(k)\right) - R_0 i_{dj}(k) \tag{32}$$

where $u^*_{dj}(k+1)$ represents the reference value of the arm unbalance voltage of phase j at time instant $k+1$ to eliminate the ac component of the circulating current.

Assuming that the capacitor voltages of SMs are well-balanced, the average capacitor voltage of the arm can be expressed as

$$U_{crj\_av}(k) = \frac{1}{N}\sum_{i=1}^{N} U_{crji}(k) \tag{33}$$

where $U_{crj\_av}(k)$ denotes the average capacitor voltage in the r arm of the phase j. Based on (32) and (33), the duty ratio correction amount for suppressing circulating currents in each arm can be formulated as

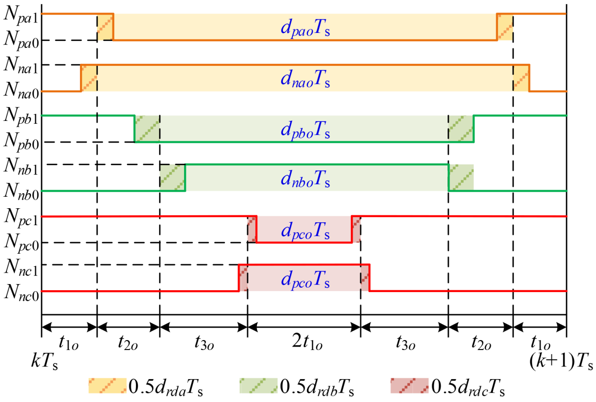


Fig. 9. Optimal duty ratio of the arms after circulation suppression.

$$d_{rdj} = \frac{u^*_{dj}(k+1)}{U_{crj\_av}(k)} \tag{34}$$

where d_{rdj} represents the duty ratio correction amount in the r arm of the phase j, which needs to be superimposed to the original optimal duty ratio d_{jo} specified in (26) during the switching process of each arm to additionally insert or bypass the extra SMs. Then, the optimal duty ratio of the arm can be derived from (26) and (34) as

$$\begin{cases} d_{pjo} = d_{jo} - d_{pdj} \\ d_{njo} = d_{jo} + d_{ndj} \end{cases} \tag{35}$$

where d_{pjo} and d_{njo} represent the optimal arm duty ratios for the upper and lower arms in phase j, respectively, through the OSS and CCS within one T_s.

To enhance clarity, Fig. 9 shows the duty ratio changes of the sequence after CCS, where the number of arm conduction SMs N_{rj0} and N_{rj1} can be obtained through the calculations from the optimal switching sequence SS_{opt} as follows:

$$\begin{cases} N_{nj0} = N_{j0} \\ N_{nj1} = N_{j0} + 1 \end{cases} \text{and} \begin{cases} N_{pj0} = N - N_{nj0} \\ N_{pj1} = N_{pj0} + 1 \end{cases}. \tag{36}$$

E. Submodule Capacitor Voltage Balance Control

The method of SM capacitor voltage balance control used in this article is based on the sorting algorithm. After the switching sequence and duty ratio are determined, the optimal number of SMs inserted in the upper and lower arms can be obtained. Therefore, with the direction of arm currents and the voltage sorting results, the SMs within the arm are inserted or bypassed in order. The flowchart of the capacitor voltage sorting algorithm is shown in Fig. 10.

If the arm current $i_{rj}(k) < 0$, the capacitor voltage is arranged in descending order, and the front N_{rjx} SMs are inserted preferentially to discharge them. If the arm current $i_{rj}(k) \geq 0$, the capacitor voltage is arranged in ascending order, and the front N_{rjx} SMs are inserted preferentially to charge them. Then, the specific switching statuses of the SMs for each arm at time instant $k+1$ can be determined.

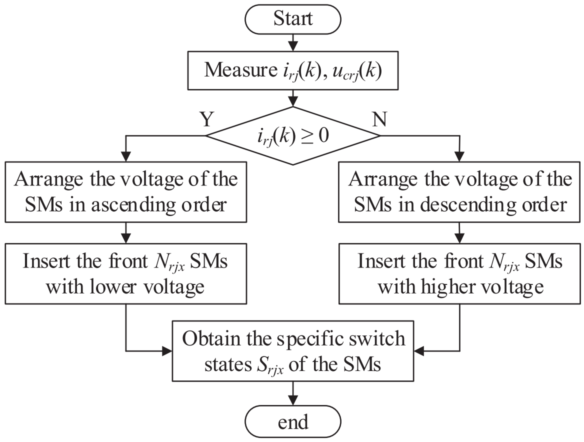


Fig. 10. Flowchart of the SMs voltage sorting algorithm.

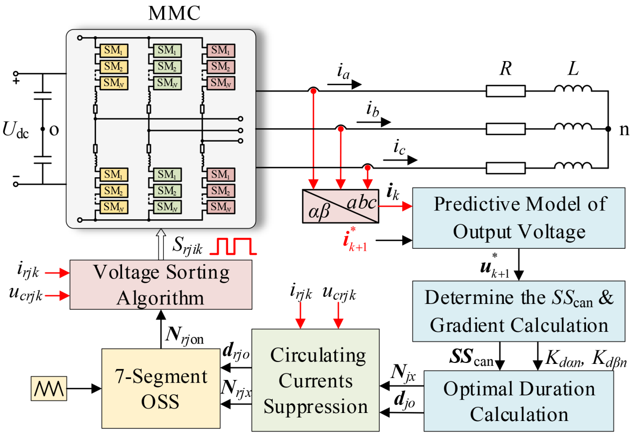


Fig. 11. Block diagram of OSS-MPC applied to MMC.

The block diagram of the proposed OSS-MPC scheme applied to MMC is presented in Fig. 11, which comprises the calculation of the optimal switching sequence and duration, CCS, and the capacitor voltage balancing algorithm for the SMs. Initially, the phase currents, arm currents, and SM capacitor voltages at time k are measured. Based on the predictive model, the reference voltage space vector for time $k+1$. Utilizing the predictive model, the reference voltage vector $\boldsymbol{u}^*(k+1)$ is determined, and redundant switching states of the candidate vectors are filtered to identify the candidate switching sequence in the g-h frame. Subsequently, the OSS and optimal duration are obtained through a fixed number of rolling optimization times based on the current gradient model. Additionally, the optimal duty ratio for the arm and the number of arm conduction SMs are obtained through the predictive model of arm unbalance voltage. Finally, a sorting algorithm is implemented to achieve the SM capacitor voltage balance control for MMC. The detailed implementation process of OSS-MPC is shown in Fig. 12.

F. Scalability Analysis of the Proposed Method

The computational burden of conventional OSS-MPC [38], [39] when applied to multilevel converters was mainly reflected in two aspects: switching sequence determination and rolling

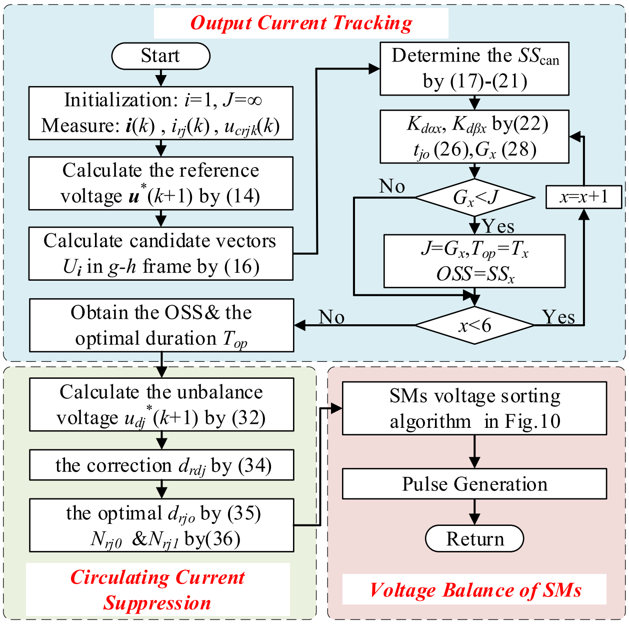


Fig. 12. Detailed flowchart of the proposed OSS-MPC.

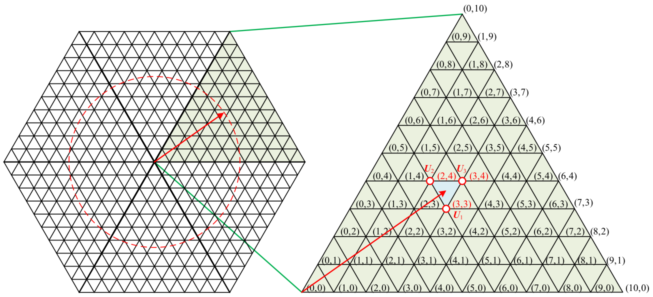
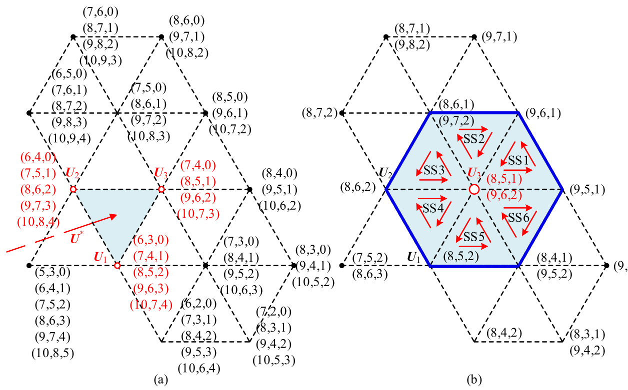


Fig. 13. 11-level space vector diagram of MMC in g-h frame.

optimization. To verify that the proposed method does not impose an obvious computational burden with increasing SM numbers, the scalability of the OSS-MPC approach is analyzed below using an 11-level MMC ($N = 10$) as an example. It should be noted that the analysis is conducted for an 11-level MMC to generate clear and interpretable space vector diagrams, while the same methodology and conclusions remain fully applicable to MMCs with dozens to hundreds of levels. Fig. 13 shows the space vector diagram of the 11-level MMC and the g-h coordinates of the base vectors in Sector I, respectively.

During the switching sequence determination process, the reference voltage vector $\boldsymbol{U}^*$at time $k+1$ is first obtained based on the prediction model (14). Subsequently, the three nearest base voltage vectors $\{\boldsymbol{U}_1, \boldsymbol{U}_2, \boldsymbol{U}_3\}$to $\boldsymbol{U}^*$in Fig. 13 are identified based on (16) and (17). Then, the switching states are filtered by (18) and (19). Similar to the space vector distribution pattern in 5-level MMC, since each voltage base vector maintains only 1 or 2 redundant switching states after screening, and considering that among $\{\boldsymbol{U}_1, \boldsymbol{U}_2, \boldsymbol{U}_3\}$ there is consistently either 1 or 2 base vectors with an even number of redundant states, the total number of candidate initial switching states corresponding to



(a) (b)

Fig. 14. Decomposition diagram of the redundant switching state screening process for 11-level MMC. (a) Redundant switching states corresponding to the base vectors. (b) Candidate switching sequence at time $k+1$.

TABLE III
COMPUTATIONAL BURDEN OF THE PROPOSED OSS-MPC FOR MMC WITH DIFFERENT NUMBERS OF SMS

Computational burden	The number of submodules N		
	4	10	200
The number of base vectors to be calculated	3	3	3
The candidate initial switching states to be considered	4 or 5	4 or 5	4 or 5
The number of candidate switching sequences	6	6	6
The times of rolling optimization	6	6	6

$\{\boldsymbol{U}_1, \boldsymbol{U}_2, \boldsymbol{U}_3\}$ remains either 4 or 5. Notably, this quantity remains unaffected by the number of SMs.

The redundant states of the base voltage vectors before and after filtering are shown in Fig. 14(a) and (b), respectively. As evident from Fig. 14(a), the sequence determination process becomes particularly challenging due to their excessive quantity. This represents the fundamental reason why the conventional SVM becomes less practical for MMCs with higher SM counts. In contrast, the proposed OSS-MPC can conveniently determine the candidate switching sequences for time $k+1$ using the filtered redundant states according to (17)–(21). Therefore, the process of determining switching sequences becomes independent of the number of SMs, and the number of candidate switching sequences can be fixed at six.

Based on the above analysis of the key steps of the proposed OSS-MPC under varying SM counts, Table III compares the computational burden across four critical aspects for configurations with 4, 10, and 200 SMs. The results demonstrate that the proposed method exhibits excellent scalability without introducing additional computational burden as the number of SMs increases.

G. Comparison Between the Existing MPC Methods and the Proposed OSS-MPC

Table IV presents the key performance comparisons between the existing MPC methods and the proposed OSS-MPC for MMC. It is important to note that the corresponding conventional and improved methods are listed in different categories of MPC (FCS-MPC, MMPC, and OSS-MPC) to ensure the comprehensiveness and fairness of the comparison.

The key performance comparison can be summarized based on the following aspects.

1) Steady-State Performance: The proposed OSS-MPC, deadbeat-MPC [30], and prior OSS-MPC [39] all employ multiple vectors within a single sampling period, resulting in a lower current ripple and fixed switching frequency compared to the single-vector methods of FCS-MPC in [17] and [23]. Furthermore, the predictive model of the proposed OSS-MPC based on the trajectory of output current changes takes into account the current changes after different vector inputs in one sampling period shown in Fig. 6, which can further improve the steady-state performance. In addition, the utilization of the dc link has increased in the proposed method.

2) Dynamic Performance: The prior OSS-MPC in [39] restricts the optimization range and simplifies computations due to the numerous space vectors. However, this limitation compromises the dynamic performance. In contrast, the proposed OSS-MPC retains the fast response characteristics of the MPC approaches in [23] and [30]. This is achieved through its unique method for determining the candidate switching sequence, as shown in Fig. 4, while maintaining low computational complexity.

3) Computational Burden: The proposed method efficiently generates candidate switching sequences through prefiltered redundant switching states while maintaining a fixed number of six rolling optimization steps per control cycle. Crucially, its computational burden remains independent of the number of SMs, demonstrating significantly higher efficiency compared to both conventional FCS-MPC and prior OSS-MPC approaches.

4) Robustness Performance: The method preserves six candidate switching sequences, retaining the essential characteristics of FCS-MPC. This design ensures robust performance even under parameter mismatch conditions, as the rolling optimization process continuously selects sequences that minimize current tracking errors. Consequently, the algorithm achieves reduced sensitivity to model parameter variations while delivering superior control performance characterized by lower current ripple and smaller tracking errors compared to existing methods.

Based on the above theoretical analysis and comparisons, among the discussed MPC methods, the proposed OSS-MPC demonstrates essential advantages in reducing current ripple, achieving a fixed switching frequency, improving dc voltage utilization, robustness, and optimizing computational complexity.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Testbed Description

To verify the effectiveness of the proposed OSS-MPC, an experimental prototype of a three-phase five-level MMC has been built, as shown in Fig. 15. The overall control is implemented through a two-layer control system presented in Fig. 16 to achieve the control requirements of numerous switching devices in the MMC.

TABLE IV
COMPARISON OF THE KEY PERFORMANCE FOR DIFFERENT MPC METHODS

Key performance		Conventional MPC methods			Improved MPC methods		
		FCS-MPC[17]	MMPC [24]	Prior OSS-MPC [39]	Cascaded FCS-MPC [23]	Deadbeat-MPC [30]	Proposed OSS-MPC
Calculation Burden	Rolling optimization	$3C_{2N}^{N}$	$3N+1$	42	$3(N+1)+18$	0	6
	Cost Function	Yes	Yes	Yes	Yes	No	Yes
	Weight Factor Design	Yes	Yes	No	No	No	No
Steady-State Performance	Output currents ripple	Normal	Normal	Good	Good	Good	Better
	Circulating currents suppression	Limited	Limited	Good	Normal	Good	Better
	Switching Frequency	Variable	Fixed	Fixed	Variable	Fixed	Fixed
	DC Voltage Utilization	Normal	Normal	High	Normal	Normal	Higher
Dynamic Performance	Response speed	Fast	Fast	Limited	Fast	Fast	Fast
Robustness Performance	Model parameter sensitivity	Limited	Limited	Good	Limited	Limited	Better

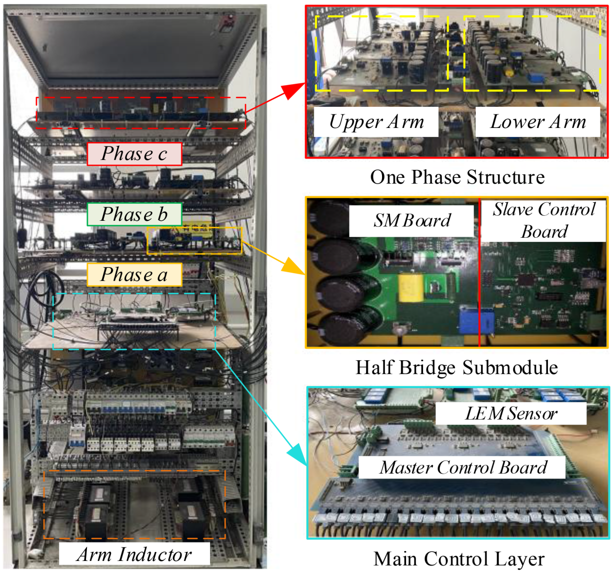


Fig. 15. Three-phase MMC experimental prototype.

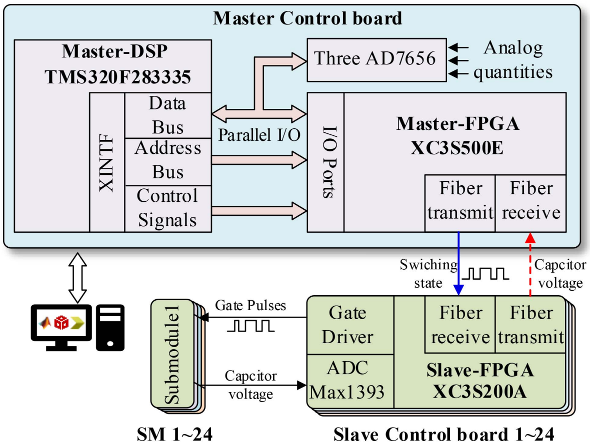


Fig. 16. Hardware architecture of the two-layer control system.

TABLE V
EXPERIMENTAL PARAMETERS OF THE MMC

Parameter	Symbol	Value
DC bus voltage	U_{dc}	300 V
Number of SMs per arm	N	4
SM capacitance	C_{SM}	1880 μF
Arm inductance	L_0	4 mH
Equivalent arm resistance	R_0	0.1 Ω
AC-side load inductance	L	10 mH
AC-side load resistance	R	25 Ω
Sampling period	T_s	250 μs
Rated output frequency	f	50 Hz

As shown in Fig. 16, the master control layer consists of a DSP (TI-TMS320F28335), an FPGA (Xilinx-XC3S500E), and three analog-to-digital converters (ADI-AD7656). The DSP is utilized to implement the relevant MPC algorithm and modulation algorithms, whereas the FPGA executes the capacitor voltage sorting algorithm for each SM. Furthermore, the slave control layer includes 24 slave control boards, each corresponding to one of the 24 SMs. Each board contains an FPGA (Xilinx-XC3S200A) and an ADC (MAXIM-MAX1393) to generate pulse signals for the SMs and sample the capacitor voltage. Additionally, the master control board communicates the on/off status of each SM to the slave control boards via optical fiber and receives the capacitor voltages from all 24 SMs through the universal asynchronous receiver/transmitter (UART) protocol.

Comparative simulations and experiments are conducted for cascaded FCS-MPC [23], prior OSS-MPC [39], deadbeat MPC [30], and the proposed OSS-MPC in the following sections. It should be mentioned that all four strategies use the two-step prediction model introduced in [32] to achieve delay compensation. The relevant experimental parameters are shown in Table V.

B. Simulation Results

To ensure a fair comparison of the performance for these four MPC methods, it is crucial to maintain the same switching frequency for the MMC switching devices under each strategy. However, since the specific SM pulse signals for these four methods are ultimately determined by the sorting algorithm, the switching frequency is influenced not only by the voltage level transitions but also by the results of the capacitor voltage sorting. This means that additional switching actions may exist to ensure capacitor voltage balance. Therefore, it is necessary to ensure that the average switching frequency f_{asw} remains consistent in both the comparative simulation and experiment.

TABLE VI
COMPARISON OF SWITCHING FREQUENCY OF THE FOUR MPC METHODS

Methods	Sampling f_s	Switching f_{asw}
Cascaded FCS-MPC[23]	10 kHz	1.04 kHz
Prior OSS-MPC[39]	4 kHz	1.07 kHz
Deadbeat MPC[30]	4 kHz	1.26 kHz
Proposed OSS-MPC	4 kHz	1.19 kHz

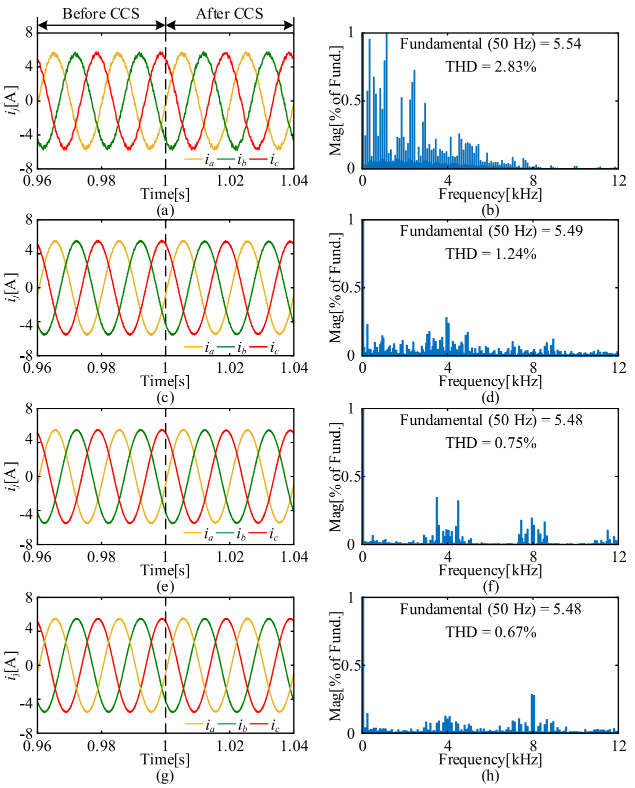


Fig. 17. Simulation comparison of output current waveforms and FFT analysis for four MPC methods. (a) and (b) Cascaded FCS-MPC, (c) and (d) prior OSS-MPC, (e) and (f) deadbeat MPC, and (g) and (h) proposed OSS-MPC. (a), (e), (f), and (g) Output currents. (e)–(h) Harmonic spectrum of i_a.

The calculation method is as follows:

$$f_{asw} = \frac{\sum\limits_{j=a,b,c\,r=p,n} \sum_{m=1}^{M} \sum_{i=1}^{N} \Delta S_{rji}(m)}{3NT_s} \tag{37}$$

$$\Delta S_{rji}(m) = |S_{rji}(k+1) - S_{rji}(k)| \tag{38}$$

where M denotes the total number of sampling time intervals employed in calculating the average switching frequency. $\Delta S_{rji}(m)$ represents the number of switching actions of the SM during the mth sampling period.

After statistical verification through repeated simulations, the sampling frequency for FCS-MPC is set to 10 kHz, whereas the sampling frequency for the other MPC methods is set to 4 kHz. This configuration ensures that the four MPC methods achieve an average switching frequency of approximately 1 kHz, as calculated by (37) and shown in Table VI.

Fig. 17 shows the simulation results of the output current waveforms and FFT analysis for the four MPC methods. The reference value of currents is set to 5.5 A. It can be observed that the output currents remain unaffected before and after activating the CCS for these MPC methods. According to the FFT analysis in Fig. 17, the output currents obtained by the proposed OSS-MPC exhibit the lowest THD of 0.67%. Regarding harmonic spectrum distribution, the cascaded FCS-MPC shows a wide and irregular distribution due to the use of a single optimal vector in each control period. In contrast, the harmonics of OSS-MPC and deadbeat-MPC are mainly concentrated at multiples of the carrier frequency, as these strategies incorporate a modulation module. Furthermore, the harmonic distribution under the proposed OSS-MPC is more focused as this method selects the specific seven-segment optimal switching sequence combination in each control period. Based on the simulation results and analysis, it can be verified that the proposed OSS-MPC outperforms the other methods in reducing output current ripple and ensuring a centralized switching frequency.

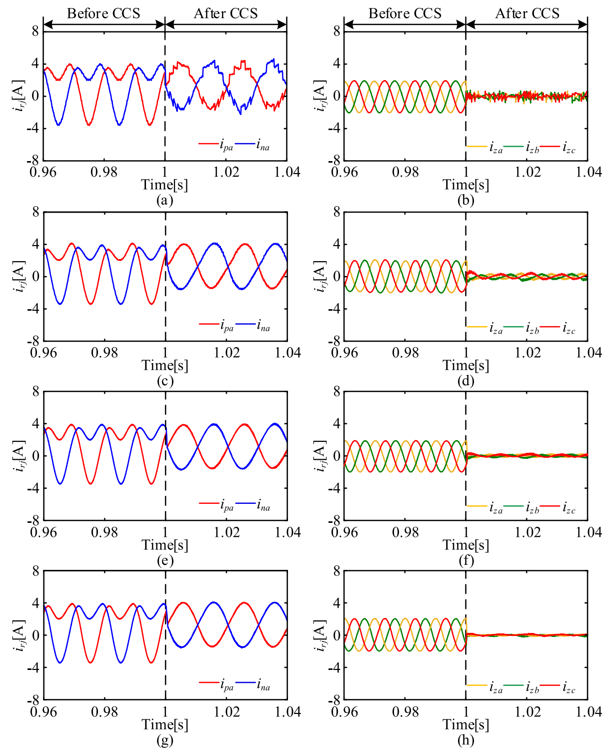


Fig. 18. Simulation Comparison of arm currents of phase a and ac component of circulating currents for four MPC methods. (a) and (b) Cascaded FCS-MPC, (c) and (d) prior OSS-MPC, (e) and (f) deadbeat MPC, and (g) and (h) proposed OSS-MPC.

Fig. 18 shows the simulation results of the sensitivity to phase a and the circulating currents for the four MPC methods before and after activating the CCS. As shown in Fig. 18, circulating currents are effectively suppressed under the four MPC methods. The arm current of the cascaded FCS-MPC exhibits significant distortion and poor waveform quality in Fig. 18(a), which is an inherent characteristic of the CCS method in cascaded FCS-MPC when the number of SMs is limited. In contrast, as shown in Fig. 18(b)–(d), the other three methods effectively suppress circulating currents while maintaining a near-sinusoidal characteristic of the arm current. Furthermore, the proposed OSS-MPC demonstrates the best performance

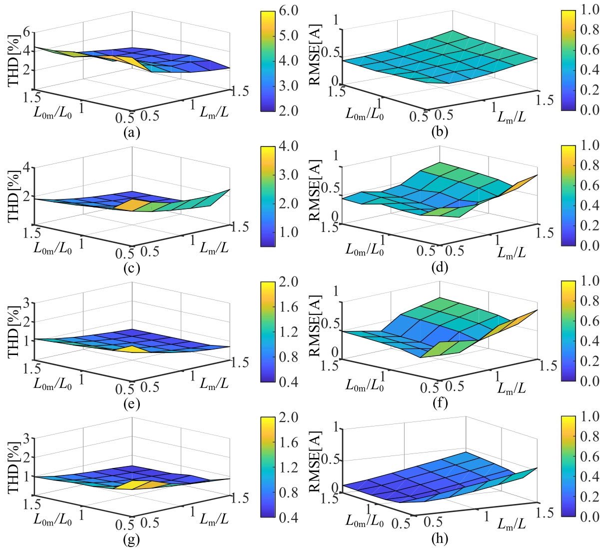


Fig. 19. Simulation comparison for four MPC methods under the model mismatch of arm inductance L_0 and load inductance L. (a) and (b) Cascaded FCS-MPC, (c) and (d) prior OSS-MPC, (e) and (f) deadbeat MPC, and (g) and (h) proposed OSS-MPC.

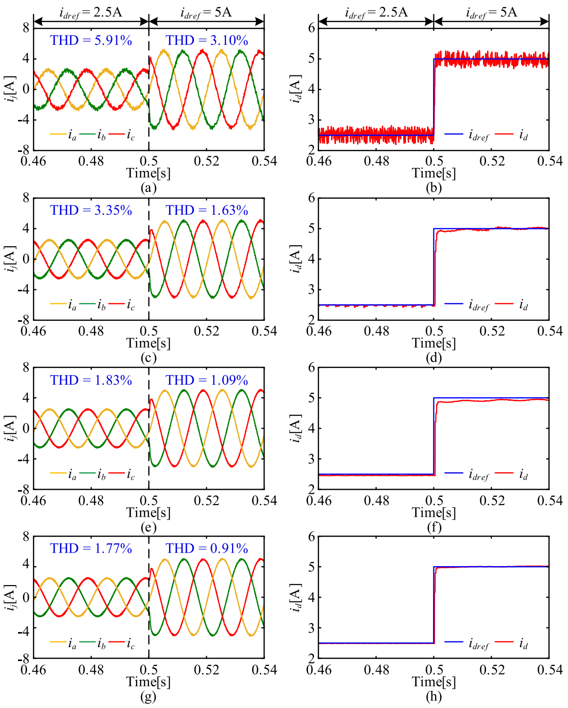


Fig. 20. Simulation Comparison of the dynamic response of output currents for four MPC methods. (a) and (b) Cascaded FCS-MPC, (c) and (d) prior OSS-MPC, (e) and (f) deadbeat MPC, and (g) and (h) proposed OSS-MPC.

in CCS, with the ac component i_{zj} exhibiting only a 0.11 A fluctuation amplitude.

Fig. 19 shows the simulation results demonstrating the sensitivity of the four MPC methods to model parameter mismatches, evaluated across a range of -50% to +50% for the inductance errors of both the arm and the load. The THD of output currents and the root mean square error are calculated under steady-state conditions. It can be observed that cascaded FCS-MPC exhibits overall poor THD and tracking performance in Fig. 19(a), whereas the prior OSS-MPC and Dead-beat MPC are sensitive to arm inductance parameter mismatches, with their tracking error varying significantly in Fig. 19(d) and (f). In contrast, the proposed OSS-MPC maintains the lowest THD and the highest tracking accuracy despite the model parameter mismatches.

Fig. 20 shows the simulation results of the dynamic response of the output currents under the four MPC methods, providing both the dynamic response of the output currents and the d-axis current. Compared to the reference current i_d, all four MPC methods can track the reference value within 1–2 T_s. Among them, the proposed OSS-MPC achieves the smallest tracking error of 0.081 A and the lowest THD across different modulation indices, demonstrating that the proposed OSS-MPC preserves the original rapid response characteristic of MPC while improving tracking accuracy.

C. Experimental Results

1) Steady-State Performance Comparison: Figs. 21 and 22 show the experimental results of the steady-state performance when the reference value of output currents is 5.5 A under the four MPC methods. Additionally, the harmonic spectrum distribution of the output and circulating currents is plotted in MATLAB, based on experimental data obtained from the oscilloscope. From the output currents' harmonic spectrum in Fig. 21, it is evident that cascaded FCS-MPC displays a wide and irregular distribution of harmonics, while the harmonic spectra of the other three MPC control strategies are more concentrated, facilitating the achievement of a fixed switching frequency. According to Fig. 21(f) and (j), compared to deadbeat-MPC and the proposed OSS-MPC, the prior OSS-MPC exhibits a larger output current ripple, and the concentration effect of the harmonic frequency distribution is less pronounced. This is due to the use of a four-segment asymmetric switching sequence for modulation, which sacrifices output power quality to reduce the number of rolling optimization iterations and the inherent complexity of the prior OSS-MPC. On the contrary, the proposed OSS-MPC employs a seven-stage SVM due to the simplicity of the proposed OSS determination method, which does not require rolling optimization. As a result, the harmonic spectrum distribution under the proposed OSS-MPC is more concentrated as shown in Fig. 21(l).

Furthermore, the experimental results of CCS and SM capacitor voltage balance control are shown in Fig. 22. It can be seen that the negative second-order component is effectively suppressed across all methods, with OSS-MPC containing much less second-order component. In addition, the capacitor voltages of the SMs have been well balanced under the four MPC methods. Therefore, compared with the other three control strategies, the proposed OSS-MPC has the optimal steady-state performance, characterized by the smallest current ripple, the most concentrated switching frequency, and the most effective CCS.

2) Dynamic Performance Comparison: Fig. 23 shows the dynamic response performance when the reference value of output currents changes from 2.5 A (modulation index $m = 0.42$)

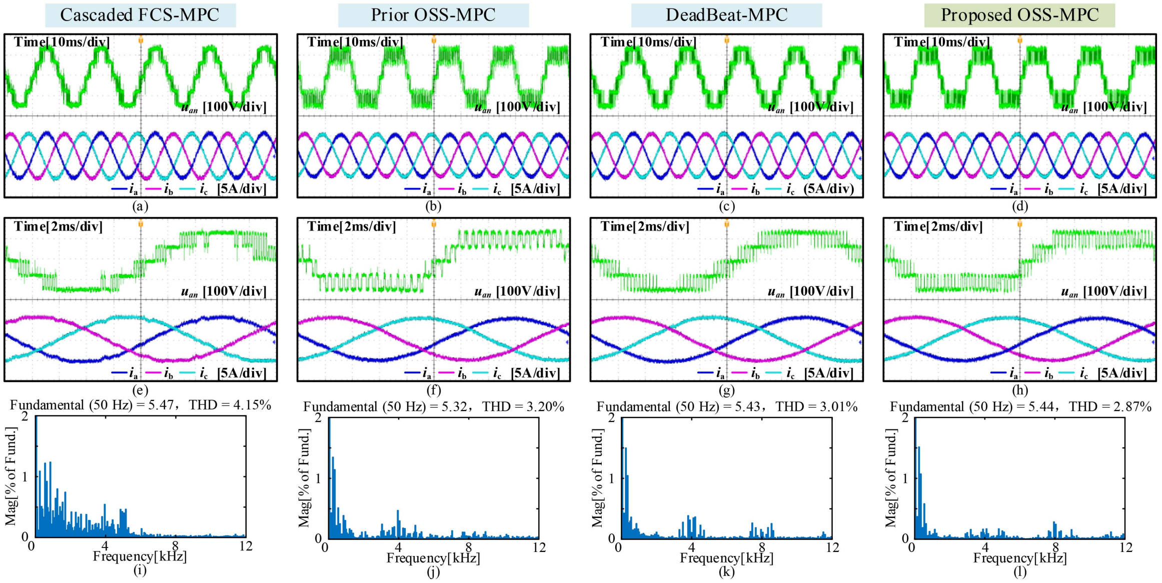


Fig. 21. Experimental results of the steady-state performance of voltage of phase a and output currents for (a), (e), and (i) Cascaded FCS-MPC, (b), (f), and (j) prior OSS-MPC, (c), (g), and (k) deadbeat MPC, and (d), (h), and (l) proposed OSS-MPC. (a)–(d) Voltage of phase a and output currents. (e)–(h) Partial magnification of phase a and output currents. (i)–(l) Harmonic spectrum of i_{a}.

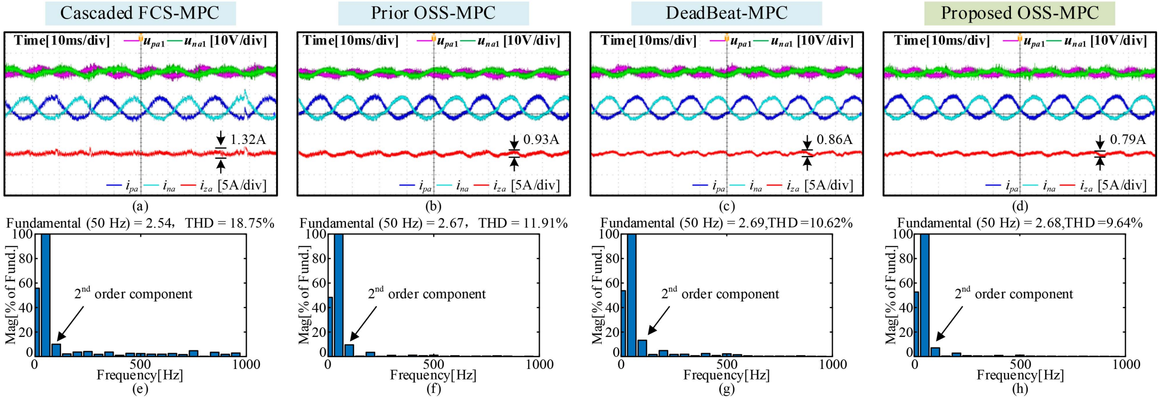


Fig. 22. Experimental results of the steady-state performance of circulating currents suppression and submodule capacitor voltage balance control for (a) and (e) Cascaded FCS-MPC, (b) and (f) prior OSS-MPC, (c) and (g) deadbeat MPC, and (d) and (h) proposed OSS-MPC. (a)–(d) Arm currents, circulating currents, and submodule capacitor voltage. (e)–(h) Harmonic spectrum of i_{pa}.

to 5 A ($m = 0.84$) under the four MPC methods. Consistent with the previous simulation results, all four MPC methods can rapidly track the specified reference value of output currents, and the circulating currents are effectively suppressed. Additionally, the fluctuations in the capacitor voltages of the SMs also increase as the arm current increases. Furthermore, as shown in Fig. 23(f)–(h), the prior OSS-MPC exhibits a limited dynamic response when the reference value of output currents changes, with a response time of 0.71 ms. This is due to the limitation of the optimization range during the rolling process, which may prevent finding the OSS within one sampling period. In contrast, the deadbeat-MPC and OSS-MPC achieve response times of 0.54 ms and 0.33 ms, respectively, with smoother and faster current transitions. The THD results in Fig. 23 indicate that under different modulation indices, OSS-MPC exhibits the lowest current harmonics (THD = 4.47% at $m = 0.42$, THD = 3.16% at $m = 0.84$) and the highest tracking accuracy while maintaining the fast dynamic response characteristics of MPC. Therefore, the proposed method has faster dynamic response and lower THD under different modulation indices, compared with the other three control strategies.

3) Overmodulation Performance Comparison: Fig. 24 shows the experimental results of the phase voltage and output currents under the overmodulation condition. The reference value of output currents is set to 6.5 A ($m = 1.1$), which exceeds the normal modulation range ($0<m<1$) for the cascaded FCS-MPC and deadbeat-MPC based on the MMC single-phase model. In Fig. 24(a) and (c), the output current exhibits significant distortion at the peak, indicating that the reference value cannot be tracked accurately. In contrast, OSS-MPC operates as an SVM model based on three-phase output voltage vector fitting, enabling it to function within the modulation index range of $1 < m < 1.15$. As shown in Fig. 24(b) and (d), OSS-MPC can still maintain effective control and high tracking

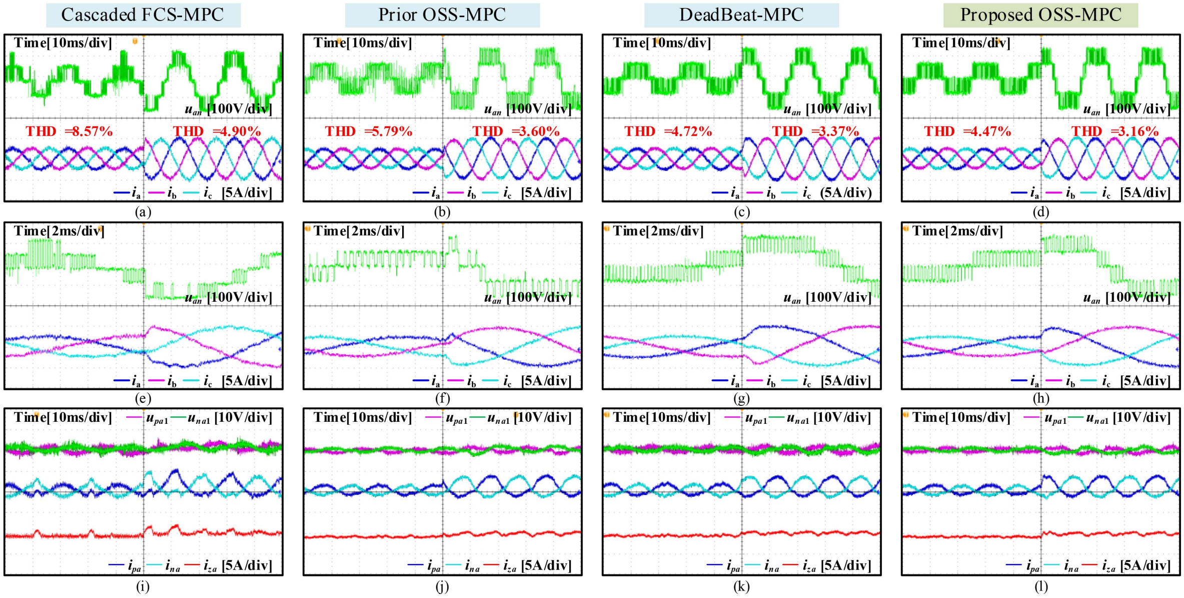


Fig. 23. Experimental results of the dynamic-state performance for (a), (e), and (i) cascaded FCS-MPC, (b), (f), and (j) prior OSS-MPC, (c), (g), and (k) deadbeat MPC, and (d), (h), and (l) proposed OSS-MPC. (a)–(d) Voltage of phase *a* and output currents. (e)–(h) Partial magnification of phase *a* and output currents. (i)–(l) Harmonic spectrum of i_{a}.

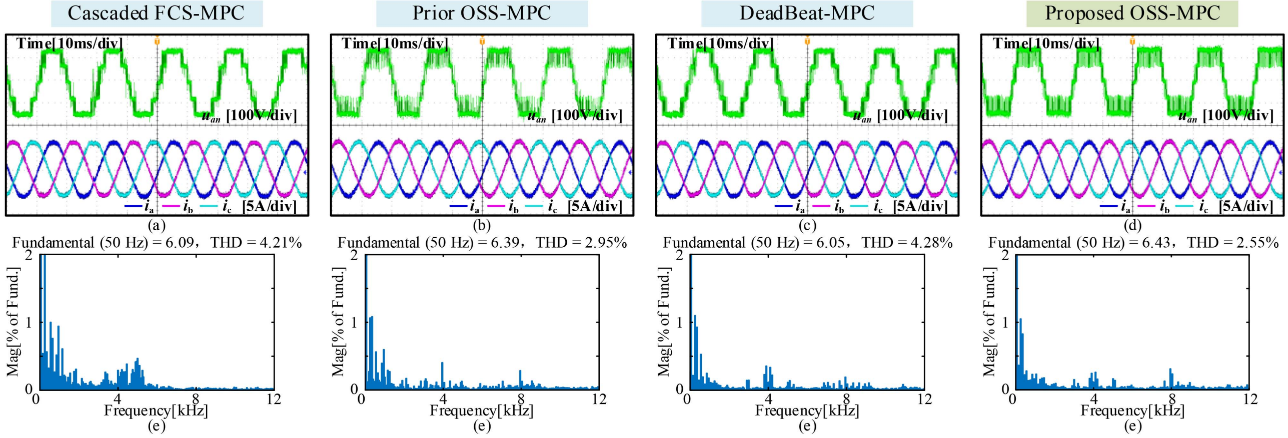


Fig. 24. Experimental results of voltage of phase *a* and output currents under overmodulation for (a) and (e) cascaded FCS-MPC, (b) and (f) prior OSS-MPC, (c) and (g) deadbeat MPC, and (d) and (h) proposed OSS-MPC.

accuracy under the condition of $1<m<1.15$. This capability highlights that the proposed OSS-MPC not only ensures higher steady-state accuracy but also effectively enhances the utilization of dc voltage to meet more stringent system control requirements.

4) Computational Burden Comparison: As detailed in Table VII, which summarizes the computational burden of each algorithmic component based on the mathematical formulation, the statistical results show a substantial reduction in operations compared to the prior method. Specifically, the proposed method requires only 154 multiplications, 12 divisions, and 189 additions/subtractions per control cycle. This represents a significant improvement over the prior OSS-MPC [39], which requires 1208 multiplications, 42 divisions, and 884 additions/subtractions.

Fig. 25 shows the experimental results of the overall program execution time in the DSP for the four MPC methods during one

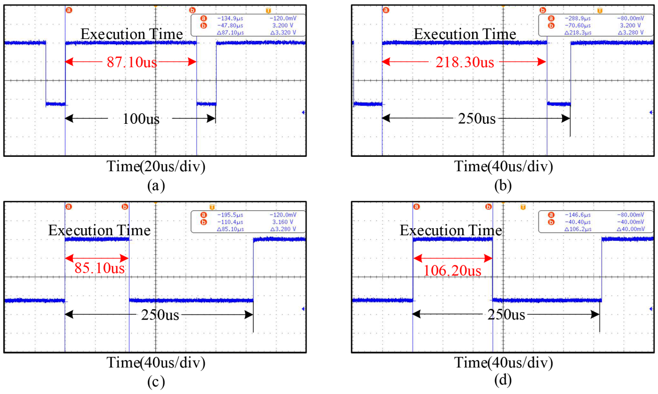


Fig. 25. Experimental results of the overall program execution time in the DSP for (a) cascaded FCS-MPC, (b) prior OSS-MPC, (c) deadbeat MPC, and (d) proposed OSS-MPC.

TABLE VII
QUANTITATIVE ANALYSIS OF COMPUTATIONAL BURDEN FOR THE PROPOSED ALGORITHM

Step	Equation No.	Multiplication	Division	Addition and Subtraction
1	(14)–(20)	24	3	52
2	(22)–(30)	116	6	112
3	(31)–(36)	14	3	25
Total		154	12	189

TABLE VIII
COMPARISON OF KEY PERFORMANCE OF DIFFERENT MPC METHODS BASED ON EXPERIMENTAL RESULTS

Key performance	Cascaded FCS-MPC	Prior OSS-MPC	Deadbeat-MPC	Proposed OSS-MPC
THD of $i_\mathrm{a}(m=0.92)$	4.15%	3.20%	3.01%	2.87%
THD of $i_\mathrm{a}(m=1.1)$	4.21%	2.95%	4.28%	2.55%
Modulation range	≤1	≤1.15	≤1	≤1.15
THD of i_{pa}	18.75%	11.91%	10.62%	9.64%
Fluctuation of i_{zj}	1.32 A	0.93 A	0.86 A	0.79 A
Response time	0.62 ms	0.71 ms	0.54 ms	0.33 ms
Algorithm execution time	87.10 μs	218.30 μs	85.10 μs	106.20 μs

sampling period. The execution time is measured by recording values of 1 and 0 at the beginning and end of the algorithm, respectively. As shown in Fig. 25(a), the overall computation time for cascaded FCS-MPC is 87.10 μs within the 100 μs sampling period ($f_\mathrm{s} = 10$ kHz). It is important to note that the computational burden of the cascaded FCS-MPC, which is related to the number of traversal optimizations, cannot be fully reflected in this experiment due to the limited number of SMs ($N = 4$). As the number of SMs increases, the computational burden of the cascaded FCS-MPC grows significantly. For the 250 μs sampling period ($f_\mathrm{s} = 4$ kHz) in Fig. 25(b)–(d), the overall execution times of prior OSS-MPC, deadbeat-MPC, and proposed OSS-MPC are 227.80 μs, 85.10 μs, and 106.20 μs, respectively.

It can be observed that the computational burden of prior OSS-MPC due to rolling optimization is quite significant. In contrast, the proposed OSS-MPC reduces the computational burden by screening candidate switching sequences and simplifying the rolling optimization process. Moreover, this computational burden remains independent of the number of SMs. Therefore, compared to the previous OSS-MPC, the proposed OSS-MPC significantly reduces algorithm complexity, while also maintaining excellent control performance.

Based on the above experimental results, the key performance metrics of the four MPC methods are summarized in Table VIII. The results demonstrate that the proposed OSS-MPC exhibits excellent performance in terms of MMC output current ripple, circulation suppression, dc voltage utilization, response time, and computational burden. In particular, compared to the prior OSS-MPC method for MMC [39], the proposed approach is no longer constrained by the complex rolling optimization, showing significant improvements in operational complexity and response time.

V. CONCLUSION

This article presents an OSS-MPC control strategy for MMC that effectively reduces current ripple, improves tracking accuracy, and achieves a fixed switching frequency while maintaining the rapid response characteristic of MPC. Additionally, the proposed OSS-MPC enhances the utilization of the dc-side voltage combined with the SVPWM. The proposed method for determining the OSS reduces and fixes the number of rolling optimization times to six per control cycle, thereby significantly lowering computational complexity. Importantly, the computational burden remains independent of the number of SMs, ensuring the method's scalability to MMCs with higher voltage levels. Finally, comparative experiments were conducted on an MMC experimental prototype with 24 SMs. Both simulation and experimental results further demonstrate that, under conditions of similar equivalent switching frequencies, the proposed OSS-MPC exhibits superior control performance.

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