Modular Equalization Architecture Using a ZVS Half-Bridge for Autonomous Energy Redistribution

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***Abstract*—This article presents a zero-voltage-switched half-bridge modular equalizer that utilizes a capacitively coupled ac link to enable scalable module-to-cell energy redistribution in a series-connected battery string. The proposed architecture transfers charges to any lower voltage cell(s) within the battery module naturally without sensing the individual cell voltage. Each half-bridge converter converts the voltage of its corresponding battery module to an ac signal, which is then transmitted to the ac link via a transformer and two decoupling capacitors. Since all modules are interconnected via the shared ac link, any low-voltage battery cell(s) receives energy from the link, thereby enabling effective energy transfer among modules. The proposed equalizer enables an adaptive current distribution among cells without relying on any selection switches. A 16-cell prototype (two modules of eight 3.6 V 18 650 cells each) was built to validate the effectiveness of the proposed topology. The equalization performances of the equalizer under single-module operation and dual-module operation have been evaluated. The proposed equalizer offers advantages in scalability, control complexity, and efficiency over conventional approaches, which makes it well suited for large-scale energy storage applications.**

***Index Terms*—Battery equalizer, battery management system (BMS), cell equalization, energy storage systems, lithium-ion batteries.**

I. Introduction

THE rapid growth of electric vehicles (EVs) and the corresponding increase in battery production have led to a significant accumulation of retired batteries [1], [2]. Although these batteries may no longer meet the stringent performance requirements for automotive applications, their remaining capacity can be effectively repurposed for stationary energy storage systems [3]. However, inherent variations in aging and degradation among second-life batteries lead to mismatches in capacity and voltage characteristics [4]. In second-life battery energy storage systems, cell equalization is, therefore, indispensable.

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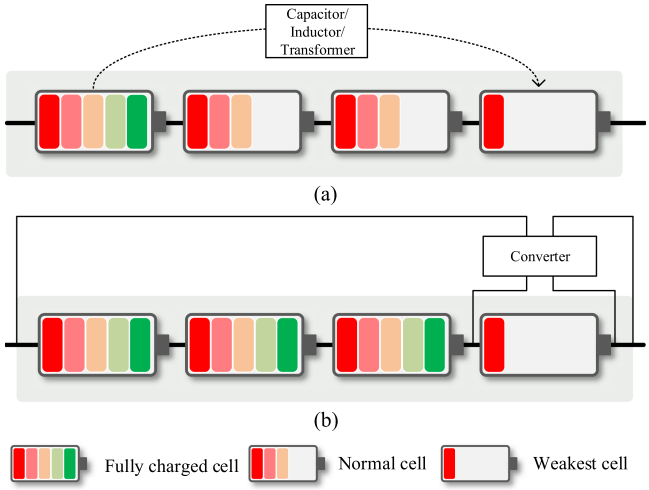

Fig. 1. (a) C2C equalization architecture. (b) P2C equalization architecture.

Without it, the "barrel effect"—where the weakest cell dictates the usable capacity—limits the overall utilization and efficiency of the system [5]. By equalizing the state of charge (SOC) between cells, usable capacity can be maximized and the life span of the pack can be enhanced [6], [7]. Furthermore, proper equalization is critical for safety: voltage imbalances during charge or discharge can drive some cells into overcharge or overdischarge, increasing the risk of thermal runaway or other failure modes [8]. Active redistribution of energy from higher voltage to lower voltage cells mitigates these hazards and ensures stable, reliable operation of the storage system [9].

Cell equalization methods can be divided into passive and active methods. Passive equalization uses resistors to bleed excess charge from cells with higher voltages, bringing every cell to the lowest voltage in the string [10]. This approach is simple and low-cost, but wastes energy and takes a long time. Active equalization, on the other hand, employs small power converters to move charge from stronger cells to weaker ones, enabling more efficient equalization at the cost of added components and control complexity.

Existing active equalization methods can be divided mainly into two categories. They are cell-to-cell (C2C) [11], [12], [13], [14] and pack-to-cell (P2C) [15], [16], [17], [18], [19]. As shown in Fig. 1(a), C2C equalization refers to the establishment of an energy transfer path between two single cells in a battery pack, transferring charge from a single cell with a higher voltage to a

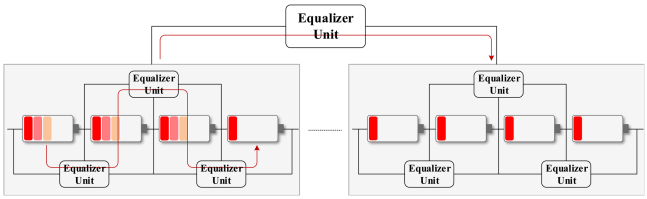

Fig. 2. Conventional modular multilevel battery equalization architecture.

single cell with a lower voltage [20]. C2C equalization strategies can be broadly classified into two categories based on the energy transfer path: adjacent C2C and direct C2C. In adjacent C2C architectures, energy can only be transferred between neighboring cells [21]. For systems with a large number of cells, adjacent C2C equalization methods result in excessively long energy transfer paths, leading to reduced equalization efficiency. As a result, such approaches are more appropriate for small-scale battery configurations. In direct C2C equalization, energy can be transferred between any pair of cells in the string, regardless of physical position [22]. However, when many batteries are connected in series, each potential equalization path requires corresponding switching and energy storage elements, significantly increasing circuit complexity and wiring requirements.

As shown in Fig. 1(b), P2C equalizers use a converter to extract energy from the entire battery pack and redistribute it to specific single cells with low SOC [23]. The structure does not require a separate energy transfer path to be established for each monomer, but instead achieves energy extraction and redistribution through the overall bus, and the circuit structure and wiring are simplified [24]. P2C equalizers can be classified into single shared converter with cell selection equalizers (SSCCSE) and multioutput converter-based equalizers (MOCE). The SSCCSE uses a single converter connected between the pack and a bank of parallel-connected switches that select the target cell. The structure utilizes centralized design to simplify energy management. However, SSCCSE requires complex switch matrix for cell selection, and sequential equalization limits speed in large scale systems. In addition, this circuit can address only one cell at a time. When the number of under-voltage cells increases, this sequential operation significantly limits the overall equalization speed. MOCE commonly utilizes multiwinding transformer to achieve simultaneous equalization of multiple cells. Consequently, accommodating a large number of cells introduces significant challenges in the design and implementation of the transformer. Furthermore, all P2C methods accommodate high voltage stress due to direct connection to the full pack, which increases the demands on power device ratings [25].

To reduce the voltage stress of the switches and achieve a more flexible equalization path, modular-based battery equalizer has been proposed. As shown in Fig. 2, this method is to divide the battery pack into multiple modules. It can realize the transfer of energy between modules and within the module. Some studies have been conducted on modular battery equalizers. Liu et al. [26] proposed a modular multilayer equalizer that employs a multiactive-bridge converter for module-level and a common-mode Class-D converter for cell-level equalization. While high-frequency operation minimizes magnetic component size, it also significantly complicates the control scheme due to the excessive frequency and number of active switches. Peng et al. [27] proposed a hierarchical equalizer that uses an *LLC* resonant converter at the module level and a buck–boost converter at the cell level, with design optimizations ensuring zero-voltage switching for all MOSFETs and optimal operation. However, the extensive use of relays before the modules undermines system reliability. Moreover, employing different topologies across the two layers of a multilevel equalizer significantly increases control complexity. Manjunath et al. [28] proposed a modular two-stage active cell equalization topology based on an enhanced buck–boost converter for series-connected lithium-ion battery strings. The aforementioned modular equalizers can only reduce the voltage stress of switches within individual modules, while the switches responsible for intermodule equalization are still subject to the full pack voltage.

To minimize the number of active components, overcome the implementation challenges associated with transformers, and reduce voltage stress of switches and the control complexity in multimodule systems, a half-bridge-based modular capacitive-coupled equalizer is proposed. The modular equalizer exhibits the following characteristics.

1) Reduced number of active components: For every n battery cells, only two selection switches are required, significantly decreasing the total number of active devices compared to the prior art.
2) Simplified control scheme: All switches are driven by a single pair of complementary pulsewidth modulation (PWM) signals, minimizing control complexity and eliminating the need for multichannel gate signal coordination.
3) Self-adaptive current distribution: The system requires no active cell selection. Current naturally flows from higher voltage cells to lower voltage cells based on their instantaneous voltage differences, enabling autonomous equalization characteristics.
4) Modular and scalable design: The architecture supports flexible modularization, allowing it to be easily scaled and applied to battery energy storage systems of various scales and voltage levels.
5) Low voltage stress: The voltage stress across each switch is limited to the local module voltage and remains independent of the total system voltage, enhancing device reliability.

The rest of this article is organized as follows. Section II describes the proposed circuit topology and its operating principles. Section III presents the design methodology along with a detailed power loss analysis. Section IV provides experimental validation. A comparative evaluation between the proposed scheme and existing solutions is given in Section V. Finally, Section VI concludes this article.

II. Proposed Equalizer and Operating Principles

A. Proposed Equalizer

Fig. 3 illustrates an equalization system architecture consisting of K modules, each comprising N battery cells. The modules

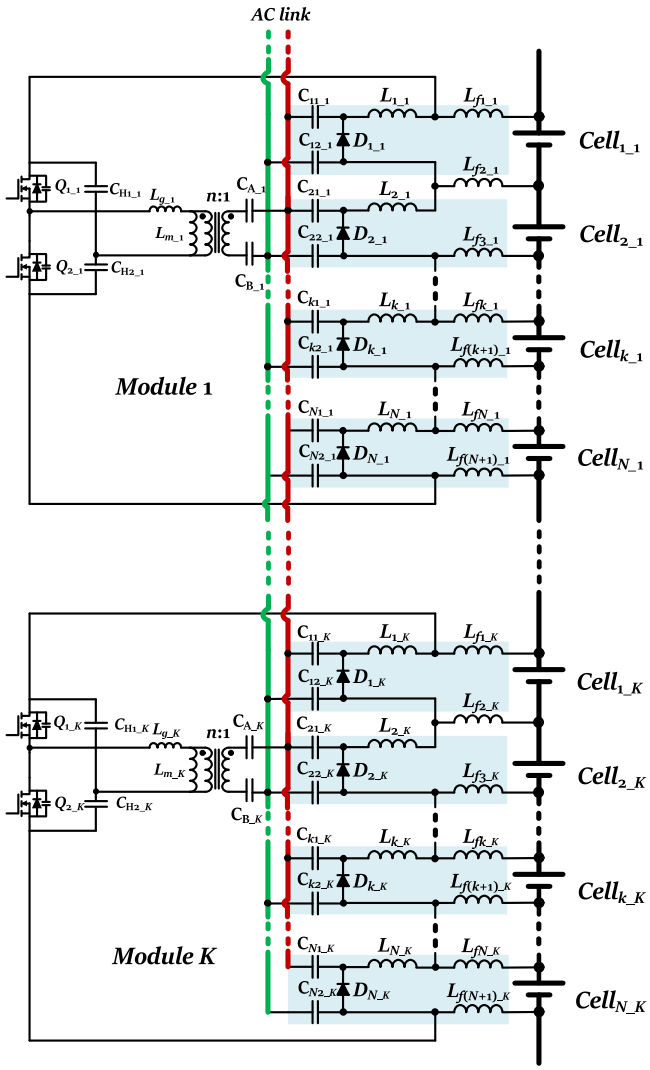

Fig. 3. Schematic of the proposed modular voltage equalization circuit module.

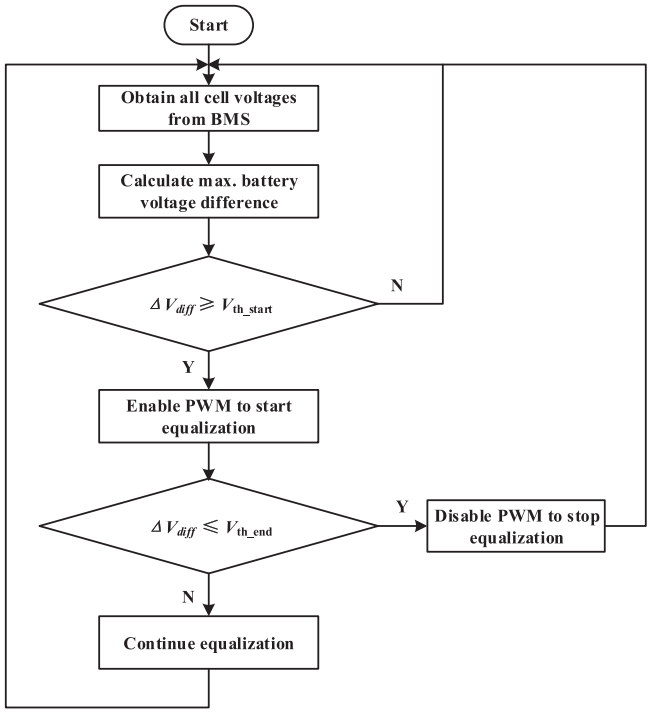

Fig. 4. Flowchart of the proposed autonomous equalization algorithm.

are interconnected through an ac link. The module battery units serve collectively as the input to the half-bridge. Capacitors ($C_{A\_1} \sim C_{A\_K}$ and $C_{B\_1} \sim C_{B\_K}$) function as decoupling capacitors, while ($C_{11\_1} \sim C_{N1\_K}$ and $C_{12\_1} \sim C_{N2\_K}$) are isolation capacitors. Diodes ($D_{1\_1} \sim D_{N\_K}$) and together with inductors ($L_{1\_1} \sim L_{N\_K}$) convert the ac signal into dc, and ($L_{f1\_1} \sim L_{f(N+1)\_K}$) serve as filter inductors.

The control flowchart is plotted in Fig. 4. The maximum voltage difference can be calculated by

$$\Delta V_{\text{diff}} = V_{\text{Cell\_max}} - V_{\text{Cell\_min}}. \tag{1}$$

When the maximum voltage difference is greater than the set start threshold $V_{\text{th\_start}}$, PWM is enabled; when the maximum voltage difference is less than the set stop threshold $V_{\text{th\_end}}$, PWM is disabled. The frequency selection of PWM will be analyzed in detail in Section III.A. Since the proposed equalization architecture is aimed to be integrated with a battery management system (BMS) that continuously measures the voltages of all cells, it first determines the maximum cell voltage difference and then selects the switching frequency. Therefore, the only variable that needs to be measured in this architecture is cell voltage. The current method for selecting the switching frequency relies on a simple table lookup, where a specific voltage difference corresponds to a designated switching frequency.

The half-bridge obtains input energy from the entire battery module, and distributes current according to the battery voltage in the module through the capacitor-coupled ac link. A lower battery voltage will have a higher equalization current, and a higher battery voltage obtains a lower equalization current. At the same time, all modules are connected together via the ac link. When the voltage of the battery(ies) in one module is higher than that in another module, the current will flow into the battery with the voltage lower than the average voltage through the ac link to achieve energy transfer between modules.

Ultimately, the voltage difference across all cells converges to zero. As the voltage difference decreases, the equalization current diminishes accordingly, leading to a progressively slower equalization process. Typically, equalization is terminated when the voltage difference of all cells falls below a designed threshold.

B. Operating Principles

Fig. 5 shows the operations of a single equalizer module when power is transferred from the total battery module to Cell_k with the lowest voltage. The current flowing out of the battery module i_M is the input current of the half-bridge. For the sake of simplicity and clarity, all components are assumed to be ideal in describing the operating principle of the equalizer. Fig. 6 shows the key operation waveforms of the equalizer. Throughout the equalization process, the input voltage of the

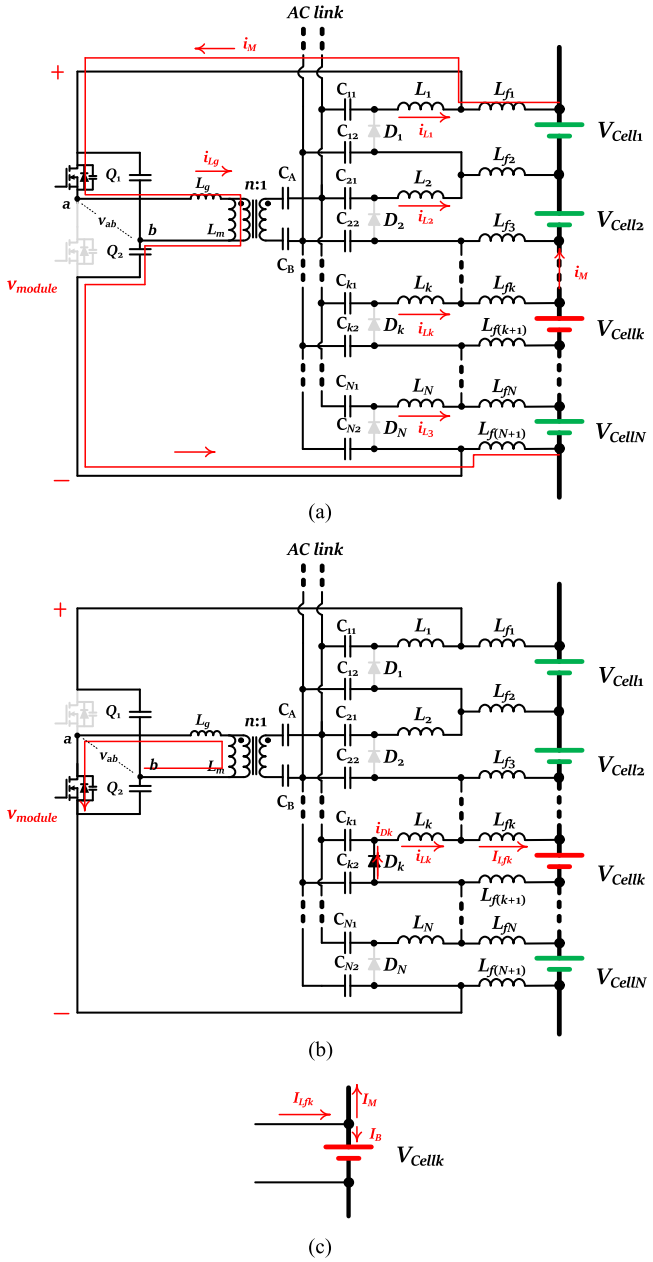

Fig. 5. Topological operation of the proposed equalizer module. (a) Q_1 is ON, Q_2 is OFF. (b) Q_2 is ON, Q_1 is OFF. (c) Definition of the current flows in Cell$_k$.

equalization module at any given time equals the sum of the voltages of the cells within the module. The module voltage can be expressed as

$$V_{\text{module}} = V_{\text{Cell1}} + \cdots + V_{\text{Cell}N} = \sum_{k=1}^{N} V_{\text{Cell}k}. \tag{2}$$

The half-bridge outputs an ac voltage with an amplitude of V_{ab}, which can be expressed as

$$V_{ab} = \frac{1}{2} V_{\text{module}}. \tag{3}$$

The MOSFETs in the half-bridge are driven by complementary PWM signals with dead-time inserted. When Q_1 is turned ON,

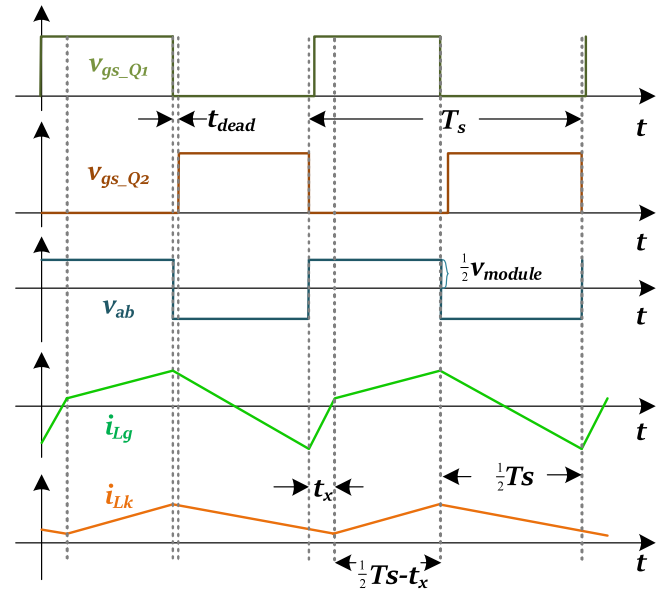

Fig. 6. Key waveforms in the steady state during equalization.

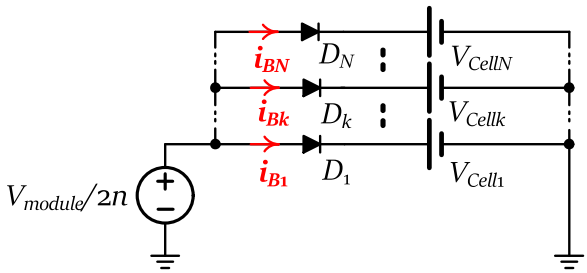

Fig. 7. DC equivalent circuit of cell rectifiers.

the leakage inductance L_g of the transformer is charged, and all diodes in the circuit are reverse-biased. During the dead time, L_g freewheels through the body diodes of the MOSFETs, enabling soft-switching. When switch Q_2 is turned ON, the dc equivalent circuit of the proposed equalizer is shown in Fig. 7. Assuming ideal diodes, when $V_{\text{module}}/2n > V_{\text{Cell}k}$, the diode is forward-biased, allowing current to flow into the Cell$_k$. Conversely, when $V_{\text{module}}/2n < V_{\text{Cell}k}$, the diode is reverse-biased, preventing current from flowing into cells with voltages higher than the average voltage. As shown in Fig. 5(c), the equalization current flowing into the Cell$_k$ is

$$I_{Bk} = I_{Lfk} - I_M \tag{4}$$

where $I_{Lfk} =< i_{Lk} >_{T_s} =< i_{Lfk} >_{T_s}$ and $I_M =< i_m >_{T_s}$. Therefore, the equalization power can be expressed as

$$P_B = I_{Bk} V_{\text{Cell}k} = I_M V_{\text{module}}. \tag{5}$$

When there are multiple battery (P) voltages within a single module that are lower than the average voltage, the equalization power can be expressed as

$$P_B = \sum_{k=1}^{P} I_{Bk} V_{\text{Cell}k}. \tag{6}$$

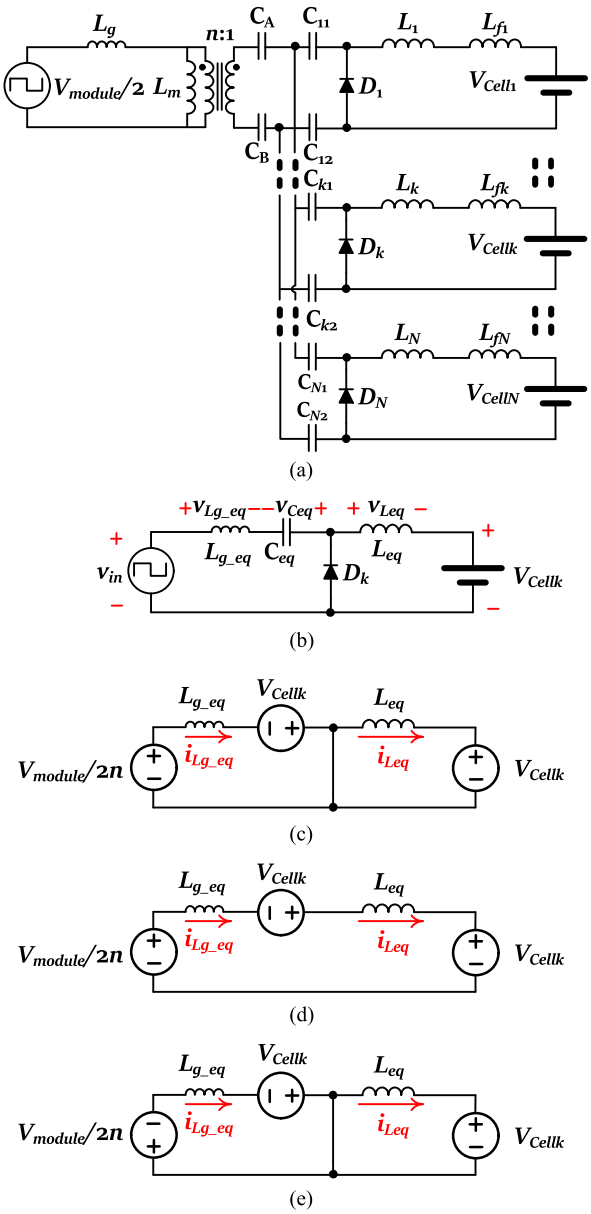

Fig. 8. Equivalent circuits. (a) Equivalent representation of the equalizer with decoupled input/output and half-bridge modeled as an ac voltage source. (b) Simplified circuit of the converter. (c) Mode 1 (t_x). (d) Mode 2 ($\frac{1}{2}T_s - t_x$). (e) Mode 3 ($\frac{1}{2}T_s$).

When multiple modules are in equalization, the overall power can be expressed as

$$P_{BM} = \sum_{i=1}^{K} I_{M\_i} V_{\text{module}\_i}. \tag{7}$$

Therefore, the equalization power of the system depends on the number of battery modules and the cell voltage within each module.

The equalizer can further be simplified as a single input, multiple output circuit, as illustrated in Fig. 8(a). For each cell with a voltage lower than the average, its equalization circuit can be equivalently represented as shown in Fig. 8(b). The equivalent

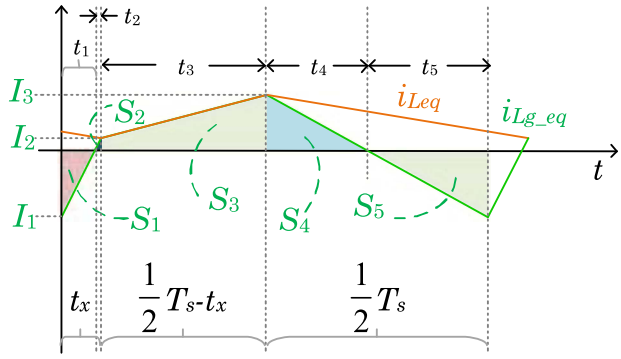

Fig. 9. Leakage inductance L_{g_eq} and inductor L_{eq} currents used for analytical modeling.

components can be represented as follows:

$$\begin{cases} L_{g\_\text{eq}} = \frac{L_g}{n^2} \\ C_{\text{eq}} = \frac{C_A C_B C_{k1} C_{k2}}{C_A + C_B + C_{k1} + C_{k2}} \\ L_{\text{eq}} = L_k + L_{fk}. \end{cases} \tag{8}$$

To simplify the analysis, dead time is neglected. Moreover, the transformer magnetizing inductance L_m can be regarded as a open circuit at high frequencies. The equivalent circuit of the equalizer is shown in Fig. 8(b). Based on the Kirchhoff's voltage law (KVL)

$$v_{\text{in}} + v_{Lg\_\text{eq}} - v_{C\text{eq}} + v_{Leq} + V_{\text{Cell}k} = 0 \tag{9}$$

where $< v_{\text{in}} >_{T_s} = 0$, $< v_{Lg\_\text{eq}} >_{T_s} = 0$, and $< v_{\text{Leq}} >_{T_s} = 0$. Therefore

$$v_{C\text{eq}} = V_{\text{Cell}k}. \tag{10}$$

The coupling capacitor can be regarded as a voltage source equal to the battery voltage. Within one switching cycle, the circuit operates in three modes, as illustrated in Fig. 8(c)–(e). Fig. 9 shows the current of the inductors i_{g_eq} and i_{Leq}.

1) *Mode 1 [t_x, Fig. 8(c)]:* During this subinterval, Q_1 is turned ON and Q_2 is turned OFF. The diode D_k conducts, the current through the inductor L_{g_eq} transitions from negative to positive, and the equivalent inductance L_{eq} sustains the current through the diode. Based on the KVL, the slope of the current of the inductor L_{g_eq} is given by

$$\frac{di_{L_{g\_\text{eq}}(t)}}{dt} = \frac{1}{L_{g\_\text{eq}}} \left(\frac{V_{\text{module}}}{2n} + V_{\text{Cell}k} \right). \tag{11}$$

Equation (11) becomes

$$I_2 - I_1 = \frac{1}{L_{g\_\text{eq}}} \left(\frac{V_{\text{module}}}{2n} + V_{\text{Cell}k} \right) t_x. \tag{12}$$

2) *Mode 2 [$\frac{1}{2}T_s - t_x$, Fig. 8(d)]:* During this subinterval, with Q_1 remaining ON, Q_2 remaining OFF and the diode OFF, the currents through the inductors L_{g_eq} and L_{eq} are equal. At this time, the slope of both inductor currents is given by

$$\frac{di_{L_{g\_\text{eq}}(t)}}{dt} = \frac{1}{L_{g\_\text{eq}} + L_{\text{eq}}} \frac{V_{\text{module}}}{2n}. \tag{13}$$

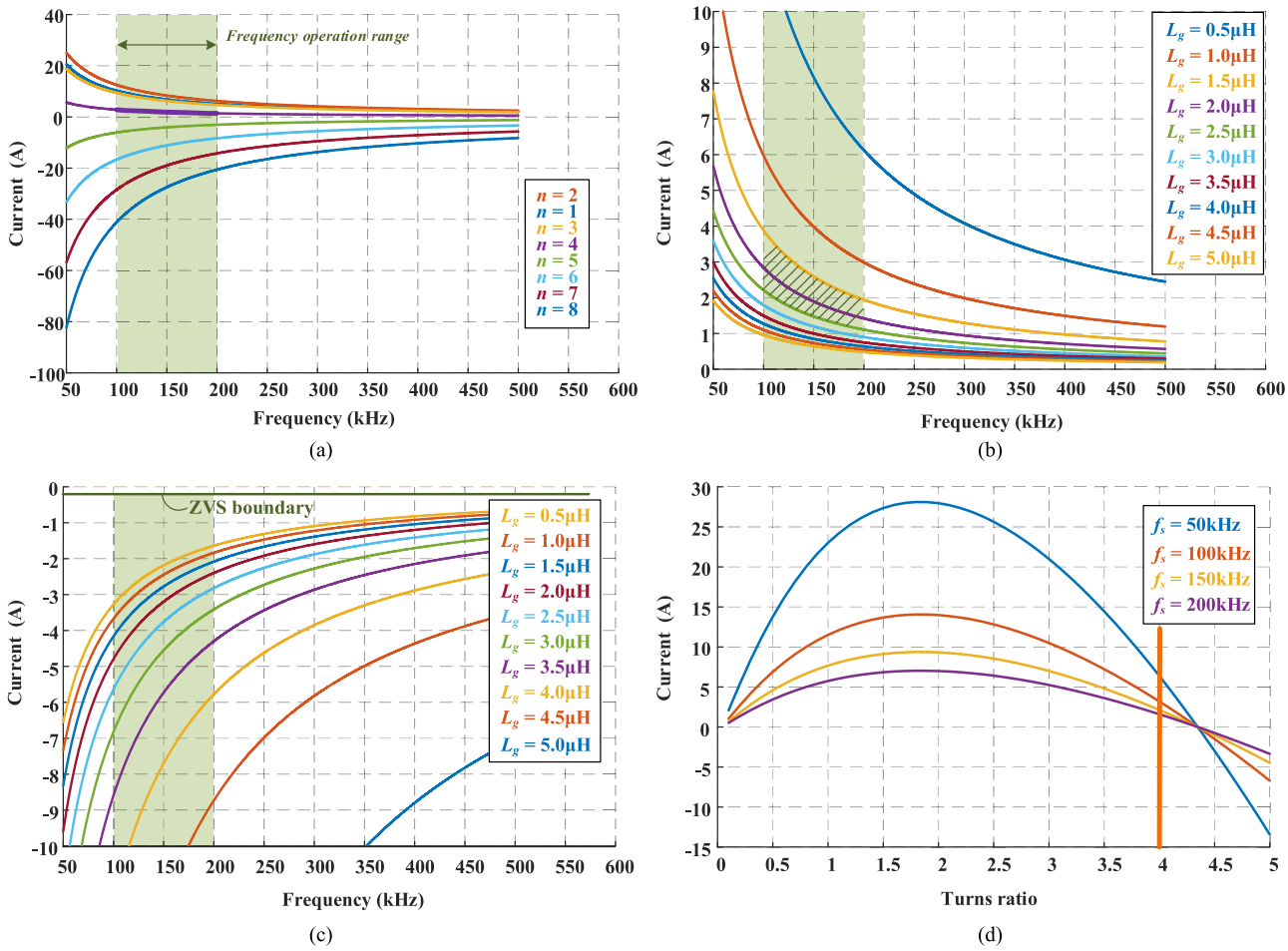

Fig. 10. (a) Output current versus frequency under different transformer turns ratios. (b). Output current versus frequency for different leakage inductance L_g values. (c) Magnitude of the leakage current when the switch is turned ON versus frequency for different leakage inductance. (d) Output current versus turns ratio under different frequency.

Equation (13) becomes

$$I_3 - I_2 = \frac{1}{L_{g\_\mathrm{eq}} + L_{\mathrm{eq}}} \frac{V_{\mathrm{module}}}{2n} \left(\frac{1}{2} T_s - t_x \right). \tag{14}$$

3) *Mode 3 [$\frac{1}{2}T_s$, Fig. 8(e)]:* During this subinterval, switch Q_1 is turned OFF and Q_2 is turned ON. At this moment, the diode conducts, and the current slopes of the two inductors are given by

$$\frac{di_{L_{g\_\mathrm{eq}}(t)}}{dt} = \frac{1}{L_{g\_\mathrm{eq}}} \left(V_{\mathrm{Cell}k} - \frac{V_{\mathrm{module}}}{2n} \right). \tag{15}$$

$$\frac{di_{L_{\mathrm{eq}}(t)}}{dt} = -\frac{1}{L_{\mathrm{eq}}} V_{\mathrm{Cell}k}. \tag{16}$$

Equations (15) and (16) become

$$I_1 - I_3 = \frac{1}{L_{g\_\mathrm{eq}}} \left(V_{\mathrm{Cell}k} - \frac{V_{\mathrm{module}}}{2n} \right) \frac{T_s}{2}. \tag{17}$$

$$I_2 - I_3 = -\frac{1}{L_{\mathrm{eq}}} V_{\mathrm{Cell}k} \left(\frac{T_s}{2} + t_x \right). \tag{18}$$

Based on (11)–(18), the t_x is derived as

$$t_x = \frac{\frac{1}{2} V_{\mathrm{module}} L_{\mathrm{eq}} - V_{\mathrm{Cell}k} (L_{g\_eq} + L_{eq})}{V_{\mathrm{module}} L_{\mathrm{eq}} + 2 V_{\mathrm{Cell}k} (L_{g\_eq} + L_{eq})} T_s \tag{19}$$

L_{g_eq} and the C_{eq} are connected in series. Thus, according to the capacitor ampere-second balance principle, the average current through L_{g_eq} is zero. Hence

$$S_1 + S_2 + S_3 + S_4 + S_5 = 0. \tag{20}$$

The areas S_1, S_2, S_4, and S_5 are triangles, and S_3 is a trapezoid. Therefore, the areas $S_1 - S_5$ can be expressed as

$$\begin{cases} S_1 = \frac{1}{2} t_1 I_1 \\ S_2 = \frac{1}{2} t_2 I_2 \\ S_3 = \frac{1}{2} t_3 (I_2 + I_3) \\ S_4 = \frac{1}{2} t_4 I_4 \\ S_5 = \frac{1}{2} t_5 I_1. \end{cases} \tag{21}$$

Based on (11), (13), and (15), $t_1 - t_5$ can be shown as

$$\begin{cases} t_1 = \frac{I_1 L_{g\_eq}}{\frac{V_{\text{module}}}{2n} + V_{\text{Cell}k}} \\ t_2 = \frac{I_2 L_{g\_eq}}{\frac{V_{\text{module}}}{2n} + V_{\text{Cell}k}} \\ t_3 = \frac{1}{2}T_s - t_x \\ t_4 = \frac{I_3 L_{g\_eq}}{\frac{V_{\text{module}}}{2n} - V_{\text{Cell}k}} \\ t_5 = \frac{I_1 L_{g\_eq}}{\frac{V_{\text{module}}}{2n} - V_{\text{Cell}k}}. \end{cases} \tag{22}$$

The areas $S_1 - S_5$ can be expressed as

$$\begin{cases} S_1 = \frac{I_1^2 L_{g\_eq}}{\frac{V_{\text{module}}}{n} + 2V_{\text{Cell}k}} \\ S_2 = \frac{I_2^2 L_{g\_eq}}{\frac{V_{\text{module}}}{n} + 2V_{\text{Cell}k}} \\ S_3 = \frac{I_2 + I_3}{2}\left(\frac{T_s}{2} - t_x\right) \\ S_4 = \frac{I_3^2 L_{g\_eq}}{\frac{V_{\text{module}}}{n} - 2V_{\text{Cell}k}} \\ S_5 = \frac{I_1^2 L_{g\_eq}}{\frac{V_{\text{module}}}{n} - 2V_{\text{Cell}k}}. \end{cases} \tag{23}$$

By combining (12), (14), (21), (22), and (23), I_2 and I_3 can be derived as

$$I_2 = \frac{(A+B)D^2 - BE^2 - CE}{2EB + 2D(A+B) + 2C} \tag{24}$$

$$I_3 = \frac{(A+B)D^2 - BE^2 - CE}{2EB + 2D(A+B) + 2C} + E \tag{25}$$

where

$$\begin{cases} A = \frac{L_{g\_eq}}{\frac{V_{\text{module}}}{2n} + 2V_{\text{Cell}k}} \\ B = \frac{L_{g\_eq}}{\frac{V_{\text{module}}}{2n} - 2V_{\text{Cell}k}} \\ C = \frac{1}{2}\left(\frac{T_x}{2} - t_x\right) \\ D = \frac{1}{L_{g\_eq}}\left(\frac{V_{\text{module}}}{2n} + V_{\text{Cell}k}\right) t_x \\ E = \frac{1}{L_{\text{eq}}} V_{\text{Cell}k}\left(\frac{T_s}{2} + t_x\right). \end{cases} \tag{26}$$

Therefore, the average output current of the equalizer is

$$I_{Leq} = \frac{I_2 + I_3}{2} = \frac{(A+B)D^2 - BE^2 - CE}{2EB + 2D(A+B) + 2C} + \frac{E}{2}. \tag{27}$$

By substituting (26) into (24) and (25), the expressions of the peak inductor current and the average output current of the equalizer are given as as (28) and (29), shown at the bottom of this page where

$$\begin{cases} V_d = \frac{V_{\text{Cell}k}}{V_{\text{module}}} \\ t_d = \frac{t_x}{T_s} \\ L_d = \frac{L_{g\_eq}}{L_{\text{eq}}}. \end{cases} \tag{30}$$

III. Design Considerations

A. Architecture Design

Based on (29), Fig. 10(a) shows the average output current of the equalizer versus switching frequency under different transformer turns ratios. The output current remains positive when the transformer turns ratio is between 1 and 4. The designed equalization current should fall within the range between 1 and 3 A. To obtain a higher initial equalization current, the switching frequency is selected within the range between 100 and 200 kHz. Lowering the switching frequency and transformer turns ratio can increase the output current, but they will lead to higher diode conduction losses. Moreover, the magnetizing inductance of the transformer will no longer be negligible at lower frequencies as the magnetizing current will increase, leading to a decrease in the efficiency. With a fixed transformer turns ratio, varying the inductance L_g shows that a smaller inductance results in a higher output current, as shown in Fig. 10(b). Therefore, the transformer leakage inductance should be designed within the range of 1.5–2.5 μH. The design process is shown in Fig. 11.

To achieve ZVS, the charge in the parallel capacitor of the half-bridge switch must be fully discharged when the switch is turned ON. This requires a negative current in the transformer leakage inductance, which must satisfy the following condition:

$$\frac{1}{2}L_g i_{Lg}(0)^2 \geq \frac{1}{2}C_{\text{oss}}V_{\text{module}}^2 \tag{31}$$

where $i_{Lg}(0) = I_1$. The curves of I_1 changing with the switching frequency at different leakage inductances are shown in Fig. 10(c). When the switch is turned ON, the leakage inductance current should satisfy

$$|i_{Lg}(0)| \geq \sqrt{\frac{C_{\text{oss}}V_{\text{module}}^2}{L_g}}. \tag{32}$$

The selected switch C_{oss} is 200 pF, and the minimum leakage inductance is 0.5 μH. The ZVS boundary can be obtained. It can be seen that all current curves are below the boundary, so ZVS can be achieved under the designed range of the leakage inductance and switching frequency.

As illustrated in Fig. 12(a), each half-bridge module functions as an ac voltage source (v_{ab_m}). Two series-connected decoupling capacitors ($C_{A\_1} \sim C_{A\_K}$) are employed to compensate for voltage differences between modules. As depicted

$$I_3 = \frac{2(1-16V_d^2n^2)\left[\frac{V_{\text{Cell}k}(T_s^2-4t_x^2)}{8L_{\text{eq}}} - \frac{V_{\text{module}}t_x^2(1+2nV_d)^2}{nL_{g\_eq}(1-16n^2V_d^2)} + \frac{nL_gV_{\text{Cell}k}(T_s+2t_x)^2}{2L_{eq}^2(V_{\text{module}}-4nV_{\text{Cell}k})}\right]}{T_s[1+6t_d+16V_d^2(16n^2L_d-n^2+2n^2t_d+2L_dn^2t_d)+4V_d(nL_d+4nt_d+2nL_dt_d)]} \tag{28}$$

$$I_{Leq} = \frac{2V_{\text{module}}t_x(1+2nV_d)(t_d+nL_dV_d+2nV_dt_d+2nL_dV_dt_d)}{nL_g[1+4nL_dV_d-16n^2V_d^2+16n^2L_dV_d^2+t_d(6+8nL_dV_d+16nV_d+32n^2V_d^2+32n^2L_dV_d^2)]} \tag{29}$$

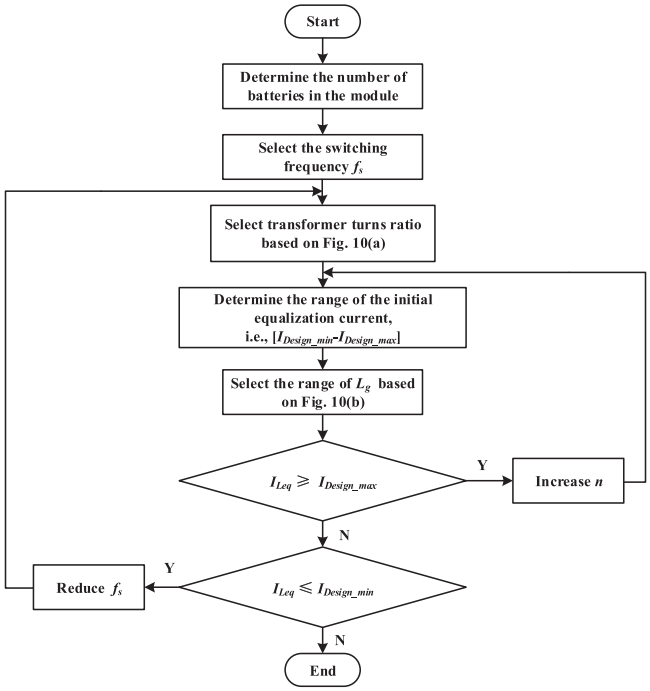

Fig. 11. Design process flow chart.

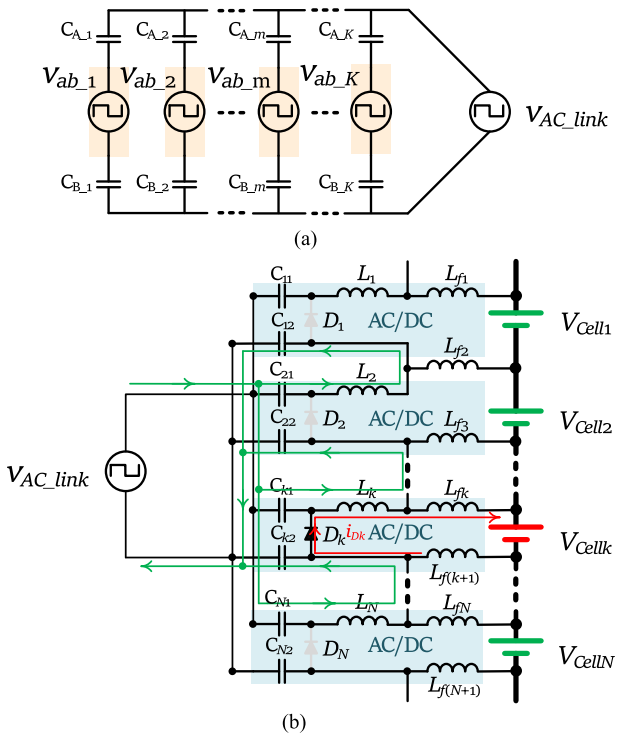

Fig. 12. (a) Equivalent circuit of the half-bridge circuit. (b) Simplified circuit of the proposed equalizer.

in Fig. 12(b), the coupled capacitors ($C_{11} \sim C_{N2}$) serve to isolate each branch, forming a single-input, multiple-output circuit topology. In addition, the filter inductors ($L_{f1} \sim L_{f(N+1)}$) present a high impedance to high-frequency components, effectively blocking ac currents. The ac path is highlighted in green while the dc path is shown in red. This guarantees that the equalization current is delivered as a pure dc output, thereby minimizing any ac-induced heating of the cells. Furthermore, the filter capacitors can be omitted to minimize the overall component count.

B. *Efficiency Analysis*

To evaluate the performance of the proposed modular equalizer, a detailed efficiency analysis is conducted. All key loss mechanisms are considered, including diode loss ($D_1 \sim D_N$), switch loss ($Q_1 - Q_2$), capacitor loss ($C_A \sim C_B$ and $C_{11} \sim C_{N1}$), and magnetic component loss (Transformer, $L_1 \sim L_N$, and $L_{f1} \sim L_{fN}$).

1) *Diode loss:* The diodes can be expressed as

$$P_{\text{diode}} = PV_D I_{Leq} \tag{33}$$

where P is the number of the cells under charging and V_D is the forward voltage of the diodes.
Moreover, due to the voltage ripple of the coupling capacitors, when the ripple exceeds the voltage difference between batteries, the diodes in higher voltage battery branches become conductive, resulting in a reduction of the equalization efficiency.

2) *Switch loss:* The switch loss arises primarily from the ON-resistance of the switches and the turn-OFF loss

$$P_{\text{con}} = R_{on} I_{Q1}^2 + R_{\text{on}} I_{Q2}^2 \tag{34}$$

where R_{on} denotes the ON-state resistance of the switching device, and I_{Q1} and I_{Q2} are the rms current of the Q_1 and Q_2.
Since Q_1 to Q_2 are turned ON under zero-voltage conditions, their turn-ON losses can be neglected. Consequently, the dominant switching losses are attributed to turn-OFF transitions. The total turn-OFF loss P_{off} is therefore given by

$$P_{\text{off}} = \frac{I_{\text{off1}}^2}{24C_{\text{oss}}} t_f^2 + \frac{I_{\text{off2}}^2}{24C_{\text{oss}}} t_f^2 \tag{35}$$

where I_{off1} and I_{off2} are the current of the switching devices at turn OFF, and t_f is the turn OFF time obtained from the datasheet.

3) *Capacitor loss:* The capacitor loss can be calculated as follows:

$$P_{\text{C}} = \left(\text{ESR}_{CA} + \text{ESR}_{CB} + \frac{\text{ESR}_{Ck1} + \text{ESR}_{Ck2}}{N} \right) \cdot n^2 \cdot I_M^2 \tag{36}$$

where ESR was measured experimentally. The rms current values for capacitors can be accurately determined through circuit simulation analysis.

4) *Transformer loss:* The loss includes core loss and copper loss in the inductors and transformers.
The coil loss of the magnetic components P_{coil} is expressed as

$$P_{\text{coil}} = R_{\text{trans}} {I_M}^2 \tag{37}$$

where R_{trans} is the dc resistance of the coil in transformer.

TABLE I
CRITICAL DESIGN PARAMETERS

Component Type	Parameters
Microcontroller	STM32F407
MOSFET(Q)	BSC320N20N
Battery	ICR18650
Diode(D)	STPS30L30CG-TR
Transformer turns ratio (n)	$4:1$
Leakage inductance (L_g)	$1.8\mu H$
Magnetizing inductance (L_m)	$170\mu H$
Switching frequency (f_s)	110kHz-200kHz
Decoupling capacitor (C_A/C_B)	$13\mu F$
Coupling capacitor ($C_{11} \sim C_{N2}$)	$20\mu F$
Inductor (L_k)	$10\mu H$
Filter inductor (L_{fk})	$4.7\mu H$

The core losses in the transformer are estimated using Steinmetz's equation

$$P_{\text{core}} = V_c \cdot K_c \cdot f_s^{\alpha} \cdot \Delta B^{\beta} \tag{38}$$

where V_c is the volume of the core, and K_c, α, and β are material-dependent coefficients obtained from the manufacturer's datasheet, and ΔB represents the peak-to-peak magnetic flux density variation. The total loss of the magnetic components is

$$P_{\text{trans}} = P_{\text{coil}} + P_{\text{core}}. \tag{39}$$

5) *Inductor loss:* The inductor loss is shown as

$$P_L = P \cdot R_{L\_\text{coil}} {I_{Lk\text{rms}}}^2 + (P+1) \cdot R_{Lf\_\text{coil}} {I_{Lf k\text{rms}}}^2 \tag{40}$$

where R_{L_coil} and R_{Lf_coil} are the dc resistance of inductors ($L_1 \sim L_N$) and ($L_{f1} \sim L_{f(N+1)}$) respectively, and $I_{Lk\text{rms}}$ is the rms current of inductors ($L_1 \sim L_N$).

IV. EXPERIMENTAL VERIFICATIONS

A. Hardware Implementation

To validate the feasibility and effectiveness of the proposed equalization architecture, a laboratory prototype was built and tested. The key parameters of the prototype system are summarized in Table I. The experimental setup includes $K = 2$ equalization modules, each consisting of $N = 8$ series-connected lithium-ion battery cells (2900 mAh). The converter operates at a switching frequency of 110 kHz, with a transformer turns ratio of $n = 4$. Fig. 13 illustrates the experimental setup, the half-bridge and transformer, the equalization module, and the rectification and filtering circuit, respectively. To improve the power conversion efficiency of the modular equalizer, low-forward-voltage Schottky diodes (TPS30L30CG-TR) are employed to reduce conduction losses. The battery voltages are monitored using a Keysight 34970A data acquisition system.

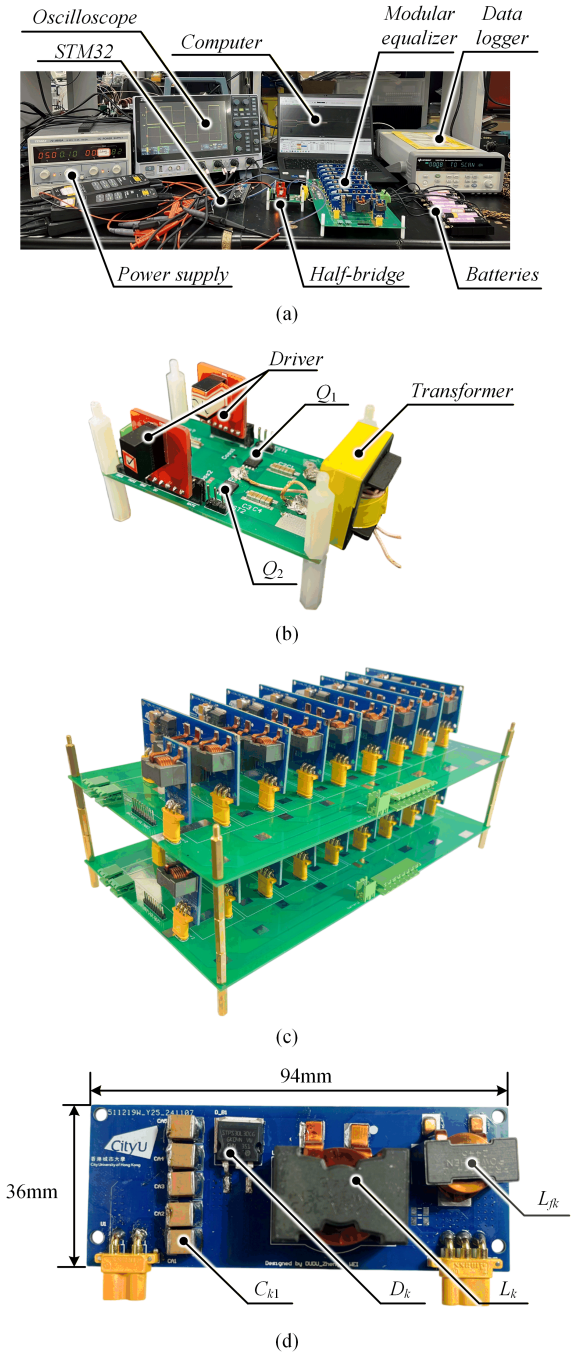

Fig. 13. (a) Photo of the experiment setup. (b) Prototype of the half-bridge with transformer. (c) Prototype of designed modular equalizer. (d) Cell rectifier and filter circuit.

B. Experimental Verification

Fig. 14(a) illustrates the measured v_{gs} and v_{ds} waveforms of switch Q_1 and Q_2 at the 200 kHz switching frequency and 1:1 turns ratio. It can be observed that the switch turns on under zero-voltage conditions, confirming the presence of ZVS. Fig. 14(b) shows the current waveforms of leakage inductance L_g and inductor L_8. Fig. 15 shows that when the frequency is reduced to 110 kHz and the transformer turns ratio is increased to

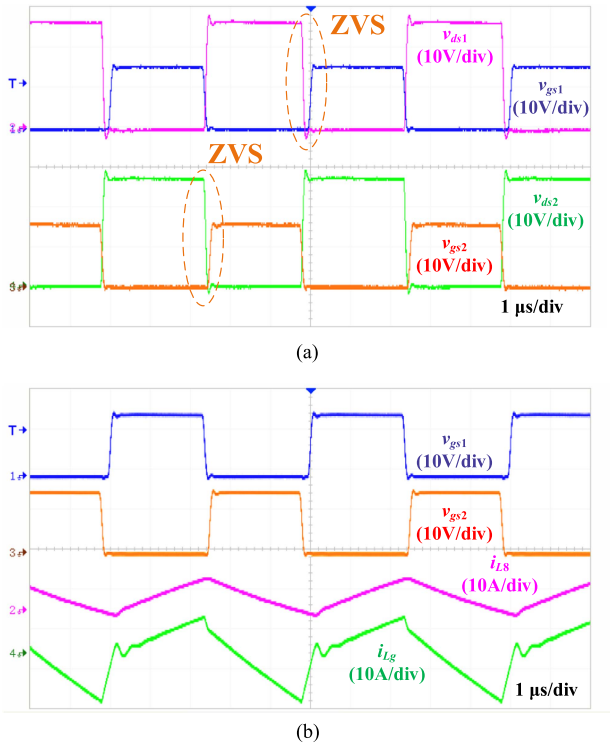

Fig. 14. Key waveforms of the modular equalizer at 200 kHz. (a) Switches Q_1 and Q_2: gate drive signal v_{gs1} and v_{gs2}, drain source voltage v_{ds1} and v_{ds2}. (b) v_{gs1} and v_{gs2}, current waveforms of leakage inductance L_g and inductor L_8.

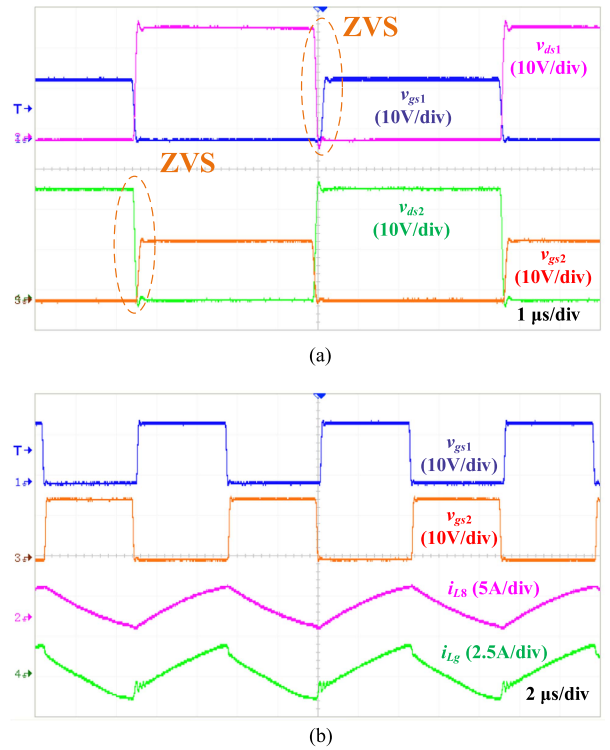

Fig. 15. Key waveforms of the modular equalizer at 110 kHz. (a) Switches Q_1 and Q_2: gate drive signal v_{gs1} and v_{gs2}, drain source voltage v_{ds1} and v_{ds2}. (b) v_{gs1} and v_{gs2}, current waveforms of leakage inductance L_g and inductor L_8.

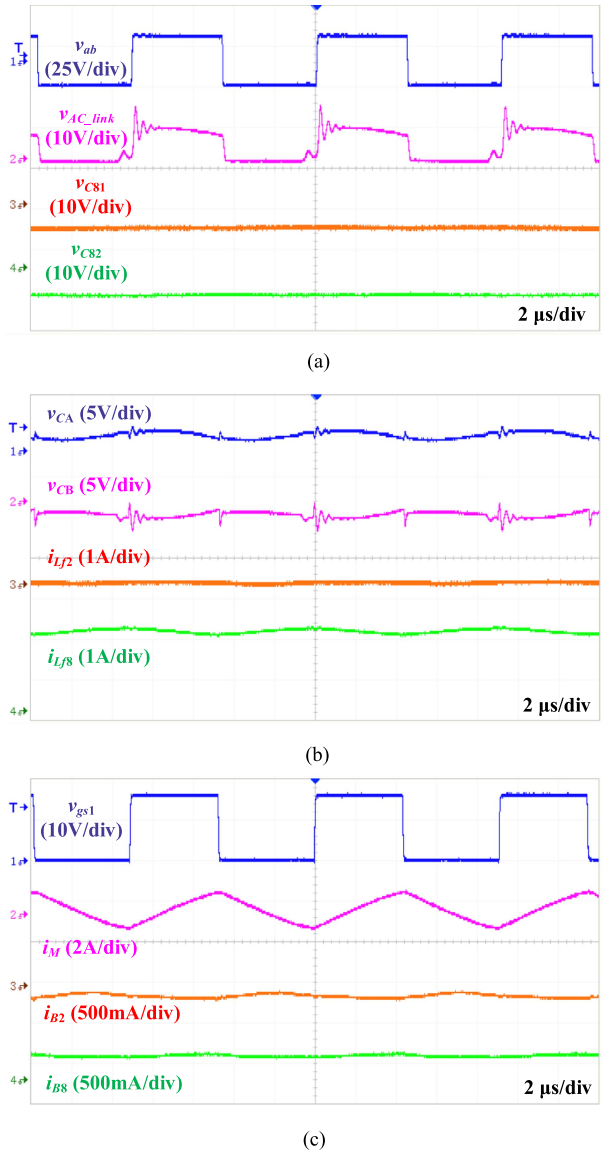

Fig. 16. Experimental waveforms of the modular equalizer. (a) Half-bridge voltage v_{ab}, AC-link voltage $v_{\mathrm{AC\_link}}$, coupling capacitor voltage v_{C81} and v_{C82}. (b) Decoupling capacitor voltage v_{CA} and v_{CB}, filter inductor current of discharging cell i_{Lf2} charging cell i_{Lf8}. (c) Gate drive signal v_{gs1}, module current i_M, equalization current i_{B2}, and equalization current i_{B8}.

4:1, the peak current decreases significantly. Both switches successfully achieve ZVS. The deadtime is 200ns. Fig. 16(a) shows the measured voltage waveforms of the half-bridge voltage v_{ab}, ac-link voltage $v_{\mathrm{AC\_link}}$, coupling capacitor voltage v_{C81} and v_{C82}. Fig. 16(b) shows the decoupling capacitor voltage v_{CA} and v_{CB}, filter inductor current of discharging cell i_{Lf2} charging cell i_{Lf8}. The module current (i_M) and equalization current (i_{B2} and i_{B8}) are shown in Fig 16(c). There are eight cells in the battery string with a maximum voltage difference of 200 mV. Cell_8 is the cell with the lowest voltage and is charged during the equalization process. Cell_2 is the cell with the highest voltage and is discharged during the equalization process. As shown, the equalization current i_{B2} is negative while i_{B8} is positive. Fig. 17 shows the measured conversion efficiency of

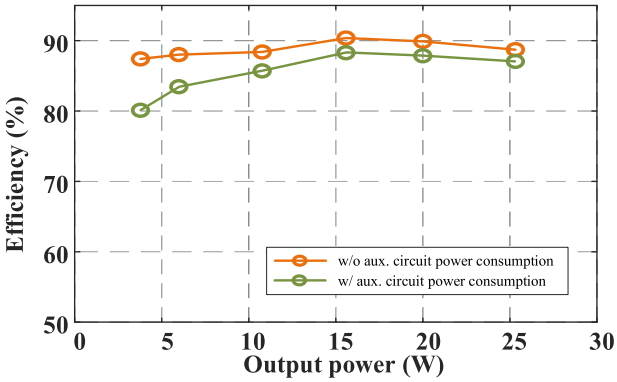

Fig. 17. Experimentally measured conversion efficiency.

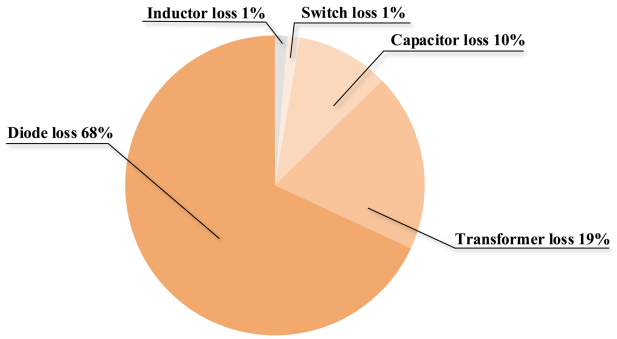

Fig. 18. Calculated power loss breakdown of design equalization circuit.

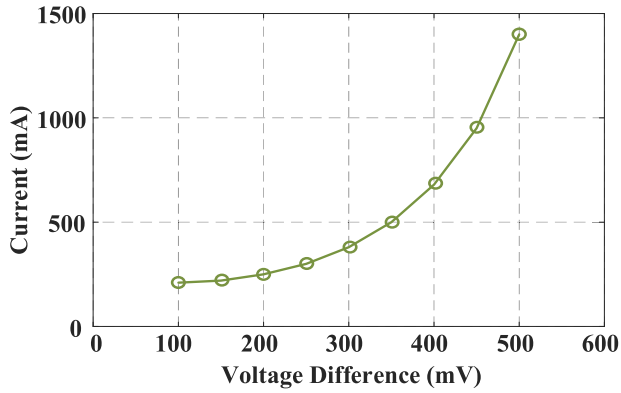

Fig. 19. Measured equalization current of the modular equalizer versus voltage difference when two cells are charging.

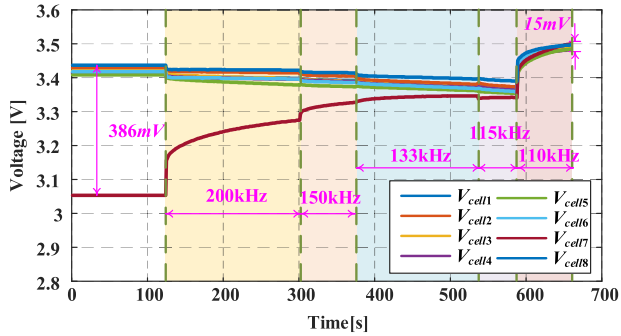

Fig. 20. Experimental results of the equalization operation with gradually reduced switching frequency.

the proposed equalizer with and without the power consumption of the auxiliary circuit included. Without taking the power consumption of the auxiliary circuit into account, the efficiency remains above 87% across various output power levels, reaching a peak efficiency of 90.37%. As shown in Fig. 18, the calculated power losses of the proposed equalizer, including diode loss, transformer loss, capacitor loss, inductor loss, and switch loss, excluding the consumption of the auxiliary circuit. The loss breakdown is analyzed under conditions where an eight-cell string consists of seven cells being discharged and one cell being charged. The voltage of the discharging cells ranges from 3.75 to 3.85 V, while the charging cell has a voltage of 3.44 V. The main auxiliary circuit is the gate driver that consumes 400 mW. If the auxiliary power consumption is taken into account, the efficiency ranges between 80% and 88.3%, as shown in Fig. 17. The diode loss accounts for the main part of the total loss. Fig. 19 illustrates the relationship between equalization current and voltage difference. As observed, the equalization current gradually decreases as the voltage deviation narrows, allowing the equalization process to terminate automatically without additional control intervention.

Fig. 20 illustrates the equalization results for an eight-cell battery pack with an initial maximum voltage difference of 386 mV. During the process, the switching frequency was gradually reduced from 200 to 110 kHz. As observed, when the frequency was lowered from 200 to 150 kHz, a noticeable voltage jump occurred in Cell_7, indicating an increase in equalization current. In addition, the voltage convergence rate was observed to slow down as the voltage deviation diminished, highlighting the reduced equalization current under small voltage differences. To accelerate the final stage of equalization, the switching frequency was further reduced to increase the equalization current. After 510 s, the voltage deviation dropped below 50 mV. At this point, the switching frequency was adjusted from 115 to 110 kHz, and a 1 A charging current was applied to emulate real-world charging conditions. After an additional 80 s, the voltage difference among cells was further reduced to 15 mV. Therefore, to accelerate the equalization process, a lower switching frequency can be applied during the initial stage to increase the equalization current. Variable-frequency equalization enables dynamic adjustments to the equalization current, a feature not available in fixed-frequency equalization. As the voltage difference between batteries decreases, the equalization current also reduces; variable-frequency equalization compensates for this by lowering the switching frequency. This approach allows for enhanced control over equalization speed compared to fixed-frequency equalization, although it does increase the complexity of the control system.

Figs. 21 and 22 present the experimental terminal voltages of individual cells with fixed 110 kHz switching frequency under different operating scenarios. Fig. 21(a) shows the equalization result for eight cells with the initial voltages of 2.914, 3.070, 3.575, 3.561, 3.571, 3.578, 3.570, and 3.083 V, respectively. During the equalization process, no charging or discharging operations are performed on the battery pack. As shown, the initial maximum voltage difference is 664 mV. After 2960 s

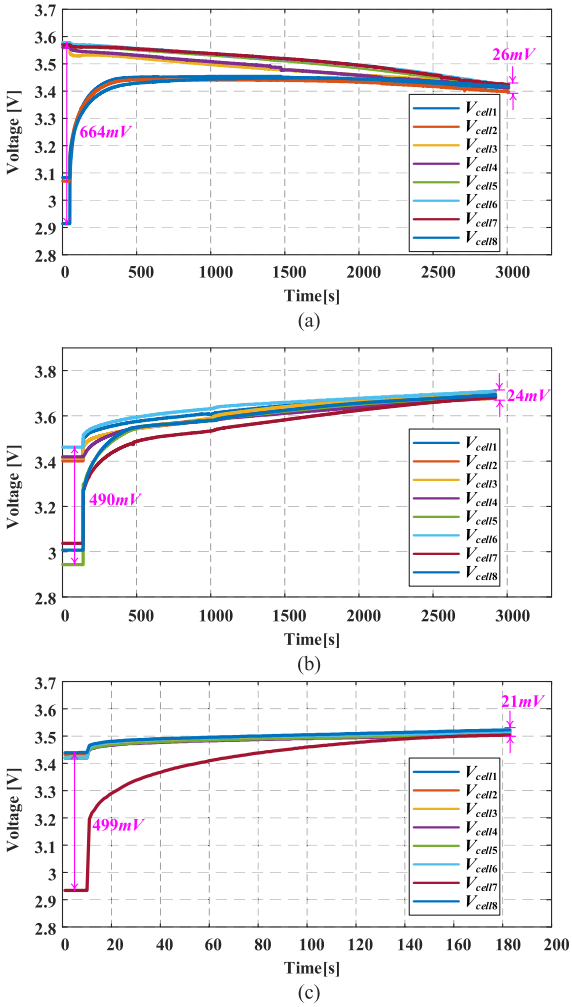

Fig. 21. Experimental results of the equalization operation with different voltage distributions. (a) Idle condition for single module equalization with an initial voltage difference of 664 mV. (b) Equalization under a 1 A charging condition with an initial voltage difference of 490 mV. (c) Equalization under a 0.5 A charging condition with an initial voltage difference of 499 mV.

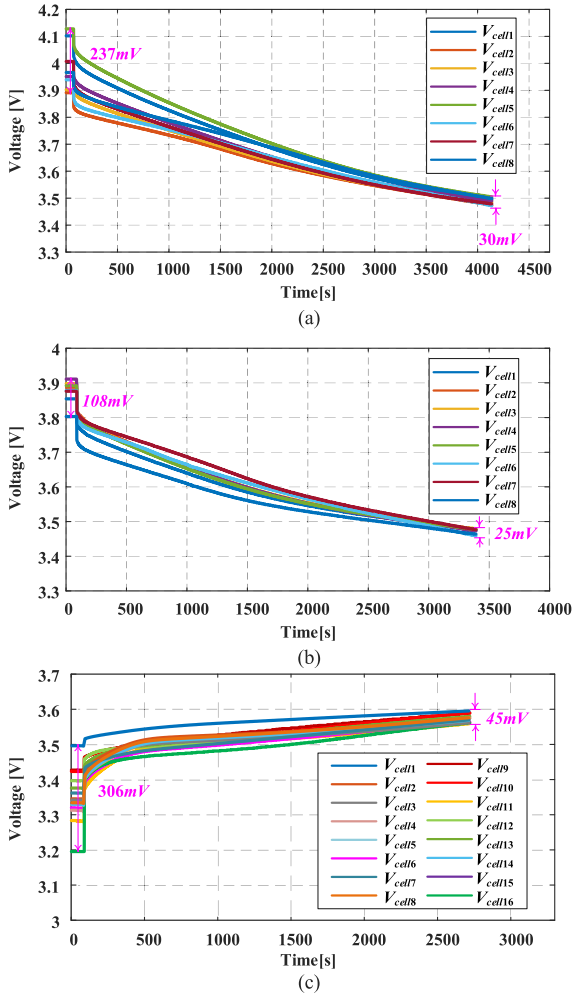

Fig. 22. Experimental results of the equalization operation with different voltage distributions. (a) Equalization under a 1 A discharging condition with an initial voltage difference of 237 mV. (b) Equalization under a 1 A discharging condition with an initial voltage difference of 108 mV. (c) Equalization of a 16-cell battery pack composed of two modules under a 1 A charging condition, with an initial voltage difference of 306 mV.

of equalization, the voltage difference is reduced to 26 mV. Fig. 21(b) illustrates the equalization results of an eight-cell battery pack under a 1 A charging condition. The initial voltage difference is 490 mV. After 2780 s of equalization, the voltage deviation is reduced to 24 mV. Fig. 21(c) presents the equalization performance when one cell has a significantly lower voltage compared to the average voltage of the battery pack. The battery pack operates under a 0.5 A charging condition. As shown, the initial voltage difference is 499 mV, which is reduced to 21 mV after 170 s of equalization. The equalization current is distributed to the under-voltage cells by the equalizer based on their voltage deviation. When only one cell has a voltage lower than the average, the entire equalization current is directed to that cell, resulting in the shortest equalization time. Conversely, when multiple cells are below the average voltage, the equalization current is shared among them, which reduces the current available to each cell and extends the equalization duration. Fig. 22(a) and (b) illustrates the equalization results under a 1 A discharging condition for two different initial voltage distributions. In Fig. 22(a), the initial voltage deviation is 237 mV, which is reduced to 32 mV after 4050 s of equalization. In Fig. 22(b), the initial voltage deviation is 108 mV, and it is reduced to 28 mV after 3300 s. Fig. 22(c) presents the experimental results of a 16-cell battery pack balanced using two equalization modules. The initial cell voltages are randomly distributed, with a maximum voltage deviation of 306 mV. After 2610 s of equalization, the maximum voltage difference is reduced to 48 mV.

V. Comparison With Prior Art

Table II summarizes key attributes of eight representative active equalization circuits reported in the literature. To facilitate a comprehensive evaluation, each equalization topology is compared across multiple dimensions: Type of energy flow refers to the overall energy flow mechanism, C2C, P2C, or hierarchical module equalizer (HME). Modularity indicates whether the architecture is inherently modular, enabling easy

TABLE II
COMPARISON OF DIFFERENT EQUALIZERS

Circuit Topology	Flyback converter [29]	Bidirectional forward converter [30]	LLC and buck-boost [27]	Class-D and multi-active-bridge [26]	Buck-boost [28]	Multiport converter [31]	Cascade DAB [32]	AC-Bus SEPIC [33]	Proposed Structure
Type of energy flow	C2C	C2C	HME	HME	HME	P2C	P2C	M2C	M2C
System modularity	No	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Multi-cell equalization	No	No	No	No	No	Yes	No	No	Yes
Increase of switch voltage stress with # of cells	No	No	Yes	No	No	Yes	No	No	No
Autonomous equalization	No	No	No	No	Yes	No	No	Yes	Yes
External supply source	Yes	Yes	No	No	No	No	No	No	No
Equalization speed**	Medium	Slow	Fast	Fast	Slow	Fast	Slow	Medium	Medium
Control complexity***	High	High	High	High	Medium	High	High	Low	Low
High-frequency switch count	6	4	$\frac{3}{2}n+2$	$2n+\frac{1}{2}n$	$n+\frac{2}{3}n+1$	$4n+4$	$\frac{1}{2}n$	$\frac{1}{2}n$	$\frac{1}{4}n$
Ratio of switch voltage stress w.r.t. cell voltage	n	n	n	4	3	$\frac{1}{2}n$	4	2	8
Reported efficiency (%)	87*	-	86.74 & 89.66 *	74 & 93	-	91.1*	84*	86	90.1
Selection switches & Drivers	$2n+2$	$n+5$	$\frac{1}{4}n+5$	0	0	$2n$	$n+1$	0	0
Diode	4	0	2	0	0	0	0	n	n
Capacitor	4	3	2	n	0	$2n+1$	$\frac{3}{4}n$	n	$2n+\frac{1}{4}n$
Inductor	0	1	$\frac{3}{4}n$	$2n$	$n+1$	$n+1$	$\frac{3}{16}n$	n	$2n+\frac{1}{8}n$
Transformer/ Coupled inductor (windings)	2(4)	$1(2)^{+}$	1(3)	1(3)	0	1(n+1)	$\frac{1}{4}n(2)$	$\frac{1}{2}n$(n)	$\frac{1}{8}n(2)$
Cost ($) ****	6.10	7.88	7.39	11.95	5.49	13.92	5.06	2.69	3.61
Number of Test Cells	12	12	8	4	15	5	10	4	16

*Power dissipation of the selection switches not mentioned.
**Slow: Non-constant current and non-multi-cell equalization; Medium: Constant current or multi-cell equalization; Fast: Constant current and multi-cell equalization.
*** High: Switch count is larger than cell count and non-autonomous equalization; Medium: Switch count is less than cell count or autonomous equalization; Low: Switch count is less than cell count and autonomous equalization; Switch count is the sum of high-frequency switches and selection switches.
**** Component cost per unit [34]: MOSFET: $0.20 – $1.75. MOSFET Driver: $1.8. GaN: $2.11. Diode: $0.17 - $0.65. Capacitor: $0.2. Inductor: $0.5. Transformer Core: $0.9. Winding: $0.2. Transformer^{+}: $2.52. Relay: $1.22 - $2.87.

scaling across battery pack sizes. Multicell equalization denotes whether the circuit can equalize multiple cells concurrently, which directly impacts equalization speed. Increase of switch voltage stress with number of cells indicates whether the voltage stress on switching devices increases with the number of series-connected cells. Autonomous equalization reflects whether the equalizer can dynamically direct energy flow between cells without external control or selection logic. External supply source identifies whether the equalization process needs to rely on a power source other than the battery pack. Equalization speed is classified as slow, medium, or fast based on whether the topology supports constant current operation and simultaneous multicell equalization. The complexity is categorized into low, medium, and high, based on the number of active switches and the support for autonomous equalization. High-frequency switch count represents the number of active switches operating at switching frequency, affecting control complexity and cost. Selection switch and drivers count refers to the number of additional switches required to route the equalization current to a specific cell. Number of diodes, Capacitors, inductors, transformers, and coupled inductor quantifies the total passive components required, which influences circuit complexity, cost, and size. Cost is the total price of all components of the equalizer divided by the number of cells. Number of test cells refers to how many cells were used in experimental validation, which reflects the maturity and scalability of the proposed design.

The authors in [29] and [30] adopted C2C architectures in which energy is transferred between individual cells through a dedicated converter and a selection switch network. These structures do not support simultaneous equalization of multiple cells and lack autonomous equalization capability, relying instead on complex control logic to identify and activate the appropriate energy path. Furthermore, both topologies require an auxiliary battery to operate, which adds additional system complexity. The authors in [27], [26], and [28] employed HME architectures, which enable energy transfer both within individual modules and across multiple modules. However, since these topologies still rely on shared converter structures, they are inherently limited in supporting single module at a time, thus realization of multi-cell equalization is a challenge. Moreover, all three designs require a large number of high-frequency switches. As the number of cells increases, both the control complexity and implementation cost rise significantly, posing challenges for large-scale deployment. The authors in [31] and [32] utilized P2C architectures. Among them, Qi et al. [31] supported multicell equalization, while Uno and Yoshino [32] adopted a capacitively coupled design

that eliminates multiwinding transformers, thereby reducing system volume. However, both topologies rely heavily on selection switches and lack autonomous equalization capability, requiring external control to manage energy flow. In contrast, Hasanpour et al. [33] employed a module-to-cell (M2C) architecture that eliminates the need for selection switches and enables autonomous multicell energy equalization. Nevertheless, it requires a large number of transformers, which increases the system's implementation complexity.

The use of numerous switches and their associated drivers presents challenges to system cost. In large-scale energy storage systems, as the number of cells increases, the controller must manage hundreds of switches, substantially increasing control complexity. Additionally, the power losses associated with switch drivers become nonnegligible. In [27], [29], and [30], relays are used as selection switches, potentially compromising system reliability. In contrast, passive components exhibit a lower failure risk compared to active switches and have significantly lower costs than semiconductor devices and their drivers. Moreover, leveraging circuit characteristics for equalization eliminates the need for the controller to manage multiple switching signals, thereby markedly reducing control complexity. The proposed equalizer, by utilizing circuit characteristics, achieves adaptive current distribution, eliminating the need for complex equalization logic and control strategies tailored to varying voltage distributions.

In summary, compared with existing approaches, the proposed equalizer eliminates the need for complex selection switch networks and multiwinding transformers, while enabling autonomous multicell energy equalization. Its modular architecture adopts a half-bridge structure composed of only two switches for every eight cells, significantly reducing the number of high-frequency switches and thereby lowering overall control complexity.

VI. Conclusion

A novel modular equalizer topology based on a half-bridge and capacitively-coupled ac link was presented and experimentally validated. The system achieves M2C equalization using a simplified control scheme with only two global PWM signals, eliminating the need for complex control circuits. All switches operate under zero-voltage switching, contributing to high efficiency and reduced switching loss. The circuit achieves adaptive current distribution without the use of selection switches or multiwinding transformers. By converting the voltage of each module into an ac signal and coupling it to a shared ac link, the system enables effective energy transfer among modules, allowing lower-voltage cells to autonomously receive energy. Extensive experimental results in multiple operating scenarios, including charging, discharging, and idle conditions, confirm that the proposed equalizer can effectively and reliably reduce cell voltage imbalances. Across different test cases, initial voltage differences ranging from 108 to 664 mV were reduced to below 50 mV within 170–4050 s, depending on the configuration.

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References

[1] M. H. Lipu et al., "Data driven health and life prognosis management of supercapacitor and lithium-ion battery storage systems: Developments, implementation aspects, limitations, and future directions," *J. Energy Storage*, vol. 98, 2024, Art. no. 113172.

[2] H. Zhang, X. Hu, Z. Hu, and S. J. Moura, "Sustainable plug-in electric vehicle integration into power systems," *Nature Rev. Electr. Eng.*, vol. 1, no. 1, pp. 35–52, Jan. 2024.

[3] W. Gao, Z. Cao, N. V. Kurdkandi, Y. Fu, and C. Mi, "Evaluation of the second-life potential of the first-generation nissan leaf battery packs in energy storage systems," *eTransportation*, vol. 20, 2024, Art. no. 100313.

[4] Y. Izadi and R. Beiranvand, "A comprehensive review of battery and supercapacitor cells voltage-equalizer circuits," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15671–15692, Dec. 2023.

[5] N. Ghaeminezhad, Q. Ouyang, X. Hu, G. Xu, and Z. Wang, "Active cell equalization topologies analysis for battery packs: A systematic review," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9119–9135, Aug. 2021.

[6] Z. Gong, A. Chowdhury, and O. Trescases, "Lifetime performance analysis of imbalanced EV battery packs and small-signal cell modeling for improved active balancing control," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13264–13276, Nov. 2022.

[7] A. Ahmad, V. Singh, A. V. R. Teja, and S. Payami, "Parallel active charge balance technique of li-ion batteries using combined phase shifted and boost DC-DC converter," in *Proc. IECON 2023- 49th Annu. Conf. IEEE Ind. Electron. Soc.*, 2023, pp. 1–6.

[8] D. Karnehm, A. Samanta, L. Anekal, S. Pohlmann, A. Neve, and S. Williamson, "Comprehensive comparative analysis of deep-learning-based state-of-charge estimation algorithms for cloud-based lithium-ion battery management systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 597–604, Apr. 2024.

[9] F. S. J. Hoekstra, H. J. Bergveld, and M. C. F. Donkers, "Optimal control of active cell balancing: Extending the range and useful lifetime of a battery pack," *IEEE Trans. Control Syst. Technol.*, vol. 30, no. 6, pp. 2759–2766, Nov. 2022.

[10] C. Zhang, N. Cui, Z. Zhou, Y. Shang, B. Duan, and Q. Zhang, "Multi-cell-to-multi-cell equalizers based on matrix and half-bridge LC converters for series-connected battery strings," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1755–1766, Jun. 2020.

[11] S. K. Dam and V. John, "A modular fast cell-to-cell battery voltage equalizer," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9443–9461, Sep. 2020.

[12] Y. Shang, C. Zhang, N. Cui, and C. C. Mi, "A delta-structured switched-capacitor equalizer for series-connected battery strings," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 452–461, Jan. 2019.

[13] P.-H. La and S.-J. Choi, "Direct cell-to-cell equalizer for series battery string using switch-matrix single-capacitor equalizer and optimal pairing algorithm," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8625–8639, Jul. 2022.

[14] J. Sahoo, R. Parnapalli, A. Patra, and S. Mukhopadhyay, "Interleaved switching for loss minimization in adjacent cell-to-cell balancing architectures," *IEEE Trans. Ind. Electron.*, vol. 71, no. 12, pp. 16834–16844, Dec. 2024.

[15] Z. Wei, F. Peng, and H. Wang, "An LCC based string-to-cell battery equalizer with simplified constant current control," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1816–1827, Feb. 2022.

[16] X. Qi, Y. Wang, and M. Fang, "An integrated cascade structure-based isolated bidirectional DC-DC converter for battery charge equalization," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12003–12021, Nov. 2020.

[17] J. Nie, R. Fu, C. Cai, J. Ma, Z. Shu, and L. Ma, "A high efficiency battery equalizing circuit based on half bridge topology with multiport transformer," *IEEE Trans. Ind. Electron.*, vol. 71, no. 3, pp. 2522–2532, Mar. 2024.

[18] R. Zhang, S. Wang, Z. Cao, and H. S.-H. Chung, "A Galvanic-isolated automatic equalization charging system for series-connected cells or battery strings," *IEEE Trans. Ind. Electron.*, vol. 71, no. 11, pp. 13943–13954, Nov. 2024.

[19] N. Jabbour, E. Tsioumas, D. Papagiannis, and C. Mademlis, "An improved equalization and energy support strategy for battery-powered electric motor drives," *IEEE Trans. Transp. Electrific.*, vol. 11, no. 1, pp. 2539–2555, Feb. 2025.
[20] Y. Shang, C. Zhang, N. Cui, and J. M. Guerrero, "A cell-to-cell battery equalizer with zero-current switching and zero-voltage gap based on quasi-resonant LC converter and boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3731–3747, Jul. 2015.
[21] M. Uno, D. Cheng, S. Onodera, and Y. Sasama, "Bidirectional buck-boost converter using cascaded energy storage modules based on cell voltage equalizers," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 1249–1261, Jan. 2023.
[22] S. K. Dam and V. John, "Low-frequency selection switch based cell-to-cell battery voltage equalizer with reduced switch count," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 3842–3851, Jul./Aug. 2021.
[23] M. M. Hoque, M. A. Hannan, A. Mohamed, and A. Ayob, "Battery charge equalization controller in electric vehicle applications: A review," *Renew. Sustain. Energy Rev.*, vol. 75, pp. 1363–1385, 2017.
[24] K. Manjunath, R. Kalpana, B. Singh, and K. R., "A two-stage module based cell-to-cell active balancing circuit for series connected lithium-ion battery packs," *IEEE Trans. Energy Conver.*, vol. 38, no. 4, pp. 2282–2297, Dec. 2023.
[25] Z. Wei, H. S.-H. Chung, and R. Zhang, "Autonomous battery equalization module using capacitively coupled input-parallel output-series structure," *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 6162–6176, Apr. 2025.
[26] M. Liu, Y. Chen, Y. Elasser, and M. Chen, "Dual frequency hierarchical modular multilayer battery balancer architecture," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3099–3110, Mar. 2021.
[27] F. Peng, H. Wang, and Z. Wei, "An LLC-Based highly efficient S2M and C2C hybrid hierarchical battery equalizer," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5928–5937, Jun. 2020.
[28] K. Manjunath, R. Kalpana, and B. Singh, "A modularized two-stage active cell balancing topology with reduced balancing time for series connected li-ion battery string," *IEEE Trans. Ind. Appl.*, vol. 61, no. 1, pp. 502–514, Jan./Feb. 2025.
[29] S. Liu, Y. Wang, S. Wang, W. Zhao, and Y. Shang, "A compact large-current equalizer based on flyback conversion for large-scale battery packs," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 738–748, Jan. 2025.
[30] S. Jinlei, L. Wei, T. Chuanyu, W. Tianru, J. Tao, and T. Yong, "A novel active equalization method for series-connected battery packs based on clustering analysis with genetic algorithm," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7853–7865, Jul. 2021.
[31] X. Qi, Y. Wang, M. Fang, H. Wang, Y. Wang, and Z. Chen, "A family of integrated cascade multiport converters for centralized equalization systems: Derivation, analysis, and verification," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7398–7415, Jun. 2023.
[32] M. Uno and K. Yoshino, "Modular equalization system using dual phase-shift-controlled capacitively-isolated dual active bridge converters to equalize cells and modules in series-connected lithium-ion batteries," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2983–2995, Mar. 2021.
[33] N. Hasanpour, M. R. Mohammadi, A. Tavakoli, and S. Ali Khajehoddin, "Modular voltage equalizer circuit with AC-bus inter-modules connection," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 682–698, Mar. 2024.
[34] "Digikey electronics electronic components distributor," Aug. 2025. [Online]. Available: https://www.digikey.com

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