Letters

Influence of Coupling Conduction Mechanism Between MOS-Channel and Body Diode on 3rd Quadrant Surge Current Capability of Planar-Gate SiC MOSFETs

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***Abstract*—This letter investigates the coupling conduction mechanism between the MOS-channel and the body diode of planar-gate SiC MOSFETs (planar MOSFETs), as well as its influence on third-quadrant surge current capability. It reveals that the MOS-channel and the body diode are not two independent current paths when the MOS-channel is turned ON; instead, the MOS-channel suppresses the conduction capability of the body diode. This coupling conduction mechanism results in weaker surge current capability of the device under positive V_{gs} compared to that under negative V_{gs}, which depends on pulse width and case temperature. The underlying mechanism is an elevated potential around the p-well region when the MOS-channel is turned ON, which reduces the effective conduction area of the body diode. This mechanism is elucidated through TCAD simulations and validated by experimental results. These findings enhance the understanding of the surge current performance of planar MOSFETs under varying gate bias conditions.**

***Index Terms*—Silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs), surge current, third quadrant.**

I. Introduction

BENEFITING from the merits of higher voltage blocking capability, higher frequency, higher operating temperature, silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) are penetrating various applications, especially in renewable energy generation and electric vehicles (EVs) [1]. These scenarios impose stringent requirements on the surge current capability of SiC MOSFETS [2].

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In renewable energy generation, grid-connected inverters must possess sufficient overcurrent capability to enhance power system robustness during disturbances [2]. The surge current capability of power devices is one of the inherent limits. In EVs, SiC MOSFETS suffer surge current under active short circuit mode, which serves to protect the motor drive system from catastrophic failure [3]. In these operating conditions, SiC MOSFETS are subjected to surge current in both the first and the third quadrants, with peak amplitudes reaching several times their rated current. Therefore, it is necessary to conduct a comprehensive investigation into the third-quadrant surge current capability of SiC MOSFETs.

The research works focusing on the third-quadrant surge current capability of SiC MOSFETs can be summarized into two aspects: 1) Investigation of the third-quadrant characteristics; 2) evaluation of the surge current capability. The third-quadrant *I-V* characteristics of SiC MOSFETs are strongly dependent on the applied V_{gs}. When V_{gs} is sufficiently negative, the MOS-channel is fully turned OFF and the device behaves like a p-i-n diode [4]. As V_{gs} approaches 0 V, a surface channel can be formed due to the body effect [4]. Some studies have developed physical models to explain the partial conduction of the MOS-channel and its impact on reverse conduction behavior [5], [6]. When a high positive V_{gs} is applied, the MOS-channel becomes fully conductive and may clamp the body diode, delaying or even suppressing its turn-ON, especially in high-voltage devices where the n-drift region resistance is dominant [7], [8].

Based on the understanding of the device third-quadrant characteristics, the surge current capability is investigated in some studies. It finds out that the surge current capability of planar MOSFETs is almost the same under different V_{gs} during a 10 ms surge event [9], [10], [11]. For double trench gate SiC MOSFETs, the surge current capability is weaker at higher V_{gs} due to the heat accumulation at the MOS-channel region [12], [13]. Besides, the surge current capability of devices with different voltage class is evaluated, and it is pointed out that the third-quadrant surge current capability of the low-voltage class SiC MOSFETs under positive V_{gs} can be enhanced by the conduction of the body diode [7], [8].

These studies provide important insights into the third-quadrant *I-V* characteristics and surge current capability of SiC MOSFETs. However, most of them treat the MOS-channel

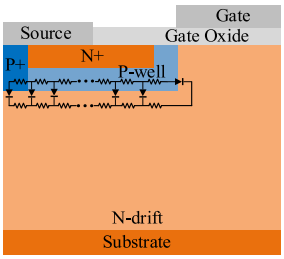

Fig. 1. Typical cell structure of planar-gate SiC MOSFETs.

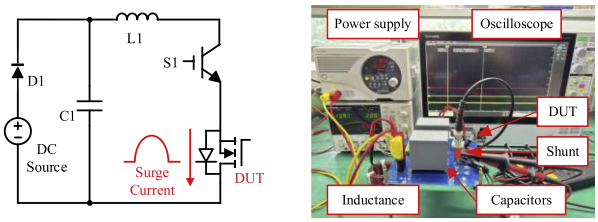

Fig. 2. (a) Schematic of the surge current test circuit. (b) Hardware prototype.

and the body diode as independent current paths. Actually, the body diode behaves more like a parallel array of diodes, as shown in Fig. 1. There is a coupling conduction between the MOS-channel and the equivalent diodes, which has not been fully investigated yet. Besides, existing studies mainly focus on the millisecond-level surges. The variations in junction temperature (T_j) strongly depend on the pulse width, and the coupling conduction between the MOS-channel and the equivalent diodes changes with T_j. These lead to differences in surge current capability across different time scales.

This letter, therefore, investigates the physical mechanism of the coupling conduction between the MOS-channel and the body diode in the third quadrant, and analyzes its influence on the third-quadrant surge current capability of planar MOSFETs. First, the third-quadrant surge current capability of planar MOSFETs under different V_{gs} is evaluated over a wide range of time scales. Then, theoretical analysis and TCAD simulations are conducted to reveal the physical mechanism. Finally, the findings are supported by experimental results.

II. Surge Current Capability of SiC MOSFETs Under Different Gate Bias

A test platform is built to conduct the third-quadrant surge current test of planar MOSFETs. The schematic of the test circuit is shown in Fig. 2(a), and the hardware prototype is shown in Fig. 2(b). A half-wave sinusoidal current is obtained based on *LC* resonance. The pulse width of the surge current (t_{surge}) varies from 25 μs to 10 ms. The devices under test (DUTs) are the planar MOSFETs from Wolfspeed (C3M0160120D). The surge current capability of the device is evaluated under different positive V_{gs}, different negative V_{gs}, and zero V_{gs} (0 V). To obtain the maximum surge current that the device can withstand

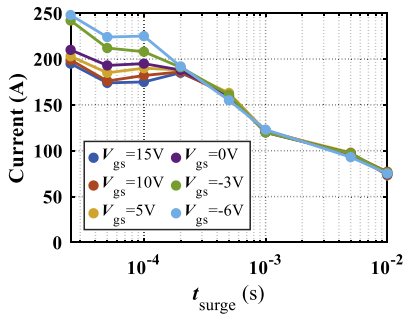

Fig. 3. Comparison of the $I_{surge,max}$ under different V_{gs}.

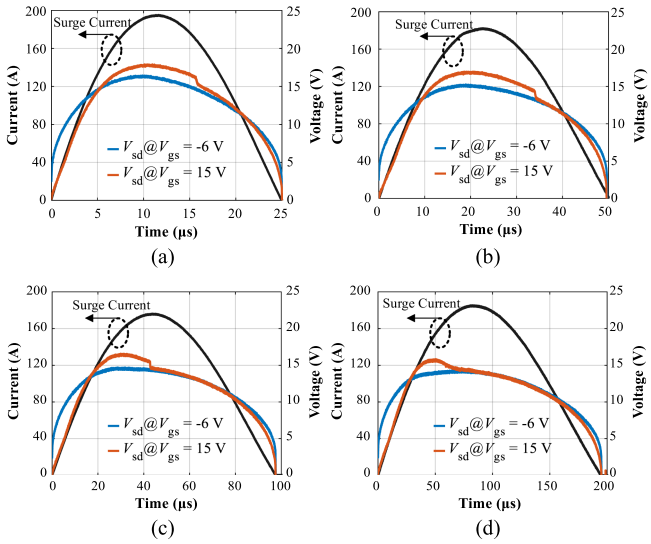

Fig. 4. V_{sd} of devices under different V_{gs} during surge current process at 25 °C. (a) t_{surge} = 25 μs. (b) t_{surge} = 50 μs. (c) t_{surge} = 100 μs. (d) t_{surge} = 200 μs.

($I_{surge,max}$) at a specific t_{surge}, the amplitude of the applied surge current is increased gradually, and the test is terminated if there is a significant drift in device static parameters. For each condition, five samples are tested, and the average failure current is taken as $I_{surge,max}$.

The $I_{surge,max}$ of devices under different V_{gs} is shown in Fig. 3. The $I_{surge,max}$ of devices is decreasing with t_{surge}. In addition, it can be observed that, when t_{surge} is shorter than 200 μs, the $I_{surge,max}$ of the device is decreasing with the increase of V_{gs}. When t_{surge} is greater than 200 μs, there is no significant difference in the $I_{surge,max}$ of devices under different V_{gs}.

Take the surge-current waveforms at 15 V V_{gs} and −6 V V_{gs} as examples. Fig. 4 shows the source-drain voltage (V_{sd}) of the device during surges under different V_{gs}. When t_{surge} is shorter than 200 μs, the device fails under the same current when V_{gs} is 15 V. The failure mode is a short circuit between the gate and source, and a drop appears in the V_{sd} waveform. Normally, it is expected that the equivalent source-drain resistance (R_{sd}) would be reduced when the body diode and the MOS-channel are turned ON simultaneously. However, Fig. 4 shows that the

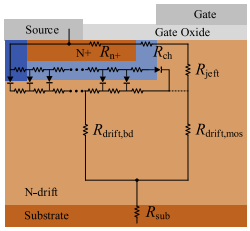

Fig. 5. Reverse conduction paths of planar-gate SiC MOSFETs.

peak V_{sd} during surge is higher under 15 V V_{gs} than under -6 V V_{gs} at the same current level. Under the same current, a higher V_{sd} results in larger power dissipation during surges, making the device more prone to breakdown. As t_{surge} increases, the V_{sd} under different V_{gs} begin to converge.

III. Coupling Conduction Mechanism

A. Theoretical Analysis on the Coupling Conduction Mechanism

The test results show that the surge current capability of the device under positive V_{gs} can be weaker than that under negative V_{gs}. This phenomenon originates from the coupling conduction mechanism between the MOS-channel and the body diode.

The conduction resistance of the MOS-channel path can be expressed as follows:

$$R_{mos} = R_{n+} + R_{ch} + R_{jfet} + R_{drift,mos} + R_{sub} \quad (1)$$

where R_{n+} is the equivalent resistance of the N+ region; R_{ch} is the equivalent MOS-channel resistance; R_{jfet} is the equivalent resistance of the JFET region; $R_{drift,mos}$ is the equivalent n-drift region resistance along the MOS-channel path, which features unipolar characteristics; R_{sub} is the equivalent substrate resistance. When the MOS-channel is turned ON, the MOS-channel current causes a voltage drop across R_{n+}, R_{ch}, and R_{jfet}. The body diode is turned ON when this voltage drop exceeds the built-in potential of the p-n junction. For the body diode path, the conduction voltage can be expressed as follows:

$$V_{bd} = V_{knee} + I\left(R_{drift,bd+}R_{sub}\right). \quad (2)$$

V_{knee} is the built-in potential of the body diode. $R_{drift,bd}$ represents the n-drift region resistance of the body-diode path, which features bipolar characteristics.

The n-drift region resistance is inversely related to the conductivity of the n-drift region and the current spreading area. The conductivities of the unipolar and bipolar paths can be expressed as follows [14]:

$$\sigma_{bipolar} = nq\,\mu_n + pq\mu_n \quad (3)$$

$$\sigma_{unipolar} = nq\,\mu_n \quad (4)$$

where n is the electron concentration, p is the hole concentration, μ_n is the mobility of the electron, μ_p is the mobility of the hole, q is the elementary charge. According to (3) and (4), during bipolar conduction, the conductivity of the n-drift region is larger than that in the unipolar conduction case.

When the MOS-channel is fully turned OFF, the current in the n-drift region is entirely composed of bipolar current. In this case, the conductivity of the n-drift region features bipolar characteristics. The high conductivity of the bipolar path results in a relatively low conduction voltage drop across the n-drift region. Moreover, as the current increases, more minority carriers are injected into the n-drift region, triggering the conductivity modulation effect and further enhancing the device's conduction capability.

When the MOS-channel is turned ON, the current in the n-drift region consists of the unipolar MOS-channel current and the bipolar body diode current. In this case, the conductivity of part of the n-drift region exhibits unipolar characteristics. According to (3) and (4), compared to the case where only the body diode conducts, the overall conductivity of the n-drift region decreases. Meanwhile, the potential around the p-well region is affected by the MOS-channel current, which in turn influences the conduction state of the equivalent diodes along the p-n junction interface. The equivalent result is that part of the equivalent diodes cannot turn ON, resulting in a reduced effective diffusion area of the body diode. The decreased bipolar current further lowers the minority-carrier concentration in the n-drift region, thereby weakening the conductivity-modulation effect. Consequently, when the MOS-channel is turned ON, the device exhibits lower conduction capability at high currents compared to the case where only the body diode conducts.

Considering the influence of temperature, the V_{knee} of the body diode decreases with the increase of temperature. For the MOS-channel path, its equivalent resistance gradually increases as the temperature rises. Thus, the current flowing through the MOS-channel path decreases with temperature. The equivalent effect is that more equivalent diodes can be turned ON at higher temperature, and the diffusion area of the body diode current expands. At the same time, the elevated temperature enhances carrier thermal generation, increasing the minority carrier concentration in the n-drift region and strengthening the conductivity modulation effect of the body diode. Thus, the reverse conduction is increasingly dominated by the body diode at high temperatures, and the coupling conduction between the MOS-channel and the body diode is significantly reduced.

B. TCAD Simulation Analysis

A TCAD simulation model of a planar MOSFET is built in Silvaco to further investigate the coupling conduction mechanism. The model is calibrated using the transfer characteristics, first-quadrant output characteristics, third-quadrant output characteristics of the DUTs. Based on this model, the static third-quadrant output characteristics of the planar MOSFET under different V_{gs} are simulated.

Fig. 6 shows the potential distribution inside the MOSFET cell under different V_{gs} at 25 °C T_j. When $V_{gs} = -6$ V, the MOS-channel remains OFF, and current flows exclusively through the body diode. The potential decreases from the left to the right, facilitating uniform bipolar conduction across the p-n junction interface. When V_{gs} is 5 V, the MOS-channel is turned ON. This MOS-channel current causes a voltage drop

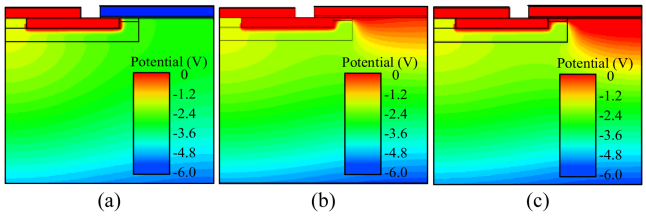

Fig. 6. Potential distribution inside the MOSFET cell under different V_{gs} when $T_j = 25$ °C, $I_{sd} = 200$ A. (a) $V_{gs} = -6$ V. (b) $V_{gs} = 5$ V. (c) $V_{gs} = 15$ V.

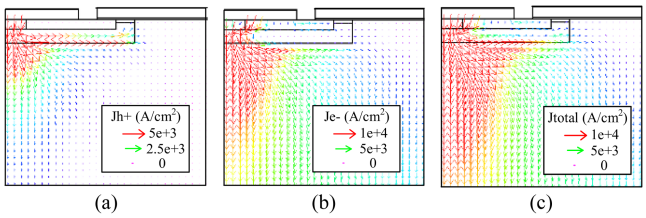

Fig. 7. Current distribution under -6 V V_{gs} when $T_j = 25$ °C, $I_{sd} = 200$ A. (a) Hole current. (b) Electron current. (c) Total current.

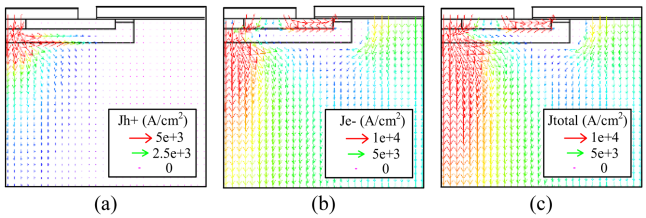

Fig. 8. Current distribution under 15 V V_{gs} when $T_j = 25$ °C, $I_{sd} = 200$ A. (a) Hole current. (b) Electron current. (c) Total current.

across the equivalent resistances of the JFET region and n-drift region, elevating the potential at the right edge of the p-well region. This localized potential rise begins to influence the body diode's forward bias, partially preventing its activation. When $V_{gs} = 15$ V, the MOS-channel is fully turned ON, and the current flowing through the MOS-channel path increases. The resultant voltage drop causes a more pronounced potential elevation near the p-well region, creating a significant potential difference along the p-n junction interface. The equivalent result is that the diffusion area of the body diode is further reduced.

The current distribution inside the MOSFET cell under different V_{gs} conditions is shown in Figs. 7 and 8, respectively. Under -6 V V_{gs}, the body diode conducts, and both hole and electron currents spread laterally along the p-n junction interface into the n-drift region. As shown in Fig. 7(a), the hole current spreads almost to the sidewall of the p-well, while the electron current extends to the rightmost region of the n-drift, as shown in Fig. 7(b). In this case, the conductivity of the whole n-drift region features bipolar characteristics. Besides, under high current conditions, the conductivity modulation can be activated due to the injection of minority carriers, which further reduces the equivalent third quadrant resistance.

When $V_{gs} = 15$ V, however, the body diode diffusion is restricted by the elevated potential induced by MOS-channel conduction. As shown in Figs. 8(a) and (b), the spread lengths

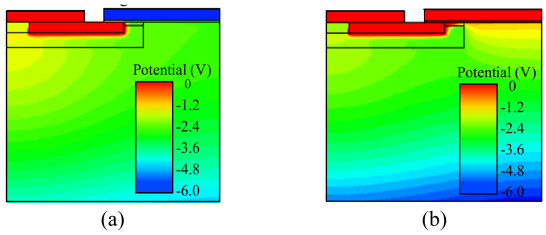

Fig. 9. Potential distribution inside the MOSFET cell under different V_{gs} when $T_j = 175$ °C, $I_{sd} = 200$ A. (a) $V_{gs} = -6$ V. (b) $V_{gs} = 15$ V.

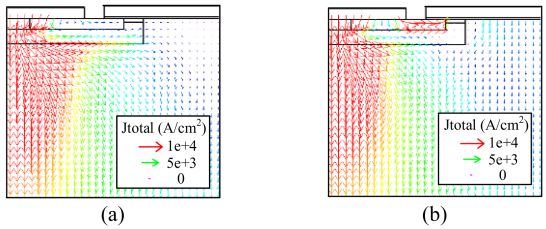

Fig. 10. Current distribution when $T_j = 175$ °C, $I_{sd} = 200$ A. (a) Total current under -6 V V_{gs}. (b) Total current under 15 V V_{gs}.

of the body diode's hole and electron current are significantly shortened. The equivalent result is that the effective conduction area of the body diode current is reduced, as shown in Fig. 8(c). A portion of the conduction path is occupied by the MOS-channel, reducing the contribution of bipolar carriers in the n-drift region and thereby weakening the conductivity modulation effect. As a result, the device exhibits a larger equivalent resistance under high current conditions in the third quadrant.

Fig. 9 shows the potential distribution at a higher T_j. At 175 °C T_j, when V_{gs} is 15 V, the potential in JFET region drops due to the reduced MOS-channel current, as shown in Fig. 9(b). The potential distribution at the p-n junction interface of the body diode tends to converge under different V_{gs}. The equivalent result is that the diffusion area of the body diode current under different V_{gs} tends to become consistent, as shown in Fig. 10. Therefore, at high temperatures, the body diode conduction becomes dominant, and the third-quadrant equivalent resistance under different V_{gs} conditions becomes nearly identical.

C. Discussion on the Surge Current Capability

Based on the aforementioned analysis, the coupling conduction between the MOS-channel and the body diode becomes weaker at higher temperatures. During the surge current process, T_j strongly depends on the pulse width, and T_j gradually increases as t_{surge} becomes longer.

Under short-pulse conditions, the coupling conduction between the MOS-channel and the body diode leads to a larger third-quadrant equivalent resistance when the MOS-channel is conducting. Consequently, the peak power dissipation during the surge event increases with V_{gs}, resulting in a weaker surge current capability under higher V_{gs}.

As t_{surge} increases, T_j is increasing, and the coupling conduction is weakened. The third-quadrant conduction characteristics

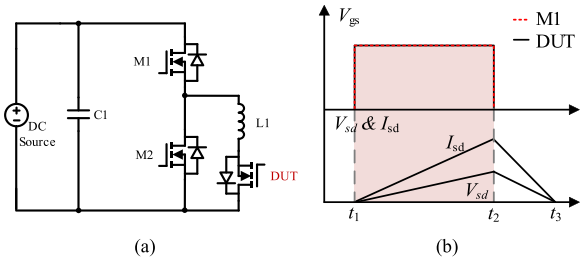

Fig. 11. (a) Test circuit of the third quadrant conduction characteristics. (b) Typical waveforms.

under different V_{gs} become nearly identical at elevated T_j. This convergence leads to similar surge current capabilities under different V_{gs} as t_{surge} increases.

IV. Experimental Verification of the Coupling Conduction Mechanism

To further verify the coupling conduction between the MOS-channel and the body diode, the third quadrant *I-V* characteristics of the device is tested under different V_{gs} and T_j. A test platform is built based on the double pulse test circuit, which is shown in Fig. 11(a). The DUT is in series connected with the load inductance $L1$. The typical voltage/current waveforms and the gate signal of the devices during the measurement process is presented in Fig. 11(b). At time t_1, M1 is turned ON, and the current flows through the DUT. M1 is turned OFF at time t_2 when the current rises to the desired value. During the current rising time, V_{sd} and I_{sd} of DUT are measured by high bandwidth voltage probe and current shunt, respectively.

Self-heating-induced deviations are evaluated by comparing *I-V* characteristics under different t_p (the time interval between t_1 and t_2). No noticeable shift is observed when $t_p < 8$ μs, indicating minimal T_j rise during conduction. Based on this, t_p are fixed at 5 μs for subsequent measurements. T_j is set to 25 °C or 175 °C.

A comparison of the third-quadrant *I-V* characteristics under different V_{gs} is performed at the same T_j, which is shown in Fig. 12. A crossover appears in the *I-V* curves at 25 °C under different V_{gs}; R_{sd} increases with V_{gs} at the right side of the crossover point. As T_j increases to 175 °C, $R_{sd,p}$ is smaller than $R_{sd,n}$ in the low-current region. With a further increase in current, the output characteristics under different V_{gs} conditions nearly coincide.

To illustrate the coupling conduction between the MOS-channel and the body diode, the device's reverse output characteristics at a V_{gs} of 15 V and a T_j of 25 °C are used as an example, which can be divided into the following distinct stages.

Stage I: V_{sd} is lower than the forward voltage of the body diode (V_f). As a result, the body diode remains OFF, and the MOS-channel serves as the sole conduction path. $R_{sd,p}$ is significantly smaller than $R_{sd,n}$ in this stage.

Stage II: In this stage, V_{sd} exceeds V_f as the current increases, and the current begins to conduct through the MOS-channel and the body diode simultaneously. The proportion of current flowing through the body diode region remains increasing in this

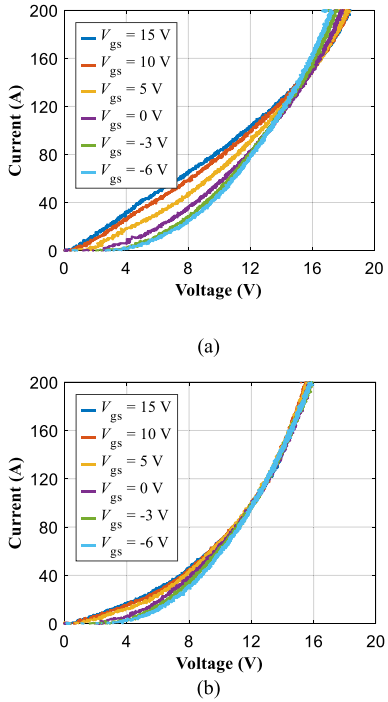

Fig. 12. Comparison of the third quadrant *I-V* characteristics of SiC MOSFETs under different gate bias. (a) $T_j = 25$ °C. (b) $T_j = 175$ °C.

stage, which is due to the bipolar characteristics and the conductivity modulation effects. $R_{sd,p}$ remains significantly lower than $R_{sd,n}$. However, it can be observed that as the current increases, the difference between $R_{sd,p}$ and $R_{sd,n}$ are gradually decreasing. This indicates that the coupling conduction between the MOS-channel and the body diode conduction is enhanced.

Stage III: The third stage begins at the crossover point of the *I-V* curves under different V_{gs}. The MOS-channel shows significant suppression of the conduction of body diode. This weaker body diode results in a higher R_{sd} under 15 V V_{gs}.

When T_j reaches 175 °C, the third-quadrant *I-V* curves of the device under different V_{gs} converge as the current increases. This indicates the coupling conduction is weakened at high temperatures. The experimental results are consistent with the simulation analysis results.

V. Conclusion

This letter investigates the coupling conduction mechanism between MOS-channel and body diode of SiC MOSFETs, and its influence on surge current capability is analyzed. It is revealed that the MOS-channel suppresses the body diode conduction under positive V_{gs}, resulting in reduced surge current capability at specific pulse width and case temperatures. The underlying mechanism is the elevated potential around the p-well region when the MOS-channel is turned ON, which decreases the effective conduction area of the body diode.

Besides, since the coupling conduction mechanism is derived from the device structure and underlying physical principles, it is universal and credible for planar MOSFETs. For different

planar MOSFETs, variations in MOSFET cell dimensions and doping concentrations can lead to differences in the conduction characteristics of the MOS-channel and the body diode, as well as in their coupling conduction degree. Therefore, in different planar MOSFETs, the coupling conduction may exert a varying degree of influence on the surge current capability.

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