High-Fidelity Device Modeling of SiC MOSFETs for Active Gate Drive Optimization

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***Abstract*—Active gate driving enables the shaping of switching waveforms in power devices, helping to mitigate overshoot and ringing. With the advent of smart, open-loop, programmable gate drivers, selecting gate control parameters is challenging, and testing these in hardware is time-consuming and potentially risky. This article proposes a faster, safer simulation-based method for optimizing gate current profiles, requiring high-fidelity device models. A commercial model is modified using measured device properties, specifically input capacitance, recovery charge, and high-voltage transfer behavior, whilst experimental switching waveforms are reserved exclusively for validation, not model tuning. Gate profile optimization begins with a measured gate current waveform, then modulates the current within a limited time window in simulation. Profiles are evaluated for overshoot, ringing, and switching loss. The most promising are validated experimentally using a 1200 V, 17 A SiC MOSFET in an 800 V, 10 A half-bridge with a custom single-chip active gate driver capable of synthesizing arbitrary current waveforms. To further assess robustness, power loop inductance is varied. The modified model shows good agreement with measurements, and the optimized gate profiles suppress 180 MHz turn-ON current ringing by 7 dB and reduce turn-OFF voltage overshoot by 20%, without increasing switching losses. This work demonstrates computationally efficient gate profile optimization, with strong potential for application in smart gate drivers.**

***Index Terms*—Active gate driver, current source, modeling, oscillation, overshoot, silicon carbide (SiC) MOSFET.**

I. Introduction

THE fast switching of silicon carbide (SiC) devices causes unwanted switching features, such as overshoot and ringing. Active gate driving has been shown, in some instances, to provide beneficial shaping of switching waveforms [1], [2], [3], [4], [5], [6], [7], by reducing these features without incurring additional switching loss. Several active gate driving concepts for SiC MOSFETs have been reported: These dynamically alter the gate driver's output resistance [2], [3], voltage [5], [6], or current [4], [7] during the switching transient. This provides control over the charging current of the MOS gate capacitance and thereby influences the device's switching trajectory. An important aspect of active gate driving is the design of suitable gate profiles, within the degrees of freedom and capability of the physical gate driver. For example, a 6-bit programmable digital driver with four time segments [8], results in over 17 M (64^4) possible combinations. Therefore, there is a trade-off between driver flexibility and ease of finding suitable driving parameters, and the driver hardware should be known prior to searching for gate driving parameters or driver output voltage or current profiles via simulation. The task of designing gate profiles would appear to be well suited to genetic search algorithms or machine learning. In [9], a simulated annealing algorithm is used in conjunction with over 2000 switching measurements to determine optimal gate profiles. A real-time hardware platform in [10] integrates online measurements with a particle swarm optimization algorithm to accelerate the search. In [11], a recurrent neural network is trained using MATLAB-based modeling, with predictions validated in LTspice. A simulation-based framework in [12] leverages the genetic algorithm NSGA-II to evaluate gate profiles under multiple objectives. These studies highlight the effectiveness of optimization-based strategies; however, their success depends on the underlying device model's ability to produce accurate waveforms, particularly at the device gate.

The study focuses on the Wolfspeed C3M0160120J device because it was the device used in our experimental test facility, and, therefore, the corresponding SPICE model served as the starting point for refinement. However, our methodology is not aimed at criticizing a specific vendor model, but at demonstrating a measurement-based refinement workflow that can be applied generically to SiC device models, should these need refinement. The workflow highlights the importance of model accuracy in key areas and provides a systematic means to identify whether refinement is needed, and if so, how to improve accuracy.

The rest of this article is organized as follows. Section II presents the optimization of gate current profiles via a comparatively simple, simulated windowed amplitude sweep method. The method incurs low computational and hardware overhead, and additionally serves as a benchmarking tool to assess the fidelity of device model improvements. Section III shows the limitations of the device manufacturer's LTspice model in terms of accurately resolving gate waveforms. The section presents

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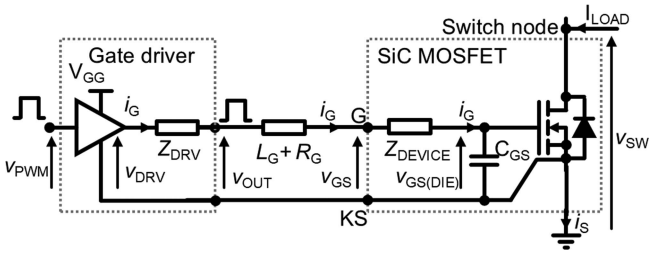

Fig. 1. Equivalent gate-loop circuit including both gate driver and SiC device, with measured gate voltage and gate current profiles at different points along the path.

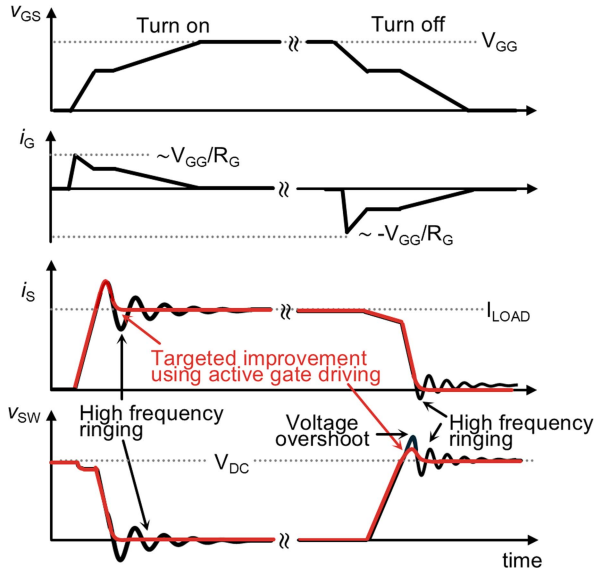

Fig. 2. Conceptual switching waveforms of the circuit in Fig. 1, for current flowing into the switch node. Single-step driving (black), and target waveforms using active gate driving (red).

how to overcome these limitations by adjusting the commercial model, and the use of practical measurement methods to obtain all required adjustment parameters. Section IV presents the experimental test facility used to validate the profile search method. This includes detail on a custom gate driver chip, first reported in [14], that is deployed in an 800 V, 10 A SiC bridge leg with 1200 V, 160 mΩ SiC MOSFETs. A duplicate test board with an identical power-loop layout and comparable gate-loop structure, but using a commercial off-the-shelf single-step driver, is used for benchmarking. This section also provides experimental validation and detailed analysis of the dynamic accuracy of the modified LTspice model of Section III.

Section V shows experimental results for the most promising subset of the set of gate profiles that were created during the optimization process. These demonstrate the simultaneous reduction in ringing and overshoot whilst maintaining the same switching loss, showing that a degree of freedom remains to potentially find further system gains. Finally, Section VI concludes this article.

II. Gate Current Profile Optimization

A. Use of Gate Current Rather Than Voltage Profiles

This study focuses on gate *current* rather than *voltage* profiles, primarily because gate current provides a more reliable indication of gate charging and discharging. In fast-switching SiC and GaN power electronics, gate voltage measurements vary significantly, due to parasitic impedances, from the driver output (V_{OUT} in Fig. 1) to the device terminal (V_{GS}) and ultimately to the die ($V_{GS(DIE)}$). In contrast, the gate current remains approximately uniform along this path.

This should not be taken to imply that the approach is limited to current source gate drivers. Rather, it develops gate current profile optimization methods that are driver-agnostic and do not require simulation models of the gate driver, its output impedances, or its power supply. An advantage of using gate current instead of gate voltage as the input to the model in this work is that the gate profile optimization method is independent of gate-loop inductance. A limitation of the method is that, once suitable current profiles are identified, a real (voltage-sourced) gate driver with too much source impedance may not be able to output this profile. In this case, either slewing should be added to the simulation, or the hardware could be redesigned with lower parasitic inductance. For smart drivers without discrete gate resistors, whose output stages consist of pull-up and pull-down transistors, this is likely to be achievable, since during much of the switching transient, these transistors operate in saturation and effectively behave as voltage-controlled current sources [9], [15].

B. Switching Waveforms to be Improved

Most gate drivers function as buffer circuits, or transimpedance amplifiers, characterized by high input impedance and the ability to drive high transient currents into low-impedance loads, namely, the gate capacitance. A driver typically transitions its output voltage from the OFF to the ON level in a single step as illustrated in Fig. 2. In this article we refer to this as a "1-step driver." This term is used to distinguish it from an "active gate driver," which transitions over multiple steps or follows more complex gate voltage or current profiles.

The single step in gate voltage initiates switching, and the resulting switching waveforms are a function of the bridge-leg's DC rail voltage, load current, power circuit parasitic impedances, temperature-dependent device characteristics, and gate network impedances. As a result, the switching transients contain unwanted features as illustrated by the black traces in Fig. 2. These include oscillations and overshoots, which are primarily driven by high *dv/dt* and *di/dt* experienced during turn-ON and turn-OFF transitions [13].

The red traces represent the desired power loop waveforms, shaped by gate signals derived in this work. These waveforms exhibit reduced current and voltage oscillations to lower EMI, and decreased voltage overshoot at turn-OFF to increase the voltage safety margin of the power devices. These improvements are achieved not by increasing the gate resistor, which would increase switching loss, but by actively shaping the gate signal.

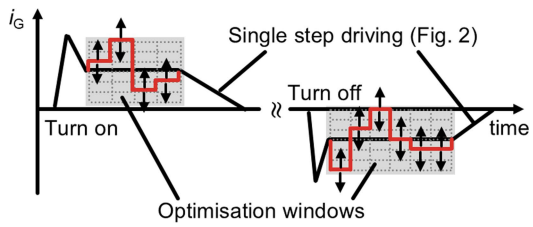

Fig. 3. Conceptual gate current waveforms for single-step driving being optimized within a designated time-window.

C. Windowed Optimization of Gate Current Profiles

An important aim of the gate current profile optimization method presented here is to identify signals of relatively low complexity, to facilitate practical implementation in hardware. To this end, the gate current profile of a 1-step driver, such as that shown in Fig. 2, is used as a reference, around which a windowed optimization is performed, as illustrated in Fig. 3. The window covers the Miller plateau interval, where relatively small changes to the gate current are known to affect hard-switched waveforms. For example, it has been shown in [22] that controlling the drain-source voltage slew rate dv_{DS}/dt toward the end of the voltage fall time (and consequently toward the end of the Miller plateau) plays a crucial role in eliminating ringing in the drain current at turn-ON. For other devices and applications, inspection of the waveforms should indicate if this window should be nudged forward or back in time to better encompass the period when the gate is able to correct specific features in the power waveforms. For example, by extending the profile search window to include the di/dt period prior to the Miller plateau should allow the current overshoot to be targeted. Kawai et al. [7] demonstrated that during the voltage-rise period at turn-OFF, appropriate adjustment of the gate current reduces voltage overshoot.

Each optimization window is divided into multiple segments, within which the gate current amplitude is varied to shape the switching waveform. The objective is to identify the gate current profile that best approximates the desired red traces shown in Fig. 2. Specifically, the optimization framework evaluates the trade-off between EMI and switching loss by comparing simulated waveforms within the defined optimization window, using the performance achieved when using the commercial off-the-shelf gate driver as a boundary reference. When using the active driver, operating points below this boundary give better EMI:Loss tradeoff. Switching loss is obtained by integrating the product of switch-node voltage and source current over the switching transient, and EMI performance is assessed by computing the spectral power of the source current within the 100–200 MHz band, which encompasses the dominant ringing frequency (186 MHz) observed in measurements.

Candidate waveforms are, therefore, evaluated on a two-axis basis (switching loss versus spectral power). The "optimal" profiles are defined as those that simultaneously reduce spectral power while maintaining switching loss at or below the level of the reference single-step driver. The "optimal" profile may depend on application, where there may be hard limits on the acceptable level of EMI and/or switching loss. In this case, we define the profiles that lie furthest from the step-driver boundary as the "most promising." The optimization is carried out virtually, to avoid damaging the circuit. The transitions between hardware and simulation are illustrated in Fig. 4.

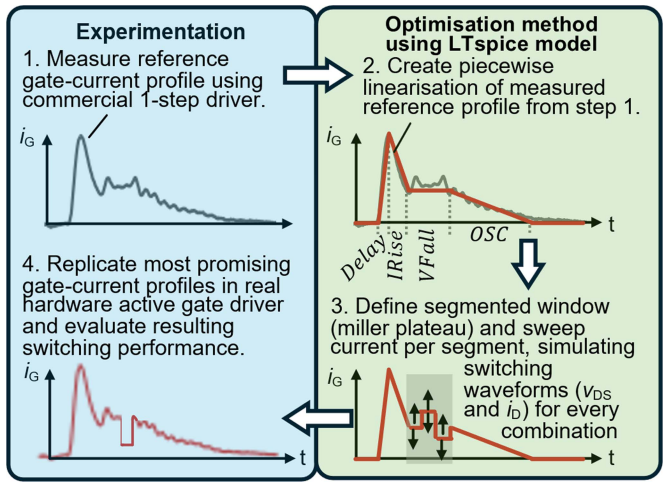

Fig. 4. Proposed 4-stage optimization process with measurement of a reference gate profile, parameter sweeps in simulation, and subsequent validation in hardware. Turn-ON waveforms are shown here; a similar procedure is used for turn-OFF.

In Stage 1, power waveforms exhibiting undesired behavior are measured, along with the gate current profile of a 1-step driver to serve as the reference for Stage 2. Here, the reference is approximated using four linear segments corresponding to turn-ON delay, current rise (IRise), voltage fall (VFall), and postswitching oscillation OSC [16], to reduce simulation time. In Stage 3, the optimization window is defined, with segments in which the current amplitude is independently varied. The segmentation is aligned with the capabilities of a specific gate driver to ensure the profile can be implemented. In principle, the optimization could instead use a finer segmentation, followed by filtering to retain only those profiles compatible with the hardware. The resulting switching waveforms are evaluated for ringing, overshoot, and switching loss. In Stage 4, the most promising gate profiles are programmed into the gate driver for experimental validation.

III. Measurement-Based Refinement of Commercial Device Model

A. Overview of Changes Made to Device Model

Rather than create a device model from first principles, the aim here is to shorten development time by identifying the minimum modifications required to a manufacturer-supplied model to obtain the accuracy necessary for gate current profile optimization. The model is not tuned or calibrated using experimental switching waveforms, instead, these waveforms are reserved exclusively for validation purposes. The modifications are based on direct measurement of physical properties of the actual device, which are then incorporated into the model structure, as illustrated in Fig. 5. Subsequent sections present

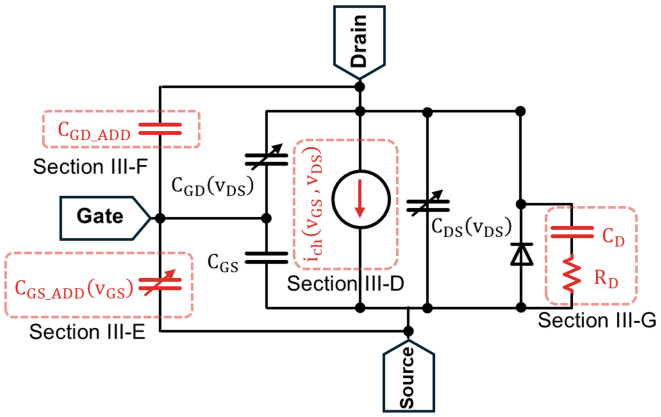

Fig. 5. Manufacturer's SiC MOSFET model, and, in red, modifications made in this work.

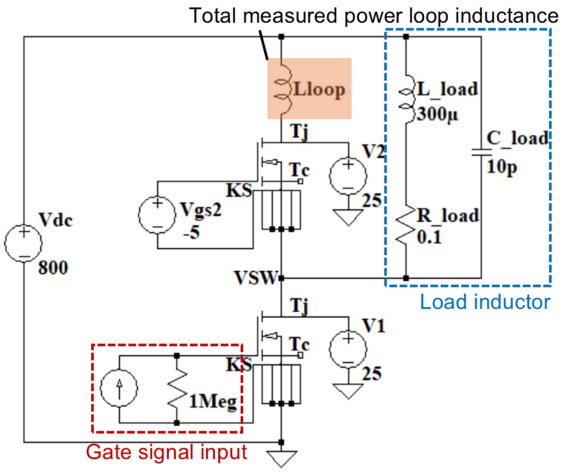

Fig. 6. Circuit simulation model with parasitic impedances.

each modification in turn. The accuracy of the resulting model is experimentally verified in Sections IV-B and IV-C.

The changes made are not unique to the SiC device model being used in this work, the authors have observed similar requirements on models of other SiC devices and modules.

B. Circuit Model and Extraction of Circuit Parasitics

Since the power loop waveforms are highly dependent on circuit parasitics, these are established first. The double-pulse test circuit containing high and low-side SiC MOSFETs that will be used for validation in Section IV is modeled in LTspice as shown in Fig. 6. The lower device is actively driven, and the upper device is held OFF via the gate.

The lower device's gate current is supplied by a programmable gate current source, allowing the input of time-varying gate current profiles. This has two uses: many profiles can be vetted and downselected through simulation, e.g., using the methods introduced in Section II, and an experimentally measured gate current profile can be entered to validate the system model. Using a current source at the node that represents the SiC device's gate terminal eliminates the need for both a gate driver model and accurate model of the gate loop impedances.

The circuit model's power loop inductance L_{loop} combines all layout-dependent parasitic inductances within the power loop formed by the dc-link capacitor, the bridge leg, and the return path to the dc-link. It also includes any intentional inductance that may have been added in the experimental circuit to correctly replicate certain applications, such as designs with busbars or tabs. The datasheet parasitic impedances of the dc film and ceramic capacitors are not used, instead an impedance measurement is carried out using a handheld NanoVNA v2 vector network analyzer, with SMA connectors mounted on a populated board. To avoid double-counting, the loop inductance already included in the device models is subtracted from the measured value, and the remainder is assigned to L_{loop}. The resulting inductance remains distributed relative to the probe points, consistent with the physical circuit.

The parasitic elements of the load inductor's model are derived from the measured self-resonant frequency obtained using a Wayne Kerr 6500B impedance analyser. The SiC MOSFETs are modeled using the C3M0160120J Spice model available in [23], which will be further refined in the following sections.

C. Limitations of Manufacturer's mosfet Model

Fig. 7 compares measured and simulated turn-ON and turn-OFF waveforms, for the unmodified device model.

The physical circuit uses the ADuM4146 10 A gate driver with an 11 Ω gate resistor. The gate current shown in the upper two subfigures is captured using a 500 MHz bandwidth infinity gate sensor [20] and checked against an optically isolated measurement over a current sense resistor. This measured gate current is used as the gate signal in the simulation.

It is apparent that there are significant discrepancies between simulation and experiment. These differences are found to be too significant to allow the proposed simulation-based gate profile optimization, and therefore an improved model is required. The principal discrepancies are summarized in Table I.

Some of the differences observed between the simulated and experimental switching waveforms are expected to correspond to discrepancies in the static input or output characteristics.

D. Requirement for an Output Characteristic in the HighPower Region

The first modification made to the model is to correct the simulated output characteristic $i_D(v_{\text{DS}}, v_{\text{GS}})$, or current-voltage (I-V) characteristic, in the region of high instantaneous power shown in Fig. 8. This figure illustrates that switching trajectories extend beyond steady-state measurable ranges that are provided in datasheets, since device analyzers are power limited.

At turn-ON, the operating point moves from blocking 800 V and conducting zero current, vertically upward to the point (800 V, 12 A) where the self-heating power is over 9 kW. This IV-trajectory was derived from the measured switching waveforms in Fig. 9, which includes time markers t_0 to t_4 corresponding to those in Fig. 8.

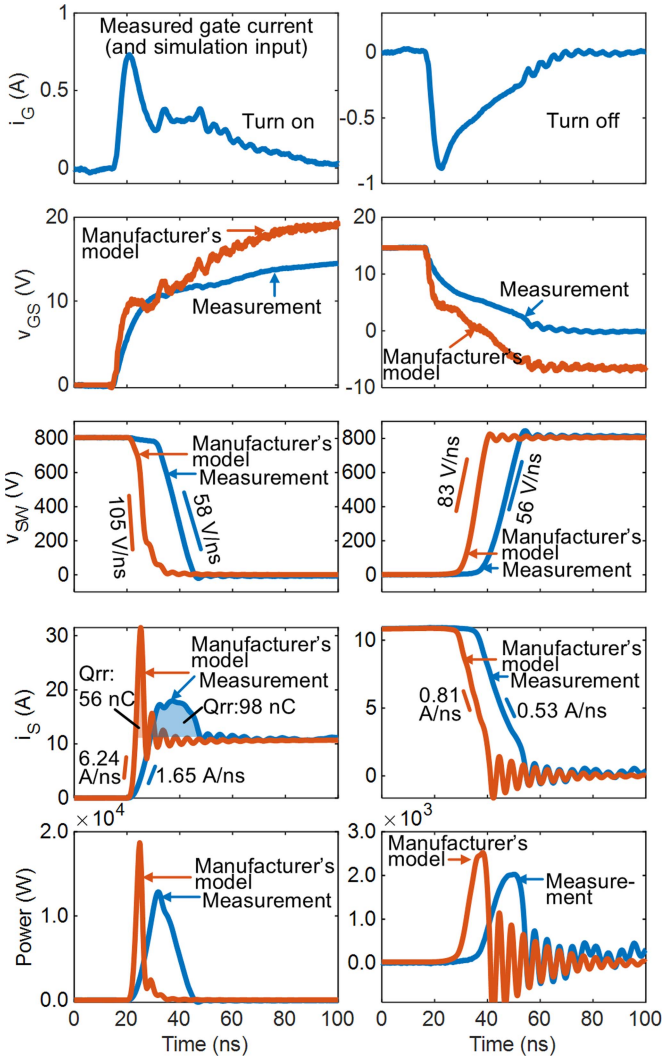

Fig. 7. Measured and simulated turn-ON and turn-OFF switching waveforms, using the manufacturer's original device model.

The device model supplied by the manufacturer reproduces the low-power region of the output characteristic relatively closely, see the detail view in Fig. 10, however in the high-power region, there is no reference for comparison.

E. Output Characteristic From Switching Waveforms

The extraction of I-V characteristic from switching waveforms has been demonstrated in [17], [18], and [19]. This method employs families of double-pulse switching tests, and typically uses portions of the turn-ON trajectory where gate voltage is constant or during the initial phase before significant self-heating occurs. In this work, the entire turn-ON trajectory is utilized, as shown in Fig. 11, with loci of constant gate voltage connected to approximate the I-V characteristic.

The discrepancy between this measured characteristic and that of the model in Fig. 10 is significant. For example, at $V_{GS} = 8$ V and $V_{DS} = 800$ V, the simulated device current I_D is around 100 A, whereas the measured I-V characteristic shows only 12 A.

TABLE I
SUMMARY OF DISCREPANCIES AND POTENTIAL CAUSES

Discrepancies observed	Potential cause
Model's v_{GS} rises above 15 V and drops below 0 V, deviating from the intended gate voltage swing of 0–15 V. Delay between model's gate pulse and switching transients is too small.	Model's gate-source capacitance C_{GS} is too low. See Section III-F.
Model's dv_{SW}/dt is too high.	Model's voltage-dependent gate-drain (Miller) capacitance C_{GD} is too low. See Section III-G.
Model's reverse recovery charge Q_{rr} appears to be too low.	The high-side device model does not have the correct voltage-dependent output capacitance or represent the correct carrier lifetime and density. See Section III-H.
Modeled di_S/dt is too high at turn-ON.	The model's transconductance may be too high, or its current saturation inadequate, possibly due to the channel current's dependency on gate voltage and drain-source voltage being inaccurate. See Section III-D.

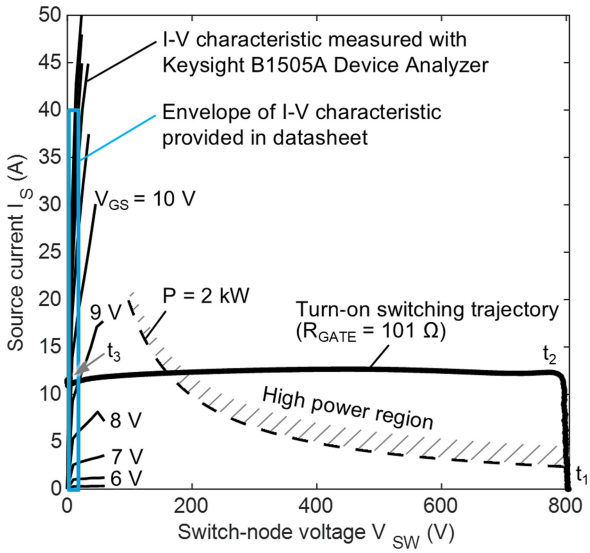

Fig. 8. Comparison of current-voltage (I-V) operating ranges for a C3M0160120J SiC MOSFET: the datasheet-specified region, the measurement envelope of a Keysight B1505A Device Analyzer, and the full I-V span observed during a switching trajectory. The overlay highlights how switching extends beyond the steady-state measurable ranges into the high-power region.

The following section outlines the precautions necessary when using the full switching trajectory, as opposed to partial trajectories used in [17], [18], and [19]. The double pulse tests in this work are performed with a relatively high-value gate resistor of 101 Ω to minimize voltage transients across parasitic inductances that could introduce measurement errors. In modules, such high resistance could cause junction temperature rises of

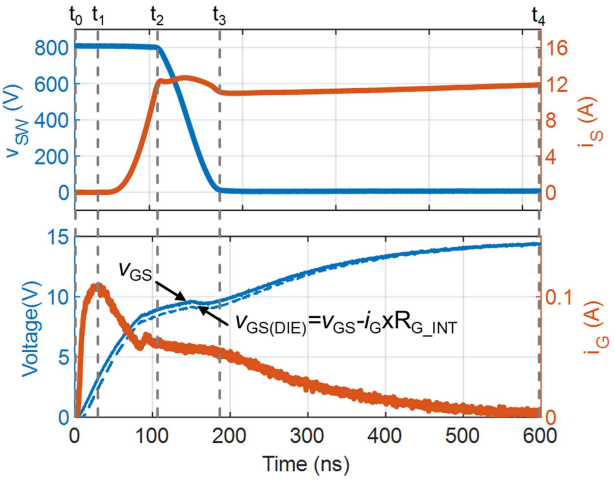

Fig. 9. Measured turn-ON switching waveforms of a C3M0160120J SiC MOSFET. $R_{GATE} = 101\ \Omega$ to minimize difference between die and terminal voltages.

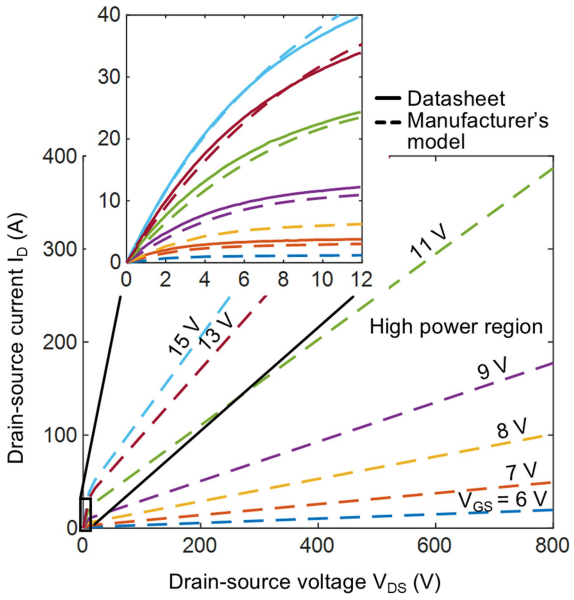

Fig. 10. Simulated (manufacturer-supplied model) and datasheet output characteristics for V_{GS} values from 6 V to 15 V, in both high-power and datasheet regions.

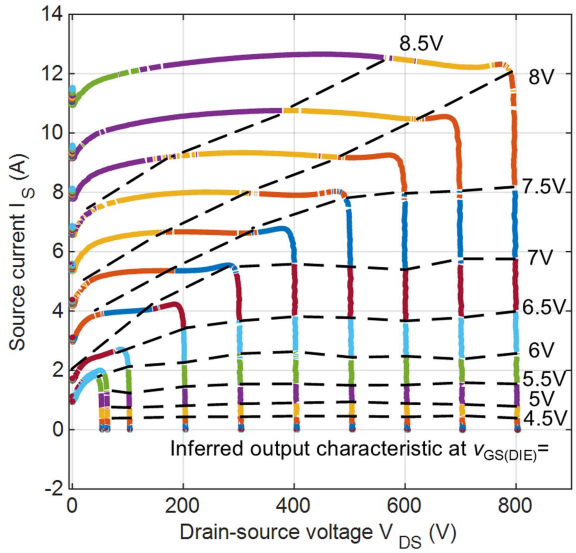

Fig. 11. Turn-ON switching trajectories from a series of 10 double-pulse tests. Dashed lines connect operating points of equal gate voltage, forming an approximate output characteristic that extends into the high-power region of Fig. 8.

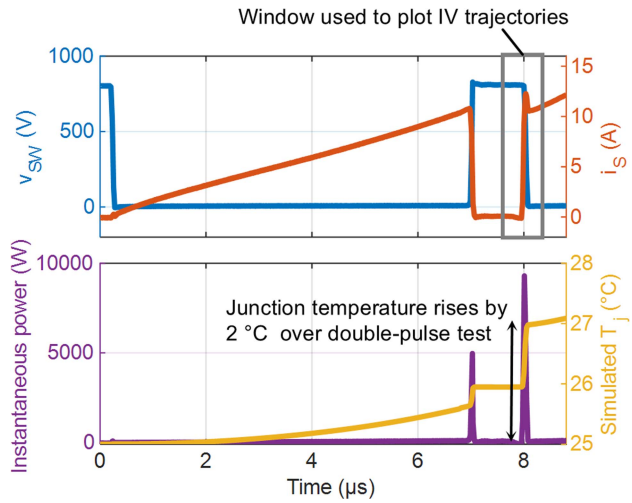

Fig. 12. Top: Measured double-pulse test waveforms for a high gate resistance (101 Ω). Bottom: Instantaneous power loss and junction temperature, derived using device thermal model supplied by the manufacturer.

many tens of degrees, however, in the discrete device used here, the thermal model predicts a rise of only 2 °C over the full test, as shown in Fig. 12, which is considered negligible. The waveforms in this figure correspond to the outermost trajectory in Fig. 11, associated with the highest loss. To permit accurate power calculations, waveforms are deskewed to within ±160 ps.

Unlike the quasistatic device analyzer measurements, the dynamic nature of the test causes voltages to be induced across package-internal parasitic impedances, such as the gate inductance L_{GS_INT} and internal resistance R_{G_INT} in Fig. 13. As a result, the measured terminal voltages differ from the actual voltages at the die that are required for the I-V characteristic. For the device used here, this inductance is 12.4 nH; the maximum rate of change of gate current is approximately 1 mA/ns, resulting in a voltage drop of only 1.2 mV. By contrast, the peak voltage over the internal resistance (8 Ω) is almost 1 V. Therefore, the inductance is neglected, and the gate voltage at the die calculated as follows:

$$v_{GS\_DIE} = v_{GS} - i_G \times R_{G\_INT}.$$

The resulting gate voltage is shown as a dashed line in Fig. 9.

Similarly, the measured switch-node voltage v_{SW} differs from the actual drain-source voltage v_{DS} due to inductive parasitics between the measurement points and the die. For the interval with the highest rate of change in current, i.e., between t_1 and

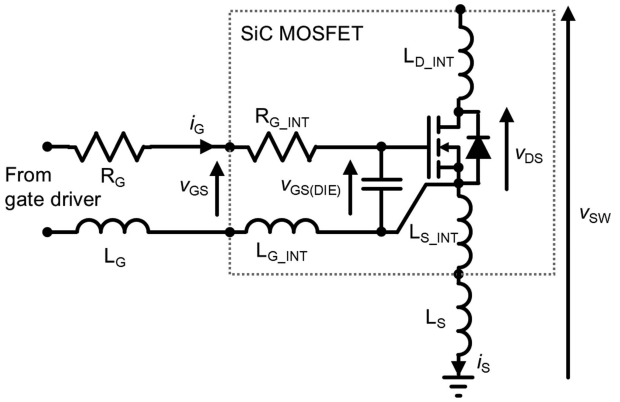

Fig. 13. Equivalent model of the low-side SiC device in the physical bridge-leg including all relevant parasitic elements.

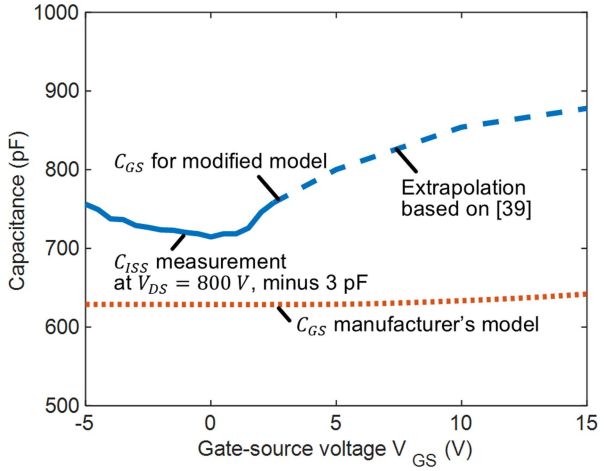

Fig. 14. Gate-source capacitance C_{GS} against gate-source voltage V_{GS}, for the C3M0160120J SiC MOSFET, at a V_{DS} of 800 V. Dotted: manufacturer-supplied model, solid+dashed: measurement with extrapolation, as used in updated model.

t_2, di_S/dt is approximately 200 mA/ns. Assuming a worst-case total inductance $L_S + L_{S\_\mathrm{INT}} + L_{D\_\mathrm{INT}}$ of 5 nH, the resulting voltage drop is only 1 V. Given the 800 V scale, this is considered negligible, and v_{SW} is taken as a valid approximation of v_{DS}.

F. Voltage-Dependent Gate-Source Capacitance

The second modification made to the model involves the gate capacitance C_{GS}. The manufacturer-supplied model assumes a nearly constant gate-source capacitance of 629 pF, independent of gate source voltage V_{GS}, see the dotted C_{GS} plot in Fig. 14. This value corresponds to the datasheet specification for $V_{\mathrm{GS}} = 0$.

The aim is to measure the gate capacitance's dependency on gate voltage and incorporate this into the model, as shown in Fig. 5. The behavior at high drain-source voltage is especially important to capture. Due to the difficulty of isolating the gate-to-source capacitance, instead C_{ISS} $(C_{\mathrm{GS}} + C_{\mathrm{GD}})$ is measured using a 1 MHz excitation frequency, and the very small datasheet value of C_{GD} at $V_{\mathrm{DS}} = 800$ V (3 pF) is assumed to be constant against V_{GS}, such that C_{GS} is given as follows:

$$C_{\mathrm{GS}} = C_{\mathrm{ISS}} - 3\ \mathrm{pF}.$$

However, a complication arises at the high V_{DS} value of 800 V – as V_{GS} approaches the threshold voltage and drain current starts to flow, the static power dissipation in the device is large. In order to avoid damage to the device, it is therefore necessary to limit the V_{GS} excursion to a maximum of 2.5 V, but the characteristic of C_{GS} versus V_{GS} is required up to 15 V. This is resolved by extrapolating the measured values based on the device physics model reported in [39]. The trend of the measurements from $V_{\mathrm{GS}} = -5$ V to $+2.5$ V show good agreement with this model, giving confidence that it is reasonable to make this extrapolation. The resulting dependency of C_{GS} on V_{GS} is significant, as shown in Fig. 14.

Voltage-controlled capacitors have been shown to pose convergence risks [24] in SPICE models. For this reason, the variable capacitance is implemented using a behavioral current source governed by the equation $i\ (t) = C(v)\frac{dv}{dt}$, where $C(v)$ is defined using a voltage-dependent lookup table derived from the measured data [24].

G. Dynamic Gate-Drain Capacitance Modeling

The third model refinement addresses the gate-drain capacitance C_{GD}, which appears to be understated in the waveforms of Fig. 7. This issue is noted and addressed in prior studies, e.g., in [25]. The total gate current $i_G(t)$ charging the input capacitance, comprising the gate-source and gate-drain capacitance, is the time derivative of the total stored charge Q, and therefore

$$i_G\ (t) = \frac{dQ_{\mathrm{Total}}}{dt} = \frac{d}{dt}\left(C_{\mathrm{GS}} v_{\mathrm{GS}} + C_{\mathrm{GD}}\left(v_{\mathrm{GS}} - v_{\mathrm{DS}}\right)\right).$$

Applying the product rule for differentiation, and noting that the capacitances are time-varying,

$$i_G\ (t) = C_{\mathrm{GS}}\frac{dv_{\mathrm{GS}}}{dt} + \frac{dC_{GS}}{dt}v_{\mathrm{GS}} + \quad + C_{\mathrm{GD}}\frac{dv_{\mathrm{GS}}}{dt} + \frac{dC_{\mathrm{GD}}}{dt}v_{\mathrm{GS}} - C_{\mathrm{GD}}\frac{dv_{\mathrm{DS}}}{dt} - \frac{dC_{\mathrm{GD}}}{dt}v_{\mathrm{DS}}.$$

During the Miller plateau, v_{GS} and C_{GS} are approximately constant, nullifying the first three terms. The expression simplifies to

$$i_G\ (t) = \frac{dC_{\mathrm{GD}}}{dt}\left(v_{\mathrm{GS}} - v_{\mathrm{DS}}\right) - C_{\mathrm{GD}}\frac{dv_{\mathrm{DS}}}{dt}.$$

Standard SPICE models account for the second term by referencing the voltage-dependent capacitance $C_{\mathrm{GD}}(v_{\mathrm{DS}})$, typically derived from small-signal measurements. However, they neglect the first term, as the look-up-table or equation based implementation does not track dC_{GD}/dt. In principle, C_{GD} could be modeled as a true voltage-dependent capacitor. This study adds a parallel correction capacitance $C_{\mathrm{GD\_ADD}}$, acknowledging its dependency on switching speed.

The value of the required additional capacitance is derived from the transient measurements shown in Fig. 9. Gate current is integrated over the interval t_2 to t_3 to obtain total gate charge during the Miller plateau (Fig. 15, left).

This gives

$$Q_{\mathrm{GD\_DY}} = 5.1\ \mathrm{nC}$$

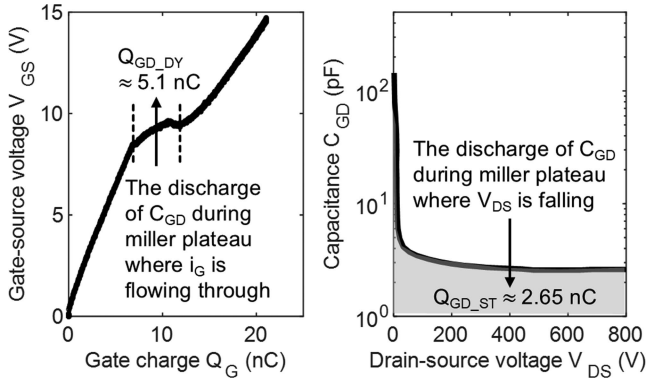

Fig. 15. Left: $V_{GS}(Q_G)$ profile obtained from measured gate waveforms in Fig. 9. The Miller plateau, indicated with the vertical dashed lines, corresponds to the interval t_2 to t_3 shown in Fig. 9. Right: Gate charge extracted through integration of the datasheet's $C_{GD}(V_{DS})$ curve.

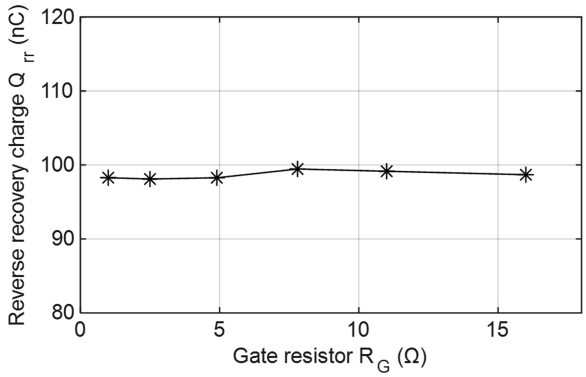

Fig. 16. Measured reverse recovery charge using the ADuM4146 gate driver with different gate resistors.

for the dynamically derived gate charge. In comparison, integrating the statically derived $C_{GD}(v_{DS})$ in the datasheet (Fig. 15, right) yields

$$Q_{GD\_ST} = 2.65\ \text{nC}.$$

This discrepancy indicates an underestimation of the dynamic gate-drain charge. The correction capacitance is thus

$$C_{GD\_ADD} = \frac{Q_{GD\_DY} - Q_{GD\_ST}}{V_{DC}} \approx 3\ \text{pF}.$$

H. Modifications to Reverse Recovery Charge Model

The fourth refinement relates to the reverse recovery charge Q_{RR}, which comprises two components: 1) The capacitive charge displacement: the change in mobile charge as V_{DS} transitions from the rail voltage to 0 V. This is captured by the datasheet's voltage-dependent output capacitance curve. 2) Injected charge: Resulting from current conduction, leading, for example, to minority carrier injection in the body diode of the device, or a copackaged antiparallel diode [30]. Whilst the manufacturer-supplied model appears to replicate the output capacitance, it appears to neglect the injected charge contribution.

The extended charge-control diode model in [26] incorporates time-dependent charge storage and removal processes. However, DeBoi et al. [27] reported that it still yields significant errors in predicted Q_{RR} and switching loss E_{ON}. In this work, the injected charge Q_I is modeled using a parallel capacitance, chosen such that its stored charge at the dc voltage equates to the discrepancy between measured and modeled Q_{RR}. This yields

$$C_D = \frac{Q_{RR,MEAS} - Q_{RR,MODEL}}{V_{DC}} \approx 50\ \text{pF}.$$

Experimental validation (see Fig. 16) confirms that Q_{RR} remains independent of gate resistance, consistent with [28], supporting the use of this parallel correction capacitor C_D.

I. Additional Device Parameters

The model refinements discussed here are found to be sufficient to allow direct transfer of gate-drive profiles from simulation to real-world hardware for the particular SiC devices and test conditions used in this work. With other models of SiC device with other baseline models, or working with the same device in different operating conditions may require additional effects to be modelled. Candidates include threshold voltage hysteresis [36], [37], [38], drain-induced barrier lowering (DIBL) [32], [33], [34], [35], and the temperature dependency of model parameters.

The manufacturer's supplied model does not include threshold-voltage hysteresis or barrier lowering effects, but it does provide temperature dependency. In this work, the devices used have planar gates and are operated with a zero volt OFF-state bias, both of which have been shown in the literature to minimize threshold voltage hysteresis [36]. Devices are operated at room temperature; if the temperature dependency is important in the application, then it should be checked that this dependency still holds true after the modifications. For the modified model in this work, the simulated output characteristic at 150 °C lies within 15% of that provided in the datasheet.

IV. Experimental Verification of Model

A. Hardware Implementation

An experimental SiC converter circuit is operated in double-pulse mode at 800 V and 10 A, to validate both the improved device model (see Section III) and the gate current profile optimization method (see Section II). A simplified schematic is shown in Fig. 17.

The ADuM4146 propagation delay affects the latency between the logic edge and the start of the switching event, but not the processes during the Miller segment where our profile shaping acts. Waveforms are time-aligned to the instant when the gate voltage at the MOSFET pin (v_{GS}) begins to rise (turn-ON) or fall (turn-OFF), removing the impact of driver's fixed latency once the transition begins.

For measurement instrumentation, the low-side gate voltage v_{GS} is measured with a 1 GHz Tektronix IsoVu TIVH08 high

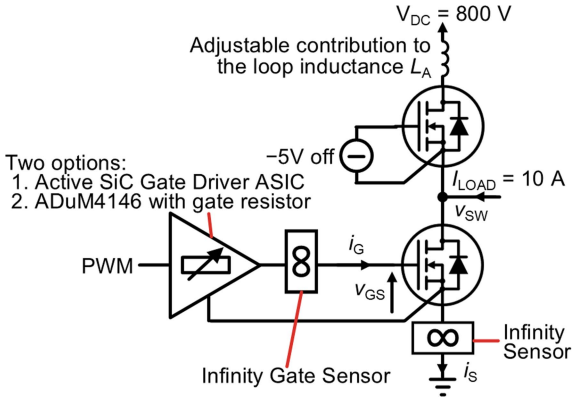

Fig. 17. Circuit schematic of double pulse test, using Bristol University's Infinity Gate Sensor [20], Infinity Sensor [31], and active gate driver chip [14].

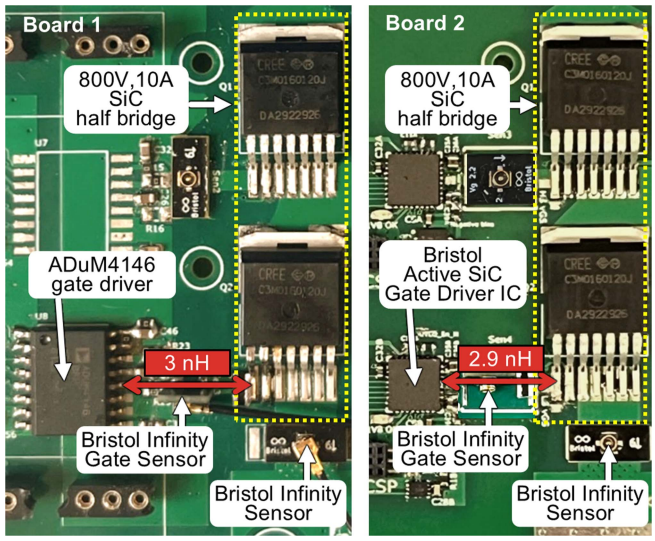

Fig. 18. Close-up of two power boards with identical power-loop: Board 1 (left) with commercial 1-step driver for benchmarking, Board 2 (right) with custom active gate driver IC. The measured gate loop inductances are labeled in red.

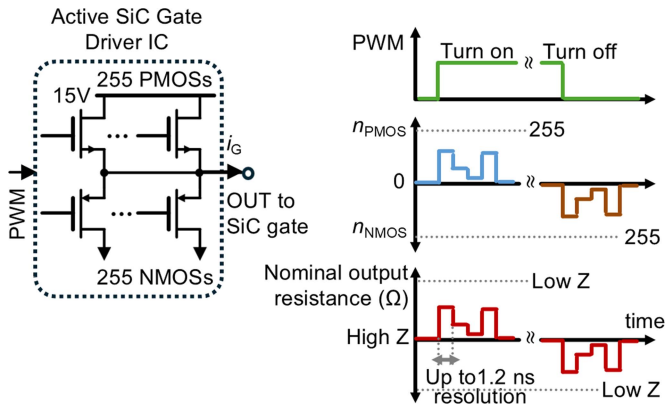

Fig. 19. Concept of the University of Bristol's active SiC gate driver IC [14] architecture and "nominal output resistance."

common-mode rejection differential probe. The switch-node voltage v_{SW} is measured using a PMK HV1000 100:1400 MHz passive voltage probe. The gate current i_G source current i_S is obtained using Infinity Sensors. Measurements are corrected through deskew calibration prior to testing, reducing the relative timing error across channels to within $\pm$160 ps. This ensures that measurement delays do not affect the extracted waveforms or the optimization procedure.

The power loop incorporates an inductor whose value is varied to emulate different converter designs (similar to [29]), ranging from compact layouts with discrete SiC MOSFETs (total loop inductances below 15 nH) to module and busbar configurations (inductances above 20 nH). For all measurements in Sections II and III, the total loop inductance is 12 nH, and later during validation, larger inductances up to 62 nH are used, in combination with high gate resistances up to 33 Ω. These relatively high values produce switching waveforms that are closer to SiC module waveforms by replicating a module's gate resistance and loop inductance per unit of SiC die active area. For example, a 400 A XM3 SiC module with a 2.5 nH busbar inductance can be viewed as comprising approximately 24 parallel 17 A dies (matching our discrete MOSFET), corresponding to about 60 nH per die. Likewise, the 33 Ω gate resistance applied in our experiments is consistent with ∼1.5 Ω per die in a large parallel module configuration. To generate both baseline 1-step driven switching waveforms and actively driven waveforms, two power boards with identical power-loop layouts and comparable gate-loop layouts are used, see Fig. 18. The gate loop inductances are measured using an R&S ZVL Vector Network Analyzer and are 3 nH and 2.9 nH.

Board 2 integrates a custom active gate driver chip, first reported in [14], along with a 500 MHz Bristol Infinity Gate Sensor [20] for measuring the gate current i_G. This SiC driver includes internal memory capable of storing predefined 100-segment arbitrary gate current waveforms. The output stage is implemented using 255 pMOS-nMOS transistor pairs, shown in Fig. 19, that operate in the saturation region for most of the gate voltage transition and thus behave like voltage-controlled current sources. The time resolution is up to 1.2 ns. Postlayout simulations indicate that a single pull-up transistor delivers a steady-state output of 37.1 mA at a chip-internal V_{DS} of 15 V (404 Ω) while a pull-down transistor delivers 77.9 mA (193 Ω). When all 255 transistors are activated; this corresponds to a theoretical maximum gate current of approximately 9.5 A for turn-ON and 19 A during turn-OFF.

In this work, the term "nominal output resistance" is used to represent the instantaneous driver configuration. It is defined as the resistance of a single transistor at a drain-source voltage of 15 V, divided by the number of active pull-up or pull-down transistors. For example, when all transistors are configured to pull down, the nominal output resistance is of 193 Ω / 255 = 0.755 Ω. This value reflects the resistance at the initial instant of turn-OFF. As the switching transition progresses and the driver output voltage decreases, the voltage over the transistors also drops. Consequently, their effective resistance decreases until they enter their linear region, where they exhibit their minimum ON-state resistance [15].

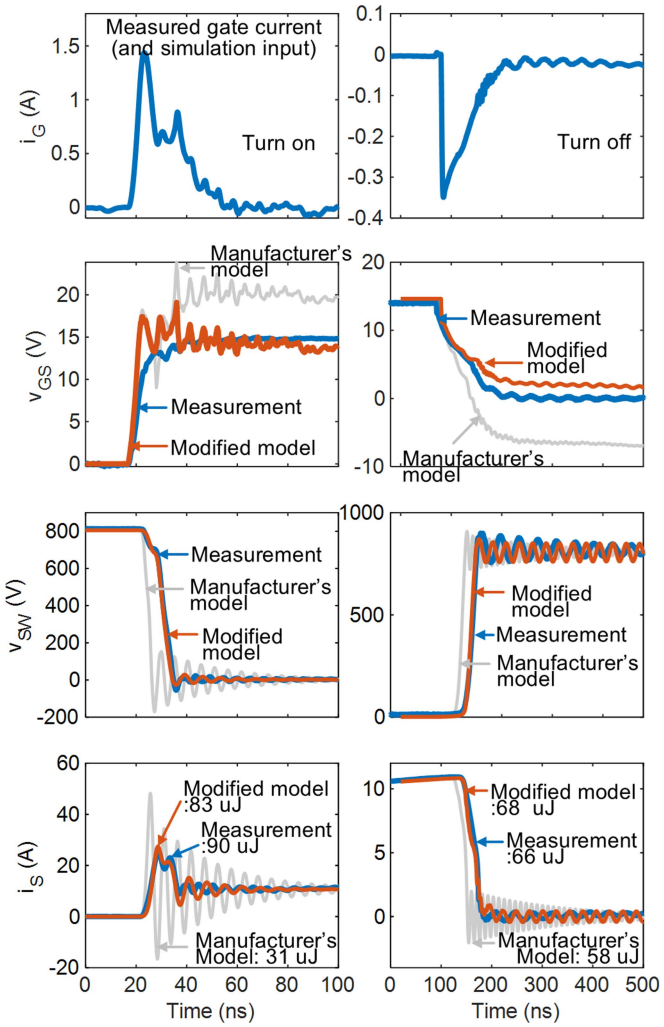

Fig. 20. Measured versus simulated switching waveforms. Left: Turn-ON with 2.5 Ω gate resistor and 17.5 nH total power loop inductance. Right: Turn-OFF with 35 Ω and 62 nH to emulate module with much larger active area.

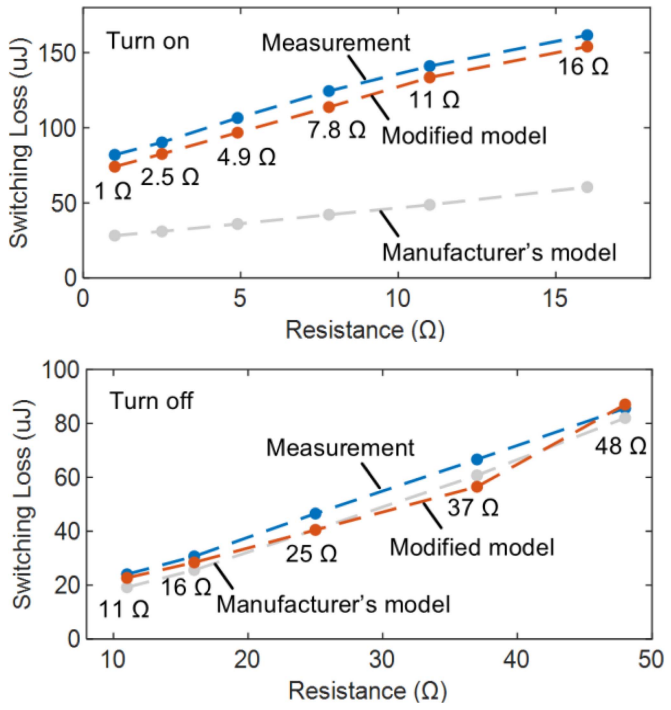

Fig. 21. Comparison of switching loss between simulated (refined model) and experiment against gate resistance. Top: Turn-ON, total loop inductance is 17.5 nH. Bottom: Turn-OFF, inductance is 33 nH.

B. Benchmark 1-Step-Driven Switching Waveforms

Fig. 20 shows the measured switching waveforms obtained using Board 1 with the 1-step driver. For the turn-ON waveforms, the power loop inductance is configured to 17.5 nH, via inductor L_A (shown in Fig. 17). For the turn-OFF waveforms, the loop inductance it is set to 62 nH, to promote ringing and overshoot. These measured results are set against simulated waveforms using both the refined device model and the original manufacturer-supplied model.

It is evident that discrepancies noted in Table have been at least partially resolved, particularly the errors in delay, rates of change, and to some extent, the final gate voltage. The simulated power loop overshoots and ringing also show relatively good agreement with the measured results. The predicted turn-ON loss is approximately 85 μJ, which is only 5.5% below the measured value of 90 μJ. In contrast, the manufacturer's model significantly underestimates the loss, predicting 31 μJ. At turn-OFF, the refined model overestimates the loss by 6%, while the manufacturer's model underestimates it by 12%. It is anticipated that remaining discrepancies are in part due to the tolerance in the gate current measurement.

C. Loss Accuracy Comparisons

Fig. 21 compares the simulated switching energy losses from the refined model with experimental results across a wide range of switching speeds, achieved by varying the gate resistance. For turn-ON events, the prediction error remains within 10% across all tested conditions. For turn-OFF events, most errors are below 15%, with greater deviations observed at higher gate resistance values.

V. Experimental Results With Optimized Gate Current Profiles

A. Optimization Process Applied to Turn-on Waveforms

The aim of this experiment is to program the custom active gate driver ASIC to suppress current oscillation in the power loop at turn ON, thereby reducing high-frequency spectral components and resulting EMI. It employs the 4-step search method described in Section II-C and illustrated in Fig. 4.

Step 1 establishes a measured baseline using the commercial 1-step gate driver with a gate resistance of 2.5 Ω. The corresponding gate current profile and switching waveforms are recorded. In Step 2, as shown in Fig. 22, the measured gate current profile (dashed line) is converted into a piecewise-linear approximation (solid line). Since the resulting switching waveforms are highly similar, the approximation preserves

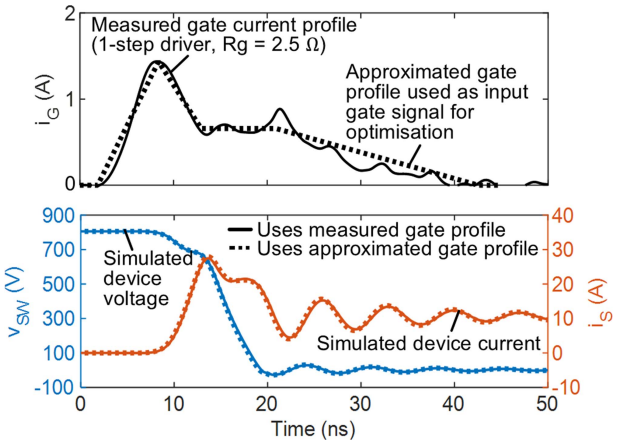

Fig. 22. Top: Measured gate current profile (dashed) and corresponding piecewise-linear approximation (solid). Bottom: Simulated switching waveforms using the measured and approximated gate current profiles as gate input signals.

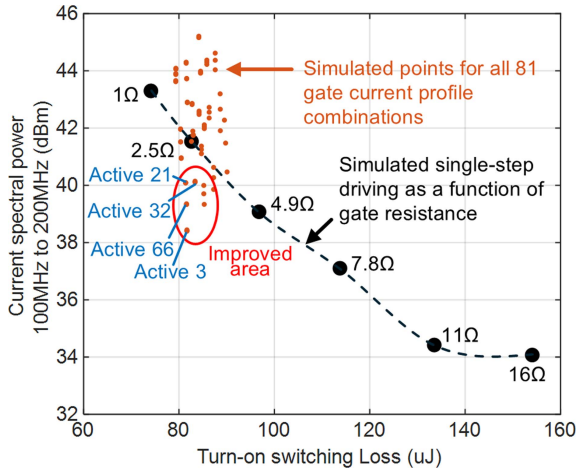

Fig. 24. Simulated turn-ON switching loss versus spectral power of the source current under active gate driving (orange dots) and single-step driving (black dots).

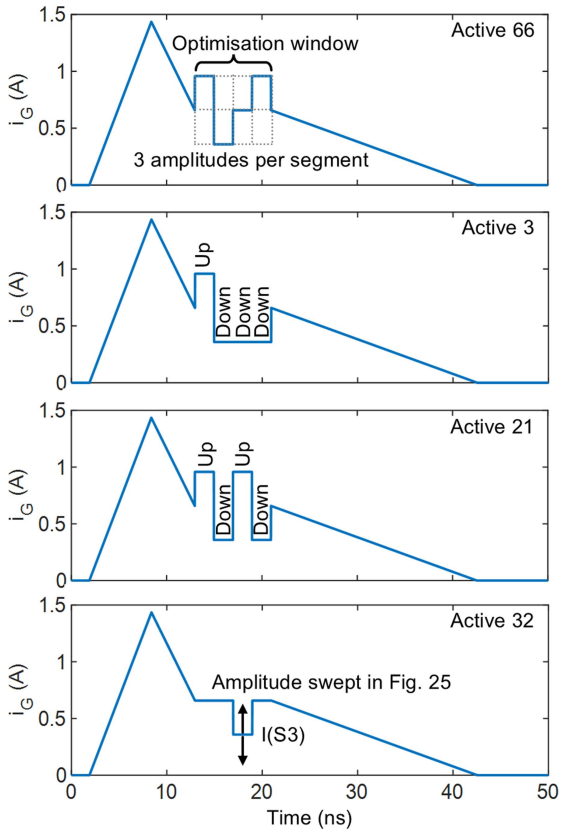

Fig. 23. Four examples of the approximated gate current profile of Fig. 22, with optimization window applied to the plateau region. Window contains four segments and three amplitude options per segment. Results for these specific profiles are highlighted in Fig. 24.

excellent fidelity while significantly reducing simulation resolution requirements.

For the simulation-based optimization (Step 3), the Miller plateau region is selected as the optimization window, as illustrated in the top panel in Fig. 23. This window spans approximately 8 ns and is divided into four 2-ns segments. Within each segment, the optimization initially selects from three discrete gate current amplitudes: maintaining the gate current at 0.658 A, or deviating from it by ±0.3 A. This results in $3^4 = 81$ possible combinations, and each gate profile is allocated an identifier "Active *n*," where *n* is a unique sequence number from 1 to 81. Four representative examples are shown in Fig. 23.

Fig. 24 presents a scatter plot of simulated turn-ON switching loss versus spectral power of the source current, for all 81 combinations. The spectral power is computed by integrating the current spectrum from 100 MHz to 200 MHz, because the dominant ringing frequency lies at 186 MHz. The figure also shows 1-step-driven results for reference.

The results of the four gate current profiles in Fig. 23 are highlighted, as each demonstrates an improvement over the EMI-loss trade-off achieved by single-step driving. Among these, "Active 66" requires three carefully timed modifications to the current across both polarities. "Active 3" involves two such modifications, "Active 21" applies four, and "Active 32" only require one.

The "Active 32" profile is further refined by adjusting the gate current in Segment 3 exclusively. Rather than using the value of 0.658 A, the current in this segment is swept from 0 to 1.4 A in 0.1 A increments. The corresponding simulation results are indicated by green dots in Fig. 25, showing that a further reduction in spectral power of 1.5 dBm has been gained. The inset shows the spectral power of the current as a function of this modification, revealing an optimum.

Step 4 involves experimentally validating the most promising gate current profile, taken here to be the further refined "Active 32" profile. This current profile is recreated using the Bristol Active SiC Gate Driver ASIC in two stages:

First, the baseline gate current (ADI driver with 2.5 Ω) is measured, and programmed into the driver. The programming method follows an iterative process, where in successive 2 ns clock cycles, the nominal output resistance is swept to approximate the required gate current for that clock cycle [14]. This

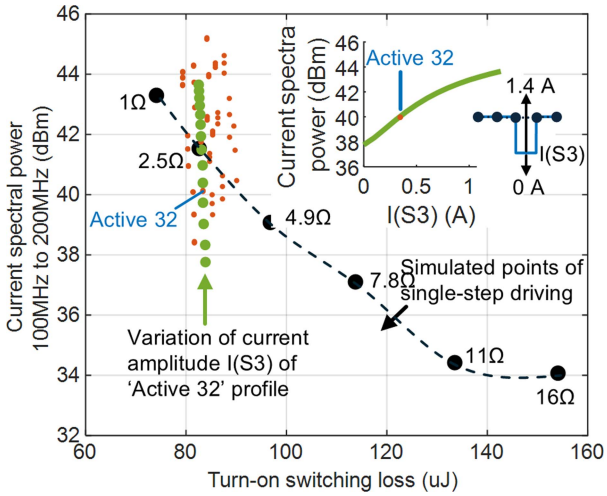

Fig. 25. Improvement in simulated spectral power based on the Active 32 profile, by varying the current amplitude I(S3) in Segment 3.

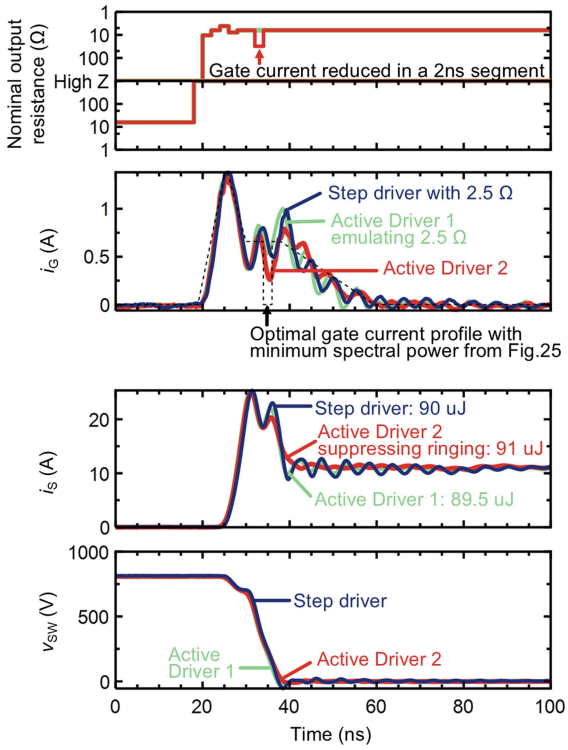

Fig. 26. Measured switching waveforms. Active Driver 1: Bristol active gate driver IC programmed to emulate ADI single-step driver. Active Driver 2: Active driver IC programmed to recreate the optimized "Active 32" profile.

yields the gate current profile "Active Driver 1," shown as the green trace in the i_G panel in Fig. 26.

Next, the refined "Active 32" profile is implemented by lowering the gate current during the third quarter of the Miller plateau, see the red gate current profile named "Active Driver 2" in Fig. 26.

As predicted by the simulations in Fig. 25, the measured switching loss is similar for each switching waveform (ADI

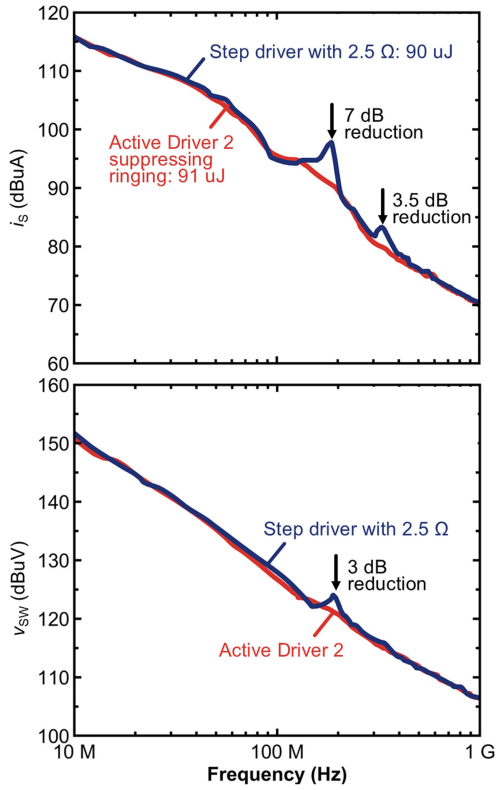

Fig. 27. Spectral envelopes, created by applying an FFT to the measured time-domain waveforms of Fig. 26.

driver 90 μJ, emulation of this driver 91 μJ, emulation of "Active 32" profile 89.5 μJ). The Active Driver 2 profile noticeably reduces ringing, and attenuates the 186 MHz peak in the spectral content of the source current by 7 dB and the peak at 333 MHz by 3.5 dB, while the corresponding peak in the voltage spectrum is reduced by approximately 3 dB, see Fig. 27.

By bridging simulation and hardware through localized current adjustments in critical phases, this approach suppresses EMI without compromising efficiency. Implementation experimentally can be completed in under 30 min.

B. *Optimization Process Applied to Turn-OFF*

The same 4-step optimization process is applied to the turn-OFF transition, aiming to increase the device's voltage margin by reducing voltage overshoot. To achieve this, the optimization window is positioned to span the rise in drain-source voltage and the overshoot region. This window is divided into four segments, within each of which the gate current amplitude is swept around the value measured with the single-step driver. The resulting hardware-implemented gate current profile "Active Driver 3" is plotted in Fig. 28. It contains a temporary reduction in gate current during the final stage of the voltage rise, followed by an increase just after the overshoot. Fig. 28 shows the corresponding measured switching waveforms compared against those of the 1-step driver.

The active driver profile reduces the drain-source voltage overshoot by 21 V, whilst slightly reducing the switching loss from 64 to 63.4 μJ.

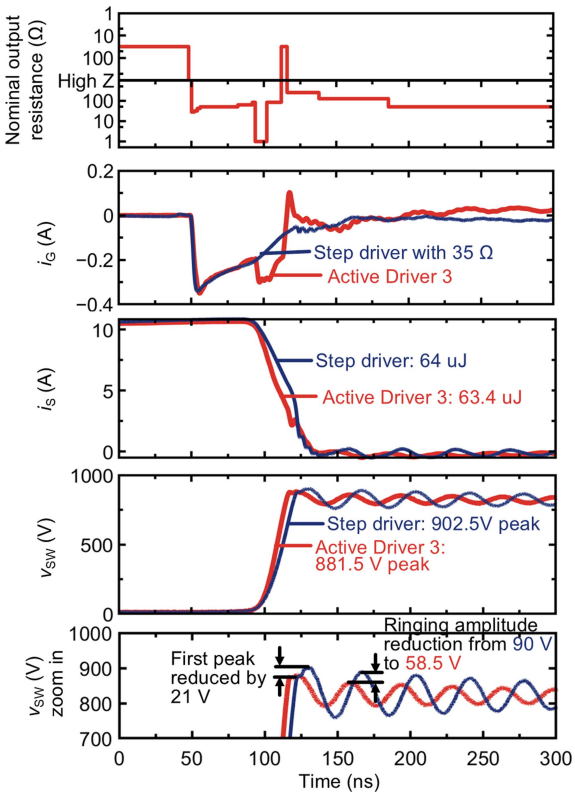

Fig. 28. Demonstration of Bristol active driver ASIC to reduce voltage ringing and overshoot at turn-OFF. Total power loop inductance = 62 nH. Gate resistor of ADI single-step driver = 35 Ω.

VI. Conclusion

This article shows that a windowed gate current profile optimization method virtually eliminates ringing at turn-ON, and reduces ringing and provides additional voltage margin at turn-OFF. This work explicitly targets the trade-off between ringing and switching loss, and the largest impacts on the waveforms are found during the Miller plateau. Other waveform features could be targeted by extending the profile search window.

The optimization was carried out in simulation and verified in hardware. To support accurate optimization, the manufacturer's original device model was refined based on experimental measurements. These modifications significantly improve the agreement between simulated and measured power loop and gate switching waveforms, and the accuracy of performance metrics applied in gate profile optimization, such as energy loss where errors are below 10% for turn-ON and 15% for turn-OFF across a range of gate resistances. The optimization technique and the underlying device model have been validated over a range of gate resistors and loop inductances and therefore appear to be valid across a wide range of circuit implementations, though further studies with specific devices or modules would be advisable.

Future work could extend the device-model refinement methodology across temperature, integrate additional device-physics effects such as threshold-voltage hysteresis and DIBL, and validate the proposed refinement and optimization methods using SPICE models from other manufacturers. For specific application scenarios, future studies could validate the model over the entire operating range of load current, bus voltage, and temperature. It is a well-known drawback of open-loop active gate drivers that the gate drive profile is potentially vulnerable to becoming suboptimal over device-to-device and operating point changes. Investigating these sensitives with measurements on real-world devices across the entire operating range requires a very large investment of person-hours and runs the significant risk of damaging power devices should an active gate drive profile become significantly suboptimal at any point across the operating space. Therefore, another significant advantage of a low-complexity high-fidelity model is the potential to rapidly investigate the sensitivity of gate drive profiles to device-to-device and operating point variations.

The modulation of gate current profiles in simulation changes the total charge provided to or removed from the gate, thereby changing the final gate voltage value. This has been neglected as its impact occurs after the switching transient. It is also notable that while the simulation assumed instantaneous current transitions, the actual driver and gate network result in finite current rise times of around 2 ns. The profiles identified in simulation under the assumption of negligeable rise times were found to be effective in hardware. For gate drivers with slower slew rates, slewing may need to be introduced in the simulation. In this way, the limitations of a driver using discrete components could be investigated.

Precise timing adjustments to gate current profiles during critical switching intervals appear to be more effective than amplitude resolution, however, these may be harder to implement for relatively complex gate profiles. A number of different gate profiles provide similar improvements. This remaining degree of freedom could potentially be exploited to adjust to operating point changes, for example during the ac cycle of an inverter.

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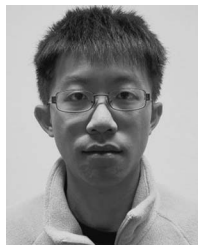

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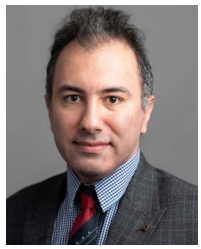

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