Enhanced Power Sharing of Dual-Frequency-Band Grid Emulator Utilizing Inductive Terminal Characteristic

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***Abstract*—The grid-interaction stability of the converter may vary with grid impedance conditions, and needs to be validated before field deployment. To facilitate stability tests toward grid-connected converters, a dual-frequency-band grid emulator has been proposed, which consists of an impedance-forming converter (IFC) switching at high frequency, and a power-supporting converter (PSC) switching at low frequency. Normally, the IFC is used to mimic the terminal characteristics of a predefined grid condition, while the PSC is expected to absorb/supply the power flowing through the converter under test. However, due to the limited control bandwidth of PSC, a large proportion of harmonic and transient power may flow through IFC under grid resonance conditions, which deviates from the design expectation. This may lead to overcurrent of IFC and limit the full use of PSC's power capacity. In this article, the power sharing of a dual-frequency-band grid emulator is studied, and an enhancement method utilizing the inductive terminal characteristic of IFC is proposed. With the proposed method, the current tracking performance of PSC is elevated, which naturally improves power sharing and extends the applicable power range of the grid emulator.**

***Index Terms*—Grid emulator, impedance emulation, power sharing, stability test.**

I. Introduction

With more and more power electronic converters integrated into modern power grids [1], the interaction stability between converter and grid is gaining concerns. In terms of the converter, its grid-interaction stability varies with grid impedance conditions [2] and needs to be checked before field deployment. To facilitate such kind of stability test, grid emulators with impedance emulation capability have been proposed [3].

The technical requirements for grid emulators are becoming more stringent [4]. On one hand, the power capacity of grid-connected converters is continuously growing, which pushes grid emulators toward higher power level. On the other hand, in order to reveal the resonance risk of converters under weak grid conditions, grid emulators are expected to synthesize grid impedance accurately till hundreds of hertz or even a few thousand hertz, which necessitates a higher control bandwidth.

For single-converter-based grid emulators [5], [6], [7], the emulating converter needs to handle all the power from the converter under test (CUT). Consequently, its switching frequency is limited, and hence control bandwidth is achievable. Wide band-gap (WBG) devices and linear power amplifiers (LPA) can be adopted to extend the bandwidth [8], [9]. However, the achievable power level of WBG-device-based converters and LPAs remains limited compared with silicon-IGBT-based converters. Parallelization of WBG-device-based converters helps increase the overall power level [10], [11], but a relatively high power capacity is still required for each converter, and extra attention should be paid to circulating current issues [12]. As an alternative, grid emulators employing both low- and high-switching-frequency converters have been proposed, showing promise in achieving both high power level and high control bandwidth. Typically, the low-switching-frequency converters are designed to handle most of the power, while the high-switching-frequency converters are dedicated to characteristics shaping. In [13] and [14], series configurations with coupling inductors or transformers are presented, which have been proven to be effective in voltage sag generation and high-frequency harmonic injection. Nevertheless, the magnetic coupling elements bring additional concerns, such as core saturation and voltage surges during protection events. In [15] and [16], a transformer-less parallel configuration is proposed, which has been demonstrated as a competitive solution for stability tests toward grid-connected converters. This configuration, referred to as the "dual-frequency-band" grid emulator, serves as the system studied in this article.

Fig. 1 shows the configuration of a dual-frequency-band grid emulator connected to a CUT. An interface inductor L_{ser} is put between the grid emulator and CUT. The grid emulator consists of an impedance-forming converter (IFC) switching at high frequency, and a power-supporting converter (PSC) switching at low frequency. Normally, the high-bandwidth IFC regulates the output voltage of the grid emulator $v_{\mathrm{PCC\_emu}}$ to mimic the terminal characteristics of a predefined grid condition, while the high-power PSC tracks the PCC current i_{PCC} to absorb/supply the power flowing through CUT.

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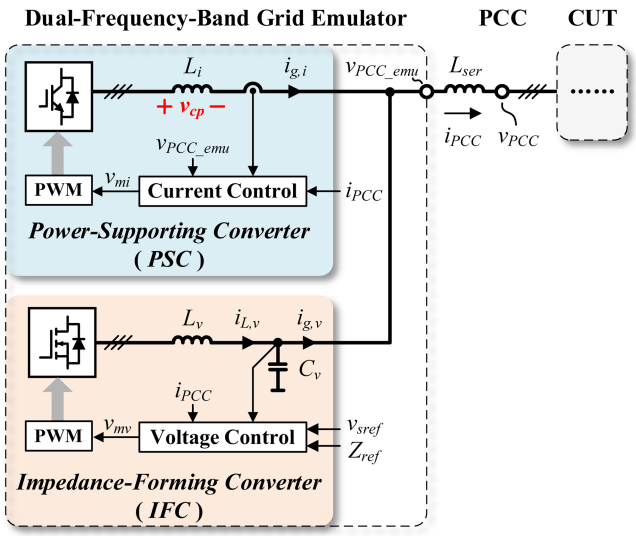

Fig. 1. Configuration of a dual-frequency-band grid emulator connected to a CUT. PCC: Point of common coupling.

However, due to the limited control bandwidth of PSC, the power sharing between IFC and PSC deviates from the design expectation as frequency increases. For example, if CUT resonates with the emulated weak grid, mid-frequency components would appear in PCC current and may flow through IFC, as PSC is unable to track them. This may lead to overcurrent of IFC, and limits the full use of PSC's power capacity. Thus, it is necessary to improve the power sharing between the paralleled IFC and PSC, which is left to be handled.

Efforts have been made to improve the power sharing among paralleled converters [17]. For voltage-controlled converters in parallel, if the output voltages of converters are mismatched or the impedances between the converters and loads are mismatched, improper power sharing can happen [18]. To deal with the first factor, output power can be fed back to adjust voltage references, which is the basic idea of the widely used droop control [19], [20]. To deal with the second factor, virtual impedance can be added to modify the power output characteristics of converters [21], [22], [23]. But these methods are not suitable for the dual-frequency-band grid emulator, for this grid emulator contains both a voltage-controlled converter (IFC) and a current-controlled converter (PSC). Furthermore, the improper power sharing of the grid emulator is due to the fact that PSC is unable to track the harmonic and transient components of PCC current, which indicates the mismatched bandwidth as the main cause, rather than the mismatched output voltages or impedances. Some research on power sharing among paralleled voltage-controlled and current-controlled converters has also been reported [24]. In such scenario, master–follower control is one of the most commonly seen methods [25], [26]. Typically, a voltage-controlled converter is defined as master, and the other converters are defined as followers, whose control references are adjusted according to the master current or load current. However, this method does not help to alleviate the mismatched bandwidth. In [27] and [28], the mismatched bandwidth between converters has been noticed, and outer loops of power comparison and impedance modification are respectively added to mitigate this issue. Nonetheless, the effect is limited by inner voltage/current loops. Meanwhile, since the switching frequencies are assumed to be similar in [27] and [28], the voltage-controlled converter exhibits slower dynamics than the current-controlled converter, which is opposite to the study case of this article. Therefore, the power sharing of the dual-frequency-band grid emulator is different from normal cases and needs to be specifically handled.

In this article, the power sharing of a dual-frequency-band grid emulator is studied. The main focus is on addressing the unsatisfactory power sharing resulting from the mismatched bandwidth between a fast voltage-controlled converter (IFC) and a slow current-controlled converter (PSC). This focus distinguishes the article from the existing works that deal with mismatched voltages, mismatched impedances, or mismatched bandwidth between a slow voltage-controlled converter and a fast current-controlled converter. The main contributions are summarized as follows.

1) A power sharing enhancement method utilizing the inductive terminal characteristic of IFC is proposed. With this method, the current tracking performance of PSC is elevated, which naturally improves both harmonic and transient power sharing of the grid emulator.
2) The effectiveness of the proposed method, as well as its impact on the stability of grid emulator, is analyzed under different emulated impedance conditions, which provides guidance for application.

The rest of this article is organized as follows. Section II compares the commonly seen power configurations for converter-based grid emulators in low-voltage scenarios, thereby clarifying the advantages of dual-frequency-band configuration and justifying further improvement on its power sharing. Section III elaborates the operating principles and power sharing characteristics of the dual-frequency-band grid emulator. Section IV clarifies the basic idea and detailed implementation of the proposed power sharing enhancement method. Section V investigates the power sharing performance and stability of the grid emulator considering the proposed method. Section VI presents simulation and experimental validations. Finally, Section VII concludes the article.

II. Power Configuration Comparison for Converter-Based Grid Emulators in Low-Voltage Scenarios

In this section, a comparative analysis of commonly seen power configurations for converter-based grid emulators in low-voltage scenarios has been conducted. The focus has been put on paralleled configurations, while the cascaded configurations, which are widely adopted in medium-voltage scenarios, are not discussed here. More details on medium-voltage configurations can be referred in [29].

Five configurations are considered: a single low-switching-frequency converter [7], a single high-switching-frequency converter [9], paralleled low-switching-frequency converters [30], paralleled high-switching-frequency converters [10],

TABLE I
POWER CONFIGURATION COMPARISON OF CONVERTER-BASED GRID EMULATORS IN LOW-VOLTAGE SCENARIOS

	Single converter with low f_{sw}	Single converter with high f_{sw}	Paralleled converters with low f_{sw}	Paralleled converters with high f_{sw}	Paralleled converters with low and high f_{sw} (Dual-frequency-band)
Cost of power semiconductor devices	Low	High	Low	High	Medium
Achievable control bandwidth	Low	High	Medium	Very high	High
Achievable power level	High	Low-Medium	Very high	Medium-High	High
Extra considerations	/	/	Circulating current, synchronization		Internal stability, power sharing

* The comparison of device cost is based on the assumption that all configurations are designed for the same rated power capacity.
* The comparison of achievable performance is based on the assumption that the paralleled configurations only involve two converters. If more converters are involved, the overall performance of the paralleled configurations can be further improved, but the relative ranking of their performance remains unchanged.

and paralleled converters with both low and high switching frequencies, i.e., the dual-frequency-band configuration [15]. The comparison covers the cost of power semiconductor devices, achievable control bandwidth, achievable power level, and extra considerations on control and stability issues. The results are summarized in Table I.

In terms of the cost of power semiconductor devices, the comparison is made under the assumption that all configurations are designed for the same rated power capacity. A low-switching-frequency converter typically employs Si IGBTs, which are cost-effective. A high-switching-frequency converter usually adopts WBG devices, which are roughly 3–8 times more expensive than their Si counterparts [31], thereby exhibiting a high device cost. For paralleled configurations with identical switching frequencies (either low or high), though the total number of power devices increases, the current handled by each device is proportionally reduced. Since the cost of power devices is positively correlated with their current ratings [31], such paralleled configurations are expected to have a comparable device cost to single-converter configurations with the same switching frequency. For the dual-frequency-band configuration, PSC and IFC can be taken as low- and high-switching-frequency converters, respectively. Although IFC employs WBG devices, it handles significantly less power than PSC. Therefore, the device cost of IFC is expected to be lower than that of PSC, and the overall device cost of the dual-frequency-band configuration is regarded as medium.

In terms of achievable control bandwidth, the main limitations arise from time delay and output filters. A higher switching frequency not only helps reduce the time delay introduced by modulation, but also allows using a smaller output filter with a higher cut-off frequency. Consequently, the achievable control bandwidth is positively correlated with the switching frequency. In general, a low-switching-frequency converter exhibits a limited control bandwidth, while a high-switching-frequency converter can achieve a high control bandwidth. For paralleled configurations with identical switching frequencies (either low or high), the interleaving technique helps increase the equivalent switching frequency [32], thereby extending the control bandwidth. If only two converters are involved, the paralleled configurations with a low or high switching frequency are expected to achieve a medium or very high control bandwidth, respectively. For the dual-frequency-band configuration, the output terminal characteristics are primarily determined by the high-switching-frequency IFC. Therefore, its achievable control bandwidth is regarded as high.

It should be noted that with more converters involved, the overall performance of the paralleled configurations can be further improved, but the relative ranking of their performance remains unchanged.

In terms of achievable power level, there is a tradeoff between power level and switching frequency. Although WBG devices have partially alleviated this tradeoff, their current ratings remain limited compared with Si devices [33]. Consequently, a low-switching-frequency converter can achieve a high power level, while a high-switching-frequency converter is typically restricted to a low-to-medium power level. Since parallel operation enables current sharing, if only two converters are involved, the paralleled configurations with a low or high switching frequency are expected to achieve a very high or medium-to-high power level, respectively. For the dual-frequency-band configuration, most of the power is processed by the low-switching-frequency PSC. Therefore, its achievable power level is regarded as high.

In terms of extra considerations, the control and design of a single-converter configuration are relatively mature. Paralleled configurations with identical switching frequencies may suffer from circulating current issues [12], which can be mitigated by applying magnetic components and circulating current control algorithms. As the number of paralleled converters increases, synchronization also needs careful design [33]. For the dual-frequency-band configuration, the interaction between PSC and IFC may introduce internal stability issues, which will be analyzed in Section V-B. Meanwhile, the power sharing between PSC and IFC is important, which will be discussed and improved in this article.

In summary, the dual-frequency-band configuration offers a feasible solution to achieve both high control bandwidth and high power level with a moderate increase in device cost. Moreover, this configuration may serve as a flexible upgrade scheme: by incorporating an IFC or PSC, it is possible to independently enhance the control bandwidth or power capacity of an existing grid emulator. Thus, it is reasonable to further improve its power sharing performance.

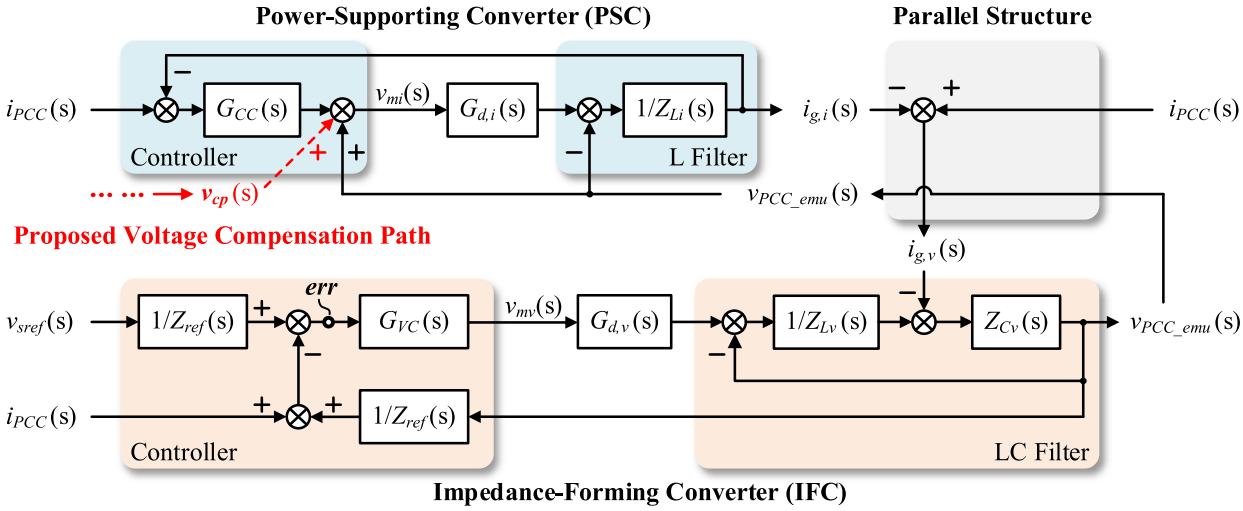

Fig. 2. Block diagram of dual-frequency-band grid emulator.

III. Modeling of Power Sharing Characteristics of Dual-Frequency-Band Grid Emulator

In this section, the operating principles of the individual PSC and IFC are elaborated first, and their impedance models are derived. Then, the equivalent circuit of the entire grid emulator is established, so that its power sharing characteristic can be extracted, which facilitates the analysis on power sharing enhancement in Section IV.

It should be noted that the control of the dual-frequency-band grid emulator is directly implemented in the stationary *abc* reference frame, rather than in the rotating *dq* reference frame. This is because the output waveforms of the grid emulator may contain a large number of harmonic and transient components [4]. In such an application scenario, the rotating reference frame cannot ensure minimal steady-state error in voltage/current tracking. Instead, the Park transformation may introduce inter-phase coupling [34], which increases the complexity of modeling and control. Therefore, the stationary reference frame is adopted, and a symmetrical system is assumed, which allows using single-input single-output modeling to simplify the analysis. The Laplace transform variable "s" is omitted in figures (except block diagrams) and transfer functions for brevity.

A. Operating Principles and Impedance Modeling of the Individual PSC and IFC

Fig. 2 shows the block diagram of dual-frequency-band grid emulator, corresponding to the configuration in Fig. 1.

Due to the parallel structure, PSC and IFC have identical terminal voltage $v_{\mathrm{PCC\_emu}}$, and their output currents together constitute PCC current.

In terms of PSC, a PI controller G_{CC} is adopted to regulate its output current $i_{g,i}$, and an L filter is used to attenuate switching-frequency current ripples. Since i_{PCC} is directly taken as the current reference, PSC is expected to track the power flowing through CUT. $G_{d,i} = \mathrm{e}^{-s\cdot(1.5T_{\mathrm{sw},i})}$ denotes the time delay of PSC, where $T_{\mathrm{sw},i}$ is the switching period of PSC. Z_{Li} denotes the impedance of L_i branch of PSC, corresponding to that in Fig. 1. v_{mi} denotes the modulation signal for PSC.

Take $v_{\mathrm{PCC\_emu}}$ and i_{PCC} as inputs, the output current of PSC $i_{g,i}$ can be expressed as (1), where G_{CCL} and $Z_{\mathrm{out\_PSC}}$, respectively, denotes the reference tracking performance and output impedance of PSC

$$i_{g,i} = G_{\mathrm{CCL}} \cdot i_{\mathrm{PCC}} - \frac{v_{\mathrm{PCC\_emu}}}{Z_{\mathrm{out\_PSC}}} \tag{1}$$

$$G_{\mathrm{CCL}} = \frac{i_{g,i}}{i_{\mathrm{PCC}}}\Big|_{v_{\mathrm{PCC\_emu}}=0} = \frac{G_{CC}\cdot G_{d,i}}{Z_{Li} + G_{CC}\cdot G_{d,i}} \tag{2}$$

$$Z_{\mathrm{out\_PSC}} = \frac{v_{\mathrm{PCC\_emu}}}{-i_{g,i}}\Big|_{i_{\mathrm{PCC}}=0} = \frac{Z_{Li} + G_{CC}\cdot G_{d,i}}{(1 - G_{d,i})}. \tag{3}$$

In terms of IFC, the virtual admittance control proposed in [35] is adopted to emulate grid impedance, and a passively damped LC filter is used to attenuate switching-frequency voltage ripples. v_{sref} and Z_{ref}, respectively, denote the voltage and impedance reference of the emulated grid. G_{VC} denotes the model-embedded controller proposed in [36]. $G_{d,v} = \mathrm{e}^{-s\cdot(1.5T_{\mathrm{sw},v})}$ denotes the time delay of IFC, where $T_{\mathrm{sw},v}$ is the switching period of IFC. Z_{Lv} and Z_{Cv}, respectively, denote the impedance of L_v and C_v branches of LC filter, corresponding to that in Fig. 1. v_{mv} denotes the modulation signal for IFC.

According to the controller structure of IFC, as shown in Fig. 2, the control error err of IFC can be written as (4). In (4), the term "v_{sref} - i_{PCC}·Z_{ref}" can be taken as the control reference, and thus the emulation of a power grid with impedance can be realized. The grid impedance is simplified to an inductor L_{ref} in series with a resistor R_{ref}, as given in (5), which is commonly used in weak grid emulation [37], [38], [39]

$$\begin{aligned} \mathrm{err} &= \frac{v_{\mathrm{sref}}}{Z_{\mathrm{ref}}} - \left(i_{\mathrm{PCC}} + \frac{v_{\mathrm{PCC\_emu}}}{Z_{\mathrm{ref}}}\right) \\ &= \frac{1}{Z_{\mathrm{ref}}}\left[(v_{\mathrm{sref}} - i_{\mathrm{PCC}}\cdot Z_{\mathrm{ref}}) - v_{\mathrm{PCC\_emu}}\right] \end{aligned} \tag{4}$$

$$Z_{\mathrm{ref}} = s\cdot L_{\mathrm{ref}} + R_{\mathrm{ref}}. \tag{5}$$

Take "v_{sref} - i_{PCC}·Z_{ref}" and $i_{g,v}$ as inputs, the output voltage of IFC $v_{\mathrm{PCC\_emu}}$ can be expressed as (6), where G_{VCL} and

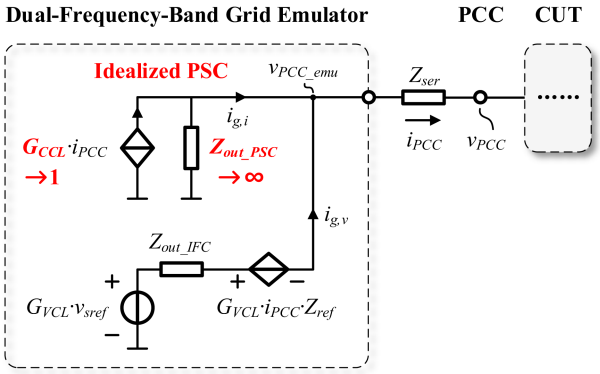

Fig. 3. Equivalent circuit of dual-frequency-band grid emulator.

$Z_{\text{out\_IFC}}$, respectively, denote the reference tracking performance and output impedance of IFC

$$v_{\text{PCC\_emu}} = G_{VCL}\cdot(v_{\text{sref}} - i_{\text{PCC}}\cdot Z_{\text{ref}}) - i_{g,v}\cdot Z_{\text{out\_IFC}} \quad (6)$$

$$G_{VCL} = \frac{v_{\text{PCC\_emu}}}{v_{\text{sref}} - i_{\text{PCC}}\cdot Z_{\text{ref}}}\Big|_{i_{g,v}=0} = \frac{\frac{1}{Z_{\text{ref}}}\cdot G_{VC}\cdot G_{d,v}\cdot\frac{Z_{Cv}}{Z_{Lv}}}{1+\frac{1}{Z_{\text{ref}}}\cdot G_{VC}\cdot G_{d,v}\cdot\frac{Z_{Cv}}{Z_{Lv}}+\frac{Z_{Cv}}{Z_{Lv}}} \quad (7)$$

$$Z_{\text{out\_IFC}} = \frac{v_{\text{PCC\_emu}}}{-i_{g,v}}\Big|_{v_{\text{sref}}-i_{\text{PCC}}\cdot Z_{\text{ref}}=0} = \frac{Z_{Cv}}{1+\frac{1}{Z_{\text{ref}}}\cdot G_{VC}\cdot G_{d,v}\cdot\frac{Z_{Cv}}{Z_{Lv}}+\frac{Z_{Cv}}{Z_{Lv}}}. \quad (8)$$

B. Power Sharing Characteristic of the Entire Grid Emulator

According to (1) and (6), Norton and Thevenin circuits [40], respectively, are used to represent the PSC and IFC inside the grid emulator. And the equivalent circuit of the entire grid emulator, corresponding to the topology in Fig. 1, is given in Fig. 3. Z_{ser} is the impedance of the interface inductor L_{ser}.

By utilizing the superposition theorem, the output current of IFC $i_{g,v}$ can be expressed as

$$i_{g,v} = Y_{\text{inner}}\cdot v_{\text{sref}} + G_{PS}\cdot i_{\text{PCC}} \quad (9)$$

where Y_{inner} represents the inner coupling characteristic from the voltage reference of the emulated grid v_{sref} to IFC current $i_{g,v}$; G_{PS} represents the power sharing characteristic from PCC current i_{PCC} to IFC current $i_{g,v}$.

Based on circuit theory, the transfer functions of Y_{inner} and G_{PS} can be derived from Fig. 3 as

$$Y_{\text{inner}} = \frac{i_{g,v}}{v_{\text{sref}}}\Big|_{i_{\text{PCC}}=0} = \frac{\frac{G_{VCL}}{Z_{\text{out\_PSC}}}}{1+\frac{Z_{\text{out\_IFC}}}{Z_{\text{out\_PSC}}}} \quad (10)$$

$$G_{\text{PS}} = \frac{i_{g,v}}{i_{\text{PCC}}}\Big|_{v_{\text{sref}}=0} = \frac{1-G_{CCL}-\frac{G_{VCL}\cdot Z_{\text{ref}}}{Z_{\text{out\_PSC}}}}{1+\frac{Z_{\text{out\_IFC}}}{Z_{\text{out\_PSC}}}}. \quad (11)$$

In this article, the main focus has been on the power sharing performance G_{PS} of the grid emulator. And $|G_{\text{PS}}|$ is expected to be small, where $|\cdot|$ represents the magnitude of "·."

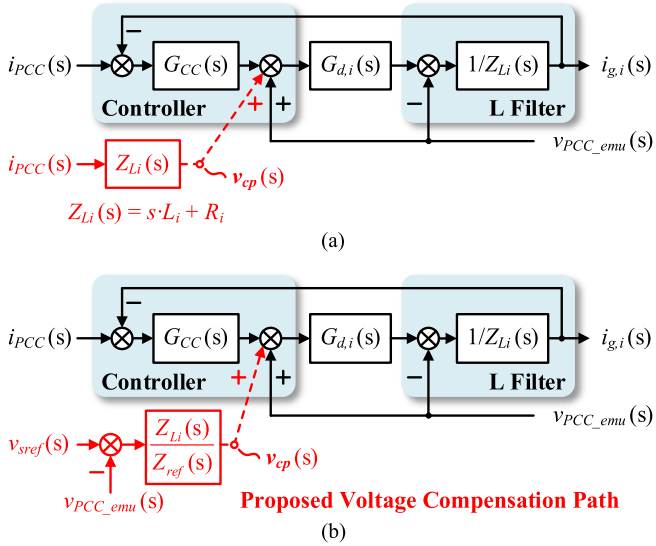

Fig. 4. Block diagram of PSC with voltage compensation path. (a) Basic idea. (b) Derivative-less implementation.

IV. Proposed Voltage Compensation Path for Power Sharing Utilizing Inductive Terminal Characteristic

In the ideal case, the PSC should absorb/supply all the power flowing through the CUT, while the IFC is only responsible for shaping the terminal characteristics of the grid emulator. In other words, the control target is to achieve $i_{g,v}/i_{\text{PCC}} = 0$, which can be realized by making $G_{CCL} \to 1$ and $Z_{\text{out\_PSC}} \to \infty$ according to the power sharing characteristic given in (11). This is attainable in low-to-mid frequency band by leveraging the inductive terminal characteristics of IFC, and detailed implementation is elaborated in this section.

A. Voltage Compensation Path to Improve Current Tracking Performance of PSC

As analyzed above, making $G_{\text{CCL}} \to 1$ and $Z_{\text{out\_PSC}} \to \infty$ helps improve the power sharing performance of the grid emulator. In terms of $Z_{\text{out\_PSC}}$, consider that the time delay $G_{d,i}$ approximates unity in low-to-mid frequency band, as highlighted in (3), the magnitude $|Z_{\text{out\_PSC}}|$ naturally approaches infinity. However, when it comes to G_{CCL}, there remains a gap between $|G_{CCL}|$ and unity. This is because the denominator of G_{CCL} contains one more term than the numerator, i.e., the Z_{Li} highlighted in (2). Therefore, to achieve $G_{CCL} \to 1$, the basic idea is to introduce an extra Z_{Li} term into the numerator of G_{CCL}.

According to Mason's Gain Formula, this idea can be realized by adding a forward path to the original control structure of PSC, as illustrated in Fig. 4(a). The added voltage v_{cp} and the resulting tracking performance G_{CCL_idea} of PSC, respectively, are given as

$$v_{cp} = i_{\text{PCC}}\cdot Z_{Li} \quad (12)$$

$$G_{CCL\_\text{idea}} = \frac{i_{g,i}}{i_{\text{PCC}}}\Big|_{v_{\text{PCC\_emu}}=0} = \frac{Z_{Li}\cdot G_{d,i} + G_{CC}\cdot G_{d,i}}{Z_{Li}+G_{CC}\cdot G_{d,i}}. \quad (13)$$

As can be seen in (13), a new term $Z_{Li} \cdot G_{d,i}$ appears in the numerator, which makes $G_{CCL} \to 1$ valid in low-to-mid frequency band. In this case, the PSC current is close to the PCC current in low-to-mid frequency band, and the added voltage $v_{cp} = i_{\text{PCC}} \cdot Z_{Li} \approx i_{g,i} \cdot Z_{Li}$ can be taken as the compensation for the voltage drop across the inductor L_i (highlighted in Fig. 1). Consequently, the added forward path in Fig. 4 is referred to as the "voltage compensation path."

B. Derivative-Less Synthesis of Voltage Compensation Utilizing Inductive Terminal Characteristics of IFC

The voltage compensation path helps G_{CCL} to approach unity in the low-to-mid frequency band. However, the $Z_{Li} = \text{s}{\cdot}L_i + R_i$ on the voltage compensation path contains a derivative term, which may introduce noise amplification issues. To avoid differentiation, algebra-based methods [23], [28], [41] and low-pass filter (LPF)-based methods [42], [43], [44] are widely adopted. For algebra-based methods, the compensation voltage can only be synthesized at discrete frequencies, making it unsuitable for wide-band power sharing enhancement. Moreover, extracting individual harmonic currents takes extra effort. On the other hand, LPF-based methods inevitably involve a tradeoff between accuracy and noise attenuation, and the selection principle of cut-off frequency is relatively vague. To avoid these limitations, the inductive terminal characteristics shaped by IFC can be utilized to synthesize the compensation voltage, which is elaborated below.

Consider that the control bandwidth of IFC is much higher than that of PSC, the output voltage of IFC $v_{\text{PCC\_emu}}$, as given in (6), can be approximated as (14) from the aspect of PSC

$$v_{\text{PCC\_emu}} \approx v_{\text{sref}} - i_{\text{PCC}} \cdot Z_{\text{ref}}. \tag{14}$$

Then, combine (12) and (14) to eliminate i_{PCC}, the compensation voltage v_{cp} can be written as (15), and the derivative terms in Z_{Li} and Z_{ref} are counteracted, which achieves the derivative-less synthesis of v_{cp}. As can be seen, the implementation is straightforward, requires no parameter tuning, and remains effective within the impedance emulation bandwidth of the grid emulator, i.e., (14) holds

$$\begin{aligned} v_{cp} &= i_{\text{PCC}} \cdot Z_{Li} \approx \frac{v_{\text{sref}} - v_{\text{PCC\_emu}}}{Z_{\text{ref}}} \cdot Z_{Li} \\ &= (v_{\text{sref}} - v_{\text{PCC\_emu}}) \cdot \frac{Z_{Li}}{Z_{\text{ref}}} \,[\text{Counteraction}]\,. \end{aligned} \tag{15}$$

Detailed implementation is illustrated in Fig. 4(b). And the characteristics of the modified PSC can be described as (16), in which G_{CCL} remains unchanged, and the output impedance of PSC is modified into $Z_{\text{out\_PSC\_tc}}$, as given in (17). Meanwhile, an extra coupling G_{vi_tc} is introduced, as given in (18). The subscript tc stands for "terminal characteristics"

$$i_{g,i} = G_{CCL} \cdot i_{\text{PCC}} - \frac{v_{\text{PCC\_emu}}}{Z_{\text{out\_PSC\_tc}}} + G_{vi\_\text{tc}} \cdot v_{\text{sref}} \tag{16}$$

$$Z_{\text{out\_PSC\_tc}} = \frac{v_{\text{PCC\_emu}}}{-i_{g,i}}\Big|_{i_{\text{PCC}}\&v_{\text{sref}}=0} = \frac{Z_{Li} + CC \cdot G_{d,i}}{1 - G_{d,i} + \frac{Z_{Li}}{Z_{\text{ref}}} \cdot G_{d,i}} \tag{17}$$

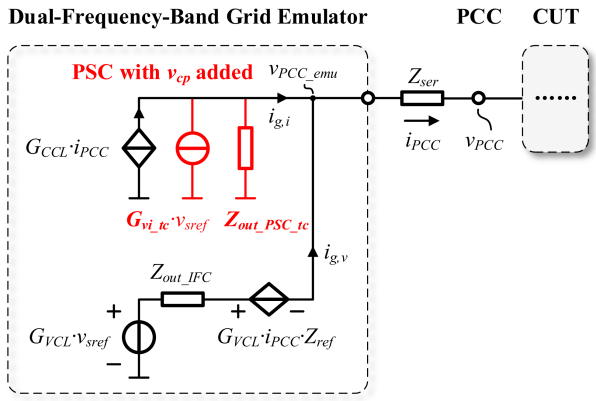

Fig. 5. Equivalent circuit of the modified grid emulator (with the proposed voltage compensation path added).

$$\begin{aligned} G_{vi\_\text{tc}} &= \frac{i_{g,i}}{v_{\text{sref}}}\Big|_{v_{\text{PCC\_emu}}=0\&i_{\text{PCC}}=0} \\ &= \frac{Z_{Li} \cdot G_{d,i}}{Z_{Li} + CC \cdot G_{d,i}} \cdot \frac{1}{Z_{\text{ref}}}. \end{aligned} \tag{18}$$

C. Power Sharing Characteristic of the Grid Emulator With Proposed Voltage Compensation Path

According to (6) and (16), Thevenin and Norton circuits, respectively, are used to represent IFC and the modified PSC inside the grid emulator. And the equivalent circuit of the modified grid emulator (with the proposed voltage compensation path added) is shown in Fig. 5.

Similarly, based on circuit theory, the IFC current $i_{g,v}$ can be rewritten as (19). And the modified inner coupling characteristic $Y_{\text{inner\_tc}}$ and power sharing characteristic $G_{\text{PS\_tc}}$, respectively, are given as (20) and (21)

$$i_{g,v} = Y_{\text{inner\_tc}} \cdot v_{\text{sref}} + G_{\text{PS\_tc}} \cdot i_{\text{PCC}} \tag{19}$$

$$Y_{\text{inner\_tc}} = \frac{i_{g,v}}{v_{\text{sref}}}\Big|_{i_{\text{PCC}}=0} = \frac{\frac{G_{VCL}}{Z_{\text{out\_PSC\_tc}}} - G_{vi\_\text{tc}}}{1 + \frac{Z_{\text{out\_IFC}}}{Z_{\text{out\_PSC\_tc}}}} \tag{20}$$

$$G_{\text{PS\_tc}} = \frac{i_{g,v}}{i_{\text{PCC}}}\Big|_{v_{\text{sref}}=0} = \frac{1 - G_{CCL} - \frac{G_{VCL} \cdot Z_{\text{ref}}}{Z_{\text{out\_PSC\_tc}}}}{1 + \frac{Z_{\text{out\_IFC}}}{Z_{\text{out\_PSC\_tc}}}}. \tag{21}$$

The models established above facilitate further performance evaluation and stability analysis in Section V.

V. Power Sharing Performance Evaluation and Stability Analysis Considering the Proposed Voltage Compensation Path

The proposed voltage compensation path alters the power sharing behavior of dual-frequency-band grid emulator. To verify the theoretical effectiveness, the power sharing performance before and after modification is compared in this section. Meanwhile, the impact of the proposed voltage compensation path on the stability of grid emulator is also investigated to assess the applicability.

The parameters used for analysis are listed in the Appendix, and their selection principles are clarified here. A commonly

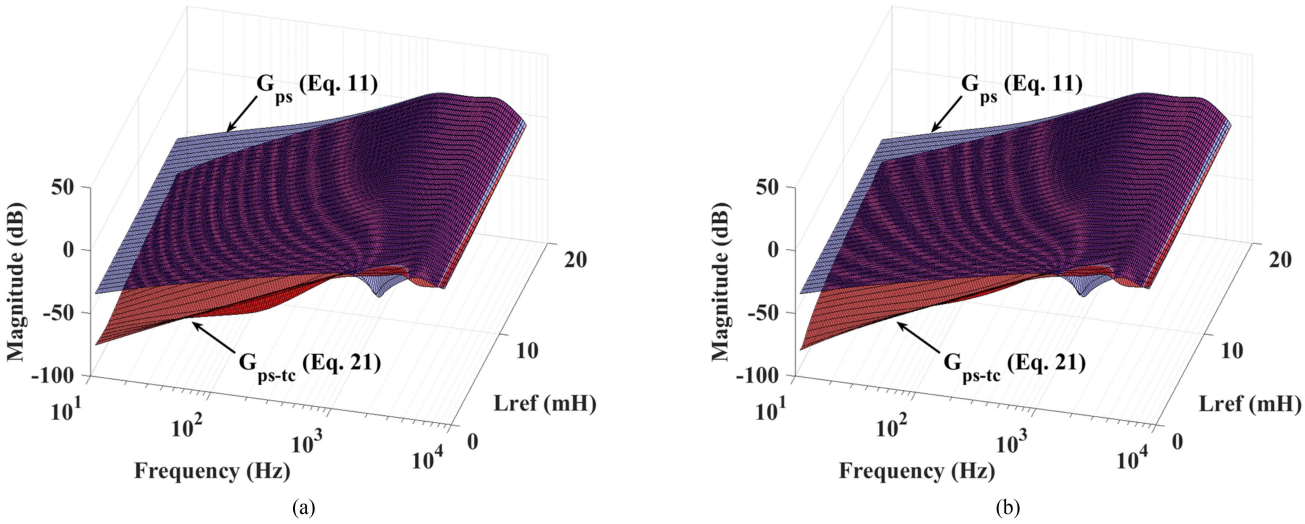

Fig. 6. Magnitude-frequency response of power sharing characteristic from PCC current i_{PCC} to IFC current $i_{g,v}$. $|G_{\text{PS\_tc}}|$ is clearly lower than $|G_{\text{PS}}|$ below 1000 Hz, indicating that the proposed voltage compensation path helps reduce the $i_{g,v}$ sourced by i_{PCC}. (a) Inductive. (b) Inductive-resistive, X/R = 2.

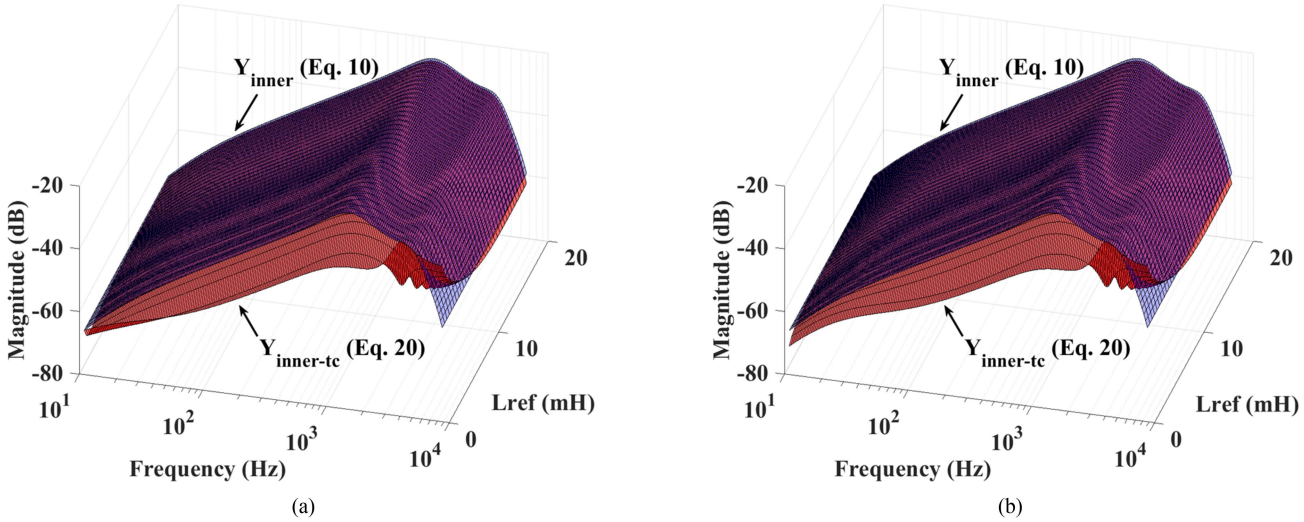

Fig. 7. Magnitude-frequency response of inner coupling characteristic from the voltage reference of the emulated grid v_{sref} to IFC current $i_{g,v}$. $|Y_{\text{inner\_tc}}|$ is lower than $|Y_{\text{inner}}|$ below 3000 Hz, indicating that the proposed voltage compensation path helps reduce the $i_{g,v}$ induced by v_{sref}. (a) Inductive. (b) Inductive-resistive, X/R = 2.

seen *LCL*-filter-based converter with single-loop current control [45] is adopted as CUT, which enables direct regulation of PCC current and helps evaluate the power sharing performance of the grid emulator. The filter parameters of CUT are designed to meet the harmonic current distortion limits specified in the IEEE 1547 standard [46], and the resonant frequency of the *LCL* filter is set to 1/10 of the switching frequency of CUT. The control parameters of CUT are tuned to achieve a phase margin of 45°.

As for the grid emulator, PSC is designed to handle the power from CUT, while IFC is designed to shape the terminal characteristics of the grid emulator. Accordingly, the power capacity of PSC should be comparable to or greater than that of CUT, and its switching frequency should be similar to or less than that of CUT. In this article, the switching frequency of PSC is set equal to that of CUT, i.e., 16 kHz. The filter parameters of PSC are selected to limit its converter-side current ripple to less than 10% of the PCC current. The control parameters of PSC are tuned to achieve a phase margin of 60°. On the other hand, to ensure sufficient control bandwidth, the switching frequency of IFC is set to ten times that of CUT, i.e., 160 kHz. Such a high switching frequency limits the power capacity of IFC, and thus enhancing the power sharing performance of dual-frequency-band grid emulator is important. The filter parameters of IFC are selected to satisfy:

1) its converter-side current ripple is less than 20% of PCC current;
2) the resonant frequency of *LC* filter is 1/20 of the switching frequency of IFC;
3) the damping resistors are set to half of the capacitor impedance at the resonant frequency of the *LC* filter.
4) The control parameters of IFC are tuned to achieve a phase margin of 45°.

In summary, the parameters used for analysis follow the widely adopted design principles, thereby ensuring a fair and representative discussion.

A. Evaluation on Power Sharing Performance of Dual-Frequency-Band Grid Emulator

First, the power sharing characteristics of the grid emulator before and after adding the proposed voltage compensation path are compared. As indicated by (11) and (21), the power sharing behavior varies with both frequency and impedance reference Z_{ref}.

Fig. 6 shows the magnitude-frequency response of the power sharing characteristic from PCC current i_{PCC} to IFC current $i_{g,v}$. The frequency ranges from 10 to 8000 Hz, and the emulated grid inductance L_{ref} ranges from 1 mH (0.03 p.u.) to 18 mH (0.5 p.u.). In Fig. 6(a) and (b), Z_{ref} is assumed to be purely inductive and inductive-resistive with a low X/R ratio of 2, respectively. In both cases, the magnitude of $G_{\text{PS\_tc}}$ is clearly lower than that of G_{PS} below 1000 Hz, regardless of Z_{ref}. This indicates that the proposed voltage compensation path helps reduce the ratio $|i_{g,v}/i_{\text{PCC}}|$, and the power sharing performance of the grid emulator is enhanced.

On the other hand, according to (9) and (19), part of the IFC current $i_{g,v}$ is induced by the voltage reference of the emulated grid v_{sref}. Therefore, it is also necessary to check the inner coupling characteristic of the grid emulator both before and after adding the proposed voltage compensation path.

Fig. 7 shows the magnitude-frequency response of the inner coupling characteristic from v_{sref} to $i_{g,v}$. Similarly, the frequency ranges from 10 to 8000 Hz, and the emulated grid inductance L_{ref} ranges from 1 mH (0.03 p.u.) to 18 mH (0.5 p.u.). In Fig. 7(a) and (b), Z_{ref} is assumed to be purely inductive and inductive-resistive with a low X/R ratio of 2, respectively. In both cases, it can be seen that the magnitude of $Y_{\text{inner\_tc}}$ is lower than that of Y_{inner} below 3000 Hz, regardless of Z_{ref}. This indicates that the proposed voltage compensation path alleviates the inner coupling $|i_{g,v}/v_{\text{sref}}|$, thereby reducing the IFC current sourced by v_{sref}.

B. Analysis on Stability of Dual-Frequency-Band Grid Emulator

The unintended resonance in the dual-frequency-band grid emulator can arise from three factors: IFC itself, PSC itself, and the interaction between IFC and PSC. As stated at the beginning of this section, IFC and PSC are designed to be self-stable. Therefore, the primary concern is their interaction stability, which is determined by the output impedances $Z_{\text{out\_IFC}}$, $Z_{\text{out\_PSC}}$ (without compensation), and $Z_{\text{out\_PSC\_tc}}$ (with compensation).

Since a model-embedded controller proposed in [36] is adopted by IFC, $Z_{\text{out\_IFC}}$ is independent of Z_{ref}. $Z_{\text{out\_PSC}}$ is also independent of Z_{ref}, as no Z_{ref} term appears in (3). However, applying the proposed voltage compensation path introduces a Z_{ref} term into the denominator of (17), which makes $Z_{\text{out\_PSC\_tc}}$ dependent on Z_{ref}.

Fig. 8 shows the bode diagram of $Z_{\text{out\_IFC}}$, $Z_{\text{out\_PSC}}$, and $Z_{\text{out\_PSC\_tc}}$. In Fig. 8(a) and (b), Z_{ref} is assumed to be purely inductive and inductive-resistive with a low X/R ratio of 2, respectively. In both cases, the magnitude of $Z_{\text{out\_IFC}}$ is always lower than that of $Z_{\text{out\_PSC}}$. According to Nyquist stability criterion, the grid emulator without compensation is always stable, regardless of Z_{ref}. With the proposed voltage compensation, the

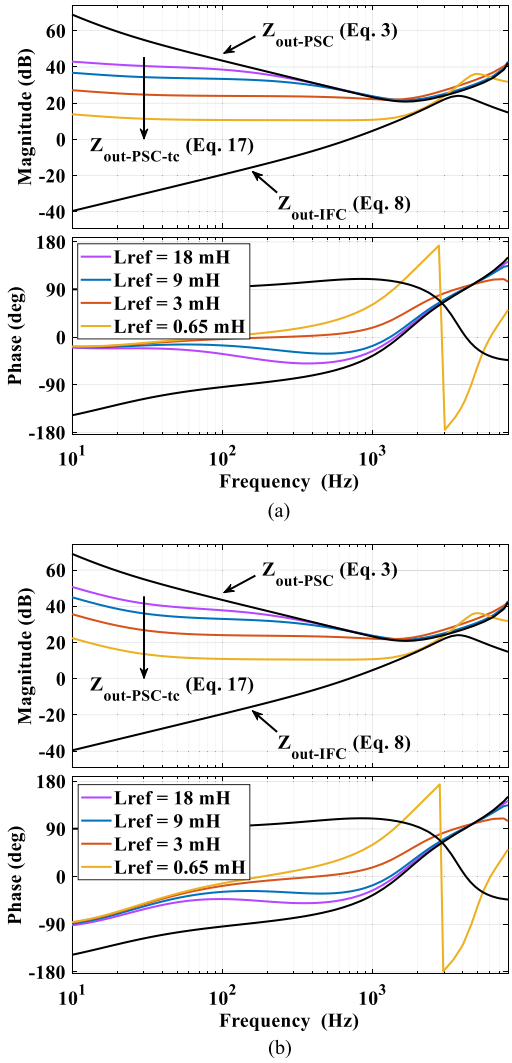

Fig. 8. Bode diagram of $Z_{\text{out\_IFC}}$, $Z_{\text{out\_PSC}}$, and $Z_{\text{out\_PSC\_tc}}$. The magnitude-frequency curve of $Z_{\text{out\_PSC\_tc}}$ moves downwards as L_{ref} decreases. When $L_{\text{ref}} = 0.65$ mH, the magnitude-frequency curves of $Z_{\text{out\_IFC}}$ and $Z_{\text{out\_PSC\_tc}}$ intersects around 2000 Hz, which brings potential risk of interaction instability. (a) Inductive. (b) Inductive-resistive, X/R = 2.

magnitude-frequency curve of $Z_{\text{out\_PSC\_tc}}$ moves downwards as L_{ref} decreases. When L_{ref} is reduced to 0.65 mH (0.02 p.u.), the magnitude-frequency curves of $Z_{\text{out\_IFC}}$ and $Z_{\text{out\_PSC\_tc}}$ intersects around 2000 Hz, which brings potential risk of interaction instability. Therefore, the proposed voltage compensation path should only be enabled when L_{ref} exceeds a certain lower limit, which varies from case to case. In this article, $L_{\text{ref}} = 1$ mH (0.03 p.u.) is chosen as the lower limit, which is normally not a difficult condition to be met.

On the other hand, the interaction stability between the grid emulator and CUT is also an important research topic. Due to the time delay introduced by digital control, sampling, modulation, etc., the output impedance of the grid emulator tends to be non-passive in the high-frequency band, which can lead to unintended resonances at a few thousand hertz [47], [48]. To avoid this unintended high-frequency resonance in both simulation and experiment, a 1 mH interface inductor L_{ser} is inserted, as shown in Fig. 1. This inductor supplements Z_{CUT}, ensuring that the

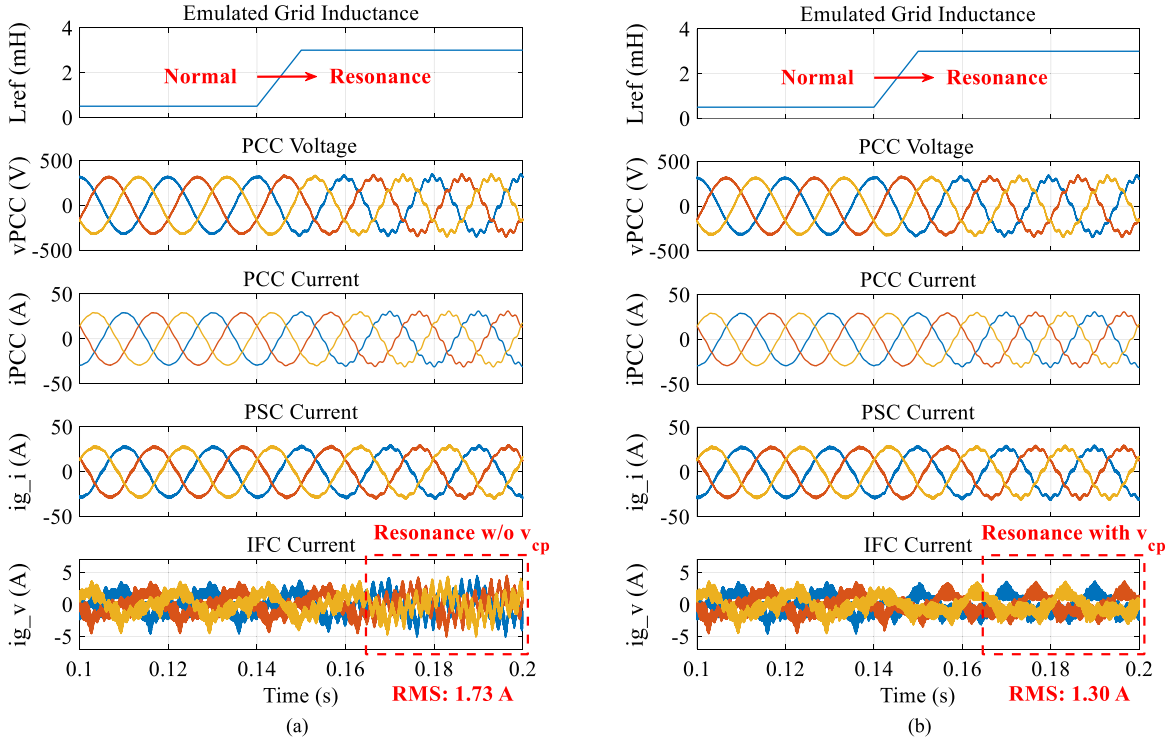

Fig. 9. Simulated waveforms of the grid emulator-CUT system under Scenario 1. At 0.14 s, the emulated grid inductance is intentionally increased to trigger a mid-frequency resonance. With the proposed voltage compensation path enabled, the RMS value of IFC current under resonance condition is reduced by 25 %, compared with the uncompensated case. (a) Without compensation. (b) With the proposed voltage compensation path.

magnitude of output impedance of the grid emulator is lower than $|Z_{\text{CUT}} + Z_{\text{ser}}|$ in high-frequency band, thereby satisfying the Nyquist stability criterion. It should be noted that this article focuses on the power sharing of dual-frequency-band grid emulator, so the discussion is confined to the grid emulator itself, and the interaction stability analysis is not further expanded. More details of this inductor-based stabilization method can be referred in [49] and [50].

VI. Simulation and Experimental Validation

In this section, the effectiveness of the proposed voltage compensation path on power sharing enhancement is evaluated under three test scenarios. In Scenario 1, the impedance reference of grid emulator Z_{ref} is intentionally increased to trigger a grid-CUT interaction resonance at several hundred hertz, so that the harmonic power sharing performance of the grid emulator can be checked. Building upon Scenario 1, Scenario 2 introduces a -50% step change in PCC current, which is designed to test the transient power sharing performance of the grid emulator under resonance conditions. In addition, a practical three-phase diode rectifier load is connected to the grid emulator, which constitutes Scenario 3 for assessing applicability and power sharing performance under nonlinear load condition.

A. Simulation Results

The simulation model of a dual-frequency-band grid emulator connected to a CUT (as shown in Fig. 1) is built in PLECS. The system parameters used in the simulation are listed in the Appendix.

First, the harmonic power sharing performance of the grid emulator is investigated. Fig. 9 shows the simulated waveforms of the grid emulator-CUT system under Scenario 1. At the beginning, the emulated grid impedance is set to a low value, and PCC voltage and current are sinusoidal waveforms at the fundamental frequency. The majority of PCC current is absorbed by PSC, while a small portion flows through IFC. Under this normal condition, the RMS value of IFC current is 1.47 A. At 0.14 s, the emulated grid inductance is intentionally increased to 3.0 mH to trigger a grid-interaction resonance at 550 Hz. The resonance introduces mid-frequency harmonics into both PCC voltage and current. In Fig. 9(a), no extra control measures are taken, and the harmonic tracking capability of PSC is not sufficient. As a result, the mid-frequency harmonics can be observed in both PSC current and IFC current. Under this resonance condition, the RMS value of IFC current is 1.73 A. In comparison, Fig. 9(b) shows the results with the proposed voltage compensation path enabled. In this case, the mid-frequency components in IFC current can hardly be observed, which means PSC absorbs most of the harmonics. And the RMS value of IFC current reduces to 1.30 A, which indicates a 25% reduction.

Fig. 10 shows the frequency spectrum of the simulated IFC current under Scenario 1 (Phase-A). Under normal conditions, the 50 and 550 Hz components are 1.73 and 0.18 A, respectively. Under resonance condition without compensation, the 50 and 550 Hz components increase to 1.75 and 1.38 A, respectively. Under resonance condition with the proposed voltage compensation path enabled, the 50 and 550 Hz components, respectively, reduce to 1.40 and 0.18 A, which indicates 20% and 87% decline compared with the uncompensated case. As can be seen, the

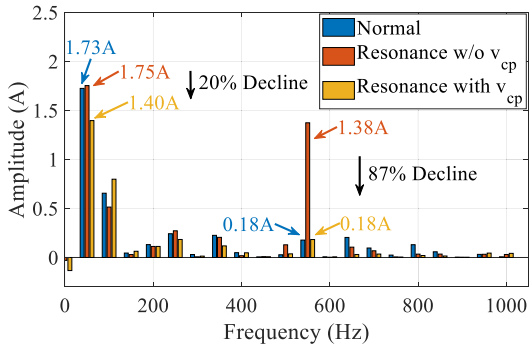

Fig. 10. Frequency spectrum of the simulated IFC current under Scenario 1 (Phase-A). Under resonance condition with the proposed voltage compensation path enabled, the 50 and 550 Hz component of i_{Lv} are reduced by 20% and 87%, respectively, compared with the uncompensated case.

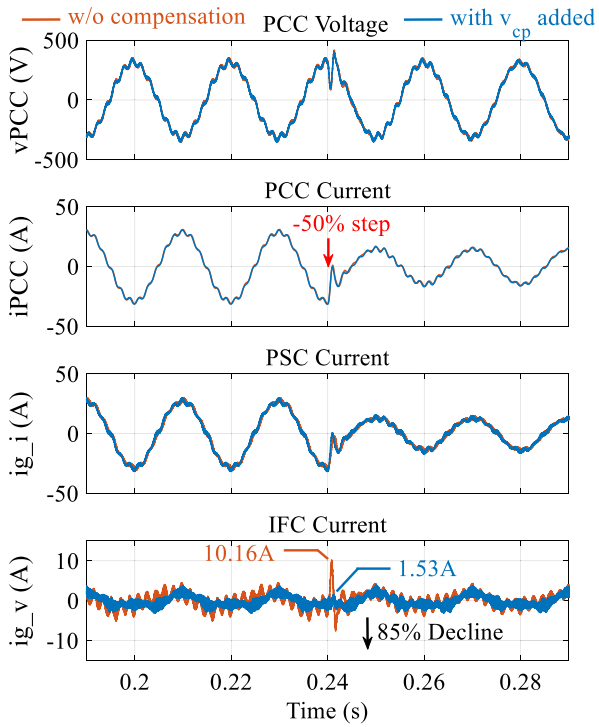

Fig. 11. Simulated waveforms of the grid emulator-CUT system under Scenario 2 (Phase-A). At 0.24 s, PCC current intentionally steps from 28.3 to 14.1 A, and a current surge can be observed in IFC current. With the proposed voltage compensation path enabled, the current surge in IFC current i_{Lv} is reduced by 85%, compared with the uncompensated case.

proposed voltage compensation path is effective at improving harmonic power sharing, and it also contributes to a moderate reduction in the fundamental component of IFC current.

Then, the transient power sharing performance of the grid emulator is investigated. Fig. 11 shows the simulated waveforms of the grid emulator-CUT system under Scenario 2 (Phase-A). At 0.24 s, the PCC current is intentionally controlled to step from 28.3 to 14.1 A, i.e., -50% step. If no extra measures are taken to improve power sharing, a current surge of 10.16 A can be observed in IFC current i_{Lv}. In comparison, with the proposed voltage compensation path enabled, the current surge in i_{Lv} is reduced to 1.53 A, which indicates an 85% decline. Obviously,

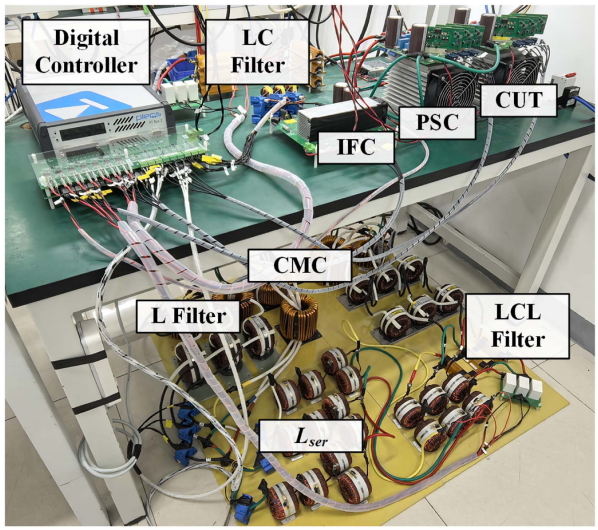

Fig. 12. Experiment setup. CMC: Common mode choke.

the transient power sharing is improved by adding the proposed voltage compensation path.

B. Experimental Results

The experimental setup is shown in Fig. 12, consisting of a dual-frequency-band grid emulator and a current-controlled converter, i.e., CUT. The topology is basically the same as that in Fig. 1, except that the dc-links of the grid emulator and CUT are connected together for power cycling. Common-mode chokes are used to block zero-sequence current. A RT-box 2 is used as the digital controller of the grid emulator and CUT. The system parameters used in the experiment are listed in the Appendix.

First, the harmonic power sharing performance of the grid emulator is examined. Fig. 13 shows the experimental waveforms of the grid emulator-CUT system under Scenario 1. Initially, the emulated grid impedance is set to a low value, and the PCC voltage and current are sinusoidal waveforms at the fundamental frequency. The majority of PCC current is absorbed by PSC, while a small portion flows through IFC. Under this normal condition, the RMS value of IFC current is 1.82 A. Then, the emulated grid inductance is intentionally increased to trigger a grid-interaction resonance at 550 Hz. The resonance introduces mid-frequency harmonics into both PCC voltage and current. In Fig. 13(a), no compensation methods are taken, and the mid-frequency harmonics can be observed in both PSC current and IFC current. Under this resonance condition, the RMS value of IFC current is 1.96 A. In comparison, Fig. 13(b) shows the results with the proposed voltage compensation path enabled. In this case, the mid-frequency components in the IFC current are significantly reduced. And the RMS value of IFC current is 1.45 A, which indicates a 26% reduction compared with the uncompensated case. If the power capacity of IFC is the only constraint to be considered, the applicable power range of the entire grid emulator can be extended to 135% of that without compensation in Scenario 1 (i.e., 1 / (1–26%) ≈ 135%).

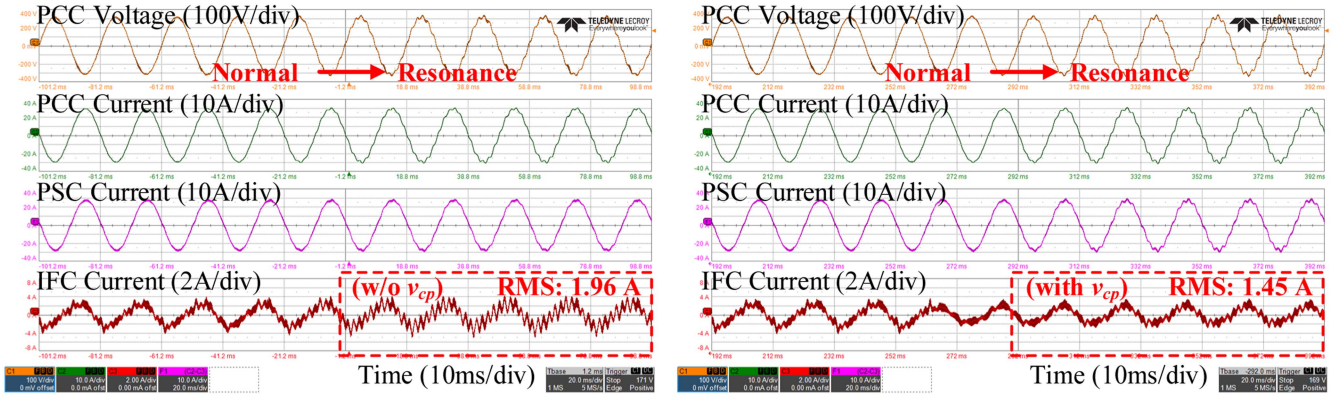

Fig. 13. Experimental waveforms of the grid emulator-CUT system under Scenario 1 (Phase-A). The emulated grid inductance is intentionally increased to trigger a grid-interaction resonance. With the proposed voltage compensation path enabled, the RMS value of IFC current under resonance condition is reduced by 26%, compared with the uncompensated case. (a) Without compensation. (b) With the proposed voltage compensation path enabled.

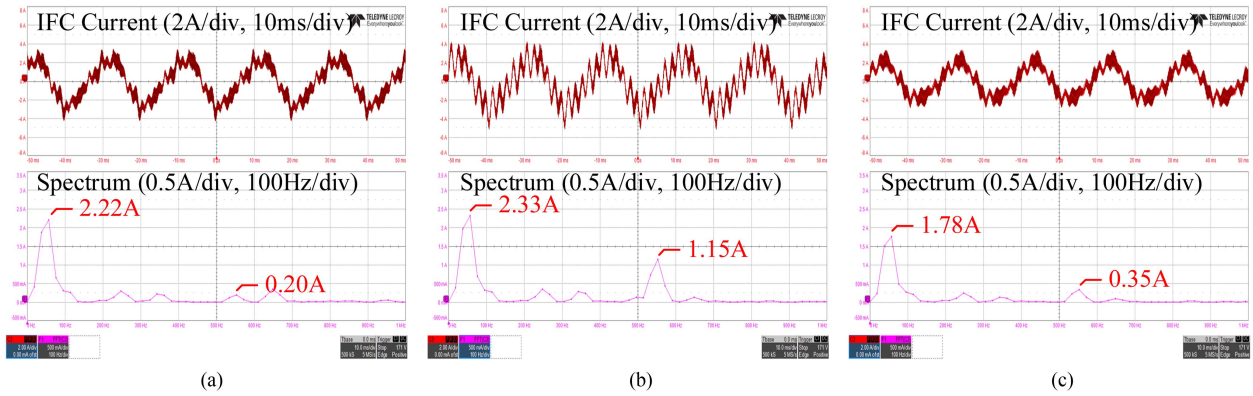

Fig. 14. FFT analysis of the experimental IFC current under Scenario 1 (Phase-A). With the proposed voltage compensation path enabled, the 50 and 550 Hz component of i_{Lv} under resonance condition is reduced by 24% and 70%, respectively, compared with the uncompensated case. (a) Normal. (b) Resonance without compensation. (c) Resonance with v_{cp} added.

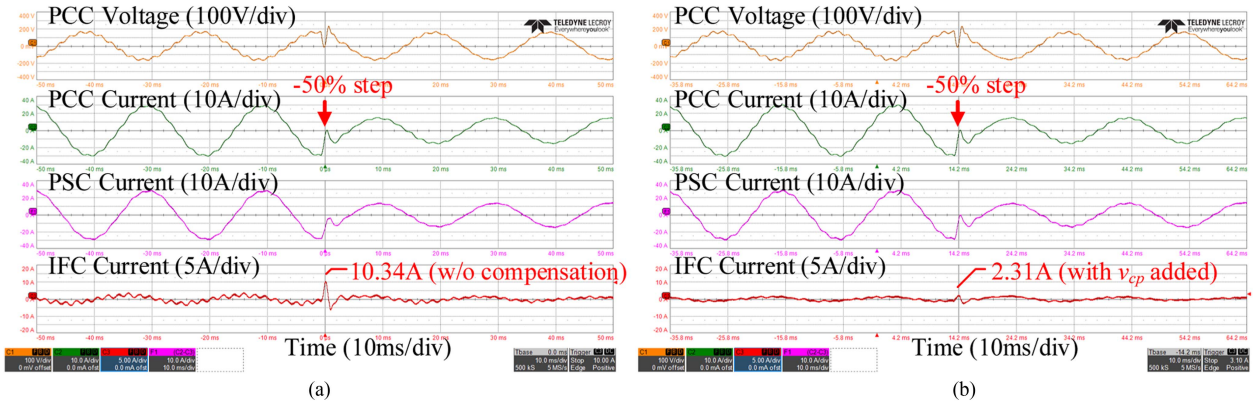

Fig. 15. Experimental waveforms of the grid emulator-CUT system under Scenario 2 (Phase-A). PCC current steps from 28.3 to 14.1 A, and a current surge can be observed in IFC current. With the proposed voltage compensation path enabled, the current surge in i_{Lv} is reduced by 77%, compared with the uncompensated case. (a) Without compensation. (b) With v_{cp} added.

Fig. 14 shows the FFT analysis of the experimental IFC current under Scenario 1 (Phase-A). Under normal conditions, the 50 and 550 Hz components are, respectively, 2.22 and 0.20 A. Under resonance condition without compensation, the 50 and 550 Hz components, respectively, increase to 2.33 and 1.15 A. Under resonance condition with the proposed voltage compensation path enabled, the 50 and 550 Hz components, respectively, reduce to 1.78 and 0.35 A, which indicates 24% and 70% decline compared to that without compensation. The above experimental results prove that the proposed voltage

TABLE II
SUMMARIZATION OF SIMULATION AND EXPERIMENTAL RESULTS

	Scenario	IFC Current	Without compensation	With v_{cp} added	Percentage Reduction
Simulation	1	RMS	1.73 A	1.30 A	25 %
		50 Hz component	1.75 A	1.40 A	20 %
		550 Hz component	1.38 A	0.18 A	87 %
	2	Surge	10.16 A	1.53 A	85 %
Experiment	1	RMS	1.96 A	1.45 A	26 %
		50 Hz component	2.33 A	1.78 A	24 %
		550 Hz component	1.15 A	0.35 A	70 %
	2	Surge	10.34 A	2.31 A	77 %
	3	RMS	1.56 A	0.67 A	57 %

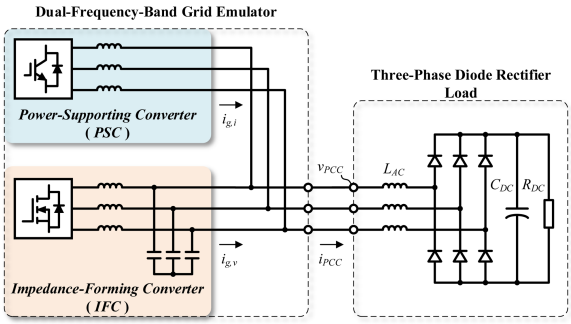

Fig. 16. Experimental topology under nonlinear load condition.

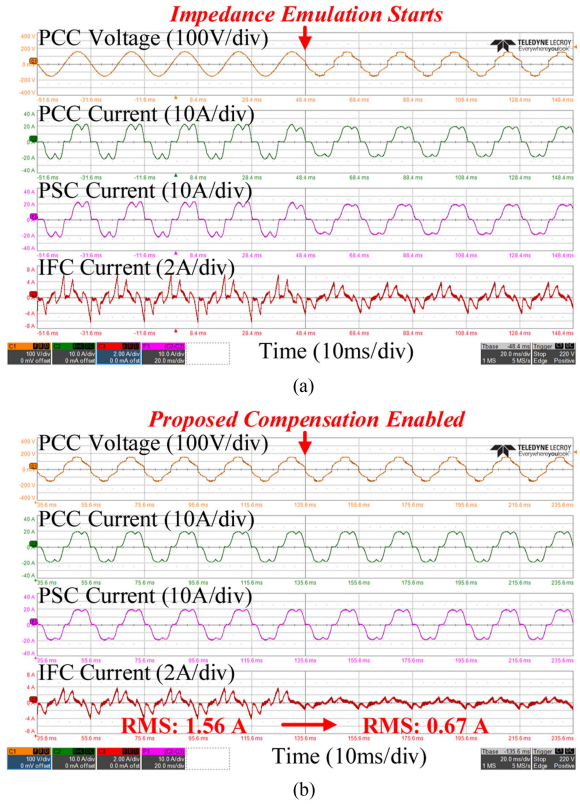

Fig. 17. Experimental waveforms under nonlinear load condition (Phase-A). (a) Emulated grid impedance changes from 0 Ω to s·0.003 Ω, and the current harmonics are reflected on the PCC voltage. (b) Proposed voltage compensation path is enabled, and IFC current clearly decreases.

compensation path is effective at enhancing harmonic power sharing, and it also helps reduce the fundamental component in IFC current to some extent.

Then, the transient power sharing performance of the grid emulator is tested. Fig. 15 shows the experimental waveforms of the grid emulator-CUT system under Scenario 2 (Phase-A). A −50% step is intentionally introduced to the PCC current to check the transient power sharing performance. To avoid triggering over-voltage protection, this experiment is conducted at 400 V dc-link voltage. In Fig. 15(a), no compensation methods are adopted, and a current surge of 10.34 A can be observed in IFC current i_{Lv}. In Fig. 15(b), with the proposed voltage compensation path enabled, the current surge in i_{Lv} is reduced to 2.31 A, which indicates a 77% decline. As can be seen, the proposed voltage compensation path is effective at improving transient power sharing. If the power capacity of IFC is the only constraint to be considered, the applicable power range of the entire grid emulator can be extended to 434% of that without compensation in Scenario 2 (i.e., 1 / (1 – 77%) ≈ 434%).

Finally, the applicability and power sharing performance of the grid emulator is checked under nonlinear load condition. The corresponding experimental topology is given in Fig. 16, where L_{AC}, C_{DC}, and R_{DC}, respectively, denote the ac-side inductor, dc-side capacitor, and dc-side resistor of the nonlinear three-phase diode rectifier load. The load parameters are taken from [51], with $L_{\mathrm{AC}} = 2$ mH, $C_{\mathrm{DC}} = 1100$ μF, and $R_{\mathrm{DC}} = 12$ Ω.

Fig. 17 shows the experimental waveforms under nonlinear load condition. In Fig. 17(a), the emulated grid impedance is initially set to zero, and the PCC voltage is smooth with THD = 2.0%. Since a nonlinear load is connected, a large number of harmonics can be observed in PCC current, PSC current, and IFC current. Then, the emulated grid impedance is increased to s·0.003 Ω, consistent with other experiments. Due to the presence of emulated grid impedance, the current harmonics are reflected on the PCC voltage, resulting in visible voltage distortion. In Fig. 17(b), the emulated grid impedance remains at s·0.003 Ω. Then, the proposed voltage compensation path is enabled, and the IFC current clearly decreases. The RMS values of the IFC current before and after compensation, respectively, are 1.56 and 0.67 A, which indicates a 57% reduction. It can be seen that the dual-frequency-band grid emulator is applicable to

TABLE III
SYSTEM PARAMETERS OF CUT

Symbol	Description	Value
$f_{sw,CUT}$	Switching/Control/Sampling frequency	16 kHz
V_{DC}	DC-link Voltage	750 V
I_{Rated}	Rated output current (RMS)	20 A
Z_{Lf}	Impedance of L_f branch	1.6 mH
Z_{Lg}	Impedance of L_g branch	0.8mH
Z_{Cf}	Impedance of C_f branch	15 μF + 5 Ω
k_p	Proportional gain of PI controller	9.5
k_i	Integral gain of PI controller	10000
f_{LPF}	Cut-off frequency of V-sampling LPF	4000 Hz

TABLE IV
SYSTEM PARAMETERS OF PSC

Symbol	Description	Value
$f_{sw,PSC}$	Switching/Control/Sampling frequency	16 kHz
Z_{Li}	Impedance of L_i branch	1.9 mH
k_{p_PSC}	Proportional gain of current controller	10
k_{i_PSC}	Integral gain of current controller	1000

TABLE V
SYSTEM PARAMETERS OF IFC

Symbol	Description	Value
$f_{sw,IFC}$	Switching/Control/Sampling frequency	160 kHz
V_{DC}	DC-link Voltage	750 V
V_{Rated}	Rated phase voltage (RMS)	220 V
Z_{ref}	Grid impedance reference	s·3.0 mH
f_{Rated}	Fundamental frequency	50 Hz
Z_{Lv}	Impedance of L_v branch	0.1 mH + 2.5 Ω
Z_{Cv}	Impedance of C_v branch	3.3 μF + 1 Ω
k_{i_IFC}	Integral gain of voltage controller	16000

nonlinear loads, and the proposed voltage compensation path remains effective under nonlinear load conditions. The simulation and experimental results are summarized in Table II.

VII. CONCLUSION

In this article, the power sharing of a dual-frequency-band grid emulator is studied. The PSC and IFC inside grid emulator, respectively, are designed to handle the power from CUT and recreate the terminal characteristics of a predefined grid condition. However, if CUT resonates with the emulated weak grid, mid-frequency components would appear and flow through IFC, because PSC is unable to track them. This may lead to overcurrent of IFC, and limit the full use of PSC's power capacity. To address this issue, a voltage compensation path is proposed, and the inductive terminal characteristic of IFC is utilized to synthesize the compensation in a derivative-less way. According to the simulation and experimental results, the proposed voltage compensation path helps reduce the harmonic and transient components of IFC current by over 70%. And the applicable power range of the dual-frequency-band grid emulator can be extended.

APPENDIX

Detailed system parameters of CUT, IFC, and PSC are given in Tables III, IV, and V, respectively.

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