Electrothermal Circuit Modeling and Practical Evaluation of GaN Power Switches for Mega-Hertz Soft-Switching Operation

Mingshuo Zhu, *Student Member, IEEE*, Kerui Li, *Member, IEEE*, Siew-Chong Tan, *Fellow, IEEE*, and Shu Yuen Ron Hui, *Fellow, IEEE*

***Abstract*—This article investigates the switching performance and electrothermal behavior of gallium nitride (GaN) high-electron-mobility transistors (HEMTs) in megahertz (MHz) soft-switching operations, focusing on conversion efficiency, thermal stability, and electromagnetic interference. Contrary to the datasheets of GaN HEMTs manufacturers that highlight the reverse-conducting characteristics of the devices, this study finds that the performance of GaN HEMTs degrades significantly at MHz operations due to elevated reverse conduction losses, high-frequency oscillations, and thermal instability from self-heating. Totem-pole GaN inverters with and without antiparallel Schottky diodes are compared practically and with the help of an electrothermal circuit model for operations at 1, 6.78, and 13.56 MHz. Electrothermal circuit modeling and experimental results demonstrate that GaN switches with antiparallel Schottky diodes can reduce dead-time switching power losses by 85% and improve overall converter efficiency by 2.7% –6.9% in prototypes of 24–29 W. This approach also mitigates thermal runaway risks by lowering the junction temperature of GaN HEMTs, therefore increasing thermal stability. Furthermore, the junction capacitance of the diodes can dampen high-frequency dv/dt transients and reduce electromagnetic emission. The experimental results show reductions of 24.41 dBm in magnetic field emissions and 26.57 dBm in electric field emissions. These findings challenge the prevailing industry assumption that external antiparallel diodes are unnecessary for GaN HEMTs, providing a validated design framework for MHz-range applications.**

***Index Terms*—Efficiency, gallium nitride (GaN) high-electron-mobility transistors (HEMTs), megahertz (MHz) power conversion, power semiconductor, thermal stability.**

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Mingshuo Zhu, Kerui Li, and Siew-Chong Tan are with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong (e-mail: m.zhu@my.cityu.edu.hk; kerui.li@cityu.edu.hk; siewctan@cityu.edu.hk).

Shu Yuen Ron Hui is with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong, and also with the Department of Electrical and Electronics Engineering, Imperial College London, SW7 2AZ London, U.K. (e-mail: eeronhui@cityu.edu.hk).

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I. Introduction

Advancements in gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have enhanced their intrinsic capability to conduct current in the reverse direction without relying on a traditional body diode—a feature attributed to their lateral device structure and two-dimensional electron gas (2-DEG) channel [1], [2]. The fact that GaN HEMT lacks reverse recovery charge also enables efficient operation during the reverse conduction state, despite a higher reverse voltage drop [3]. Therefore, industrial proponents argue that this characteristic eliminates the need for external antiparallel diodes in applications such as wireless power transfer or energy storage systems, particularly at switching frequencies below 1 MHz. For example, most GaN-based converter evaluation boards developed by EPC do not have freewheeling diodes. Infineon & GaN Systems [4], Texas Instruments [5] and Innoscience [6] claim that antiparallel diodes are not required for GaN Systems transistors as is the case for insulated gate bipolar transistors to achieve reverse conduction performance.

As the switching frequency is being extended into the megahertz (MHz) regime in emerging applications, the industrial practice of not using body diodes in GaN switches requires re-examination for several reasons.

1) Under zero voltage switching (ZVS) conditions, the dead time of GaN HEMTs operating at MHz frequencies occupies a higher proportion of the switching cycle when compared to low-frequency operation [7]. This results in a proportional increase in reverse conduction losses [8].
2) Repetitive switching leads to cumulative switching losses, which intensify self-heating effects. When combined with the positive temperature coefficient of its on-state resistance [9], [10], this significantly heightens the risk of localized hot spots. This, in turn, increases the likelihood of thermal runaway or catastrophic failure during sustained high-frequency operation, especially in GaN-based devices with high power densities exceeding 100 W/cm^2 [11], [12], [13].
3) The absence of a low-resistance anti-parallel body diode in GaN HEMTs limits their ability to clamp voltage spikes induced by parasitic inductance during switching transitions. This deficiency exacerbates high-frequency oscillations and elevates electromagnetic interference (EMI),

particularly in MHz applications where excessively fast switching speeds generate high dv/dt, further aggravating voltage overshoot and EMI generation [14], [15], [16].

These issues, often negligible at lower frequencies, become critical bottlenecks for MHz converters aiming for ultra-high efficiency and power density.

Without using external antiparallel diodes, existing industrial practice relies on the third-quadrant operation of GaN HEMTs to maintain current flow during dead-time intervals [17], [18]. Some works proposed minimizing reverse conduction losses through optimized dead-time control [19], [20], [21], [22]. However, this strategy faces limitations in MHz power conversion systems. Under ZVS conditions, the adjustable range of dead time becomes extremely narrow. Besides, the propagation delays and timing jitter in gate-drive circuits, which are negligible at lower frequencies, become comparable to the dead-time duration itself at MHz operation [23], [24]. This uncertainty often necessitates conservative dead-time margins, inadvertently prolonging reverse conduction intervals and negating the benefits of dead-time optimization [25]. Consequently, for high-frequency applications, reverse conduction losses in GaN HEMTs typically constitute a non-negligible portion of total system losses, significantly constraining efficiency improvements [26], [27].

In summary, the lack of systematic evaluation of GaN HEMTs in MHz applications has led to inherent flaws in mainstream converter designs for high-frequency operation. To address these limitations, this study compares the practical performance of totem-pole GaN-HEMT inverters ***with*** and ***without*** antiparallel Schottky diodes for switching operations at 1 to 13.56 MHz. Due to the highly compact layout of MHz circuit, some internal variables such as switch current and power losses cannot be measured directly. A detailed electrothermal circuit model is developed for the GaN switch to assist the comparative study. The model parameters are empirically derived from the external voltage and current measurements of the device using a similar approach that is adopted in [28]. An analysis of various operating states within a switch's cycle reveals that the low forward-voltage and fast recovery characteristics of Schottky diodes can significantly enhance converter performance in terms of power loss, thermal behavior, and EMI at MHz operations. This discovery fundamentally challenges conventional industrial recommendations and has not been previously documented in the literature.

II. Operating Model and Power Loss Analysis of GaN HEMTs

A. Equivalent Circuit and Operating State Analysis

The typical I-V characteristics and switching trajectories of the GaN HEMTs are plotted in Fig. 1. When a gate signal is applied to the GaN HEMT while it is in the off-state, the gate-source voltage v_{gs} does not change abruptly but instead exhibits a nonlinear ramp-up behavior caused by the junction capacitance. This delayed response creates multiple intermediate conduction states as v_{gs} progressively exceeds the specific threshold value, resulting in a v_{gs}-dependent current modulation, as represented mathematically in (1), where g_m is transconductance of the GaN HEMTs, and V_{th} is the threshold voltage. The drain current stabilizes only after v_{gs} reaches its steady-state value, where the fully turned-ON device current is determined by the input voltage and load impedance. Symmetric transient dynamics operating in reversal are observed during turn-OFF

$$i_{ds} = g_m(v_{gs} - V_{th}). \quad (1)$$

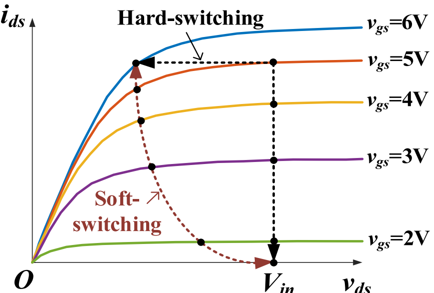

Fig. 1. Typical I-V characteristics and switching trajectories of the GaN HEMTs.

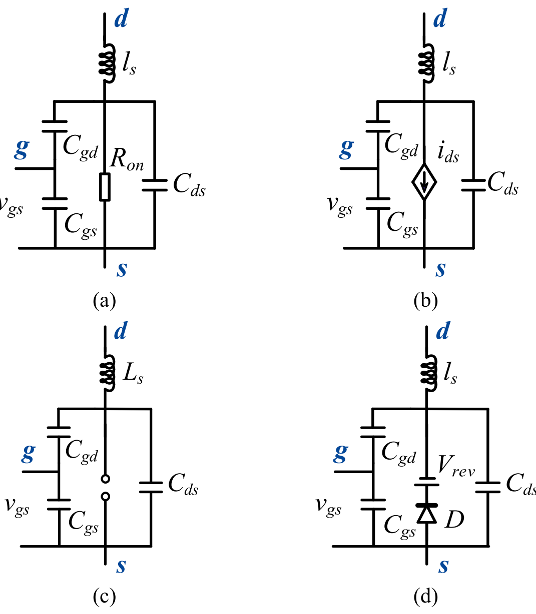

Fig. 2. Simplified equivalent circuit of GaN HEMTs. (a) Steady on-state conduction. (b) v_{gs}-modulated transition period. (c) Complete off-state blocking. (d) Reverse conduction.

The switching trajectory analysis reveals three sequential operational phases:

1) steady on-state conduction,
2) v_{gs}-modulated transition period, and
3) complete off-state blocking.

Besides, GaN HEMTs can also operate in reverse-conduction mode during freewheeling scenarios, which is considered phase 4). Based on their operational characteristics, four dedicated equivalent circuit models are employed to accurately represent the device behavior within each respective phase, as shown in Fig. 2.

The inductor L_s represents the equivalent parasitic inductance introduced by the leads and terminals of the power switch; R_{on}

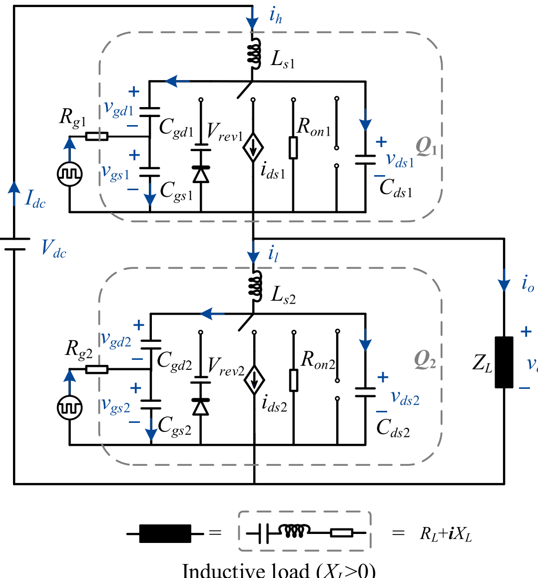

Fig. 3. Equivalent circuit structure of the totem-pole inverter.

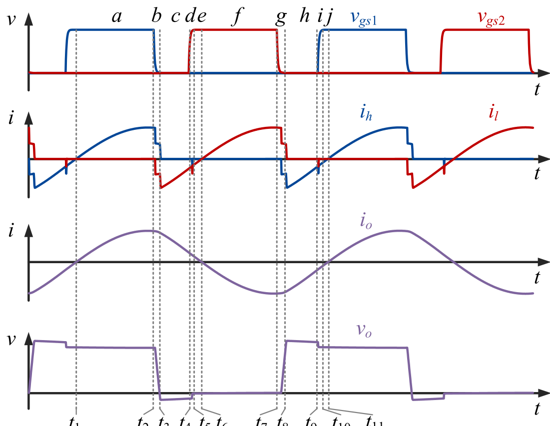

Fig. 4. Switching sequence and waveform of the totem-pole inverter.

represents the on-state resistance and accounts for the forward conduction loss; $C_{\rm ds}$, $C_{\rm gs}$, and $C_{\rm gd}$ are the junction capacitances between the drain and the source, the gate and the source, and the gate and the drain, respectively; the diode D represents the reverse conduction capability of the GaN HEMT, and $V_{\rm rev}$ is the reverse conduction voltage drop.

A totem-pole GaN inverter topology is considered in this study. By replacing each GaN HEMT with the simplified equivalent circuits given in Fig. 2, the structure of the totem-pole inverter can equivalently be derived as depicted in Fig. 3. When the totem-pole inverter drives an inductive load, the switching sequence of the transistors, the voltage, and current waveforms are illustrated in Fig. 4. Based on the switching states of the two power transistors (Q_1 and Q_2), the totem-pole inverter operates in ten distinct modes, labeled as stages *a* through *j* within one operational cycle. Fig. 5 illustrates the current paths for each operational mode.

Stage a: During $t_1 < t \leq t_2$, GaN HEMT Q_1 is conducting while GaN HEMT Q_2 is turned OFF, allowing the current i_o to

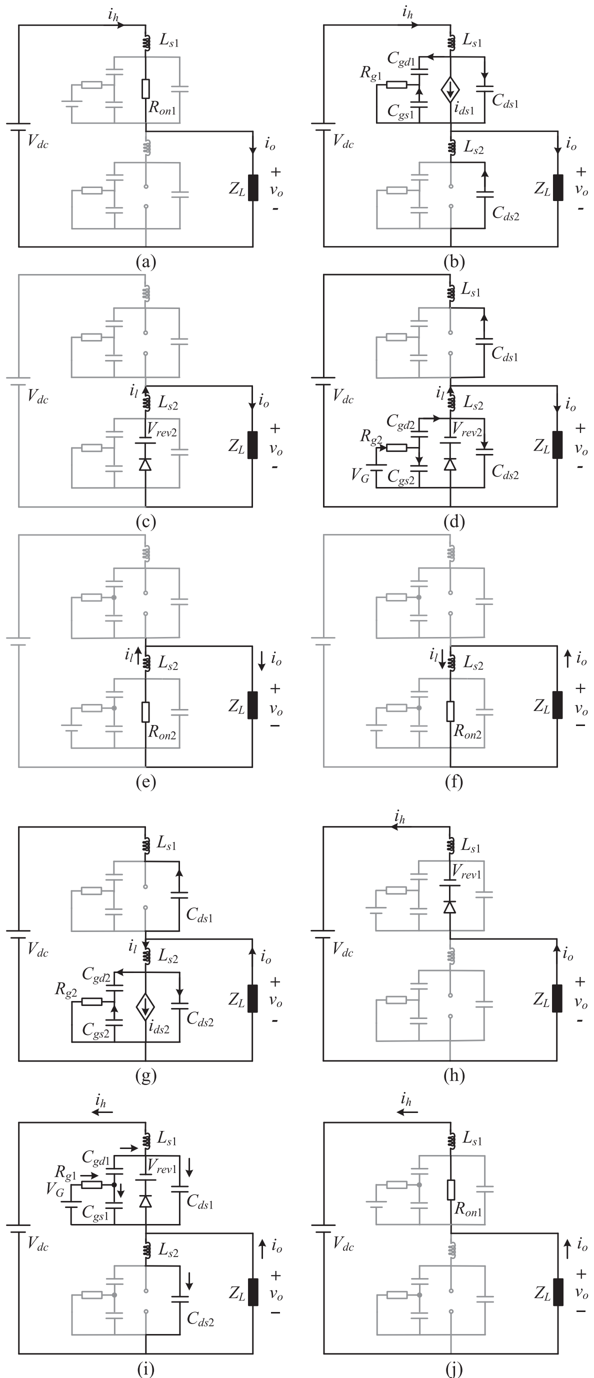

Fig. 5. Equivalent circuits and current paths from stages *a* through *j* within one operational cycle. The arrows indicate the actual current directions in each stage.

flow from the power supply $V_{\rm dc}$ through Q_1 to the inductive load $Z_L = R_L + \boldsymbol{i}X_L$ ($X_L > 0$).

Stage b: For $t_2 < t \leq t_3$, the gate driving signal of GaN HEMT Q_1 is switched from high to low. Gate current i_{g1} discharges through the input capacitance $C_{\rm iss}$ ($C_{\rm iss} = C_{\rm gs} + C_{\rm gd}$), causing $v_{\rm gs1}$ to start decreasing. During this stage, Q_1 operates in the $v_{\rm gs}$-modulated transition mode, and the gradual reduction in $v_{\rm gs1}$ leads to a corresponding decrease in $i_{\rm ds1}$. When $v_{\rm gs1}$ falls below the threshold voltage, Q_1 turns OFF. Subsequently, i_h

begins to charge C_{ds1}, resulting in a gradual increase in v_{ds1}. Simultaneously, v_{o} starts to decrease, and a discharge current flows through C_{ds2}.

Stage c: Between $t_3 < t \leq t_4$, both Q_1 and Q_2 are turned OFF, resulting in a dead-time period. During this phase, Q_2 conducts in reverse mode to provide freewheeling current to the load. Due to the presence of V_{rev2}, the load voltage remains nonzero, and a reverse voltage develops across the drain-source junction capacitance C_{ds2}.

Stage d: During $t_4 < t \leq t_5$, a positive gate driving signal is applied to Q_2, and the input capacitances C_{gs2} and C_{gd2} begin charging, leading to an increase in v_{gs2}. When v_{gs2} exceeds the threshold voltage, the channel of Q_2 gradually conducts current, initiating the discharge of the negative voltage across C_{ds2}. Consequently, the negative voltage of v_o gradually decreases and eventually disappears. Simultaneously, the voltage across v_{ds1} decreases from $V_{\mathrm{dc}} + V_{\mathrm{rev2}}$ to V_{dc}, releasing a discharge current in the process.

It is important to note that, due to the inductive load current, Q_2 remains in reverse conduction mode, when a positive gate driving signal is applied.

Stage e: For $t_5 < t \leq t_6$, Q_2 continues to operate in reverse conduction mode to sustain the load current. But at this point, v_{gs2} exceeds the threshold voltage, and Q_2 is fully turned ON. Thus, the reverse current flows through the conducting channel (R_{on} path) of the GaN HEMT.

Stage f: Between $t_6 < t \leq t_7$, the load current reverses, and Q_2 conducts forward, completing the loop with the inductive load.

Stage g: During $t_7 < t \leq t_8$, the gate of the GaN HEMT Q_2 is switched from high to low. Subsequently, i_1 begins charging C_{ds2}, causing v_o to rise gradually.

Stage h: For $t_8 < t \leq t_9$, this period represents the dead-time for the negative half-cycle. Q_1 conducts in reverse to sustain the load current. Due to the reverse voltage V_{rev1} on Q_1, the load voltage slightly exceeds the supply voltage.

Stage i: During $t_9 < t \leq t_{10}$, a gate signal is applied to Q_1. Similar to the process in Stage d, the channel of Q_1 opens, initiating the discharge of the negative voltage across C_{ds1}. The voltage v_o gradually decreases from $V_{\mathrm{dc}} + V_{\mathrm{rev1}}$ to V_{dc}. Q_1 is compelled to remain in reverse conduction mode to sustain the negative output current.

Stage j: In the interval $t_{10} < t \leq t_{11}$, the load current forces Q_1 to continue reverse conduction. As Q_1 is fully turned ON, the reverse current flows through the conducting channel.

Experimental measurements of the drain-source voltage v_{ds} waveform across GaN HEMTs (EPC2012C) and the output current i_o in a totem-pole inverter operating at a switching frequency of 6.78 MHz were captured over switching cycles to extract parameters for the model in Fig. 2. Using the approach in [28] and by considering the typical device parameters in the datasheet, the model parameters are repeatedly searched with the MATLAB optimization toolbox until the errors between the measured and simulated waveforms are within a tight tolerance. The parameter fitting results and the comparison between simulated and experimental waveforms are summarized in Table I and shown in Fig. 6, respectively. The results demonstrate that the proposed model accurately characterizes the dynamic behavior of GaN HEMTs across all transient stages during switching operation, including turn-ON, conduction, turn-OFF, and dead-time intervals.

TABLE I
EQUIVALENT CIRCUIT PARAMETERS EXTRACTION RESULTS

Parameters	Values
L_s	2.2137 nH
C_{gd}	0.6 pF
C_{gs}	100 pF
C_{ds}	127 pF
R_{on}	0.4 Ω
V_{rev}	2.3 V

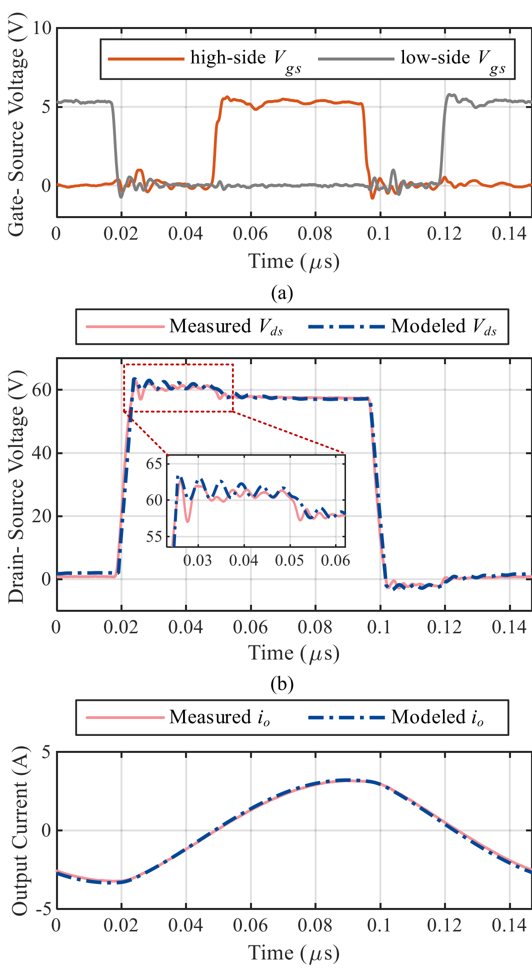

Fig. 6. Comparison between experimental and model waveforms. (a) Input gate-source signal. (b) Output drain-source waveforms. (c) Output current waveforms.

B. Power Loss Analysis

1) Dead-Time Conduction Loss: During the commutation process of the inverter bridge arm, the reverse current in the dead-time interval requires a freewheeling path. When the GaN HEMT conducts in reverse direction to provide freewheeling current for the load, reverse conduction losses are incurred during the dead-time period. Within a single switching cycle, there are two dead-time intervals, denoted as t_{d1} and t_{d2}. The losses

generated by the GaN HEMT during the dead-time intervals can be expressed as

$$P_{\text{dead-time}} = \frac{1}{T}\int_{t_3}^{t_4} v_{\text{rev2}} i_o dt + \frac{1}{T}\int_{t_8}^{t_9} v_{\text{rev1}} (-i_o)\, dt. \quad (2)$$

The reverse conduction voltage of GaN HEMTs with identical models and production batches shows minimal variation overall. In the totem-pole circuit, the operation of the power switches on the high-side and low-side is symmetrical. Consequently, the dead-time intervals on both sides are typically designed to be equal. Under these conditions, (2) can be simplified as

$$P_{\text{dead-time}} = 2v_{\text{rev}} \frac{1}{T}\int_{t_{rs}}^{t_{rs}+t_{\text{rev}}} i_o(t)\, dt \quad (3)$$

where t_{rs} represents the reverse conduction start time, and t_{rev} denotes the duration of reverse conduction.

As derived from (3), the magnitude of dead-time losses is determined by the reverse conduction time and reverse conduction voltage. Although GaN HEMTs have bidirectional conduction potential, their reverse conduction voltage is relatively high. For certain enhancement-mode GaN HEMTs, the reverse conduction voltage v_{rev} can reach 3–4 V. This could result in significant dead-time conduction losses caused by freewheeling current during the third quadrant operation.

For MHz operations, the adjustable range of the dead-time is extremely narrow under ZVS conditions, making it challenging to effectively reduce dead-time losses by shortening the reverse conduction time. However, Schottky diodes exhibit a forward voltage drop (V_F) typically ranging from 0.3 to 0.5 V, which is lower than that of silicon-based diodes (approximately 0.7–1.2 V). When an antiparallel Schottky diode is added to the GaN HEMT, its low forward-voltage-drop and conduction resistance can ensure that the load current flows through the Schottky diode (instead of the GaN HEMT) during modes *c*, *e*, *h*, and *j*. Moreover, Schottky diodes, which operate based on metal-semiconductor contact, do not experience minority carrier storage effects and exhibit an almost negligible reverse recovery charge. These characteristics enable antiparallel Schottky diodes to effectively reduce reverse conduction losses during freewheeling phases without significantly impacting the switching speed of the power switches.

2) On-State Conduction Loss: During the forward conduction of GaN HEMTs, current flowing through the on-state resistance leads to conduction losses. Similarly, the conduction loss over one cycle can be calculated using the following formula:

$$P_{\text{on}} = \frac{1}{T}\int_{t_1}^{t_2} {i_o}^2 R_{\text{on1}} dt + \frac{1}{T}\int_{t_6}^{t_7} {i_o}^2 R_{\text{on2}} dt. \quad (4)$$

When an antiparallel Schottky diode is connected across the GaN HEMT, the junction capacitance of the diode affects the load of the original circuit. This changes the equivalent load impedance and introduces a phase shift in the load current. The equivalent load impedance $Z_{L\text{eq}}$, after adding the diode's junction capacitance C_j, is increased

$$|Z_{L\text{eq}}| = \left| \frac{1}{\frac{1}{Z_L} + i\omega C_j} \right| > |Z_L|. \quad (5)$$

This inequality holds as long as the following condition is satisfied:

$$\frac{2X_L}{\omega (R^2 + X_L^2)} > C_j. \quad (6)$$

Since the junction capacitance of a Schottky diode is relatively small, typically only a few tens of pico-Farads, this condition can be easily met. The junction capacitance of the antiparallel Schottky diode introduces a slight phase shift to the load network. This phase shift reshapes the switch current waveform, reducing its rms value during the on-state period and thereby lowering the conduction loss, while the output power is maintained constant.

3) Turn-Off Loss: During turn-off, the GaN HEMTs experience hard-switching turn-off. Accurately calculating the turn-off loss would require acquiring the transient data of the current flowing solely through the channel and the voltage across the power switch during the turn-off process [29]. However, this approach is impractical in real-world applications. This is because the switching current measurable in an actual circuit is the sum of the current through the channel and the current through its output capacitance C_{oss} ($C_{\text{oss}} = C_{\text{gd}} + C_{\text{sd}}$). Using this total current together with the transient voltage waveform would lead to an overestimation of the switching loss.

Therefore, to achieve a more practical and accurate evaluation, the turn-off loss of the GaN HEMTs in this work is calculated using (3), (4), and the following indirect method:

$$P_{\text{turn - off}} = P_{\text{total}} - P_{\text{on}} - P_{\text{dead-time}}. \quad (7)$$

The introduction of antiparallel Schottky diodes brings additional junction capacitance in parallel with the GaN HEMT's output capacitance C_{oss}, which extends the turn-OFF duration. However, according to analysis in [29] and [30], this increase in C_{oss} would ultimately reduce the turn-OFF loss of the GaN HEMTs.

4) Switching Trajectories of the Devices: A simulation model of the inverter circuit is constructed using the GaN HEMTs (EPC2012C) and Schottky diodes (V10P20) with parameters extracted from their respective datasheets and tabulated in Table II. Fig. 7 shows the switching trajectories of the GaN

TABLE II
SIMULATION MODEL PARAMETERS

Components	Parameters	Values
Circuit configuration	DC input voltage V_{dc}	60 V
	RMS value of output current I_{RMS}	3.54 A
EPC2012C	Duty cycle D	0.4
	On-state resistance R_{on}	100mΩ
	Threshold gate voltage V_{th}	1.4 V
	Transconductance g_m	150
	Gate-source capacitance C_{gs}	100 pF
	Gate-drain capacitance C_{gd}	0.8 pF
	Drain-source capacitance C_{ds}	70 pF
	Reverse conduction voltage V_{rev}	3 V
V10P20	Forward Voltage V_f	0.7 V
	Junction capacitance C_j	90 pF

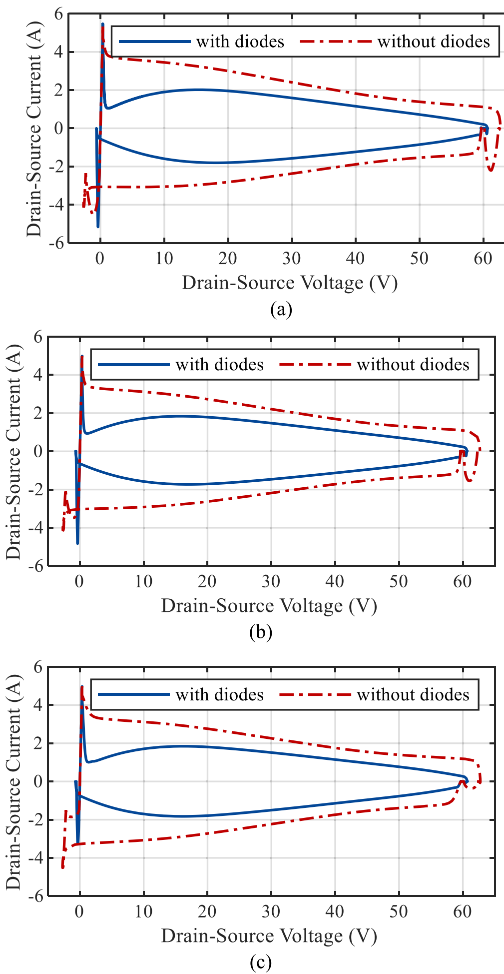

Fig. 7. Switching trajectories of the GaN HEMTs with and without antiparallel diodes in one cycle. (a) 1 MHz operating frequency. (b) 6.78 MHz operating frequency. (c) 13.56 MHz operating frequency.

TABLE III
POWER DISTRIBUTION OF GAN HEMTS AND SCHOTTKY DIODES FROM SIMULATION

Frequency (MHz)	Loss type	Without diodes		With diodes	
		Value (W)	**%**	**Value (W)**	**%**
1	Turn-on	0	0	0	0
	Turn-off	0.0128	0.72	0.0094	1.26
	On-state	0.5532	31.23	0.5297	71.07
	Dead time	1.2054	68.05	0.2062*	27.67
	Total	**1.7714**	100	**0.7453**	100
6.78	Turn-on	0	0	0	0
	Turn-off	0.0972	6.18	0.0686	9.59
	On-state	0.5401	34.32	0.5145	71.97
	Dead time	0.9361	59.50	0.1318*	18.44
	Total	**1.5733**	100	**0.7149**	100
13.56	Turn-on	0	0	0	0
	Turn-off	0.2154	14.11	0.1120	16.51
	On-state	0.6098	39.94	0.5129	75.62
	Dead time	0.7014	45.95	0.0534*	7.87
	Total	**1.5266**	100	**0.6783**	100

(Note: * The dead time loss is from the Schottky diodes.)

TABLE IV
EXPERIMENTAL PARAMETER SETTINGS

Parameters		**Values**
DC input voltage V_{dc}		60 V
DC bus capacitor C_{dc}		0.3 μF
Gate-source voltage V_{gs}		5 V
1 MHz	Dead-time intervals	0.2 μs
	Circuit parameters for the inductive load	4.29Ω, 3.8μH, 9 nF
6.78 MHz	Dead-time intervals	0.0369 μs
	Circuit parameters for the inductive load	4.31Ω, 0.81μH, 0.82 nF
13.56 MHz	Dead-time intervals	0.026 μs
	Circuit parameters the inductive load	4.27Ω, 0.24μH, 0.8 nF

HEMTs with and without the anti-parallel diodes in one cycle of 1, 6.78, and 13.56 MHz. The voltage and current stresses on the GaN HEMTs are reduced after adding Schottky diodes. Comparative analysis of loss distribution within one switching cycle was performed for both pre- and postparallel diode configurations. The power losses in GaN HEMTs and Schottky diodes are listed in Table III.

The simulation results demonstrate two critical improvements with the use of the antiparallel diodes.

1) The total switching losses in GaN HEMTs exhibit a notable reduction, primarily attributed to the transfer of dead-time losses from GaN HEMTs to Schottky diodes.
2) The combined losses of the antiparallel diode and GaN HEMTs become lower than the standalone GaN device losses prior to diode implementation.

To more intuitively demonstrate the reduction in switching losses during the dead time by experimentally observing voltage and current waveforms, current shunts are used to obtain the current waveforms of the power switches. The experimental measurements were captured under 1 MHz operating conditions described in Table IV. The voltage and current waveforms of the power switches are shown in Fig. 8, in which i_{ds} and i_d represent the current flow through the GaN HEMT and the Schottky diode, respectively.

As shown in the highlighted region of Fig. 8, the introduction of the Schottky diode redirects the reverse conduction current from the GaN HEMT to the Schottky diode. Consequently, the dead-time loss is transferred from the GaN HEMT to the Schottky diode. Although the reverse currents through both devices are nearly identical, the Schottky diode's lower forward voltage drop reduces the reverse conduction voltage, thereby decreasing dead-time losses.

Furthermore, the switching trajectory depicted in Fig. 9 demonstrates a reduction in electrical stress experienced by the GaN HEMT, which is consistent with the simulation results shown in Fig. 7. The discrepancy between the simulated and experimental switching trajectories is attributed to a combination of measurement limitations and the nonideal behavior of semiconductor components. Primarily, the experimental setup introduces a non-negligible parasitic inductance (approximately 0.09 μH) from the current shunt leads. This parasitic element prolongs the switching transients and excites excessive oscillations in the switching loop that is not present in the idealized

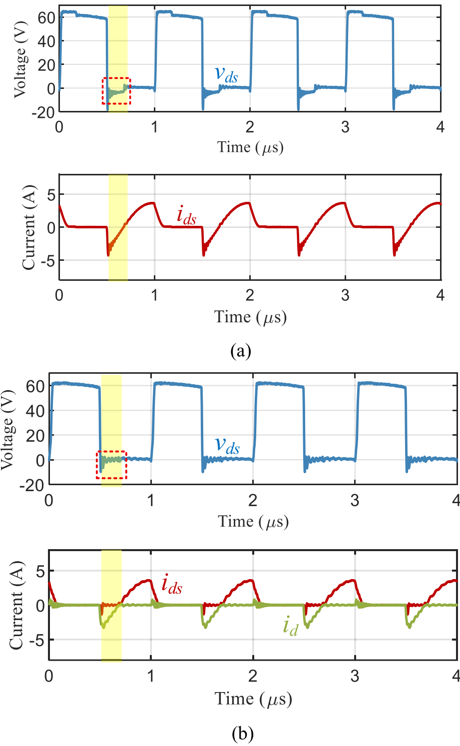

Fig. 8. Experimentally captured switching waveform of the inverter at 1 MHz. (a) Without Schottky diodes. (b) With Schottky diodes.

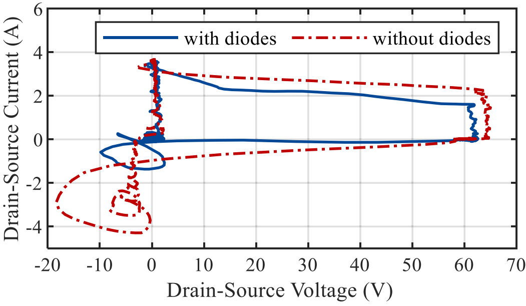

Fig. 9. Experimentally captured switching trajectories of the GaN HEMTs.

simulation environment. This effect is particularly pronounced at higher frequencies (e.g., 6.78 MHz and 13.56 MHz). Thus, some discrepancies between the simulated and measured switching current waveforms are expected. Nevertheless, the results obtained at 1 MHz are sufficiently representative to capture the general behavior of the system.

Furthermore, the conventional compact models used in simulation cannot fully capture the energy dissipation associated with the nonlinear $C_{\rm oss}$ of the devices. As discussed in [31] for GaN HEMTs and in [32] and [33] for Schottky diodes, the $C_{\rm oss}$ of these components exhibits hysteresis. This could lead to a situation where the combined GaN-diode configuration exhibits a smaller effective Coss hysteresis loss than what would be expected from a simple simulation of individual components.

Despite the observed discrepancy, this synergistic loss reduction mechanism effectively enhances the overall converter efficiency under MHz operating conditions. The simulation and

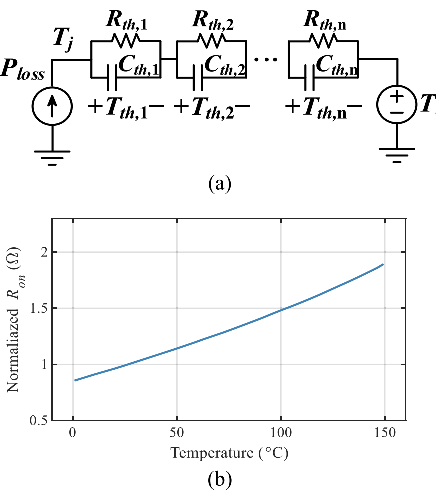

Fig. 10. (a) nth-order thermal model for GaN HEMTs. (b) Typical normalized on-state resistance as a function of junction temperature.

experimental results agree with the theoretical analysis presented above, confirming the effectiveness of the antiparallel Schottky diode configuration in the reduction of power switching losses.

III. Electrothermal Analysis of GaN HEMTs

A. Thermal Model of GaN HEMTs

The junction temperature T_j of GaN HEMTs can be determined through an nth-order foster-type thermal network model as shown in Fig. 10(a), where $P_{\rm loss}$ represents the total power loss in the GaN HEMT; $R_{{\rm th},i}$ and $C_{{\rm th},i}$ denote the thermal resistance and thermal capacitance parameters respectively, which can be obtainable from device datasheets; T_a represents the ambient temperature. The mathematical expression of the n-order foster-type thermal network model is written as

$$\begin{cases} \frac{dT_{\rm th,1}}{dt} = \frac{P_{\rm loss}}{C_{\rm th,1}} - \frac{T_{\rm th,1}}{R_{\rm th,1}C_{\rm th,1}} \\ \frac{dT_{\rm th,2}}{dt} = \frac{P_{\rm loss}}{C_{\rm th,2}} - \frac{T_{\rm th,2}}{R_{\rm th,2}C_{\rm th,2}} \\ \vdots \\ \frac{dT_{{\rm th},n}}{dt} = \frac{P_{\rm loss}}{C_{{\rm th},n}} - \frac{T_{{\rm th},n}}{R_{{\rm th},n}C_{{\rm th},n}} \end{cases}$$
$$T_j = T_a + T_{\rm th,1} + T_{\rm th,2} \cdots + T_{{\rm th},n}. \tag{8}$$

Previous studies have identified temperature-dependent variations in key GaN HEMT electrical parameters, including g_m, $V_{\rm th}$, $R_{\rm on}$, etc. [34], [35]. For example, $R_{\rm on}$ exhibits an approximately linear positive correlation with junction temperature as depicted in Fig. 10(b). This interdependency creates a feedback loop between the electrical model and the thermal model. The junction temperature caused by power consumption will alter certain electrical parameters and characteristics of GaN HEMTs, which in turn affects the power loss and junction temperature through the electrothermal coupling mechanism (see Fig. 11). $V_{\rm th}$ and g_m also have temperature dependence. Generally, $V_{\rm th}$ and g_m both decrease with increasing T_j due to reduced carrier mobility and velocity saturation effects.

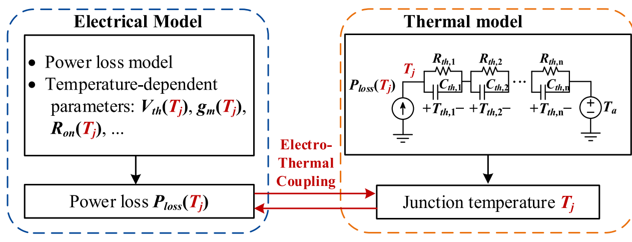

Fig. 11. Electrothermal coupling mechanism of GaN HEMTs.

B. Electrothermal Coupling Analysis

Fig. 11 shows the electrothermal coupling mechanism of GaN HEMTs. Specifically, the temperature-dependent circuit parameters and loss model are used to account for electrothermal coupling analysis. The interaction between electrical parameters and temperature forms a closed-loop system.

1) *Initial Operation:* The device operates at a certain T_j (ambient or previous state), with corresponding $R_{on}(T_j)$,$V_{th}(T_j)$ and $g_m(T_j)$.
2) *Power Dissipation:* Current flow and switching events cause P_{loss}, based on the current R_{on}, V_{th}, g_m, and circuit conditions.
3) *Temperature Rise:* This P_{loss} heats the device, leading to an increase in junction temperature (ΔT_j). The thermal impedance path determines the magnitude and dynamics of this rise.
4) *Parameter Shift:* The increased T_j causes: V_{th} to decrease, g_m to decrease, and R_{on} to increase.
5) *Impact on Subsequent Losses* (The Coupling): Lower V_{th} and g_m can lead to reduced turn-ON delay and slower switching speed. This typically increases switching losses because switching losses are proportional to the overlap time of voltage and current during transitions. Higher R_{on} directly increases conduction losses for any given drain current.
   Under ZVS conditions, switching loss contributes minimally to the total loss [36], [37], so the impact of changed junction temperature on switching loss is not obvious.
6) *Feedback:* The increased losses - lead to further power dissipation, driving T_j even higher. This creates a positive feedback loop that can lead to thermal runaway if not properly managed, especially under high-stress conditions.

The GS61004B GaN HEMTs are taken as an example to illustrate the electrothermal coupling analysis. The thermal network parameters can be determined based on the datasheet and cooling experiments [38]. The validity of the model during switching operation is more complex due to the presence of switching loss and dead time loss. The operating waveforms of a 60 V totem-pole inverter at 1 MHz are captured, as illustrated in Fig. 12.

The measured input and output power are 31.2 W and 28.99 W, respectively. The power loss associated with each GaN HEMT is therefore calculated as (31.2 W$-$28.99 W)/2 = 1.105 W. The on-state loss, derived from the operating waveform at this operating point is 0.1514 W. As a result, the combined turn-OFF loss and dead-time loss are 0.9536 W.

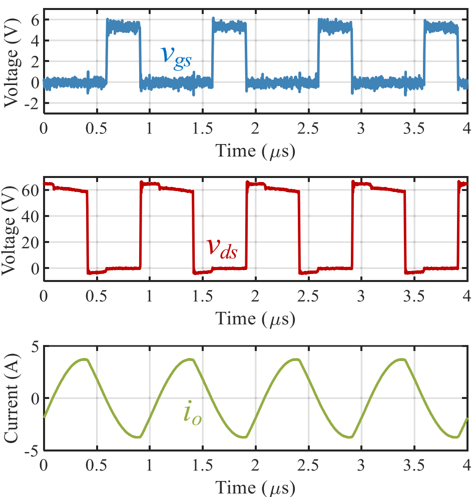

Fig. 12. Waveforms of the inverter for electrothermal coupling analysis.

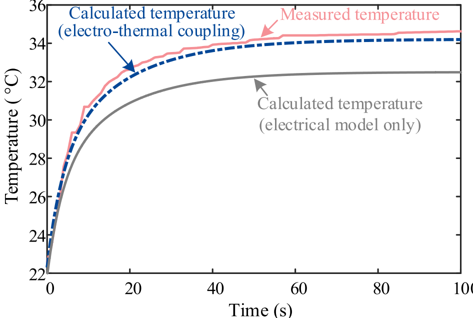

Fig. 13. Dynamic operating temperature calculated results.

To simplify the evaluation of power losses during switching, it is assumed that the turn-OFF and dead-time losses remain constant, given their weak temperature dependence under ZVS operation. Consequently, the total power loss of a GaN HEMT during switching operation can be expressed as

$$P_{\text{loss}} = I_{\text{on}}^2 \times R_{\text{on}}\left(T_j\right) + P_{\text{dead_time}} + P_{\text{turn-off}} \tag{9}$$

where I_{on} represents the rms value of the forward conduction current through the GaN HEMT. The measured value of I_{on} in this test is 2.84 A.

After characterizing the power loss during the switching operation, the electrothermal coupling model is validated. During switching operations, the inverter utilizes forced air cooling for thermal management. This cooling configuration is modeled by a second-order RC thermal network [39]. The parameters of the thermal network are: R_{hs1} = 7.32 °C/W, C_{hs1} = 0.61 J/°C, R_{hs2} = 3.21 °C/W, C_{hs2} = 4.38 J/°C.

A Type-K thermocouple (CMT-LL-T-K-24-ZX) is affixed to the chip surface, while its output terminal is connected to the HIOKI U8552 Logger Unit. This setup allows real-time recording of the temperature variations in the power switch during the heating process. The recorded temperature data are then compared with the temperature values calculated using the electrothermal coupling model, as illustrated in Fig. 13. The pink curve represents the temperature measurements obtained

from the thermocouple, the blue curve corresponds to the calculated temperatures from the electrothermal coupling model, and the grey curve denotes the predicted temperatures without accounting for the electrothermal coupling effects.

The results indicate that ignoring electrothermal coupling in device operation leads to a significant temperature error of up to 3.2% compared to the actual measurements, whereas incorporating electrothermal coupling reduces the error to merely 0.4%. Compared to electric circuit models, the electrothermal model provides a more accurate representation of the temperature variation process in GaN HEMTs.

C. Discussion on Steady-State Operating Temperature

The steady-state temperature, obtained from the electrothermal coupling analysis, is influenced by the temperature-dependent power loss $P_{\mathrm{loss}}(T_j)$, and the heat dissipation. The total dissipated power (P_{diss}) in Watts is equal to the thermal conductivity coefficient (K), multiplied by the cross-sectional area (A) perpendicular to the direction of heat dissipation, and the temperature difference (ΔT) between the starting surface and the final surface, divided by the length (L) over which the heat travels. For multilayer structure such as GaN HEMTs, the formula can be written as

$$P_{\mathrm{diss}} = \sum_{i=1}^{n} \frac{K_i A_i}{L_i} (T_j - T_a) . \tag{10}$$

Besides, the thermal resistance can be calculated by

$$R_{\mathrm{th},i} = \frac{L_i}{K_i A_i}. \tag{11}$$

Thus, the heat dissipation power can be written as

$$P_{\mathrm{diss}} (T_j) = \frac{T_j - T_a}{\sum_{i=1}^{n} R_{\mathrm{th},i}}. \tag{12}$$

The steady-state temperature can be obtained by solving the following equation:

$$P_{\mathrm{loss}} (T_j) - \underbrace{\frac{T_j - T_a}{\sum_{i=1}^{n} R_{\mathrm{th},i}}}_{P_{\mathrm{diss}}(T_j)} = 0 \tag{13}$$

of which, $\sum_{i=1}^{n} R_{\mathrm{th},i}$ represents the total thermal resistance from the junction to the environment, which comprises multiple components: the junction-to-package thermal resistance (determined by the device packaging), the package-to-heatsink thermal resistance (which includes the contact resistance of thermal grease), and the heatsink-to-environment thermal resistance (dependent on heatsink surface area and cooling conditions such as forced air or natural convection).

Fig. 14 shows the curves of power loss and heat dissipation versus junction temperature. The intersection points of these two curves represent steady-state operating temperature. Several factors can influence this temperature.

First, operating GaN HEMTs in a high ambient temperature environment causes the power dissipation curve P_{diss} to shift horizontally to high temperature region, resulting in higher steady-state junction temperature [see Fig. 14(a)]. Second, an increase in thermal resistance reduces the slope of the heat dissipation curve P_{diss}, also leading to a higher steady-state junction temperature [see Fig. 14(b)].

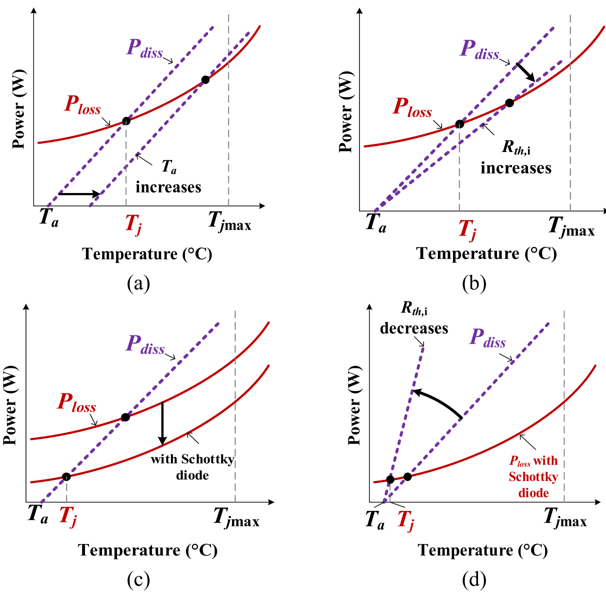

Fig. 14. Steady-state operating temperature analysis. (a) Effect of increased ambient temperature. (b) Effect of increased thermal resistance. (c) Power loss reduction due to parallel connection of Schottky diode. (d) Synergistic effect on junction temperature reduction.

Implementing parallel-connected Schottky diodes offers two key benefits that lower the steady-state junction temperature. These Schottky diodes reduces the reverse conduction losses within the GaN HEMTs. This power loss reduction shifts the power loss curve P_{loss} downwards to low power region [see Fig. 14(c)]. Moreover, the parallel-connected Schottky diodes effectively increase the heat dissipation area, leading to a decrease in thermal resistance and an increase in the slope of power dissipation curve P_{diss}. A further reduction in the junction temperature is observed [see Fig. 14(d)].

Notably, the intersection of the power loss and heat dissipation curves is not guaranteed, especially when operating under high ambient temperatures or with substantial thermal resistance. In this scenario, the power loss continuously exceeds the heat dissipation, leading to thermal runaway and subsequent failure of GaN HEMTs.

To summarize, integrating Schottky diodes not only expands the thermal stability margin but also effectively limits the increase in junction temperature. This synergistic optimization not only enhances power conversion efficiency but also alleviates thermal management challenges for GaN HEMTs. In addition, the reduction in junction temperature helps slow down device aging, thereby extending the lifespan of the power converter and enhancing system reliability.

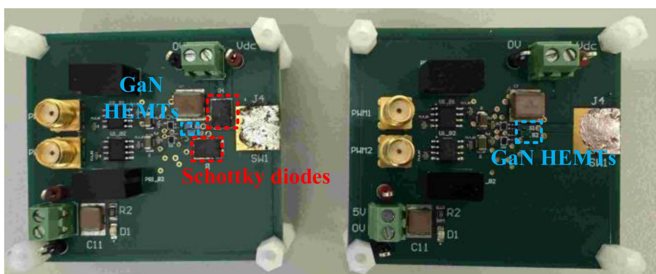

Fig. 15. Prototypes of totem-pole inverters.

IV. Experimental Verification and Evaluation

A. Prototypes and Experimental Setups

For the comparative studies, we constructed totem-pole inverter prototypes both with and without Schottky diodes. The prototypes utilized GaN HEMTs EPC2012C and Schottky diodes V10P20.

Comparative evaluations were conducted at three switching frequencies (1, 6.78, and 13.56 MHz). The circuit parameters for the inductive load are adjusted to ensure consistent R_L and X_L values across these three operating frequencies. Critical circuit parameters are summarized in Table IV and the prototypes of totem-pole inverters are shown in Fig. 15.

B. Key Waveforms of the Inverters

The key waveforms of the inverters are shown in Fig. 16. The v_{gs} and v_{ds} waveforms for the high-side and low-side GaN HEMTs in the circuit verify that both the high-side and low-side switches achieve zero-voltage switching (ZVS) during turn-ON.

C. MHz AC Power and Efficiency Measurements

To ensure measurement accuracy, two methods were employed for cross-validation:

1) Instantaneous Power Integration and Averaging: Discrete sampling of ac output voltage and current signals allows calculation of the average ac power over a switching period by integrating the instantaneous power within one signal cycle, as shown in (14), where n represents the number of sampling points in one cycle

$$P = \frac{1}{n}\sum_{i=1}^{n} v_o(i)\cdot i_o(i). \tag{14}$$

To calibrate nanosecond-level channel delays in oscilloscope measurements of ac voltage and current waveforms, the setup in Fig. 17 is used. A power amplifier is used to inject power into an RF resistor, then voltage and current waveforms of the RF resistor are measured.

Taking the voltage waveform as the reference, the time delay of the current signal sampling channel is determined using an optimization algorithm. The objective function is defined as follows:

$$\max_{t_D} \frac{1}{T}\int_0^T v_{\mathrm{probe}}(t)\, i_{\mathrm{probe}}(t+t_D)\, dt \tag{15}$$

TABLE V
Results of Two AC Power Calculation Methods

Frequency	Power (Method 1)		Power (Method 2)	
	Without diodes	With diodes	Without diodes	With diodes
1 MHz	27.45 W	27.24 W	27.21 W	27.44 W
6.78 MHz	24.10 W	24.17 W	23.82 W	24.03 W
13.56 MHz	24.09 W	23.29 W	24.39 W	23.74 W

TABLE VI
Efficiency Comparison of the Two Circuit Configurations

Frequency	Configuration	Output current	Input power	Output power	Efficiency
1 MHz	*Without* diodes	2.53 A	29.02 W	27.45 W	94.60%
	With diodes	2.53 A	27.97 W	27.24 W	97.39%
6.78 MHz	*Without* diodes	2.35 A	26.77 W	24.10 W	90.02%
	With diodes	2.36A	24.85 W	24.17 W	97.28%
13.56 MHz	*Without* diodes	2.39 A	27.43 W	24.09 W	87.85%
	With diodes	2.37A	24.57 W	23.29 W	94.81%

where $v_{\mathrm{probe}}(t)$ and $i_{\mathrm{probe}}(t)$ are the voltage and current waveforms, T is the period of the ac signal, and t_D represents the delay between the current waveform $i_{\mathrm{probe}}(t)$ and the voltage waveform $v_{\mathrm{probe}}(t)$.

2) Resistive Component Power Calculation: The active power of the inductive load can be characterized by measuring the real part of its impedance and the root mean square (rms) value of the output current

$$P = I_{o_\mathrm{rms}}^2 \times R_L \tag{16}$$

of which $I_{o\cdot\mathrm{rms}}$ is the rms value of the output current. The magnitude of the resistive component R_L can be measured using an impedance analyzer.

3) Cross-Validation of AC Power and Efficiency Measurements: Using the two methods above, the output power of the totem-pole circuit operating at MHz frequencies was calculated, and the results are shown in Table V. The calculated power values from both methods were highly consistent. This cross-validation approach effectively mitigates instrumentation-induced errors, ensuring reliable power measurements in high-frequency switching systems.

The conversion efficiency of the totem-pole inverter was calculated from the measured power data, with comparative results summarized in Table VI, in which the ac power losses are calculated by method I. The analysis confirms that reverse-paralleling Schottky diodes significantly improves efficiency at MHz switching frequencies, primarily through loss redistribution during dead-time intervals.

D. Thermal Performance

1) Surface Temperature Measurement: The operating temperatures of the GaN HEMTs during the inverter's operation

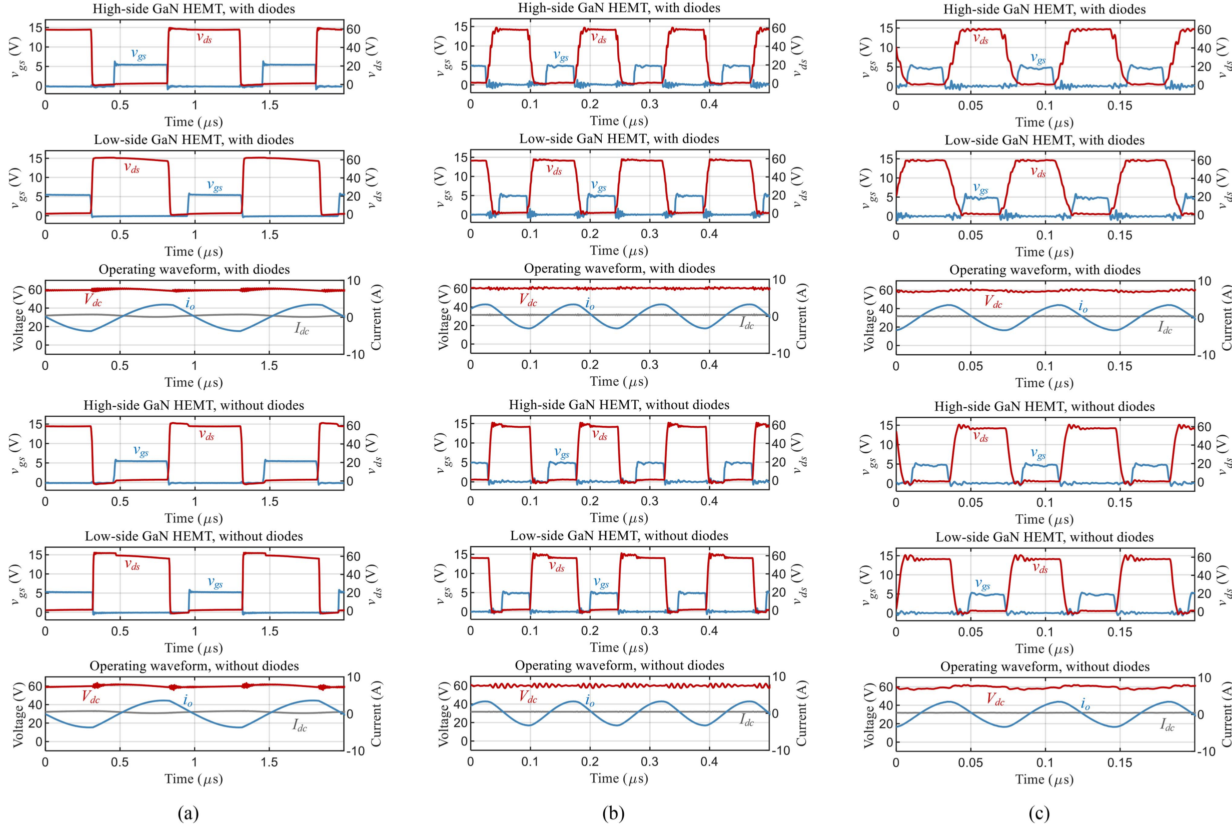

Fig. 16. Key waveforms of the inverter. (a) 1 MHz operating frequency. (b) 6.78 MHz operating frequency. (c) 13.56 MHz operating frequency.

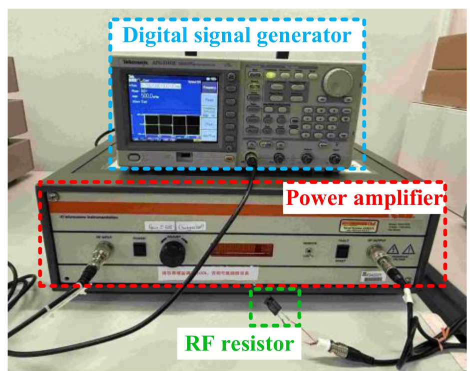

Fig. 17. Oscilloscope calibration setup.

were observed with a thermal imaging camera, as shown in Fig. 18. For GaN HEMTs EPC2012C, which have a high level of integration and a very small heat dissipation area (1.53 mm^2), the operating temperature can reach nearly 80 °C at a switching frequency of 6.78 MHz in the absence of freewheeling diodes. However, after adding the reverse-parallel Schottky diodes, the temperature of the GaN HEMTs is significantly reduced to approximately 45 °C. Because the Schottky diodes handle the freewheeling current during the dead time, the thermal stress on the GaN HEMTs is reduced.

Furthermore, another GaN HEMTs (Model number: GS61004B), which feature larger thermal dissipation area and better heat dissipation performance, are also tested. In this configuration, Schottky diode RB218RSM15STF is used. Fig. 19 shows the surface temperatures of the totem-pole inverter with the GaN HEMT GS61004B. The measurements show that the Schottky diodes lower the operating temperature by approximately 15−20 °C.

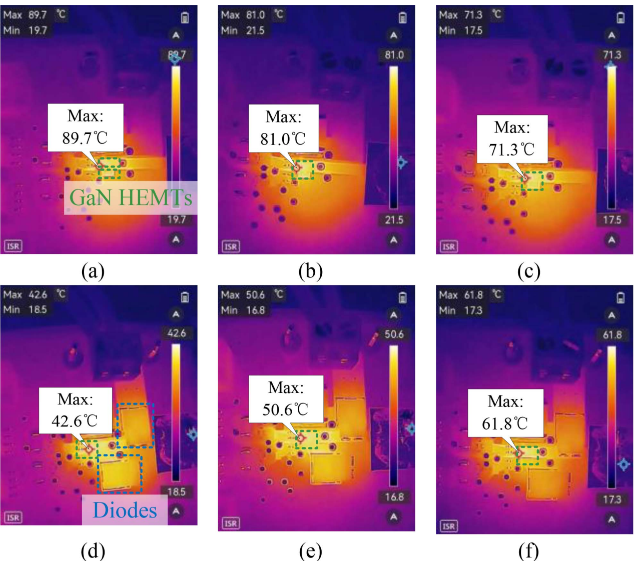

Fig. 18. Surface temperatures of the totem-pole inverter with GaN HEMT EPC2012C. (a) 1 MHz, without diodes. (b) 6.78 MHz, without diodes. (c) 13.56 MHz, without diodes. (d) 1 MHz, with diodes. (e) 6.78 MHz, with diodes. (f) 13.56 MHz, with diodes.

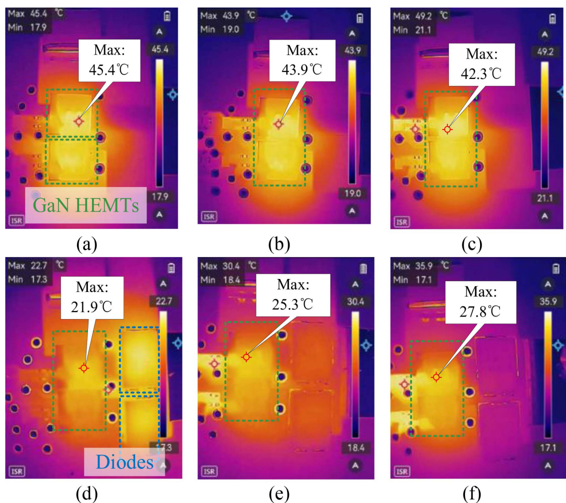

Fig. 19. Surface temperatures of the totem-pole inverter with GaN HEMT GS61004B. (a) 1 MHz, without diodes. (b) 6.78 MHz, without diodes. (c) 13.56 MHz, without diodes. (d) 1 MHz, with diodes. (e) 6.78 MHz, with diodes. (f) 13.56 MHz, with diodes.

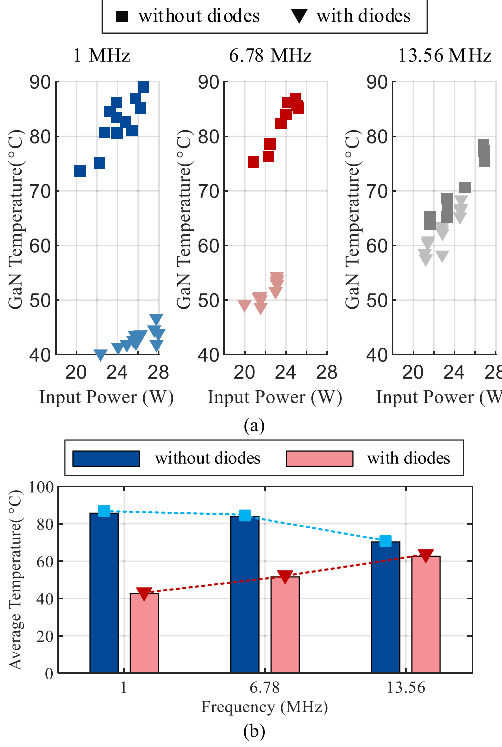

Fig. 20. Surface Temperature of the inverter. (a) Surface temperature as a function of input power. (b) Average surface temperature of the inverter at three operating frequencies.

This reduction in temperature greatly enhances the reliability of the inverter, as the failure rate of power switches is positively correlated with their junction temperature.

2) Discussion: Fig. 20(a) shows the surface temperature of the totem-pole inverter as a function of input power. Fig. 20(b) summarizes the average inverter surface temperature at three operating frequencies. In general, the inverter with Schottky diodes shows a lower surface temperature compared to its counterpart

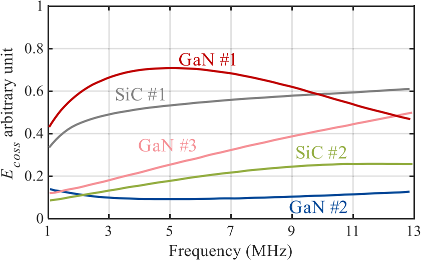

Fig. 21. Frequency dependence of C_{oss} loss for serval SiC and GaN transistors [40].

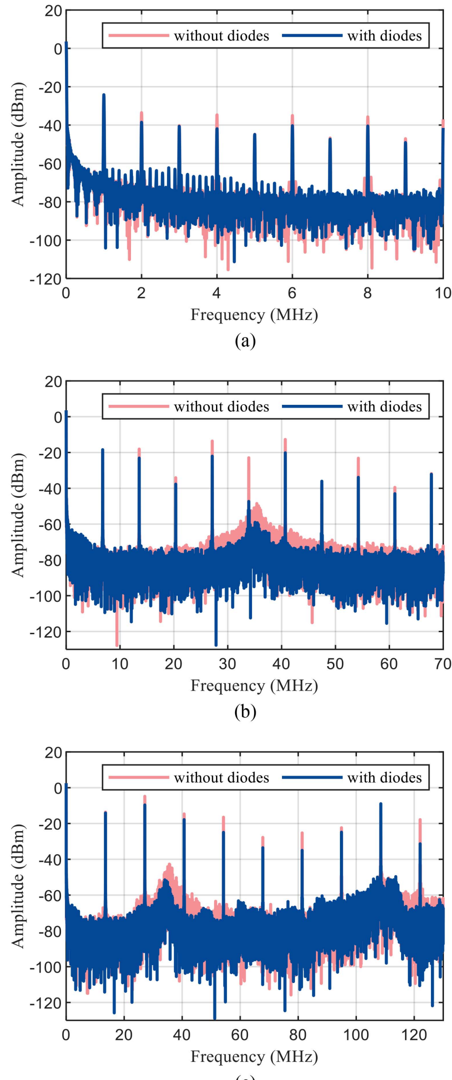

Fig. 22. Magnetic field emissions of the GaN HEMTs. (a) 1 MHz operating frequency. (b) 6.78 MHz operating frequency. (c) 13.56 MHz operating frequency.

without Schottky diodes. These results suggest the effectiveness of the solution.

Interestingly, the surface temperature of the GaN HEMTs (EPC2012C and GS61004B) decreases slightly with increasing operating frequency, demonstrating an inverse relationship. This may be attributed to the C_{oss} loss of the GaN HEMTs. Existing

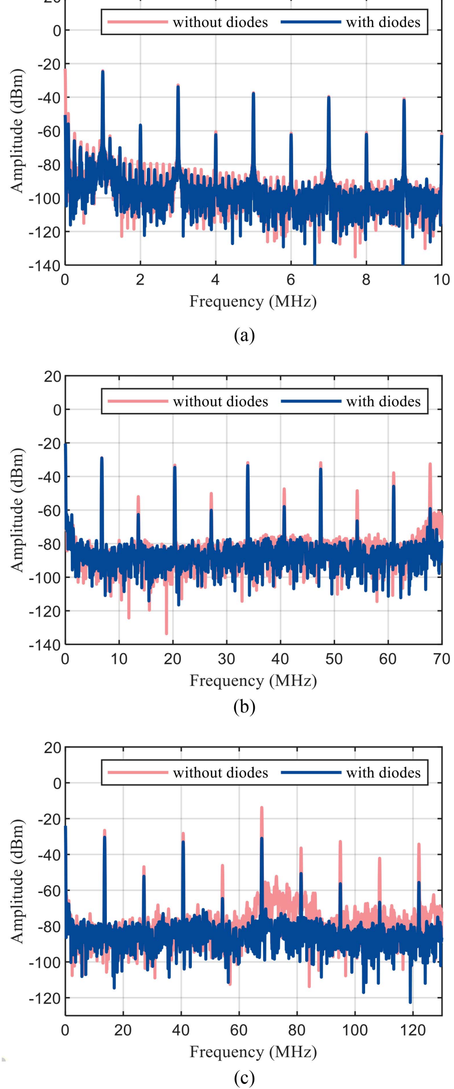

Fig. 23. Electric field emission of the GaN HEMTs. (a) 1 MHz operating frequency. (b) 6.78 MHz operating frequency. (c) 13.56 MHz operating frequency.

research indicates that this type of loss varies with switching frequency, as shown in Fig. 20 [40]. The trends observed for both the EPC2012C and GS61004B align with curve GaN #1 in Fig. 21. In addition, the frequency-dependent behavior of the dc-link capacitor also contributes to the observed efficiency decrease at higher frequency. As the operating frequency increases, the capacitor's effective capacitance diminishes as it approaches its self-resonant frequency [41], impairing its ability to suppress ripple current and further leading to a consequent loss generation.

E. EMI Reduction Evaluation

To further provide the evidence regarding EMI performance, we conducted additional verifications using near-field probes (RSH400-1 for magnetic field emissions and RSE02 for electric field emissions). These probes are positioned 1 cm above the GaN HEMTs to capture the magnetic field and electric field emissions. These measurement results are used to evaluate the EMI performance. As specifically illustrated in Figs. 22 and 23, both magnetic and electric field emission levels are reduced in the MHz range. The magnetic field emissions are alleviated by up to 24.41 dBm, while electric field emissions are alleviated by up to 26.57 dBm. This reduction is attributed to the damping effect introduced by the diode's junction capacitance.

Notably, the EMI reduction is attributed to slowed-down switching transitions. In hard-switching conditions, this may increase switching loss. However, in this article, we focus on the MHz operation of the GaN-based power converter. The switching loss caused by the hard switching of GaN HEMTs could reach a very high level and cause thermal instability issues. Therefore, soft switching is mainly adopted in MHz operation and the switching loss only takes up a very small part of GaN's total loss [31], [42].

V. Conclusion

This study systematically investigates the performance of GaN power switches in MHz-frequency operations based on detailed electrothermal modeling and practical evaluation. It addresses critical challenges such as high reverse conduction losses, thermal instability potential, and EMI. By using Schottky diodes in an antiparallel configuration with GaN HEMTs, significant improvements in converter efficiency, thermal management, and EMI reduction can be achieved. Key findings reveal that the use of antiparallel diodes improves converter efficiency by up to 6.9% and further enhances thermal stability. Thermal imaging confirms a temperature reduction of up to 47 °C in GaN HEMTs when Schottky diodes are employed. The EMI is also reduced due to the lower dv/dt caused by the addition of Schottky diode's junction capacitance. These findings challenge the conventional approach that omits external diodes in GaN-based converters and provide a practical solution for high-frequency power electronics.

The success of Schottky diodes in mitigating reverse conduction losses and thermal runaway risks underscores the potential for further optimization of GaN devices. Specifically, our findings suggest that GaN HEMT designers could explore integrating or implanting structures similar to Schottky diodes within the conductive channel to create optimized reverse conduction paths. Such innovations could inherently improve the performance of GaN HEMTs, eliminating the need for external components while retaining the benefits observed in this study.

It is noteworthy that, while the external Schottky diode reduces reverse-conduction, it increases system cost. This tradeoff is justified in the applications where efficiency outweighs cost.

Acknowledgment

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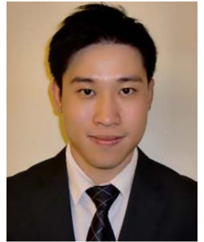
Mingshuo Zhu (Student Member, IEEE) received the B.Eng. and M.Eng. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2021 and 2024, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the City University of Hong Kong, Hong Kong.

His current research interests include wireless power transfer and the reliability of power electronic devices.

Kerui Li (Member, IEEE) received the B.Eng. degree in electrical engineering from the South China University of Technology, Guangzhou, China, in 2013, the M.Eng. degree in electrical engineering from the Sun Yat-sen University, Guangzhou, China, in 2016, and the Ph.D. degree in electrical engineering from The University of Hong Kong, Hong Kong, in 2021.

Since 2025, he has been with City University of Hong Kong, Hong Kong, where he is currently an Assistant Professor in the Department of Electrical Engineering. Prior to that, he was a Research Fellow with Nanyang Technological University, Singapore, and a Research Assistant Professor with The Hong Kong Polytechnic University and The University of Hong Kong.

Dr. Li’s professional services and research have been recognized with several prestigious awards, including the IEEE Transactions on Power Electronics Outstanding Reviewer Award (2025), two IEEE Transactions on Power Electronics Prize Paper Awards (second place for the year 2023 and first place for the year 2022), the IEEE Power Electronics Society Ph.D. Thesis Talk Award (2022), and the University of Hong Kong Power Engineering Prize (2020).



Siew-Chong Tan (Fellow, IEEE) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, Hong Kong, in 2005.

From September to October 2009, he was a Visiting Scholar with Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, and an Invited Academic Visitor of Huazhong University of Science and Technology, Wuhan, China, in 2011. He is currently a Chair Professor with Department of Electrical Engineering, City University of Hong Kong, Hong Kong. His research interests include the areas of power electronics and control, LED lightings, smart grids, and clean energy technologies.

Shu Yuen Ron Hui (Fellow, IEEE) received the B.Sc. (Eng.) (Hons.) in electrical and electronic engineering from the University of Birmingham, Birmingham, U.K., in 1984, and the D.I.C. and Ph.D. degree in electrical engineering from Imperial College London, London, U.K., in 1987.

He is currently a Chair Professor of Power Electronics with the City University of Hong Kong, and Imperial College London. Previously, he held academic positions with the University of Nottingham, and University of Sydney, and endowed professorship at the University of Hong Kong. He has authored or coauthored more than 500 research papers, including 330 refereed journal publications. His IEEE Xplore patent citations exceed 1280. Over 150 of his patents have been adopted by industry worldwide. His inventions on wireless charging platform technology underpin key dimensions of Qi, the world’s first wireless power standard, with freedom of positioning and localized charging features for wireless charging of consumer electronics. He also developed the Photo-Electro-Thermal Theory for LED Systems and Electric Spring technology for the smart grid. His research interests include power electronics, wireless power, sustainable lighting, and smart grid.

Dr. Hui is the recipient of the IEEE Rudolf Chope R&D Award and the IET Achievement Medal (The Crompton Medal) in 2010, IEEE William E. Newell Power Electronics Award in 2015, and the IET JJ Thomson Medal in 2024. He is a Fellow of the Australian Academy of Technology & Engineering, US National Academy of Inventors, and Royal Academy of Engineering, U.K.