Dual-Mode Thermal Management of a Power Module for Normal and Short-Term Overcurrent Operation

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***Abstract*—Integrating phase change material (PCM) in a power module could mitigate the temperature surge during short-term overcurrent (OC). However, PCM in the path of heat conduction could impede cooling in normal operation. This article proposes a dual-mode thermal management approach for a three-dimensional loop packaging design of a half-bridge SiC MOSFET power module, in which the PCM is placed away from the primary heat conduction path and is only activated by the OC. This offers thermal buffering during OC without notably increasing the steady-state thermal resistance. Chip temperatures of the upper and lower legs, on the two sides of the PCM, are almost equal and consistent with values in a package without PCM. The 1200 V, 80 A prototype is shown to have superior performance to a conventional module with single-sided cooling. Testing under 3 p.u. and 10 s OC shows that integrating PCM can reduce the chip temperature rise by about 11°C. The PCM thermal buffering effect in repetitive transients is demonstrated and evaluated. Double pulse testing shows improved switching characteristics. The parasitic loop inductance is measured to be 5.67 and 7 nH in static and dynamic conditions, respectively, and the simulated value is 5.25 nH. Thermal cycling results confirm the proposed module's reliability comparable to the conventional double-sided design.**

***Index Terms*—Heat conduction, packaging, phase change material (PCM), power module, thermal management.**

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I. Introduction

With low-carbon targets set by various governments, the share of renewable generation in power systems has been steadily increasing [1], [2], [3], [4]. Power devices are essential in converters to enable efficient energy conversion and interface control [5], [6], [7]. This has presented challenges to power system operation, reducing its regulation capability and introducing new modes of instability [8]. Some studies have shown that, as a core constituent, power semiconductors not only need to improve conversion efficiency and power density but also tolerate overcurrent (OC) to certain extent [9]. The latter is needed especially during transients such as grid faults and motor restarting. In such situations, the power devices must possess the robustness that they do not currently have [10].

Traditional power system apparatus such as a synchronous generator or transformer can tolerate OC for seconds and even minutes, whereas a power device, such as Si-based insulated gate bipolar transistor (IGBT), can only withstand modest OC for approximately 10 ms [9], which is inadequate for the power system need. Some expect for the emerging grid-forming systems to sustain operation with OC of 3 p.u. for no less than 10 s [11], to effectively reinforce the grid during transients. Derating devices/systems for short-term capacity can be costly. Alternative solutions should be sought.

Integrating phase change material (PCM) in the module can provide thermal buffering during OC [12], [13], [14], [15], [16]. Tests on a 1200 V/50 A half-bridge IGBT module showed that the chip temperature can be kept below 130°C for a 3 p.u. OC lasting for 3 s [17], [18]. However, the PCM container was placed between the chip and direct bonded copper (DBC) substrate in the primary heat conduction path from the chip. This can increase the steady-state thermal resistance of the power module. Heterogeneous integration of a thermally anisotropic graphite sheet and PCM was used to reduce the thermal resistance [19] leveraging the graphite's thermal diffusivity. Nevertheless, the approach added an extra layer and the PCM was still placed in the primary path of heat conduction. In [20], PCM was placed on the chip's top metallization to reduce temperature fluctuation. This solution is not ideal due to the exposure of PCM to air and the difficulty with small chips.

Initial studies, which are still quite rare, are usually about optimizing PCM integration to enhance the thermal storage/absorbing capability, emphasizing the thermal buffering effect in OC conditions [17], [18], [19], [20], [21]. It would be

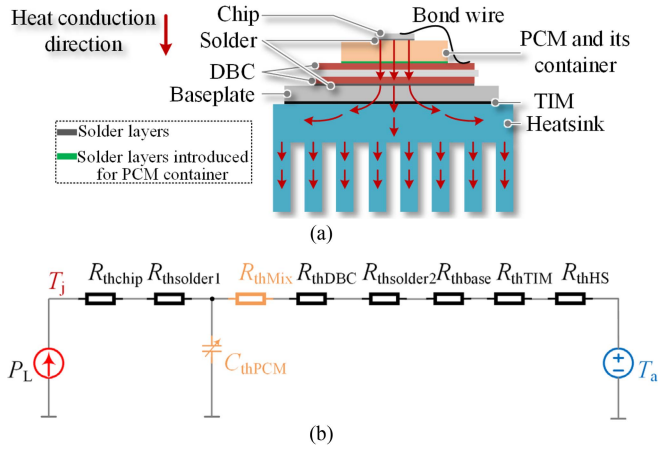


Fig. 1. Configuration of previous PCM-integrated power module: (a) configuration diagram; and (b) its thermal network.

useful to explore alternative packaging designs to integrate the PCM without affecting cooling in normal operation; the thermal buffering effect is released only upon the occurrence of OC. This necessitates a dual-mode design approach to separate the steady-state and OC transient.

This article presents a PCM integration scheme in line with such an approach. The PCM is placed away from the primary heat conduction path to ensure that its relatively low thermal conductivity will not affect the steady-state thermal resistance but it can be activated for the desired short-term OC capability when needed. The resulting 3-D vertical loop design also reduces the parasitic inductance of the power module.

II. Motivation of Dual-Mode Thermal Management Power Module Design

A. Side Effect of PCM-integration

Taken from [18], a previous PCM-integrated IGBT package consists of the chip, solder layer, PCM in container, DBC substrate, baseplate, thermal interface material (TIM), and a heatsink, as shown in Fig. 1(a). The corresponding thermal network for this setup is illustrated in Fig. 1(b), where R_{thchip}, R_{thsolder}, R_{thMix}, R_{thDBC}, R_{thbase}, R_{thTIM}, and R_{thHS} represent the thermal resistance of the chip, solder layers, PCM (including container and additional solder layer needed), DBC, baseplate, TIM, and heatsink respectively. C_{thPCM} denotes the dominant heat capacity of the PCM that can be released.

The PCM is placed in the path of heat conduction from the chip to release its high heat capacity (C_{thPCM}) when melting. Its low thermal conductivity causes significant thermal resistance (R_{thMix}) to be added in the primary direction, particularly when the footprint on the DBC and baseplate needs to be small.

PCM integration changes the total thermal resistance from (1) to (2). The % increase in thermal resistance is calculated as in (3). PCM integration usually increases the total thermal resistance although some other terms may reduce due to the change of heat flux pattern

$$R_{\text{con}}^{\text{before}} = R_{\text{thchip}} + R_{\text{thsolder1}} + R_{\text{thDBC}} + R_{\text{thsolder2}} + R_{\text{thbase}} + R_{\text{thTIM}} + R_{\text{thHS}} \quad (1)$$

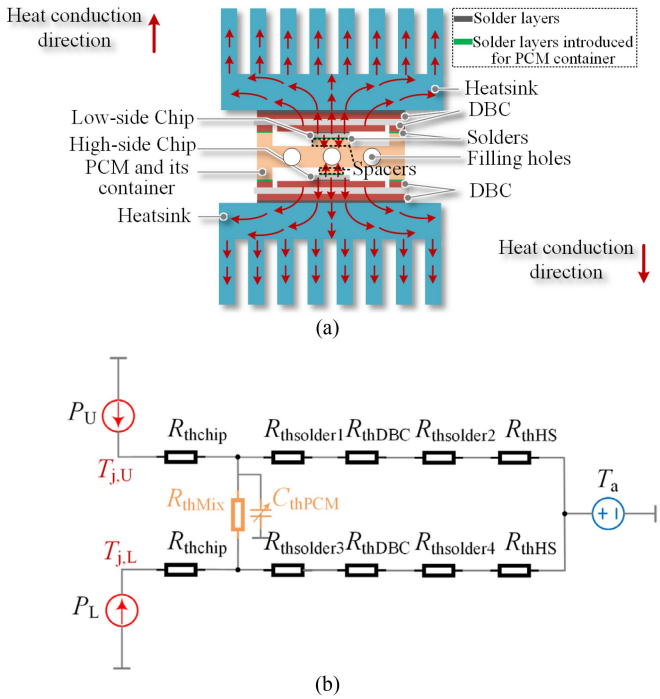


Fig. 2. Configuration of a dual-mode thermal management for a PCM-integrated power module: (a) configuration diagram; and (b) its thermal network.

$$R_{\text{con}}^{\text{after}} = R_{\text{thchip}} + R_{\text{thsolder1}} + R_{\text{thMix}} + R_{\text{thDBC}} + R_{\text{thsolder2}} + R_{\text{thbase}} + R_{\text{thTIM}} + R_{\text{thHS}} \quad (2)$$

$$\Delta R_{\text{con}} = \frac{R_{\text{con}}^{\text{after}} - R_{\text{con}}^{\text{before}}}{R_{\text{con}}^{\text{before}}} \times 100\% = \frac{R_{\text{thMix}}}{R_{\text{con}}^{\text{before}}} \times 100\%. \quad (3)$$

B. Dual-Mode Heat Flow Analysis

The design proposed here is a new thermal management approach to integrate PCM in power modules. It addresses simultaneously the steady-state and transient conditions. The design focuses on two aspects.

1) *Steady state:* optimal layout prevents the low thermal conductivity of the PCM from impeding steady-state heat transfer, ensuring that the performance reach that of a traditional single-side cooled module.
2) *Transient:* the PCM absorbs the additional power loss through its latent heat upon the occurrence of transient OC, containing the chip temperature surge.

Fig. 2(a) shows the proposed dual-mode packaging design for a half-bridge power module (unit). The high- and low-side chips (SiC MOSFETs without anti-parallel diodes) eventually dissipate heat to the ambient through heatsinks, along the primary paths in the vertical direction. A spacer of similar dimensions to the chip limits the heat transfer to the PCM container, which is in the middle of the arrangement, making this path a secondary heat dissipation path. Fig. 2(b) shows the corresponding thermal network (equivalent circuit).

Without PCM in the container, the thermal resistance from each chip to the ambient is derived as (4). With PCM, this is modified to (5) and the relative change can be calculated as in (6). A negative change would indicate a reduction

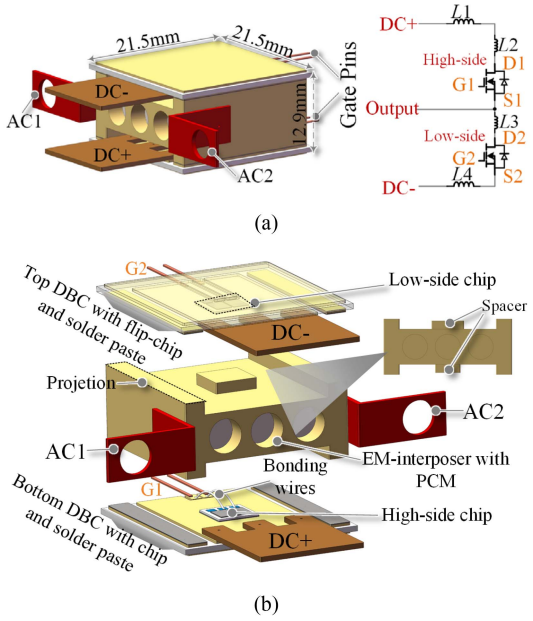


Fig. 3. 3-D model of the proposed half-bridge power module. (a) Overview and the circuit diagram. (b) Exploded view.

in thermal resistance compared to the case before PCM is put in

$$\begin{cases} R_{\mathrm{U}}^{\mathrm{before}} = R_{\mathrm{thchip}} + R_{\mathrm{thsolder1}} + R_{\mathrm{thDBC}} + R_{\mathrm{thsolder2}} + R_{\mathrm{thHS}} \\ R_{\mathrm{L}}^{\mathrm{before}} = R_{\mathrm{thchip}} + R_{\mathrm{thsolder3}} + R_{\mathrm{thDBC}} + R_{\mathrm{thsolder4}} + R_{\mathrm{thHS}} \end{cases} \tag{4}$$

$$\begin{cases} R_{\mathrm{U}}^{\mathrm{after}} = R_{\mathrm{thchip}} + \frac{R_1 \times (R_{\mathrm{thMix}} + R_2)}{R_1 + R_2 + R_{\mathrm{thMix}}} \\ R_{\mathrm{L}}^{\mathrm{after}} = R_{\mathrm{thchip}} + \frac{R_2 \times (R_{\mathrm{thMix}} + R_1)}{R_1 + R_2 + R_{\mathrm{thMix}}} \\ R_1 = R_{\mathrm{thsolder1}} + R_{\mathrm{thDBC}} + R_{\mathrm{thsolder2}} + R_{\mathrm{thHS}} \\ R_2 = R_{\mathrm{thsolder3}} + R_{\mathrm{thDBC}} + R_{\mathrm{thsolder4}} + R_{\mathrm{thHS}} \end{cases} \tag{5}$$

$$\begin{cases} \Delta R_{\mathrm{U}} = \frac{R_{\mathrm{U}}^{\mathrm{after}} - R_{\mathrm{U}}^{\mathrm{before}}}{R_{\mathrm{U}}^{\mathrm{before}}} \times 100\% = \frac{-R_1^2}{(R_1 + R_2 + R_{\mathrm{thMix}}) R_{\mathrm{U}}^{\mathrm{before}}} \times 100\% \\ \Delta R_{\mathrm{L}} = \frac{R_{\mathrm{L}}^{\mathrm{after}} - R_{\mathrm{L}}^{\mathrm{before}}}{R_{\mathrm{L}}^{\mathrm{before}}} \times 100\% = \frac{x - R_2^2}{(R_1 + R_2 + R_{\mathrm{thMix}}) R_{\mathrm{L}}^{\mathrm{before}}} \times 100\%. \end{cases} \tag{6}$$

III. Design of PCM-Integrated Power Module With Dual-Mode Thermal Management

A. Module Layout for PCM Integration

Fig. 3 shows the packaging design of the SiC MOSFET half-bridge module with a three-dimensional (3-D) power loop. For illustration, the module consists of 2 × 1.2 kV/80 A SiC MOSFETs, and the low-side chip is attached as a flip-chip to the DBC substrate with AlN. The gate and Kelvin source pads of the low-side chip are directly led through the circuit pattern of the DBC substrate, while those of the high-side chip are led by Al bonding wires.

The power loop is completed by a customized mechanical–electrical (EM) interposer, with central spacers connecting the power source pad of the high-side chip to the power drain pad of the low-side chip. Due to the difference in area between the power drain pad and the power source pad of the SiC MOSFET chip, there is a slight asymmetry in the overall design. The EM-interposer's projections on both sides are soldered to the DBC substrates, providing ac output, additional heat dissipation, and mechanical support. All power terminals are located on the same side, while the gate connectors are on the opposite side. The overall dimensions, excluding terminals, are 21.5 mm × 21.5 mm × 12.9 mm.

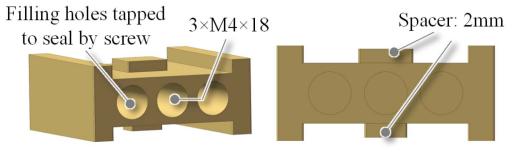


Fig. 4. Details of EM-interposer.

TABLE I
Properties of Some Commercially Available PCMs

Materials	Melting temperature (°C)	Thermal conductivity (W/m·K)	Latent heat (kJ/kg)	Specific heat (kJ/kg·K)
Paraffin wax	60	1	208.7	0.386
Liquid metal LM108	108	35	45	0.25
Gallium	30	40.6	80.2	0.368
In97Ag3	143	71	34	0.17–0.295

Thanks to high thermal conductivity of copper, the EM-interposer acts as an ideal container for PCM (Fig. 4). Three M4 filling holes with a depth of 18 mm are made, and 3 mm-deep threads are tapped to facilitate sealing with screws and high-temperature sealing films.

The most commonly used solid–liquid PCMs include organic, inorganic, and eutectic types [22], [23]. For power device applications, the ideal PCM should offer high latent heat per unit volume. At the same time, thermal conductivity and an appropriate melting point are also critical for low thermal resistance and compatibility with the operational conditions. Minimal volume change, stable performance, and nontoxicity are further important factors [24]. To meet the design requirements of the PCM and the cooling demand in short-term OC conditions, this article establishes a systematic design methodology and a set of guidelines. The objective is to provide a structured framework for the efficient integration of PCM in power modules operating with transient OC stresses. The design flowchart is presented in Fig. 5.

Table I summarizes the common PCMs used in electronic cooling, with LM108 emerging as an ideal candidate. The melting point of LM108 is close to the operating temperature of the power chip. Compared to organic and eutectic PCMs [22], it has higher thermal conductivity, and its latent heat is within an acceptable range while exhibiting a small volume change (∼5%) before and after melting [25].

The density of LM108 is 7300 kg/m^3, and the maximum mass of the integrated PCM is calculated to be 4.13 g using (7). However, to prevent PCM leakage caused by sudden pressure changes during melting, a certain amount of space is reserved,

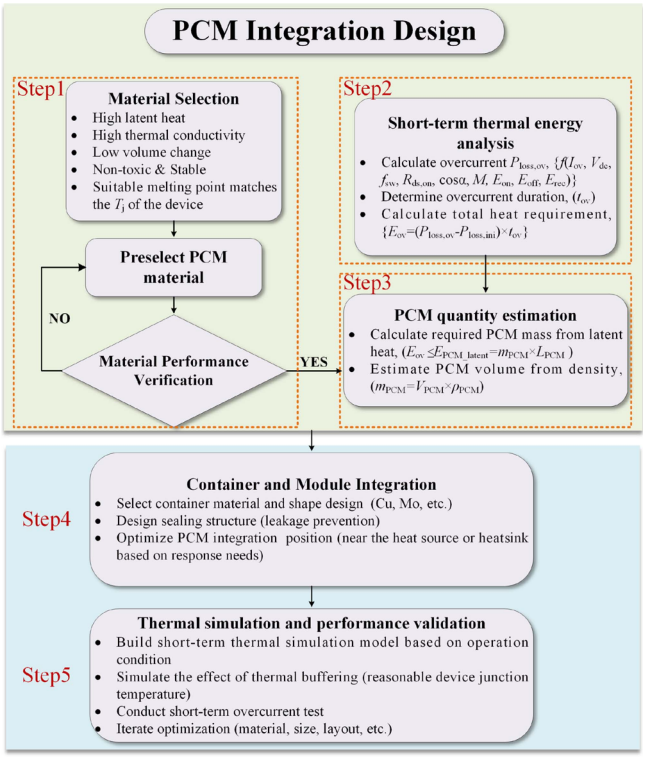


Fig. 5. PCM integration design flowchart.

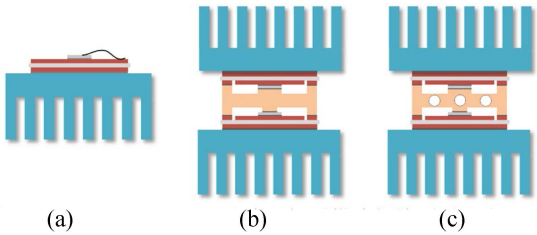


Fig. 6. Three cases for simulation comparison. (a) Conventional single sided cooling module. (b) The designed undrilled module. (c) The designed module with integrated PCM.

reducing the mass of the integrated PCM to approximately 3.6 g. According to (8), 3.6 g of LM108 can absorb 162 J of latent heat. In practice, the energy change before and after an OC fault may be required not to exceed the latent heat of the PCM

$$m_{\mathrm{LM108}} = 3 \times V_{\mathrm{single-hole}} \times \rho_{\mathrm{LM108}} \tag{7}$$

$$E_{\mathrm{PCM\_latent}} = m_{\mathrm{LM108}} \times L_{\mathrm{LM108}} \tag{8}$$

where m_{LM108} is the mass of integrated LM108, $V_{\mathrm{single\text{-}hole}}$ the volume of a single drilled hole, ρ_{LM108} the density of LM108, and $E_{\mathrm{PCM\_latent}}$ the energy that can be absorbed.

B. Thermal Simulation

To evaluate the thermal performance of the power module and illustrate the impact of the integrated PCM, finite-element simulations are conducted using COMSOL Multiphysics. As shown in Fig. 6, three cases are simulated for comparison: Case A, a conventional single chip device with single-sided cooling; Case B, a power module similar to the proposed design

TABLE II
THERMAL SIMULATION PARAMETERS USED IN COMSOL MULTIPHYSICS

Layers	SiC MOSFET chip	SiC, 400 W/m·K
	Solder 1	SAC305, 60 W/m·K
	Solder 2	Sn63Pb37, 51 W/m·K
	Solder 3	SAC305, 60 W/m·K
	Solder 4	Sn63Pb37, 51 W/m·K
	DBC copper	Cu, 385 W/m·K
	DBC ceramic	AlN, 170 W/m·K
	Copper heatsinks	Cu, 385 W/m·K
	EM-interposer	Cu, 385 W/m·K
	Wire bonds	Al, 238 W/m·K
Heat source	SiC MOSFET	20 W each chip
Cooling condition	Pin fin shape	Square, side width 1mm
	Pin fin pitch, height	1.5 mm, 20 mm
	Base plate thickness	2 mm
	Convection coefficient	50 W/m²K
	Ambient temperature	25 °C

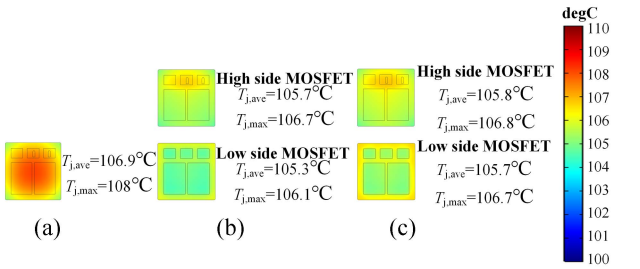


Fig. 7. Simulation results of chip temperature in three cases. (a) Conventional single sided cooling module. (b) The proposed undrilled module. (c) The proposed module with integrated PCM.

but without holes drilled or PCM integration; and Case C, the proposed power module with integrated PCM. The heatsinks feature square pin fins with a side width of 1 mm and a height of 20 mm, soldered directly to the metal layer on the backside of the DBC substrates. In simulation, each SiC MOSFET acts as a heat source (20 W), and each surface of the heat sink is set to 50 W/m^{2}K for forced air convection [26]. The materials and conditions are listed in Table II.

Under these conditions, Fig. 7 presents the temperature distribution for the chips in each case. The chip temperatures of the high-side and low-side chips in Case B are nearly identical, with both maximum and average chip temperatures being ∼106 °C. Case C shows similar temperatures. For the conventional device with single-side cooling, the average and maximum chip temperatures are 106.7°C and 108°C, respectively. This indicates that the proposed design would not adversely affect the steady-state temperature.

For all the three cases, the power loss of each SiC MOSFET chip is next increased from 10 to 50 W (in 10 W steps), with other conditions remaining the same as in Table II. Fig. 8(a) summarizes the simulation results for the steady state, plotted as chip temperature with respect to power loss. The variation from case to case remains within 2.5%. Similarly, the heat transfer coefficient is increased from 10 to 210 W/m^{2}K (in 50 W/m^{2}K steps). Fig. 8(b) summarizes the simulation results, where the chip temperature decreases as the heat transfer coefficient increases. The difference among the three cases is still small,

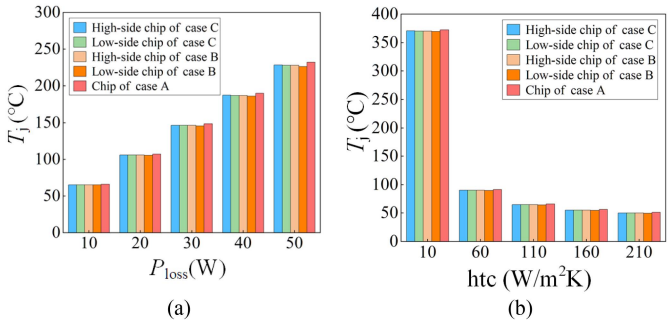


Fig. 8. Simulation results of three cases: (a) maximum chip temperature vs power loss and (b) maximum chip temperature vs heat transfer coefficient.

TABLE III
REDUCTION IN MAXIMUM CHIP TEMPERATURE FOR VARIOUS POWER PULSE DURATION (SIMULATION RESULTS)

Duration(s)	Reduction in T_{jmax} of high-side chip (°C)	Reduction in T_{jmax} of low-side chip (°C)
3	2.6	4.7
5	5.5	7.8
10	8.2	8.8

within 2.2%. It can be concluded that the proposed half-bridge power module design can always keep the temperatures of the high- and the low-side chips the same, and there is little difference in the chip temperature regardless of whether PCM is integrated or not.

Next, simulation is performed to evaluate the effect of the PCM integrated in power module as in Case C. With other simulation conditions as in Table II, the heat source power per chip is stepped up from 19 to 60 W and then stepped back to 19 W. The pulse duration is set to 3, 5, and 10 s, respectively. Fig. 9(a), (b), and (c) plots the maximum chip temperature response with or without PCM.

Before the power pulse, the maximum steady-state chip temperature in Case C, with or without the PCM, stabilizes around 100°C, which is lower than the phase change temperature, i.e., 108°C. After the power step-up, the chip temperature rises quickly. As shown in Fig. 9, the integrated PCM mitigates the temperature rise through the phase change effect. Table III summarizes the maximum chip temperature reduction for each power pulse duration. For a 10 s power pulse, the slope of the temperature curve changes significantly after 7 s, indicating that the PCM is all melted at this time.

During the power pulse, the module without integrated PCM exhibits a temperature difference between the high-side and low-side chips due to the slight structural asymmetry caused by the spacer mentioned in Section III-A. The temperature difference further intensifies during the power pulse.

To better explain the chip temperature difference in the PCM-integrated power module during the phase change, phase change cross-sections at different moments after the start of the power pulse are obtained as shown in Fig. 10 based on the cross-section selection shown in Fig. 11.

The left side of each cross-section corresponds to the region near the low-side chip, while the right side corresponds to the region near the top-side chip. During power pulsing, difference in the melting proportion of the PCM near the high-side and low-side chips at the same moment can be observed, indicating that the slight asymmetry of the proposed structure causes difference in heat distribution.

TABLE IV
ANSYS Q3D SIMULATION RESULTS

Parameter	AC resistance (mΩ)	AC inductance (nH)
DC + → DC –, L1 + L2 + L3 + L4	3.24	5.25
DC + → High-side MOSFET drain, L1 + L2	1.59	3.05
High-side MOSFET source → Low-side MOSFET drain, L3	0.94	1.96
Low-side MOSFET source →DC –, L4	1.4	3.28
DC + → DC – (without terminals)	2.78	3.12

C. Parasitic Parameter Extraction

The parasitic parameters are extracted using ANSYS Q3D at a 10 MHz ac excitation frequency [27]. Fig. 3(a) indicates the distribution of the parasitic inductance and Table IV lists in detail the parameters extracted. Simulation results indicate that the proposed power module's parasitic inductance is 5.25 nH, which is decreased to 3.12 nH without including the power terminals. This simulated value highlights the contribution of the internal packaging structure and should be interpreted as the lower bound of the module's parasitic inductance. In the 3-D design, significant mutual inductance cancellation reduces the inductance by nearly half compared to a more conventional design. Further optimization of power terminal layout and use of decoupling capacitors could achieve even lower parasitic inductance for high-frequency applications.

IV. FABRICATION AND RELIABILITY ANALYSIS

A. Materials Used in Module

Table V lists the materials used to fabricate the designed power module. The SiC MOSFET chips are rated at 1.2 kV/80 A, with drain pads plated with titanium/nickel/silver (Ti/Ni/Ag) and source and gate pads plated with nickel/palladium/gold (Ni/Pd/Au) for double-sided soldering. The copper layer on the DBC substrate features a custom-designed solder mask to facilitate soldering, and both power and gate terminals are specifically tailored to fit the DBC substrate. In the power module design, the high-side chip's Kelvin source and gate pads are bonded by 8 mil Al wires, while the low-side chip utilizes a flip-chip, to avoid wire bonding. The EM-interposer is precision-machined on a CNC. The heatsinks and PCM are commercially sourced. For soldering, SAC305 and Sn63/Pb37 solder sheets, along with Sn42/Bi58 solder paste, are used.

B. Module Assembly

As shown in Fig. 12, the laboratory manufacturing process begins with ultrasonic cleaning of parts. SAC305 preformed

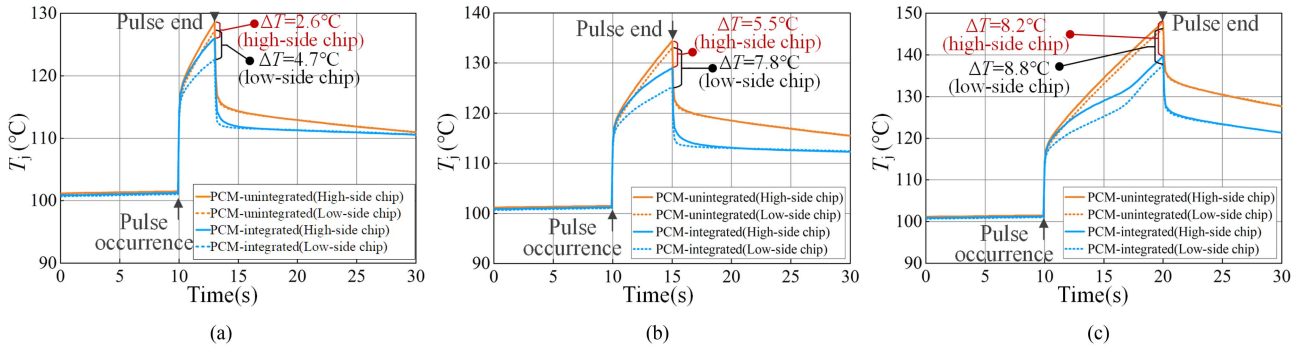


Fig. 9. Chip temperature response of power modules with and without integrated PCM: (a) 3 s pulse duration; (b) 5 s pulse duration; and (c) 10 s pulse duration.

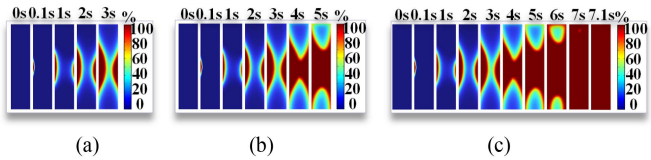


Fig. 10. Cross-sectional diagrams of phase-change melting in three different power pulse durations: (a) 3 s; (b) 5 s; and (c) 10 s.

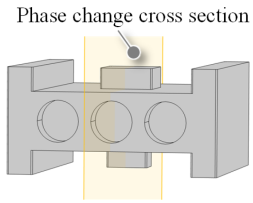


Fig. 11. Schematic diagram of selected phase change cross-section.

TABLE V
LIST OF MATERIALS USED INSIDE POWER MODULE

Part	Material	Description
SiC MOSFETs	SiC	1200 V/80 A; 5mm*5mm*0.2mm; top pads: G & S, AlSiCu+Ni/Pd/Au; bottom pad: D, Ti/ Ni /Ag
DBC substrates	Copper/AlN/copper	Size: 22mm×22mm; thickness: 0.3 mm/0.635 mm/0.3 mm
Bonding wires	Al	8 mil
EM-interposer	Copper	Matching with DBC
Terminals	Copper	Customize
Heatsinks	Copper	Pin fin shape: side width 1mm; Pin fin pitch: 1.5 mm; Pin fin height: 20 mm; Base plate thickness: 2 mm
Liquid metal LM108	Bi-based alloy	Lamellar
Solder I	Sn96.5/Ag3/Cu0.5	217°C, preformed solder sheet
Solder II	Sn63/Pb37	183°C, preformed solder sheet
Solder III	Sn42/Bi58	138°C, Soldering paste

solder sheets are coated with flux and placed on the patterned DBC substrates. SiC MOSFET chips and terminal connectors are positioned in their designated locations and secured with high-temperature polyimide tape. The EM-interposers and two ac terminals are similarly soldered using SAC305 solder sheet.

TABLE VI
MECHANICAL PARAMETERS OF MATERIALS IN THE MODULES

Material	CTE ($10^{-6}K^{-1}$)	Young's modulus (GPa)	Poisson's ratio
SAC305	25	38.7	0.35
SiC	4.3	501	0.45
Copper	17	110	0.35
AlN	4.5	310	0.24

After completing the assembly of components, the first vacuum reflow soldering is performed.

Following that, the high-side chip is wire-bonded using an automatic bonding machine, resulting in three independent subassemblies: parts 1, 2, and 3. These subassemblies are then aligned and soldered together using 183°C Sn63/Pb37 preformed solder sheets in second vacuum reflow soldering, with custom fixtures to ensure alignment. Finally, the copper layer on the back of the DBC substrate is uniformly coated with 138°C Sn42/Bi58 solder paste, and a third vacuum reflow soldering process integrates the copper heatsinks. At this point, the fabricated power module is ready for PCM filling and sealing.

C. Reliability Analysis

To evaluate the reliability of the proposed module, thermomechanical simulations are conducted in COMSOL. Thermal cycling (TC) can induce higher stress due to the mismatch in coefficients of thermal expansion (CTEs). The cycle ranging from −45 °C to +125 °C (15 min dwell, 8.5 °C/min ramp) is applied for five cycles to steady state [28].

The proposed structure is compared with two configurations: a planar module with integrated PCM and a double-sided cooling (DSC) module, as shown in Fig. 13. All use SAC305 solder for attachment. The thermomechanical properties of the materials used are summarized in Table VI.

Fig. 14 shows the maximum von Mises stress curves of each chip during TC, while Table VII summarizes the maximum values at the last cycle. The maximum stress of the proposed module is 169.5 MPa, which is higher than that of the planar module (115.7 MPa), but comparable to the DSC module (153.0 MPa). The thermomechanical stress is a common issue in stacked structures and reflects a tradeoff inherent in designs

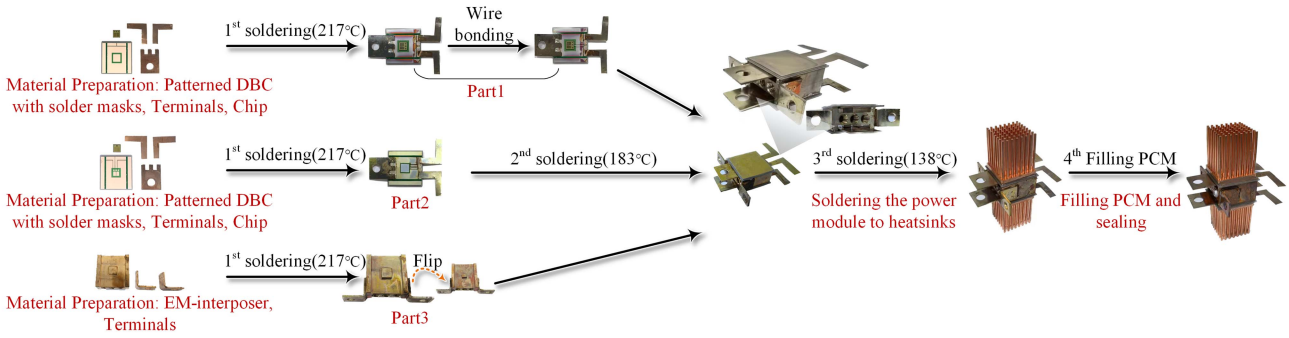


Fig. 12. Laboratory manufacturing process of the proposed power module.

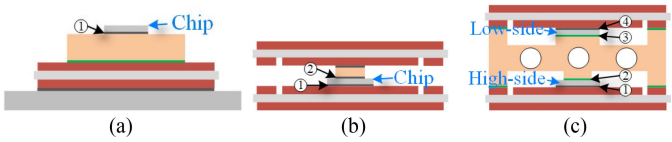


Fig. 13. Three modules for comparison: (a) planar module; (b) DSC module; and (c) proposed module.

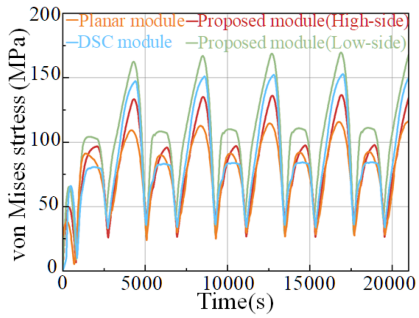


Fig. 14. Curve of maximum von Mises stress of chips under TC simulations.

TABLE VII
MAXIMUM THERMAL STRESS OF THE CHIP DURING THE LAST CYCLE

Chips	Maximum equivalent von Mises stress (MPa)
The planar module	115.7
The DSC module	153.0
Proposed module (high-side chip)	136.6
Proposed module (low-side chip)	169.5

that pursue improved thermal performance at the expense of higher mechanical stresses.

Reported Weibull characteristic strengths for SiC microtensile specimens range from 420 to 880 MPa, depending on the process [29]. Under current TC, this stress is well below the lower bound of SiC strength (420 MPa), indicating a sufficient safety margin.

Further, solder thermomechanical behavior and fatigue life are evaluated using Anand model parameters for SAC305 solder [28]. Fig. 15(a) shows the maximum plastic shear strain near the

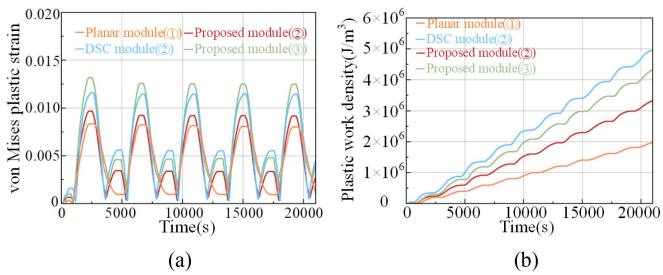


Fig. 15. TC simulation results in different solder layers. (a) Equivalent plastic strain. (b) Plastic work density.

TABLE VIII
MAXIMUM AND MINIMUM SHEER STRAIN FOR MODULES

	Max sheer strain	Min sheer strain	N_f
Planar module	0.00802	0.00094	1271.7
DSC module	0.01141	0.00047	597.7
Proposed module	0.01250	0.00217	660.3
	0.00918	0.00034	865.2

chips under identical temperature profiles. The fatigue life is predicted using the Coffin–Manson model as described in [28].

Table VIII summarizes the plastic shear strain and fatigue life of the solder layer from the last TC cycle. Results show that fatigue life differs between structures: the planar module shows the longest lifetime, approximately twice that of the proposed and DSC modules. The fatigue life of the proposed design is slightly higher than that of the DSC module, but is comparable. The plastic work density indicates the energy accumulation leading to fatigue failure. The results in Fig. 15(b) further confirm this fatigue life trend.

In summary, the proposed structure comes with slightly higher mechanical fatigue stresses than the planar module but is comparable to the conventional DSC module. Such tradeoffs between mechanical reliability and thermal performance are common in stacked designs. Improvement can be obtained by optimizing the spacer design (e.g., trenched copper plate [30] or X-shaped spacer [31]), using material replacement (e.g., MoCu or gold-plated Mo [30]), adopting silver sintering [32], or adjusting the solder layer thickness [33]. These approaches

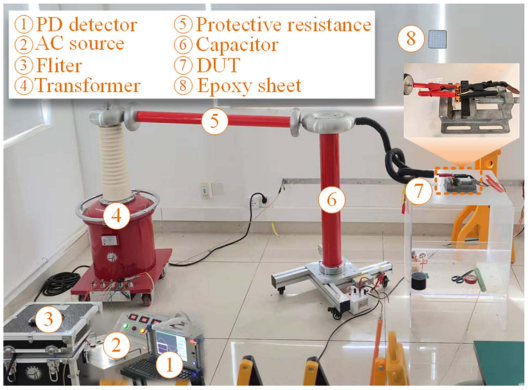


Fig. 16. PD test setup.

can effectively alleviate thermomechanical stress and enhance reliability.

V. Electrical and Thermal Tests of Power Module With Dual-Mode Thermal Management

To evaluate the electrical and thermal performance of the proposed design, three tests are conducted: a partial discharge (PD) test to assess structural insulation, a static electrical parameter test combined with a double-pulse test (DPT) to analyze the parasitic inductance and dynamic switching characteristics, and a thermal test to analyze the dual-mode thermal management effect.

A. PD Test

To verify insulation capability, PD tests are conducted. Considering that the SiC MOSFET contain a body diode that may interfere with accurate PD measurement, the chips are replaced with epoxy sheets of equivalent dimensions to test the packaging structure. As shown in Fig. 16, the PD test setup uses the pulse current method to detect discharge signals. The input voltage is increased in 0.5 kV steps, with each level held for 60 s, until noticeable PD pulses (>50 pC) are observed.

Tests are performed across three terminal pairs: dc+ to dc−, dc+ to ac, and dc− to ac. As shown in Fig. 17, the first PD event occurred between dc+ and ac terminals at 1.7 kV rms. The results confirm that the proposed module structure can provide robust insulation within the intended operating voltage range of 600–800 V.

B. Electrical Test

1) Static Electrical Measurement: After calibrating the test port with open, short, and load connections, impedance measurements are performed using an Agilent E5061B vector network analyzer. The module is then connected to a customized PCB fixture for testing. The test setup and results are shown in Figs. 18 and 19. Each measurement is repeated three times for accuracy.

From Fig. 19, the average parasitic inductance of the PCB fixture combined with the power module is 12.45 nH, while the standalone fixture measures 6.78 nH. Therefore, the power loop

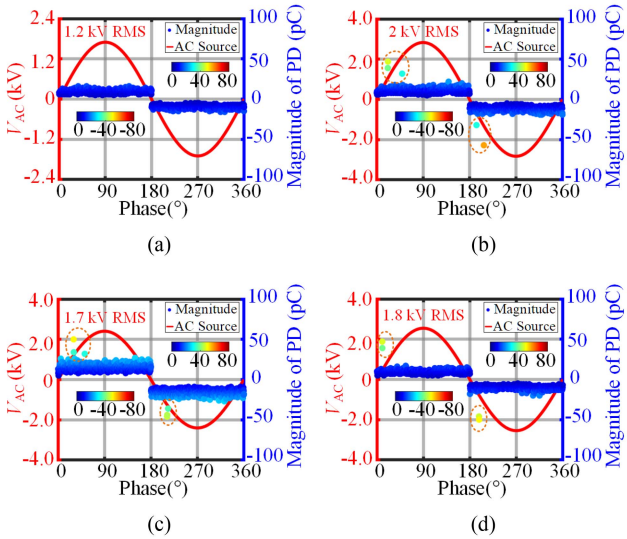


Fig. 17. PD test results: (a) initial phenomena preceding partial discharge; (b) applied voltage is 2 kV rms between DC+ and DC−; (c) applied voltage is 1.7 kV rms between DC+ and AC; and (d) applied voltage is 1.8 kV rms between DC− and AC.

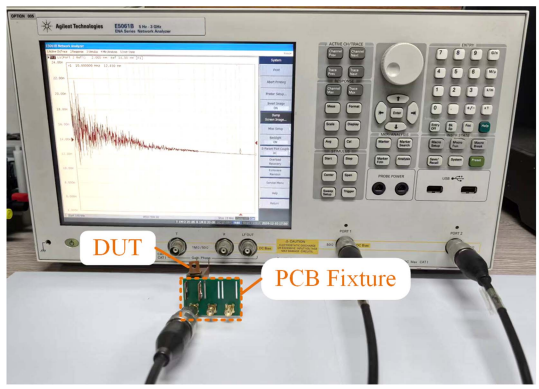


Fig. 18. Test setup of parasitic inductance.

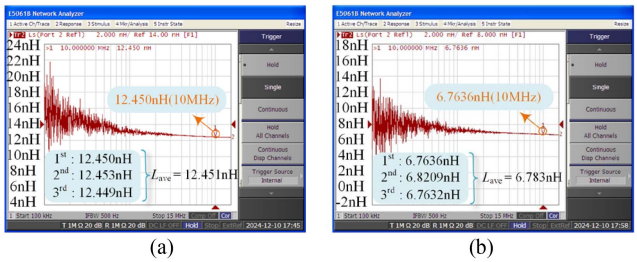


Fig. 19. Parasitic inductance test results: (a) combined test results of the DUT and PCB fixture; and (b) test results of the PCB fixture alone.

parasitic inductance of the proposed power module is 5.67 nH, which closely matches the simulation result.

2) Dynamic Electrical Measurement: To evaluate switching performance and parasitic inductance, a DPT was conducted. The test schematic is shown in Fig. 20, and the parameters are listed in Table IX.

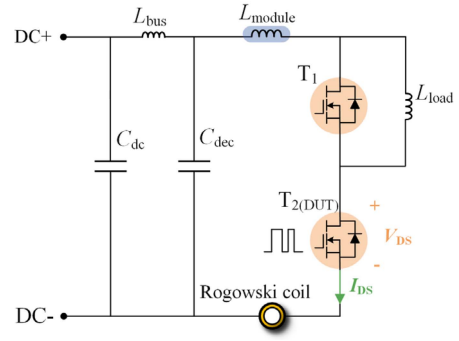


Fig. 20. Schematic of the DPT.

TABLE IX
PARAMETERS OF THE DPT TEST CIRCUIT

Parameters	Value
C_{dc}	45 μF, 1100 V
L_{load}	400 µH
V_{dc}	600 V
R_G	5 Ω

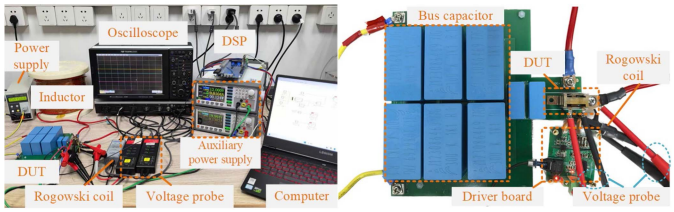


Fig. 21. DPT setup: (a) hardware setup and (b) module connection.

During testing, the gate and Kelvin source of the high-side chip were shorted, while the gate of the low-side chip was driven with +18 V during turn-ON and −3 V during turn-OFF. The experimental setup is shown in Fig. 21.

At a dc bus voltage of 600 V, a load current of 80 A, and with a 5 Ω external gate resistor, the switching waveforms are shown in Fig. 22. The maximum drain-source voltage overshoot is 41.8 V, less than 7% of the bus voltage. The $|dv_{DS}/dt|$ is 24.6 V/ns for the turn-ON and 31.9 V/ns for the turn-OFF transients, while the $|di_{DS}/dt|$ values are 6.6 and 6.0 A/ns, respectively.

The parasitic inductance can be alternatively calculated by the voltage overshoot and current variation rate during the turn-OFF transient [34] or by the voltage oscillation during turn-OFF transient [35]

$$L_{DS} = \frac{\Delta v_{DS}}{di_{DS}/dt} \tag{9}$$

$$L_{DS} = \frac{1}{4 \cdot \pi^2 \cdot {f_v}^2 \cdot C_{oss}} \tag{10}$$

where Δv_{DS} represents the voltage overshoot. C_{oss} is the output capacitance (270 pF), which can be obtained from the *C-V* curve. f_v is the voltage oscillation frequency during the turn-OFF transient, calculated as 1/8.7 ns from Fig. 22.

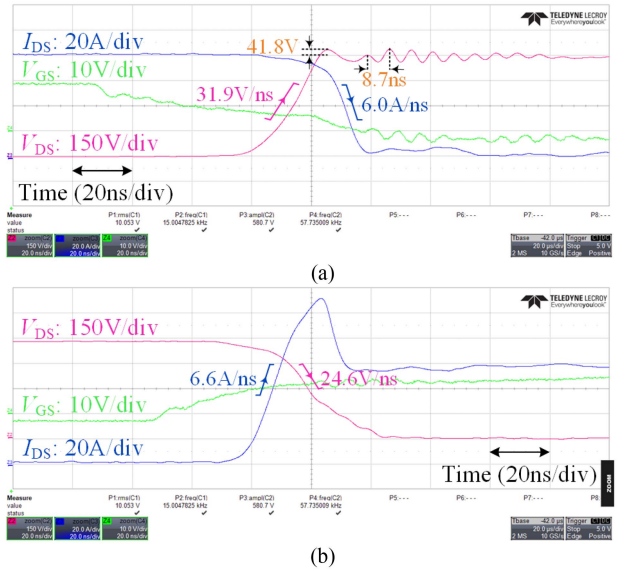


Fig. 22. DPT waveform: (a) V_{GS}, V_{DS}, and I_{DS} waveforms for the turn-OFF transient; and (b) V_{GS}, V_{DS}, and I_{DS} waveforms for the turn-ON transient.

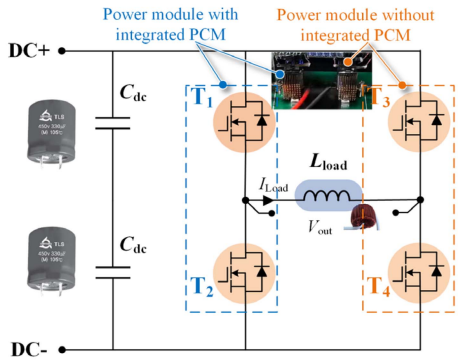


Fig. 23. Test circuit diagram for chip temperature measurement.

The loop parasitic inductances calculated based on (9) and (10) are 7 and 7.1 nH, respectively, with deviations of less than 1.5 nH from the static electrical test results, probably due to probe connection and measurement errors. These results demonstrate the effectiveness of the proposed module in achieving improved switching performance. In electrical tests, the DPT measurement best represents the module's parasitic inductance in practical application, with the static measurement as a complementary verification.

C. Thermal Tests

As shown in Fig. 23, a full H-bridge inverter circuit is used to validate the proposed dual-mode thermal management of the PCM-integrated power module. The experimental setup, shown in Fig. 24, is built under natural air-cooling condition to ensure that the chip temperature is in the required range. The two half-bridge modules are of the same design but one is filled with PCM and the other is not. The chip temperature curve and power module temperature distribution are captured

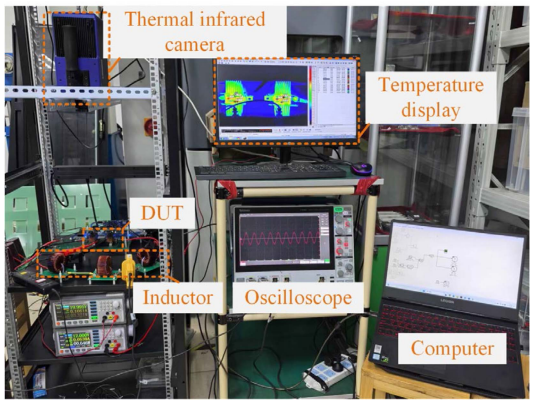


Fig. 24. Experimental setup for chip temperature measurement.

TABLE X
EXPERIMENTAL SETUP SPECIFICATIONS

Power module with integrated PCM	Rating 80 A/1200 V
Power module without integrated PCM	Rating 80 A/1200 V
Power supply	Rating 25 A/800 V
Inductor	1.5 mH, 100 A
Capacitor	1500 μF, 900 V
Thermal infrared camera	Scan frequency: 100 Hz

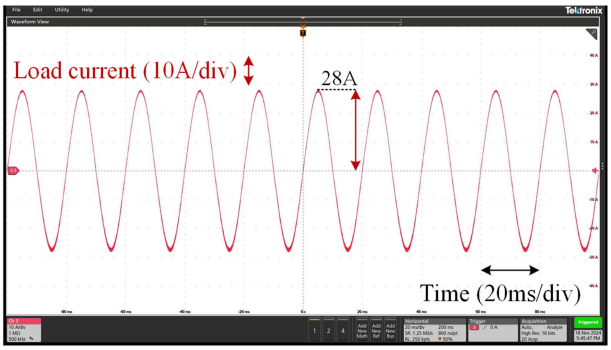


Fig. 25. Output current waveform of the experimental platform.

by a calibrated infrared camera. Detailed specifications of the experimental setup are listed in Table X.

This experimental study focuses on evaluating the thermal characteristics of the power module. For safety reason, the dc voltage is set to 50 V and the switching frequency is maintained at 20 kHz. The amplitude of the 50 Hz ac current is adjusted by varying the PWM modulation index. A sample output current waveform, with a peak value of 28 A (50 Hz), is illustrated in Fig. 25. This is taken as the rated current of the power module because the cooling has been reduced in the experiment and the chip temperature reaches about 100°C. It is believed that this reduced current and cooling would not invalid the logic to test the PCM effect during OC transient and its influence on the steady-state thermal resistance.

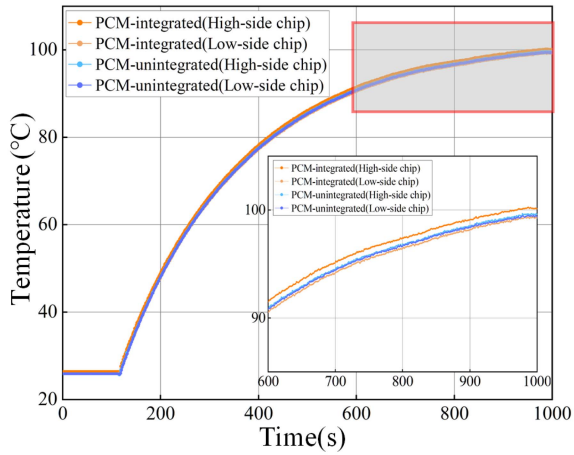


Fig. 26. Temperature response of the DUT measured by the thermal infrared camera with the load current peak held at 28 A.

TABLE XI
REDUCTION IN MAXIMUM DEVICE TEMPERATURE FOR VARIOUS POWER PULSE DURATION (EXPERIMENTAL RESULTS)

Duration(s)	Reduction in T_{jmax} of high-side chip (°C)	Reduction in T_{jmax} of low-side chip (°C)
3	2.45	2.7
5	4.2	4.8
10	10.6	10.8

The thermal infrared camera is utilized to simultaneously measure the temperature distributions of two devices under test (DUT), one with PCM integration and the other without, at a sampling frequency of 100 Hz (frames per second). The thermal infrared camera was taken from the drive side of the proposed power module, providing a clear view of the chip's side and the temperature of the surrounding spacer area. Due to the high thermal conductivity of the SiC MOSFET chip and copper, the measured temperature, despite some error, can approximate the actual junction temperature very well. Fig. 26 shows the temperature response of the DUT as it transitions from room temperature to thermal steady state under a load current of 28 A peak. The progressive surface temperature distribution during the heating process is illustrated in Fig. 27.

As shown in Fig. 26, the temperatures of the high-side and low-side chips in both power modules are well-matched, with the two temperatures being almost identical, which agrees with previous simulations. Fig. 27 presents the progressive thermal images during the transition to thermal steady state, indicating that the steady-state thermal performance of the proposed packaging design is unaffected by PCM integration.

Next, the short-term OC capability of the DUTs is investigated. With the test setup unchanged and the device temperatures stabilized at approximately 100°C, the PWM modulation index was adjusted to increase the load output current to three times of the initial value, i.e., to 81 A. Fig. 28 shows the output current waveform during the test. An infrared thermal camera with a 100 Hz sampling rate is again used to track the device temperature.

The temperature response curves for different OC durations are shown in Fig. 29. Table XI summarizes the maximum chip

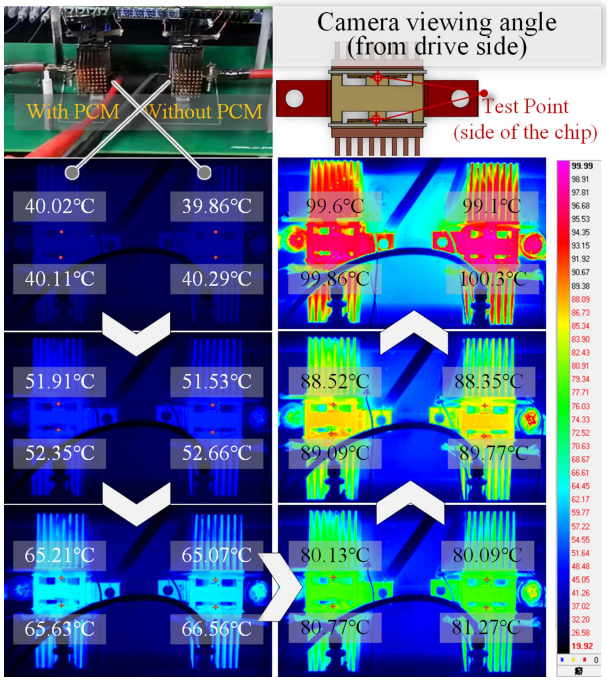


Fig. 27. Progressive IR images of DUT's surface temperature at 28 A (peak).

temperature reduction for each power pulse duration. This is due to PCM.

The results indicate that the PCM-integrated power module effectively suppresses the rapid chip temperature rise through the phase change effect, significantly reducing the slope of the chip temperature curve. During the 10 s OC duration, the integrated PCM lowers the device temperatures of the high- and low-side chips by approximately 11°C. Furthermore, around the 6th second of the OC, the slope of the chip temperature curve for the PCM-integrated power module increases rapidly again, becoming similar to that of the power module without PCM. This is because the PCM has fully melted by this point and can no longer absorb additional latent heat. The overall trend of change of the measured device temperature curve is consistent with the simulation. The temperature difference between the high- and low-side chips during the OC is primarily due to the slight asymmetry in the proposed packaging structure, which has been analyzed in Section III-B.

The critical junction temperature of the SiC device is assumed to be 175°C. As shown in Fig. 29(c), once the PCM is fully melted, the temperature rise rate becomes nearly identical to that of the baseline and follows an approximately linear trend. Considering that the high-side chip exhibits the higher junction temperature, linear fitting was performed on the temperature curves of the high-side chip for both modules after entering the linear stage, yielding slopes of $k_{\text{PCM-unintegrated}} = 3.2$ and $k_{\text{PCM-integrated}} = 2.8$, respectively. For the module without PCM, the device temperature at the 10 s OC condition is $T_{\text{10s-OC, max}} = 145.4$ °C. If the OC persists, the time to reach the critical temperature is calculated using (11) as $t_1 = 9.3$ s. For the PCM-integrated module, the corresponding time is t_2 = 14.4 s. Thus, PCM extends the safe operating time before reaching the critical junction temperature by about 5.1 s

$$t = \frac{T_{\text{critical}} - T_{\text{10s-OC,max}}}{k}. \tag{11}$$

TABLE XII
MAXIMUM DEVICE TEMPERATURE FOR VARIOUS POWER MODULE UNDER 3 P.U., 10 S OVERCURRENT CONDITION

Modules	Maximum chip temperature (°C)
The planar module	152.5 (low-side chip)
Proposed module (without PCM)	145.4 (high-side chip)
Proposed module (with PCM)	134.8 (high-side chip)

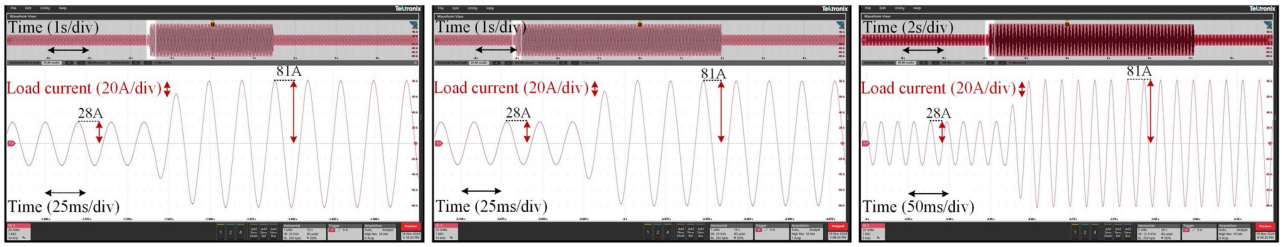
Additionally, Fig. 30 shows the temperature response of the conventional planar module under the same OC. Before the OC, high-side and low-side chip temperatures are about 101 °C, rising to 151 °C and 152.5 °C during the 10 s OC. Table XII summarizes the maximum chip temperatures of different modules. Compared with the conventional planar module, the proposed structure achieves a 17.7 °C reduction with PCM. Even without PCM integration, its maximum chip temperature remains lower than that of the planar module, mainly due to its lower thermal resistance and the additional thermal capacity provided by the large copper EM-interposer.

To emphasize the innovation and practical value of the proposed PCM integration design, a benchmark comparison of PCM-based temperature suppression strategies is conducted. Considering the differences in test conditions, PCM volume and structural design, Table XIII summarizes their temperature reduction and characteristics under OC conditions.

Further, to assess the thermal response of the proposed module under repeated OC stresses, the output current alternated between 23 and 76 A, each for 10 s, forming 20 s stress cycles. The temperature response is shown in Fig. 31. Under cyclic loading, the device's temperature fluctuated periodically and gradually stabilized into a steady oscillation. During the five cycles starting from $t = 130$ s, the PCM exhibited a clear thermal buffering effect. However, beginning with the sixth cycle, the buffering effect significantly diminished. This is attributed to the continuous accumulation of heat, which causes the device temperature to rise, keeping the PCM in a fully melted state for an extended period. Consequently, it loses the phase change thermal buffering capability as a high heat capacity material.

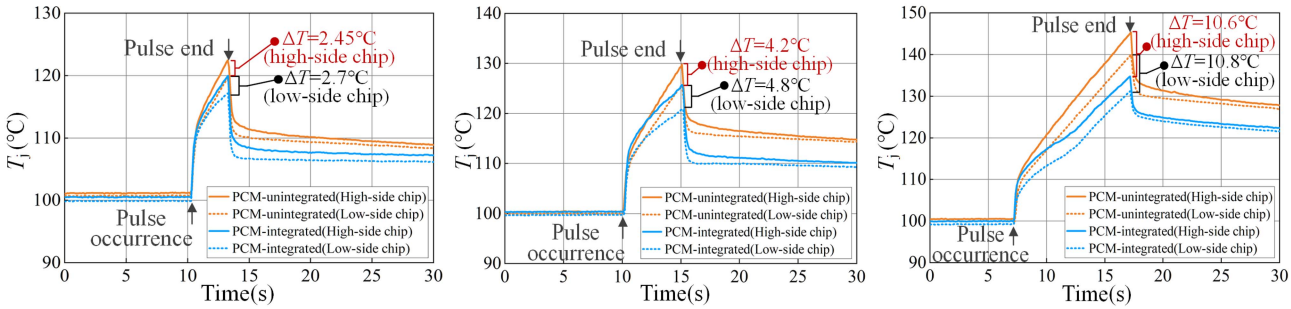
The test is further adjusted with output current alternating between 17 and 62 A, again each for 10 s. The temperature response is shown in Fig. 32. The PCM consistently exhibits thermal buffering effect. This is because the temperature variation allowed the PCM to resolidify between cycles, thereby maintaining its phase change thermal buffering capability.

Repetitive transient tests reveal the limitation of PCM's thermal buffering: under certain OC conditions [e.g., the 10 s case in Fig. 28(c)], the PCM fully melts at about 6 s, at which point the buffering effect ceases, and the temperature rise rate accelerates, matching that of the baseline. However, if the device temperature decreases sufficiently after the OC to allow PCM to resolidify,



(a) (b) (c)

Fig. 28. Output current transient waveforms of the experimental platform: (a) 3 s overcurrent duration; (b) 5 s overcurrent duration; and (c) 10 s overcurrent duration.



(a) (b) (c)

Fig. 29. Device temperature response of power modules with and without integrated PCM measured by IR camera: (a) 3 s overcurrent duration; (b) 5 s overcurrent duration; and (c) 10 s overcurrent duration.

TABLE XIII
BENCHMARK COMPARISON BETWEEN DIFFERENT SOLUTION

	Overcurrent conditions	Reduced temperature	Filling hole size	Characteristics
Dual-mode PCM integration design	3 p.u., 10 s	~11°C	3 × M4 × 18 mm	Dual-mode thermal management and low parasitics via 3-D design
Conventional PCM integration	3 p.u., 4 s [17] 1.5 p.u., 30 s [18]	T_j remains approximately at 130°C	4 × M2 × 25 mm	Only focuses on thermal buffering effect; larger parasitics
	2.4 p.u., 3 s [25]	~20°C	3 × M4 × 18.5 mm	
	2 p.u., 10 s [21]	~8°C	4 × M5 × 17 mm	
TEC+PCM	1.5 p.u., 60 s [16]	T_j remains approximately at 130°C	Embedded within the heatsink	Additional power, slow response

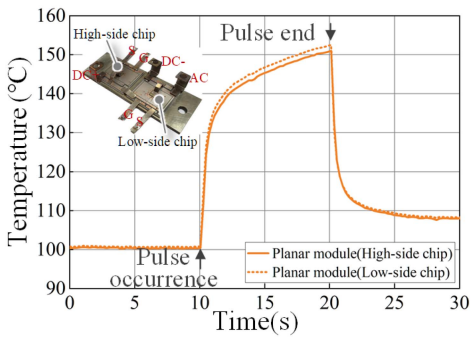


Fig. 30. Device temperature response of the planar module under 3 p.u., 10 s overcurrent condition.

the thermal buffering effect can be reactivated in subsequent events.

VI. RELIABILITY EVALUATION

To verify the reliability of the proposed module, two samples each of the proposed module and the DSC module are fabricated for TC tests. TC is employed to directly evaluate the effect of mismatched material CTE on the reliability of the packaging structure and material interfaces, independent of circuit topology.

The DSC module serving as a reference, as shown in Fig. 13(b). The thermal cycle ranging from −45°C to + 125°C (15 min dwell, 8.5°C/min ramp) and the test setup is shown in Fig. 33.

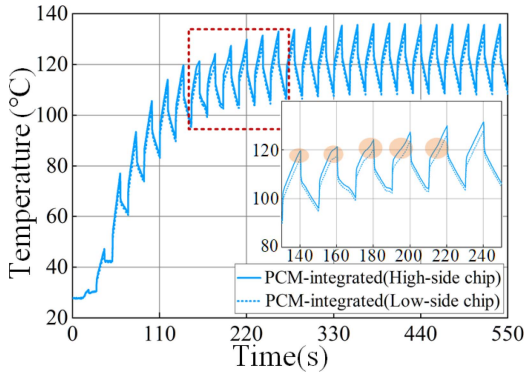


Fig. 31. Device temperature response of power module with integrated PCM measured by IR camera (output current cycles between 23 and 76 A every 10 s).

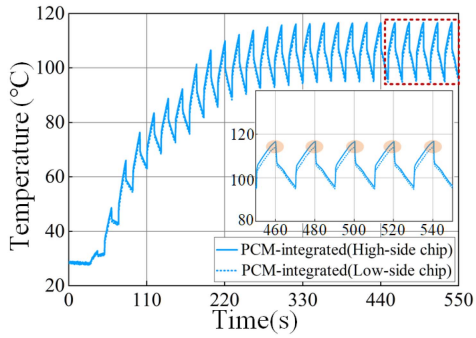


Fig. 32. Device temperature response of power module with integrated PCM measured by IR camera (output current cycles between 17 and 62 A every 10 s).

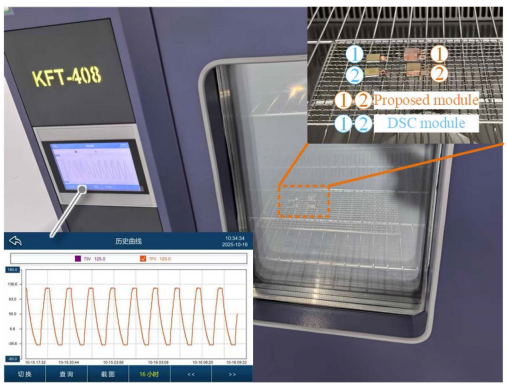


Fig. 33. Thermal cycling test setup.

The ON-state resistance (R_{dsON}) of each SiC MOSFET is measured with a B1506A curve tracer as the initial value before testing. R_{dsON} is then recorded every 10 cycles up to 100 cycles. Fig. 34 shows the evolution of R_{dsON} during cycling. The results indicate that for both the proposed and DSC modules, the variation in R_{dsON} remained below 5%, with no significant degradation in performance. After 100 cycles, the leakage current measured at 1.2 kV remained within the datasheet limit (5 μA) for all samples, as shown in Fig. 35.

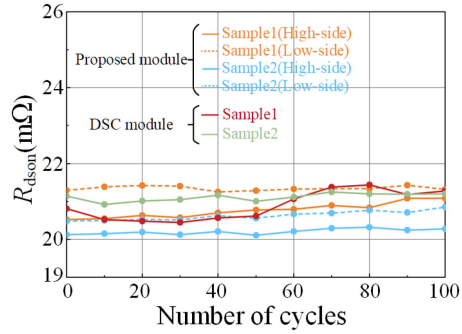


Fig. 34. Evolution of the ON-state resistance for different module samples during thermal cycling ($V_{\mathrm{GS}} = 18$ V; $I_{\mathrm{DS}} = 60$ A).

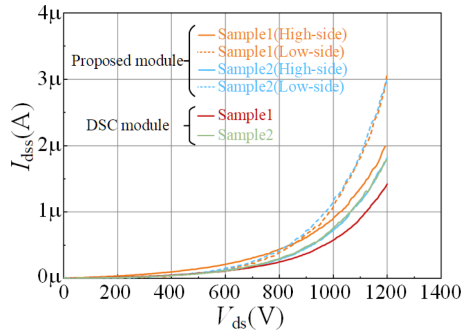


Fig. 35. Leakage current measurements after thermal cycling ($V_{\mathrm{GS}} = 0$ V).

These preliminary results indicate that the proposed module exhibits comparable reliability to the conventional DSC structure within 100 cycles. This TC aims to evaluate early-stage performance under thermal stress rather than full lifetime behavior, providing initial validation of the proposed module's reliability for practical applications.

VII. Conclusion

This article proposes an SiC half-bridge power module with dual-mode thermal management by integrating PCM in the non-primary heat conduction path, enabling independent responses to the steady-state and OC transient conditions. Through simulation, fabrication, and testing of the prototype, it is demonstrated that the proposed PCM integration improves the thermal management under the transient OC condition without compromising the steady-state heat dissipation performance. Transient tests show that under a 10 s OC condition, the phase change effect reduces the device temperature by approximately 11°C. The thermal buffering performance of the PCM under repeated transient events is also evaluated. Moreover, static and dynamic tests confirm that the module's parasitic inductance is low (5.67 and 7 nH, respectively). Simulation gives a value of 5.25 nH. This highlights its potential in high switching frequency applications. After 100 thermal cycles, the proposed module showed similar ON-state resistance and leakage current behavior as the conventional double-sided module, indicating comparable reliability.

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