Dual-Mode Isolated DC–DC Converter With Fixed-Frequency Circulant Duty Cycle Modulation for Wide Input Voltage Range

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***Abstract*—This article proposes a dual-mode isolated dc–dc (DMIDC) converter for wide input voltage range applications. Under the fixed-frequency circulant duty cycle modulation, the two operation modes of the converter and the output voltage regulation can be achieved by only controlling the total duty cycle of all lower switches of the half bridge modules (HBMs) in each bridge arm as a single control variable. Also, self-balancing of HBM capacitor voltages and zero-voltage switching of all switches can be realized. The interleaved parallel structure based on series-connected HBMs reduces input current ripple and lowers the voltage stress of switches. Compared with the *LLC* resonant converters with variable structure and variable frequency control, the proposed scheme only needs to control the total duty cycle without the need for other control variables and additional input voltage sampling circuit to achieve mode transition within a wide input voltage. Moreover, compared with other wide voltage range resonant converters, the proposed DMIDC converter not only has better load characteristics but also has lower voltage stress on primary devices. Finally, the performance of the proposed DMIDC is validated through experiments on a 400 W prototype with 75–300 V input and 330 V output.**

***Index Terms*—Dual-mode isolated dc–dc (DMIDC) converter, inherent balancing ability, wide input voltage range, zero-voltage switching (ZVS).**

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I. Introduction

ISOLATED dc–dc converters play an important role in applications such as renewable energy generation [1], [2], space electric propulsion systems [3], [4], and electric vehicles [5], [6]. For various isolated dc–dc converters, *LLC* resonant converter has become a promising candidate because of its advantages in soft switching performance and high efficiency. Generally, a wide frequency variation range is required in a traditional *LLC* converter with variable frequency control to meet the needs of a wide voltage gain range, which adds difficulties and challenges to the optimization design of magnetic components and filters and the realization of high efficiency [7], [8].

In order to achieve a tradeoff between voltage gain extension and switching frequency variation range, many optimized converter structures and modulation schemes have been studied to obtain a suitable operating frequency range of *LLC* converter. In [9], a secondary-side pulsewidth modulation (PWM) modulated *LLC* converter is proposed, which achieves voltage regulation capability by changing the duty cycle of the secondary switch. However, the switching loss is increased due to the large turn OFF current. A converter using phase-shift control strategy to extend the voltage gain is proposed in [10]. However, a wide voltage variation range leads to an increase in the adjustment range of phase-shift angle, which adds challenges to the realization of zero-voltage switching (ZVS) in switching devices. The quasi-single-stage converter proposed by [11] and [12] is an attractive solution to achieve a wide voltage gain range. In these schemes, the voltage gain is regulated by a nonisolated dc–dc stage and the *LLC* stage acts as a dc transformer. However, the voltage regulation capabilities of these converters are limited because the nonisolated dc–dc converter in each solution only processes part of the power. The single-stage boost-*LLC* converter in [13], [14], and [15] can achieve wide voltage gain by changing the duty cycle of the power switching devices. However, the switches need to withstand large voltage stress when the duty cycle is adjusted.

Another popular solution to achieve wide voltage gain is for the converter to operate in multiple modes. In [16], a converter with voltage-doubler rectifier mode and voltage-quadrupler rectifier mode is proposed, whose voltage gain can be doubled by changing the rectifier structure. But the control complexity is increased. In [17], a converter with two resonant tanks and

a three-phase arm on both the primary and secondary sides is proposed, and its voltage gain range is extended through three working modes. During mode transition, the switching frequency of the *LLC* converter is set around the required operating frequency, realizing smooth mode transition. However, the required switching frequency is different under different loads, so the performance may vary with load changes. In [18], a wide range ISOP-*LLC* converter with coupled inductor is proposed. In this scheme, by changing the phase-shift angle between the two modules, the converter can operate in high gain and low gain modes. However, the proposed scheme introduces many power devices and magnetic components. An integrated boost-*LC*-resonant flyback converter is proposed in [19], which can operate in multimode and has a weakly dependent load in high gain mode. However, the primary switching devices are subject to large voltage stress. A current-fed *LLC* resonant converter with low voltage stress is proposed in [20]. The semiconductor devices of this converter always bear a voltage stress equal to the input voltage throughout the entire voltage range, and the self-balancing of half bridge module (HBM) capacitor voltages can be achieved through a circulant phase-shift control strategy. However, this converter has only one operating mode, and it is difficult to achieve ZVS over a wide voltage range.

The main contribution of this article is to propose dual-mode isolated dc–dc (DMIDC) converter suitable for wide voltage range applications. Through fixed-frequency circulant duty cycle modulation scheme, the two voltage gain modes of the DMIDC converter can be realized by simply modulating the total duty cycle of all lower switches in each arm as a single control variable. When the total duty cycle is (00.5), the converter operates in low voltage gain mode. When the total duty cycle is (0.51), it operates in high voltage gain mode. For the proposed DMIDC, ZVS of all switches and inherent balancing ability of the HBM capacitor voltages are obtained. Therefore, there is no need to add extra HBM capacitor balancing circuits to evenly distribute the capacitor voltage, thus reducing cost and volume. The interleaved unit with series-connected HBMs not only reduces the input current ripple, but also achieves low voltage stress of switching devices. Compared with the existing *LLC* resonant converters with variable structure and variable frequency control, the proposed scheme has simple control and only needs to control the total duty cycle to achieve mode transition for a wide input voltage, without requiring other control variables and adding input voltage sampling circuit. In addition, compared with other existing wide gain range resonant topologies, the proposed DMIDC not only has a weaker dependent load but also has lower voltage stress on switching devices and moderate component counts, which can decrease costs and improve power density and efficiency.

The rest of this article is organized as follows. Section II describes the working mode configuration of the proposed DMIDC converter and the operating principles in each mode. Section III gives the self-balancing characteristics of HBM capacitor voltages, voltage gain, resonant tank parameters design considerations, voltage stress analysis of switching devices, and ZVS analysis. Section IV shows the experimental and comparative results. Finally, Section V concludes this article.

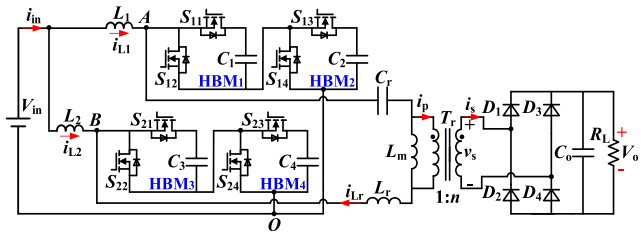

Fig. 1. Power circuit of the proposed DMIDC.

II Working Principle of the Proposed Converter

A. Description of the Proposed DMIDC

The power circuit of the proposed DMIDC is shown in Fig. 1. There are two bridge arms and a resonant tank on the primary side. Each bridge arm consists of an input inductor (L_1 or L_2) and two HBMs ($\mathrm{HBM}_{1,2}$ or $\mathrm{HBM}_{3,4}$), and the two bridge arms are interleaved. For each HBM unit, it consists of two switching devices and one capacitor. The secondary side adopts a full bridge rectifier structure composed of diodes D_1–D_4. The turns ratio of the transformer is $T_r = n{:}1$.

To facilitate analysis of the proposed DMIDC, the sum of the duty cycles of all lower switching devices on the same arm within each fundamental period T_e is defined as d_T, and $d_T = d_{S12} + d_{S14} = d_{S22} + d_{S24}$, where d_{S12}, d_{S14}, d_{S22}, and d_{S24} represent the duty cycles of the lower switches S_{12}, S_{14}, S_{22}, and S_{24}, respectively. The junction capacitors C_{oss11}–C_{oss14} of S_{11}–S_{14} and the junction capacitors C_{oss21}–C_{oss24} of S_{21}–S_{24} are both equal to C_{oss}, and the parasitic capacitors C_{d1}–C_{d4} of diodes D_1–D_4 are all represented by C_d. The HBM capacitors C_1–C_4 are equal, and the inductors L_1 and L_2 are also equal.

B. Mode Definition of the Proposed DMIDC

According to the range of the total duty cycle d_T of the lower switches in each arm within a T_e, the primary switches can be configured in different operating modes, corresponding to different voltage gains. Depending on the voltage gain, these working modes can be divided into high voltage gain (HVG) mode and low voltage gain (LVG) mode. The key operating waveforms of each mode are presented in Fig. 2 and a detailed description of these modes is shown in Table I.

When the total duty cycle d_T within a T_e meets $0.5 < d_T < 1$, the converter operates HVG mode. When d_T within a T_e satisfies $0 < d_T < 0.5$, the converter operates LVG mode. The dividing point between HVG mode and LVG mode is $d_T = 0.5$. It is worth noting that the modulation scheme in Fig. 2 and Table I can not only regulate the output voltage V_o, but also guarantee that the capacitor voltages V_{C1}–V_{C4} of HBM_1–HBM_4 are self-balanced in both gain modes (i.e., $V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_C$).

It can be seen from Fig. 2 that the circulant period T_s is twice that of fundamental period T_e. V_{GS11}–V_{GS14} and V_{GS21}–V_{GS24} represent the driving signals of switches S_{11}–S_{14} and S_{21}–S_{24} in the upper and lower bridge arms, respectively. Since the phase difference between the driving signals of two arms is 180°, the driving signals of the upper arm are selected for detailed analysis the modulation strategy of each mode within a T_s.

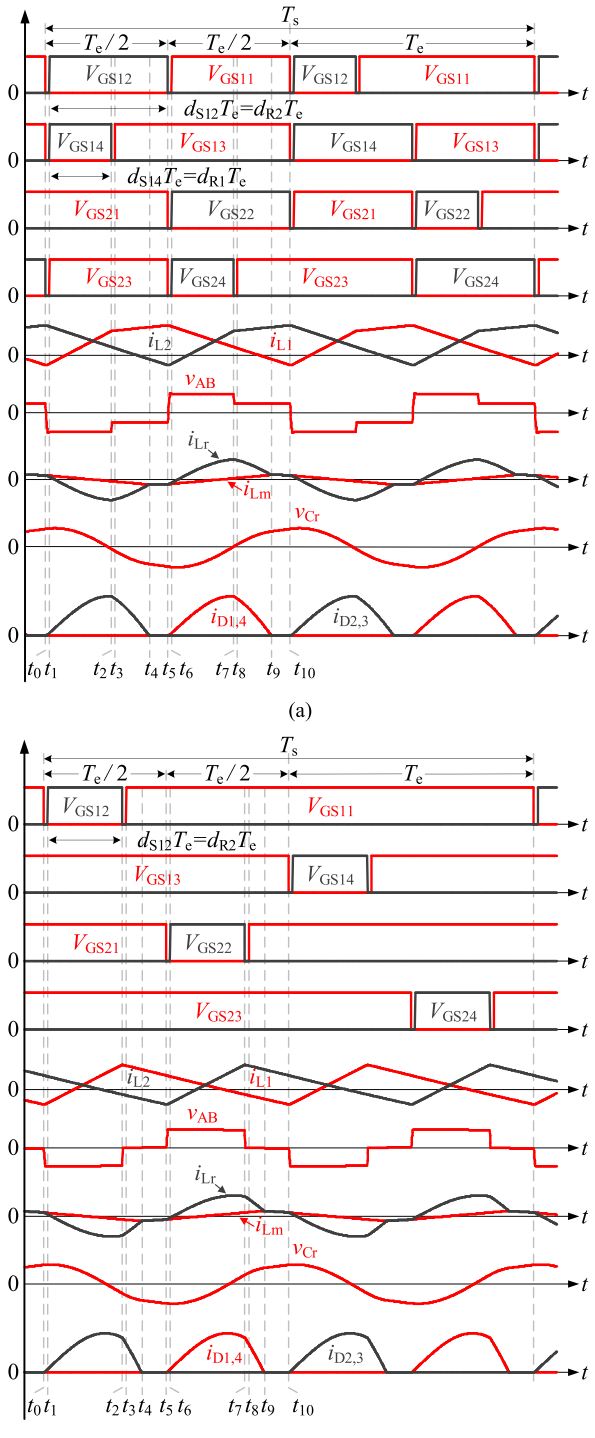

Fig. 2. Key waveforms of each mode. (a) HVG: $0.5 < d_T < 1 (0 < d_{R1} < 0.5, d_{R2} = 0.5)$. (b). LVG: $0 < d_T < 0.5 (d_{R1} = 0, 0 < d_{R2} < 0.5)$.

1). HVG Mode: $0.5 < d_T < 1$: The operating waveforms of HVG mode are given in Fig. 2(a). As seen, one of the lower switches S_{12} and S_{14} in the upper arm always operates with a fixed duty cycle of 0.5 (i.e., $d_{R2} = 0.5$), and the other works with a regulated duty cycle d_{R1} and $0 < d_{R1} < 0.5$. And in this mode, d_T can be expressed as $d_T = d_{S12} + d_{S14} = 0.5 + d_{R1}$.

TABLE I
OPERATING MODES OF THE PROPOSED DMIDC CONVERTER

Circulant period	Time	Total duty cycle d_T ($d_T=d_{S12}+d_{S14}=d_{S22}+d_{S24}$)	Gain mode
$T_s=2T_e$	First T_e	$0.5<d_T<1$ $d_{S12}=0.5$, $d_{S14}=d_{R1}$, $PSD_{S12, S14}=0$ $d_{S22}=0.5$, $d_{S24}=d_{R1}$, $PSD_{S22, S24}=0.5$	HVG
	Second T_e	$0.5<d_T<1$ $d_{S12}=d_{R1}$, $d_{S14}=0.5$, $PSD_{S12, S14}=0$ $d_{S22}=d_{R1}$, $d_{S24}=0.5$, $PSD_{S22, S24}=0.5$	HVG
$T_s=2T_e$	First T_e	$d_T=0.5$ $d_{S12}=0.5$, $d_{S14}=0$, $PSD_{S12, S14}=0$ $d_{S22}=0.5$, $d_{S24}=0$, $PSD_{S22, S24}=0.5$	Boundary
	Second T_e	$d_T=0.5$ $d_{S12}=0$, $d_{S14}=0.5$, $PSD_{S12, S14}=0$ $d_{S22}=0$, $d_{S24}=0.5$, $PSD_{S22, S24}=0.5$	Boundary
$T_s=2T_e$	First T_e	$0<d_T<0.5$ $d_{S12}=d_{R2}$, $d_{S14}=0$, $PSD_{S12, S14}=0$ $d_{S22}=d_{R2}$, $d_{S24}=0$, $PSD_{S22, S24}=0.5$	LVG
	Second T_e	$0<d_T<0.5$ $d_{S12}=0$, $d_{S14}=d_{R2}$, $PSD_{S12, S14}=0$ $d_{S22}=0$, $d_{S24}=d_{R2}$, $PSD_{S22, S24}=0.5$	LVG

PSD is short for phase-shift duty cycle.

2). LVG Mode: $0 < d_T < 0.5$: The key waveforms of LVG mode are given in Fig. 2(b). From Fig. 2(b), there is always one device in S_{12} and S_{14} whose gate signal is 0 (that is, $d_{R1} = 0$), and the other one operates with an adjustable duty cycle d_{R2} and $0 < d_{R2} < 0.5$. In this mode, d_T satisfies $d_T = d_{S12} + d_{S14} = d_{R2}$.

C. Operating Principle in HVG Mode

As can be seen in Fig. 2(a), there are ten switching states t_0–t_{10} in one T_e. Due to the symmetry of the working state within each T_e, this article only depicts the first five states (t_0–t_5), and the latter five states (t_5–t_{10}) can be obtained based on the same principle. In addition, the current-flow paths corresponding to the DMIDC in these intervals are plotted in Fig. 3.

State 1 [t_0–t_1] [see Fig. 3(a)*]:* At t_0, switches S_{11}, S_{13} and S_{24} are turned OFF. When the energy stored in C_{oss12}, C_{oss14}, and C_{oss23} is fully discharged, their body diodes are turned ON, which creates the conditions for S_{12}, S_{14}, and S_{23} to achieve ZVS in the next interval.

State 2 [t_1–t_2] [see Fig. 3(b)*]:* At t_1, switches S_{12}, S_{14}, and S_{23} obtain ZVS conduction. The voltages across inductors L_1 and L_2 are V_{in} and $V_{in}-2V_C$, respectively, which are valid for both states 1 and 2. Moreover, L_1 and L_2 satisfy $L_1 = L_2 = L_b$. Thus, the current i_{L1} flowing through the L_1 increases linearly from the initial value $i_{L1}(t_0)$ with a slope of V_{in}/L_b while the current i_{L2} flowing through the L_2 decreases linearly from the initial value $i_{L2}(t_0)$ with a slope of $(2V_C-V_{in})/L_b$. Therefore, the currents i_{L1}, i_{L2} and the differential equations of various physical quantities in the resonant tank (including the resonant inductor current i_{Lr}, the resonant capacitor voltage v_{Cr} and the magnetizing current i_{Lm}) in states 1 and 2 can be derived by (1) and (2).

State 3 [t_2–t_3] [see Fig. 3(c)*]:* At t_2, S_{14} is turned OFF. S_{12}, S_{21}, and S_{23} continue to be turned ON. The currents i_{L1} and i_{Lr} together charge and discharge C_{oss13} and C_{oss14}, respectively. When C_{oss13} is fully discharged, the difference between the

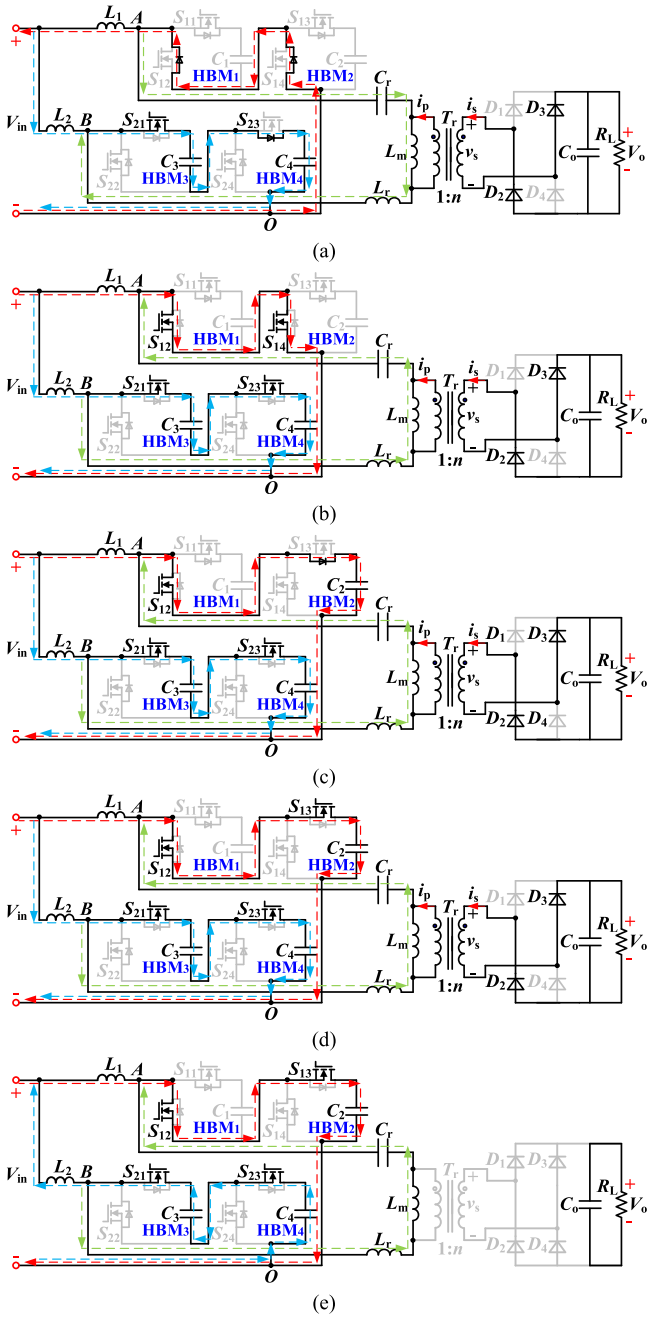

Fig. 3. Current-flow paths of the DMIDC converter in HVG mode. (a) State 1 [t_0-t_1]. (b) State2 [t_1-t_2]. (c) State 3 [t_2-t_3]. (d) State 4 [t_3-t_4]. (e) State 5 [t_4-t_5].

currents i_{L1} and i_{Lr} flows through its body diode. Therefore, it is simple to realize the ZVS of S_{13}.

State 4 [t_3–t_4] [see Fig. 3(d)*]:* At t_3, S_{13} is turned ON under ZVS condition. Within this time, the inductor L_1 is charged by

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \frac{V_{in}}{L_b}(t - t_0) \\ i_{L2}(t) = i_{L2}(t_0) - \frac{2V_C - V_{in}}{L_b}(t - t_0) \end{cases} \tag{1}$$

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{V_o/n - 2V_C - v_{Cr}(t)}{L_r} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = -\frac{V_o}{nL_m}. \end{cases} \tag{2}$$

The voltage $V_{in} - V_C$ applied across it, and the inductor L_2 is still discharged by the voltage $2V_C - V_{in}$. The input power is still delivered to the load through D_2 and D_3. Thus, i_{L2} can still be obtained from (1), and the expression of i_{L1} and the differential equations of the physical quantities i_{Lr}, v_{Cr}, and i_{Lm} in states 3 and 4 can be calculated as

$$i_{L1}(t) = i_{L1}(t_0) + \frac{V_C(d_T - 1/2)T_e}{L_b} + \frac{V_{in} - V_C}{L_b}t \tag{3}$$

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{V_o/n - V_C - v_{Cr}(t)}{L_r} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = -\frac{V_o}{nL_m}. \end{cases} \tag{4}$$

State 5 [t_4–t_5] [see Fig. 3(e)*]:* At t_4, D_2 and D_3 achieve zero current turn OFF. During this period, the current i_{L1} still increase linearly with the slope of $(V_{in} - V_C)/L_b$ and reaches its maximum value at t_5, while the current i_{L2} still decreases linearly with the slope of $(2V_C - V_{in})/L_b$ and reaches its minimum value at t_5. Also, L_m starts to resonance with C_r and L_r and the input power is no longer transmitted to the output. Therefore, i_{L2} can still be obtained from (1), and i_{L1} is still satisfies (3). The differential equations of the physical quantities i_{Lr}, v_{Cr}, and i_{Lm} can be expressed as

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{-V_C - v_{Cr}(t)}{L_r + L_m} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = \frac{di_{Lr}(t)}{dt}. \end{cases} \tag{5}$$

According to the working waveforms of HVG mode in Fig. 2(a), the volt-second balance relations of L_1 and L_2 in this mode can be, respectively, obtained by

$$\begin{cases} V_{in}(d_T - \frac{1}{2})T_e + (V_{in} - V_C)(1 - d_T)T_e = (2V_C - V_{in})\frac{T_e}{2} \\ (V_{in} - 2V_C)\frac{T_e}{2} = (V_C - V_{in})(1 - d_T)T_e - V_{in}(d_T - \frac{1}{2})T_e \end{cases}. \tag{6}$$

By simplifying (6), the mathematical relationship between the HBM capacitor voltage V_C and the input voltage V_{in} in HVG mode can be derived as

$$V_C = V_{in}/(2 - d_T) \tag{7}$$

$$\begin{cases} i_{L1}(t_0) = I_{L1\_HVG} = \frac{I_{in}}{2} - \frac{[1+(6-4d_T)(d_T-1/2)]T_eV_C}{8L_b} \\ i_{L2}(t_0) = I_{L2\_HVG} = \frac{I_{in}}{2} + \frac{[1+4(d_T-1/2)^2]T_eV_C}{8L_b}. \end{cases} \tag{8}$$

Assuming that the average value of the input current is referred to as I_{in}, and the initial values of the currents i_{L1} and i_{L2} in the HVG mode are represented by $i_{L1}(t_0) = I_{L1\_HVG}$ and $i_{L2}(t_0) = I_{L2\_HVG}$, respectively. According to the above working principle of the proposed DMIDC, power conservation law and Fig. 2(a), the values of I_{L1_HVG} and I_{L2_HVG} can be obtained by (8).

D. Operating Principle in LVG Mode

The positive direction of each voltage and current in LVG mode is assumed to be the same as those in HVG mode, so the continuity and consistency of the analysis and derivation in DMIDC can be guaranteed. As seen in Fig. 2(b), there are also ten switching states t_0–t_{10} in one T_e. Similar to the analysis of

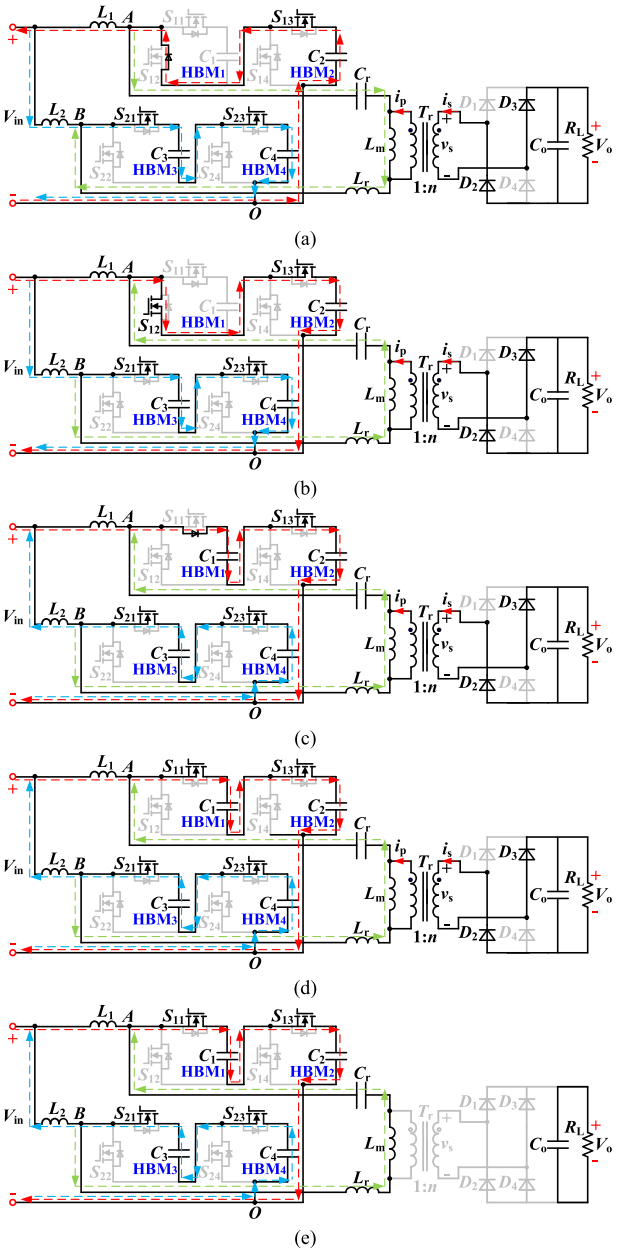

Fig. 4. Current-flow paths of the DMIDC converter in LVG mode. (a) State 1 [t_0-t_1]. (b) State2 [t_1-t_2]. (c) State 3 [t_2-t_3]. (d) State 4 [t_3-t_4]. (e) State 5 [t_4-t_5].

HVG mode, this article only selects the first five states to draw their current-flow paths, as shown in Fig. 4.

State 1 [t_0–t_1] [see Fig. 4(a)*]:* At t_0, switch S_{11} is turned OFF and S_{13}, S_{21}, and S_{23} remain ON. Due to the existence of the dead-time T_d, the switch S_{12} will not be turned ON immediately. When the energy stored in C_{oss12} is fully discharged, the body diode of S_{12} is turned ON, which is beneficial for the ZVS implementation of S_{12}.

State 2 [t_1–t_2] [see Fig. 4(b)*]:* At t_1, the ZVS of S_{12} is realized. The voltage V_{Lm} applied to the magnetizing inductor L_m is clamped by $-V_o/n$, which is satisfied for both states 1 and 2. Thus, the i_{L1}, i_{L2} and the differential equation of the physical quantities i_{Lr}, v_{Cr}, and i_{Lm} under states 1 and 2 can be given by

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \frac{V_{in}-V_C}{L_b}(t-t_0) \\ i_{L2}(t) = i_{L2}(t_0) - \frac{2V_C-V_{in}}{L_b}(t-t_0) \end{cases} \tag{9}$$

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{V_o/n - V_C - v_{Cr}(t)}{L_r} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = -\frac{V_o}{nL_m}. \end{cases} \tag{10}$$

State 3 [t_2–t_3] [see Fig. 4(c)*]:* At t_2, S_{12} is turned OFF while S_{13}, S_{21}, and S_{23} are still conducting. The charging and discharging of C_{oss11} and C_{oss12} are jointly completed by currents i_{L1} and i_{Lr}. After C_{oss11} is fully discharged, the body diode of S_{11} is turned ON, which helps to achieve ZVS of S_{11}.

State 4 [t_3–t_4] [see Fig. 4(d)*]:* At t_3, S_{11} is conducted with ZVS. The currents i_{L1} and i_{L2} decreases with the same slope $(2V_C - V_{in})/L_b$. The voltage V_{Lm} continues to be clamped by $-V_o/n$. Therefore, i_{L2} can still be obtained from (9), and i_{L1} and the differential equation of the physical quantities i_{Lr}, v_{Cr}, and i_{Lm} in states 3 and 4 can be derived as

$$i_{L1}(t) = i_{L1}(t_0) + \frac{V_{in}}{L_b} d_T T_e + \frac{V_{in} - 2V_C}{L_b}(t - t_2) \tag{11}$$

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{V_o/n - v_{Cr}(t)}{L_r} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = -\frac{V_o}{nL_m}. \end{cases} \tag{12}$$

State 5 [t_4–t_5] [see Fig. 4(e)*]:* At t_4, D_2 and D_3 are turned OFF with ZCS. The currents i_{L1} and i_{L2} still decrease at a slope of $(2V_C - V_{in})/L_b$ and i_{L2} reaches its minimum value at t_5. Also, the components involved in resonance in the resonant tank are L_m, C_r and L_r. Thus, i_{L2} can still be expressed by (9), and i_{L1} is still given by (11). The differential equation of the physical quantities i_{Lr}, v_{Cr}, and i_{Lm} can be calculated as

$$\begin{cases} \frac{di_{Lr}(t)}{dt} = \frac{-v_{Cr}(t)}{L_r + L_m} \\ \frac{dv_{Cr}(t)}{dt} = \frac{i_{Lr}(t)}{C_r} \\ \frac{di_{Lm}(t)}{dt} = \frac{di_{Lr}(t)}{dt}. \end{cases} \tag{13}$$

Based on the working waveforms of LVG mode in Fig. 2(b), the volt-second balance equations of L_1 and L_2 in this mode can be, respectively, written by

$$\begin{cases} (V_{in} - V_C)d_T T_e = (2V_C - V_{in})(1 - d_T)T_e \\ (V_{in} - 2V_C)(1 - d_T)T_e = (V_C - V_{in})d_T T_e \end{cases}. \tag{14}$$

By simplifying (14), the mathematical relationship between the voltages V_C and V_{in} in LVG mode can be represented as

$$V_C = V_{in}/(2 - d_T). \tag{15}$$

Assuming that the initial values of the currents i_{L1} and i_{L2} in the LVG mode are expressed as $i_{L1}(t_0) = I_{L1\_LVG}$ and $i_{L2}(t_0) = I_{L2\_LVG}$, respectively. Combining the aforementioned operating principle of DMIDC, power conservation law and Fig. 2(b), the values of I_{L1_LVG} and I_{L2_LVG} can be solved as

$$\begin{cases} i_{L1}(t_0) = I_{L1\_LVG} = \frac{I_{in}}{2} - \frac{(1-d_T)d_T T_e V_C}{2L_b} \\ i_{L2}(t_0) = I_{L2\_LVG} = \frac{I_{in}}{2} + \frac{d_T^2 T_e V_C}{2L_b}. \end{cases} \tag{16}$$

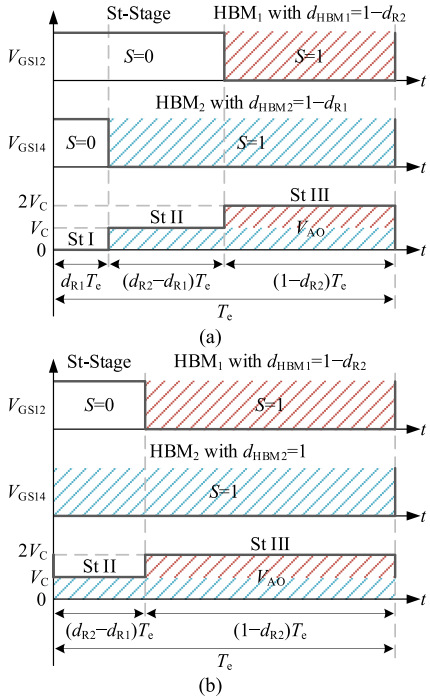

Fig. 5. Generation of upper arm voltage V_{AO} in HVG and LVG modes within the first T_{e}. (a) HVG:$0.5 < d_{\mathrm{T}} < 1 (0 < d_{\mathrm{R1}} < 0.5, d_{\mathrm{R2}} = 0.5)$. (b)LVG:$0 < d_{\mathrm{T}} < 0.5 (d_{\mathrm{R1}} = 0, 0 < d_{\mathrm{R2}} < 0.5)$.

III. Characteristics and Design Considerations

A. Self-Balancing Characteristic

One of the most attractive properties of this DMIDC is the self-balancing characteristic of the HBM capacitor voltages over the entire input voltage range. Therefore, for the HBM capacitor voltages, in order to clarify their intrinsic relationship, the mathematical relationship between them and the switching mode needs to be established [21], [22], [23]. Fig. 5 shows the generation process of upper arm voltage V_{AO} in HVG and LVG modes within the first T_{e}, where $S = 1$ and $S = 0$ means the insertion and bypass of HBM capacitor. d_{HBM1} and d_{HBM2} are defined as the ratio of the inserted-state duration of HBM capacitors C_1 and C_2 to the fundamental period T_{e}, respectively. Based on the number of HBMs connected to the circuit in the upper arm, V_{AO} with different levels is obtained. Take HVG mode as an example to analyze the generation of each level in V_{AO}. First, Stage I is defined as V_{AO} being at zero level, which means that there is no HBM inserted. Then, the HBM_2 in the upper arm is connected, causing the V_{AO} to be V_{C2}. Hence, stage II is obtained. After that, another HBM (i.e., HBM_1) in the upper arm is also connected in the circuit, the level of V_{AO} reaches the maximum and stage III originates from this. The definitions of each stage here are also applicable to LVG mode, as the LVG mode is derived from HVG mode when $d_{\mathrm{R1}} = 0$. From Fig. 5, the switching vectors of each stage in the two gain modes within the first T_{e} can be expressed as

$$\begin{cases} \boldsymbol{S}_{\mathrm{z1}} = [0 \quad 0] \\ \boldsymbol{S}_{\mathrm{o1}} = [0 \quad 1] \\ \boldsymbol{S}_{\mathrm{t1}} = [1 \quad 1]. \end{cases} \tag{17}$$

Therefore, the duty cycle vector in the first T_{e} can be derived

$$\begin{aligned} \boldsymbol{d}_1 &= d_{\mathrm{R1}} \boldsymbol{S}_{\mathrm{z1}} + (d_{\mathrm{R2}} - d_{\mathrm{R1}}) \boldsymbol{S}_{\mathrm{o1}} + (1 - d_{\mathrm{R2}})\, \boldsymbol{S}_{\mathrm{t1}} \\ &= \begin{bmatrix} 1 - d_{\mathrm{R2}} & 1 - d_{\mathrm{R1}} \end{bmatrix}. \end{aligned} \tag{18}$$

Since the working cycle of the HBM capacitors is T_{s} ($T_{\mathrm{s}} = 2T_{\mathrm{e}}$) and its duration is short, the charging and discharging cycle of the HBM capacitors is small. Therefore, the ripple of the HBM capacitor voltages can be negligible compared to its average value. Next, apply Kirchhoff's law to the voltage loop of the upper arm and combine it with the condition that the integral of the voltage V_{L1} of the inductor L_1 in a T_{e} is zero during steady-state operation, the constraints of HBM capacitor voltages on duty cycle vector and input voltage V_{in} are given

$$\boldsymbol{d}_1 \cdot \bar{\boldsymbol{v}}^{\mathrm{T}}{}_{\mathrm{C}} = V_{\mathrm{in}} \tag{19}$$

where $\bar{\mathrm{v}}_{\mathrm{C}} = [\bar{\mathrm{v}}_{\mathrm{C1}} \ \bar{\mathrm{v}}_{\mathrm{C2}}]$ is the average voltage vector of HBM capacitor. Furthermore, a set of HBM voltage equations within a circulant cycle T_{s} are derived

$$\boldsymbol{D} \cdot \bar{\boldsymbol{v}}^{\mathrm{T}}{}_{\mathrm{C}} = \begin{bmatrix} V_{\mathrm{in}} & V_{\mathrm{in}} \end{bmatrix}^{\mathrm{T}} \tag{20}$$

where the duty cycle matrix $\boldsymbol{D}$ within one T_{s} is formed by the duty cycle vectors $\boldsymbol{d_1}$ and $\boldsymbol{d_2}$ corresponding to each T_{e} and it can be written as

$$\boldsymbol{D} = \begin{bmatrix} \boldsymbol{d}_1 \\ \boldsymbol{d}_2 \end{bmatrix} = \begin{bmatrix} 1 - d_{\mathrm{R2}} & 1 - d_{\mathrm{R1}} \\ 1 - d_{\mathrm{R1}} & 1 - d_{\mathrm{R2}} \end{bmatrix}. \tag{21}$$

According to linear algebra theory, the sufficient and necessary condition for the voltage vector $\bar{\mathrm{v}}_{\mathrm{C}}$ in (20) to have a unique solution is that the determinant of its coefficient matrix $\boldsymbol{D}$ is not 0 [24], as shown in

$$\det(\boldsymbol{D}) \neq 0. \tag{22}$$

Furthermore, the matrix $\boldsymbol{D}$ is a circulant matrix, and the determinant of a two-dimensional circulant matrix $\boldsymbol{D}$ can be obtained from the circulant matrix theory [25] and given by

$$\begin{cases} \det(\boldsymbol{D}) = \prod_{j=1}^{2} f(\omega_j) \\ f(\omega_j) = 1 - d_{\mathrm{R2}} + (1 - d_{\mathrm{R1}})\omega_j \end{cases} \tag{23}$$

where $\omega_j = e^{i2\pi \cdot \frac{j-1}{2}}$ ($j = 1, 2$) and i is the imaginary unit. If there is no $f(\omega_j) = 0$, then $\det(\boldsymbol{D}) \neq 0$ always holds. When $j = 1$, $\omega_j = \omega_1 = 1$, so $f(\omega_1) = 2 - d_{\mathrm{R2}} - d_{\mathrm{R1}}$. When $j = 2$, $\omega_j = \omega_2 = -1$, then $f(\omega_2) = d_{\mathrm{R1}} - d_{\mathrm{R2}}$. In HVG mode, d_{R1} and d_{R2} satisfy $0 < d_{\mathrm{R1}} < 0.5$ and $d_{\mathrm{R2}} = 0.5$, respectively. Substituting d_{R1} and d_{R2} into $f(\omega_1)$ and $f(\omega_2)$, we can calculate $f(\omega_1) = 1.5 - d_{\mathrm{R1}} \neq 0$ and $f(\omega_2) = d_{\mathrm{R1}} - 0.5 \neq 0$. In LVG mode, d_{R1} and d_{R2} satisfy $d_{\mathrm{R1}} = 0$ and $0 < d_{\mathrm{R2}} < 0.5$, respectively. Substituting d_{R1} and d_{R2} into $f(\omega_1)$ and $f(\omega_2)$, we can get $f(\omega_1) = 2 - d_{\mathrm{R2}} \neq 0$ and $f(\omega_2) = -d_{\mathrm{R2}} \neq 0$. To sum up, there is no $j \in [1], [2]$ in these two gain modes such that $f(\omega_j) = 0$, so $\det(\boldsymbol{D}) \neq 0$ is always satisfied. Hence, under circulant duty cycle modulation, the DMIDC can achieve self-balancing of the HBM capacitor voltages in both HVG and LVG modes, and the balancing characteristics are unaffected by the regulation of d_{R1} and d_{R2}.

B. Voltage Gain Analysis

The gain M of the proposed DMIDC can be expressed as

$$M = \frac{V_o}{nV_{in}}. \tag{24}$$

The time-domain analysis method is adopted to obtain the voltage gain of the proposed DMIDC converter. Furthermore, the physical quantities in this converter are normalized and the dead-time T_d between the driving signals of S_{11}–S_{14} and S_{21}–S_{24} is not considered for the convenience of subsequent analysis. The normalized values of the time t and the physical quantities v_{Cr}, i_{Lr}, and i_{Lm} in the resonant tank are expressed as $\theta = \omega_r t$, ${v_{Cr}}^* = v_{Cr}/V_{in}$, ${i_{Lr}}^* = i_{Lr}Z_r/V_{in}$, and ${i_{Lm}}^* = i_{Lm}Z_r/V_{in}$, respectively (where $Z_r = \sqrt{L_r/C_r}$). Also, the duration of the first half cycle of the first T_e in both gain modes is redefined as Stage1 [t_0–t_2], Stage2 [t_2–t_4], and Stage3 [t_4–t_5], and the normalized parameters corresponding to these stages can be derived as [0, α], [α, β], and [β, γ], respectively.

Because the capacitor voltage and inductor current vary continuously, their normalized expressions (25)–(27) in HVG mode are obtained by normalizing (2), (4), and (5), while the normalized expressions (28)–(30) in LVG mode are achieved by normalizing (10), (12), and (13)

$$\begin{cases} {v_{Cr}}^*(\theta) = M - 2/(2-d_T) + {i_{Lr}}^*(0)\sin\theta \\ \qquad\qquad + [2/(2-d_T) - M + {v_{Cr}}^*(0)]\cos\theta \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(0)\cos\theta - [2/(2-d_T) - M + {v_{Cr}}^*(0)]\sin\theta \\ {i_{Lm}}^*(\theta) = {i_{Lm}}^*(0) - M\theta/k \end{cases} \tag{25}$$

$$\begin{cases} {v_{Cr}}^*(\theta) = M - 1/(2-d_T) + {i_{Lr}}^*(\alpha)\sin(\theta-\alpha) \\ \qquad\qquad + [1/(2-d_T) - M + {v_{Cr}}^*(\alpha)]\cos(\theta-\alpha) \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(\alpha)\cos(\theta-\alpha) \\ \qquad\qquad - [1/(2-d_T) - M + {v_{Cr}}^*(\alpha)]\sin(\theta-\alpha) \\ {i_{Lm}}^*(\theta) = {i_{Lm}}^*(\alpha) - M(\theta-\alpha)/k \end{cases} \tag{26}$$

$$\begin{cases} {v_{Cr}}^*(\theta) = -1/(2-d_T) + {i_{Lr}}^*(\beta)\sqrt{k+1}\sin[(\theta-\beta)/\sqrt{k+1}] \\ \qquad\qquad + [1/(2-d_T) + {v_{Cr}}^*(\beta)]\cos[(\theta-\beta)/\sqrt{k+1}] \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(\beta)\cos[(\theta-\beta)/\sqrt{k+1}] \\ \qquad\qquad - [1/(2-d_T) + {v_{Cr}}^*(\beta)]/\sqrt{k+1}\sin[(\theta-\beta)/\sqrt{k+1}] \\ {i_{Lm}}^*(\theta) = {i_{Lr}}^*(\theta) \end{cases} \tag{27}$$

$$\begin{cases} {v_{Cr}}^*(\theta) = M - 1/(2-d_T) + {i_{Lr}}^*(0)\sin\theta \\ \qquad\qquad + [1/(2-d_T) - M + {v_{Cr}}^*(0)]\cos\theta \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(0)\cos\theta - [1/(2-d_T) - M + {v_{Cr}}^*(0)]\sin\theta \\ {i_{Lm}}^*(\theta) = {i_{Lm}}^*(0) - M\theta/k \end{cases} \tag{28}$$

$$\begin{cases} {v_{Cr}}^*(\theta) = M + {i_{Lr}}^*(\alpha)\sin(\theta-\alpha) - [M - {v_{Cr}}^*(\alpha)]\cos(\theta-\alpha) \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(\alpha)\cos(\theta-\alpha) + [M - {v_{Cr}}^*(\alpha)]\sin(\theta-\alpha) \\ {i_{Lm}}^*(\theta) = {i_{Lm}}^*(\alpha) - M(\theta-\alpha)/k \end{cases} \tag{29}$$

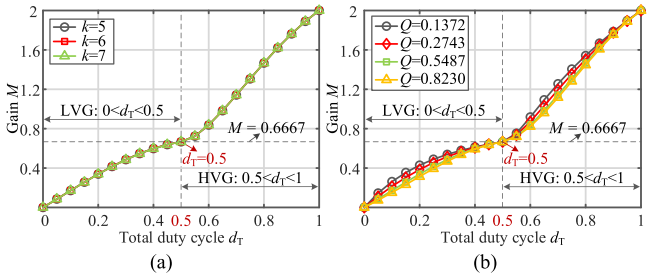

Fig. 6. Voltage gain of DMIDC with different. (a) k. (b) Q.

$$\begin{cases} {v_{Cr}}^*(\theta) = {i_{Lr}}^*(\beta)\sqrt{k+1}\sin[(\theta-\beta)/\sqrt{k+1}] \\ \qquad\qquad + {v_{Cr}}^*(\beta)\cos[(\theta-\beta)/\sqrt{k+1}] \\ {i_{Lr}}^*(\theta) = {i_{Lr}}^*(\beta)\cos[(\theta-\beta)/\sqrt{k+1}] \\ \qquad\qquad - {v_{Cr}}^*(\beta)/\sqrt{k+1}\sin[(\theta-\beta)/\sqrt{k+1}] \\ {i_{Lm}}^*(\theta) = {i_{Lr}}^*(\theta) \end{cases} \tag{30}$$

where k is the inductor ratio and $k = L_m/L_r$.

According to the fact that the voltage v_{Cr}, currents i_{Lr} and i_{Lm} satisfy the property of odd symmetry in both HVG and LVG modes, the following equation can be written:

$$\begin{cases} {i_{Lr}}^*(0) + {i_{Lr}}^*(\gamma) = 0 \\ {v_{Cr}}^*(0) + {v_{Cr}}^*(\gamma) = 0 \\ {i_{Lm}}^*(\beta) = {i_{Lr}}^*(\beta). \end{cases} \tag{31}$$

As can be seen from Fig. 2, power is not transferred from the input port to the output port during the period [t_4–t_5] in the first half of the first T_e. Based on the energy conservation law, the normalized value of the output current I_o can be derived as

$$\int_0^{\beta} |{i_{Lr}}^*(\theta) - {i_{Lm}}^*(\theta)|d\theta = {I_o}^* = MQ\gamma \tag{32}$$

where Q is the quality factor and $Q = n^2\sqrt{L_r/C_r}/R_L$.

Based on the abovementioned analysis, there are five unknowns in both HVG mode and LVG mode, namely [${i_{Lr}}^*(0)$, ${i_{Lm}}^*(0)$, ${v_{Cr}}^*(0)$, β, M]. By setting the values of V_{in}, T_e, d_T, L_b, L_r, C_r, L_m, and Q, and combining them with (24)–(27), (31), (32) in HVG mode, or with (24), (28)–(32) in LVG mode, the unknowns in both modes can be solved. The calculated voltage gains of the two gain modes under different k and Q are plotted in Fig. 6. As seen, the gain varies between 0 and 2 by adjusting d_T. The voltage gains of HVG mode and LVG mode are (0, 0.6667) and (0.6667, 2), respectively. The boundary point between these two gain modes is $d_T = 0.5$ (i.e., $d_{R1} = 0$ and $d_{R2} = 0.5$). Moreover, the variation of k hardly affects the voltage gain. And, the change in Q has little effect on the gain M, meaning that the proposed DMIDC has a weaker dependent load.

C. Resonant Tank Parameters

Taking a prototype with input voltage $V_{in} = 75-300$ V, output voltage $V_o = 330$ V, and output power $P_o = 400$ W, as an example to study the design considerations of the main circuit parameters. For the proposed DMIDC, it is necessary to analyze the impact of different characteristic impedance Z_r designs on the rms value of the resonant current i_{Lr_rms} and the turn-OFF

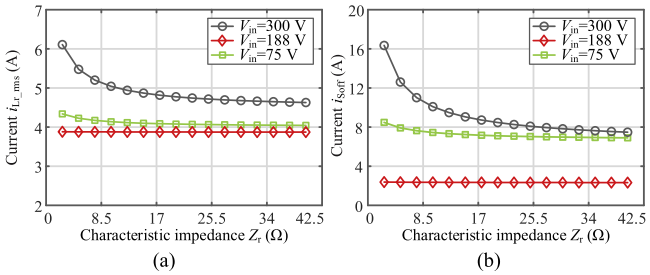

Fig. 7. Curves of $i_{\mathrm{Lr\_rms}}$ and i_{SOFF} with respect to Z_{r} and V_{in}. (a) $i_{\mathrm{Lr\_rms}}$. (b) i_{SOFF}.

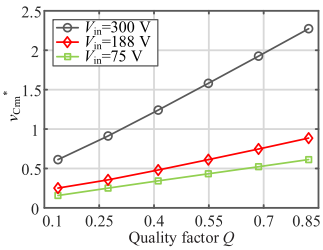

Fig. 8. Curves of $v_{\mathrm{Crm}}{}^{*}$ with different V_{in}.

current i_{SOFF} of the switching devices (where $i_{\mathrm{SOFF}} = |i_{\mathrm{Lr}}{}^{*}(\alpha) + i_{\mathrm{Lr}}{}^{*}(\gamma)|V_{\mathrm{in}}/Z_{\mathrm{r}}$), which affect the conduction loss and switching loss, respectively. Fig. 7 shows the currents $i_{\mathrm{Lr\_rms}}$ and i_{SOFF} for different Z_{r} designs at $V_{\mathrm{in}} = 75$ V (HVG), 188 V (boundary) and 300 V (LVG). It can be seen that a large Z_{r} can reduce $i_{\mathrm{Lr\_rms}}$ and i_{SOFF} when $V_{\mathrm{in}} = 75$ V (HVG) and 300 V (LVG). According to $Z_{\mathrm{r}} = \sqrt{\mathrm{L_r/C_r}} = QR_{\mathrm{L}}/n^2$, an increase in Z_{r} means an increase in Q and L_{r}. As shown in Fig. 2, the maximum value v_{Crm} of v_{Cr} is generated in the Stage $[t_1$–$t_2]$ when i_{Lr} is equal to zero for these two gain modes. Based on this, Fig. 8 shows the curves of the normalized maximum value $v_{\mathrm{Crm}}{}^{*}$ of v_{Cr} changing with Q under different input voltages (corresponding to different gain modes). As can be observed, the increase in Q result in a rise in $v_{\mathrm{Crm}}{}^{*}$ regardless of $V_{\mathrm{in}} = 75$ V, 188 V, and 300 V. Thus, the aforementioned design factors must be considered when determining the resonant tank parameters. Ultimately, the value of Q is determined to be 0.5487. Then, combined with $Q = n^2\sqrt{\mathrm{L_r/C_r}}/R_{\mathrm{L}}$ and $\mathrm{f_r} = 1/(2\pi\sqrt{\mathrm{L_rC_r}})$, the calculated L_{r} and C_{r} are 41.79 μH and 94.7 nF, respectively.

D. Voltage Stress Analysis of Switching Devices

For the proposed DMIDC converter, the voltage stress borne by each switching device when turned OFF is equal to the HBM capacitor voltage V_{C}, so voltage V_{C} is analyzed in detail. As can be seen from (7) and (15), the mathematical relationship between the HBM capacitor voltage V_{C} and the input voltage V_{in} is the same in both gain modes.

From Table I, the total duty cycle d_{T} changes between 0 and 1. Combining Table I, (7) and (15), the relationship between $V_{\mathrm{C}}/V_{\mathrm{in}}$ and d_{T} in HVG mode and LVG mode is plotted in Fig. 9. As seen, the voltage stress borne by the switching devices and HBM capacitors of the proposed DMIDC under these two voltage

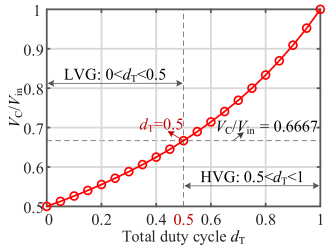

Fig. 9. Relationship between $V_{\mathrm{C}}/V_{\mathrm{in}}$ and d_{T}.

gains is lower than the input voltage V_{in}. So, the lower voltage rating primary switches and HBM capacitors can be used, which reduces component costs and system volume.

E. ZVS Analysis

From the analysis in Section II, it is clearly demonstrated that the ZVS realization principle of the proposed DMIDC during the first T_{e} and the second T_{e} is identical regardless of HVG mode or LVG mode. Therefore, the ZVS implementation of the first T_{e} in both modes is selected as an example to derive the ZVS conditions. In addition, the dead-time T_{d} between two switches of the same HBM should be considered when analyzing ZVS. As shown in the switching waveforms in Fig. 2, the ZVS of the lower switches S_{12} , S_{14} , S_{22}, and S_{24} is more difficult to achieve than that of the upper switches S_{11}, S_{13}, S_{21}, and S_{23} for both modes. Therefore, as long as the ZVS of the lower switches is achieved, the ZVS of all other switches can be guaranteed.

Based on the abovementioned analysis and Fig. 2(a), the ZVS achievement condition for the lower switches of each arm in HVG mode can be derived as

$$\begin{cases} (i_{\mathrm{Lr}}(t_0) - i_{\mathrm{L1}}(t_0))T_{\mathrm{d}} > \frac{4C_{\mathrm{oss}}V_{\mathrm{in}}}{2-d_{\mathrm{T}}} + 4C_{\mathrm{d}}V_{\mathrm{o}}n + \frac{2C_{\mathrm{w}}V_{\mathrm{o}}}{n} \\ (-i_{\mathrm{Lr}}(t_5) - i_{\mathrm{L2}}(t_5))T_{\mathrm{d}} > \frac{4C_{\mathrm{oss}}V_{\mathrm{in}}}{2-d_{\mathrm{T}}} + 4C_{\mathrm{d}}V_{\mathrm{o}}n + \frac{2C_{\mathrm{w}}V_{\mathrm{o}}}{n} \end{cases} \tag{33}$$

where C_{oss}, C_{d}, and C_{w} are the junction capacitor of the primary switches, the junction capacitor of the secondary diodes, and the total parasitic capacitor equivalent to the primary side of the transformer, respectively.

Similarly, according to Fig. 2(b), the ZVS implementation condition for the lower switches of each arm in LVG mode can be obtained by

$$\begin{cases} (i_{\mathrm{Lr}}(t_0) - i_{\mathrm{L1}}(t_0))T_{\mathrm{d}} > \frac{2C_{\mathrm{oss}}V_{\mathrm{in}}}{2-d_{\mathrm{T}}} + 4C_{\mathrm{d}}V_{\mathrm{o}}n + \frac{2C_{\mathrm{w}}V_{\mathrm{o}}}{n} \\ (-i_{\mathrm{Lr}}(t_5) - i_{\mathrm{L2}}(t_5))T_{\mathrm{d}} > \frac{2C_{\mathrm{oss}}V_{\mathrm{in}}}{2-d_{\mathrm{T}}} + 4C_{\mathrm{d}}V_{\mathrm{o}}n + \frac{2C_{\mathrm{w}}V_{\mathrm{o}}}{n}. \end{cases} \tag{34}$$

When the conditions in (33) and (34) always hold, switches S_{11}–S_{14} and S_{21}–S_{24} can achieve their respective ZVS throughout the entire operating range. Also, the ZVS commutation currents increase with the decrease of inductors L_1, L_2, and L_{m}, which is favorable for ZVS operations. However, this will cause the peak values of currents i_{L1}, i_{L2}, and i_{Lm} to increase. Furthermore, Fig. 10 and 11 show the rms values of the resonant current $i_{\mathrm{Lr\_rms}}$ and the input inductor current $i_{\mathrm{Lb\_rms}}$ ($i_{\mathrm{Lb\_rms}} = i_{\mathrm{L1\_rms}} = i_{\mathrm{L2\_rms}}$) at different inductors, respectively. It can be observed that the reduction of L_{m} causes an increase in $i_{\mathrm{Lr\_rms}}$, and the

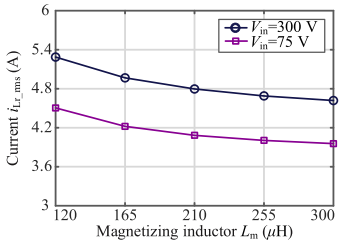

Fig. 10. Curves of $i_{\mathrm{Lr\_rms}}$ at different L_{m}.

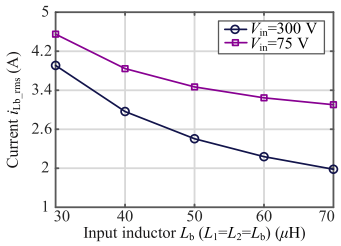

Fig. 11. Curves of $i_{\mathrm{Lb\_rms}}$ at different L_{b} ($L_1 = L_2 = L_{\mathrm{b}}$).

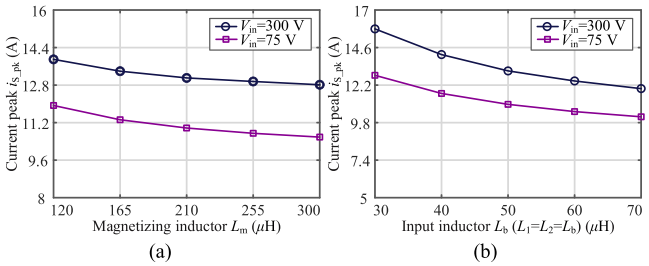

Fig. 12. Curves of $i_{\mathrm{S\_PK}}$ with different. (a) L_{m}. (b) L_{b} ($L_1 = L_2 = L_{\mathrm{b}}$).

reduction of L_1 and L_2 leads to an increase in $i_{\mathrm{Lb\_rms}}$, which results in an increase in the rms values and conduction losses of the switching devices. Fig. 12 presents the peak current $i_{\mathrm{S\_pk}}$ of the switching device under different inductors (where $i_{\mathrm{S\_pk}} = i_{\mathrm{L1}}(t_2) - i_{\mathrm{Lr}}(t_2)$). As can be seen, whether L_{m} is decreased or L_1 and L_2 are reduced, the peak current $i_{\mathrm{S\_pk}}$ will increase. Since the rated current of the switching device must meet the current rms value and peak current limits, the inductors L_1, L_2, and L_{m} should be taken as the larger value. However, this will reduce the ZVS commutation current, which is not conducive to the implementation of ZVS. Therefore, a trade-off is required between the values of inductors L_1, L_2, and L_{m} to achieve excellent performance.

IV. Experimental Verification

To validate the correctness of the theoretical analysis and the converter performance, a 400 W, 75−300 V/330 V prototype of the proposed DMIDC is established, as shown in Fig. 13. Table II gives the utilized component parameters of this prototype.

A. Experimental Waveforms

Fig. 14 presents the driving voltages of the lower switching devices under different gain modes. The driving signals

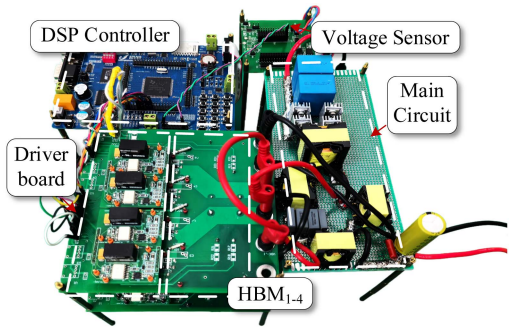

Fig. 13. Photograph of the experimental prototype.

TABLE II
Parameters and Components of the Prototype

Parameters	Values
Input voltage (V_{in})	75−300 V
Output voltage (V_{o})	330 V
Output power (P_{o})	400 W
Switching frequency f_{s}	80 kHz
Input inductors L_1 and L_2	53.3 μH
Resonant capacitor C_{r}	94.7 nF
Transformer T_{r}	PQ35/35-PC95, Turns ratio T_{r}=15: 40 Magnetizing inductor L_{m}=212 μH
Primary Switches S_1 – S_4	IPP200N15N3
Diodes D_1 and D_2	C3D10060A

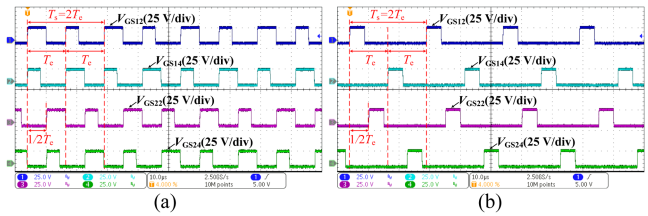

Fig. 14. Driving waveforms under different gain modes. (a) HVG. (b) LVG.

generated by the fixed-frequency circulant duty cycle control strategy are used to control the primary switches, and they match well with the driving signals in HVG mode and LVG mode, as shown in Fig. 2, respectively. The tested results of voltage V_{AB}, currents i_{L1}, i_{L2}, and i_{Lr} are shown in Fig. 15. As observed from Fig. 15(a)–(f), the operating waveforms of the DMIDC are consistent with the theoretical states in Fig. 2.

Fig. 16 shows the ZVS and voltage stress of S_{11} and S_{12} under different input voltages and loads. As seen, S_{11} and S_{12} realize ZVS in the full range. And the maximum voltage stress of the switches under 75 V input, 188 V input, and 300 V input is 67.6 V, 127.3 V, and 175 V, respectively, which verifies that the proposed DMIDC has the advantage of low voltage stress. The measured HBM capacitor voltages in different voltage gain modes are given in Fig. 17. It can be clearly seen that the HBM capacitor voltages can be equally divided under the fixed-frequency circulant duty cycle control scheme.

Figs. 18 and 19 show the dynamic waveforms of the proposed DMIDC operating in HVG and LVG modes when the input voltage or load changes. Among them, Fig. 18(a)–(d) as well as

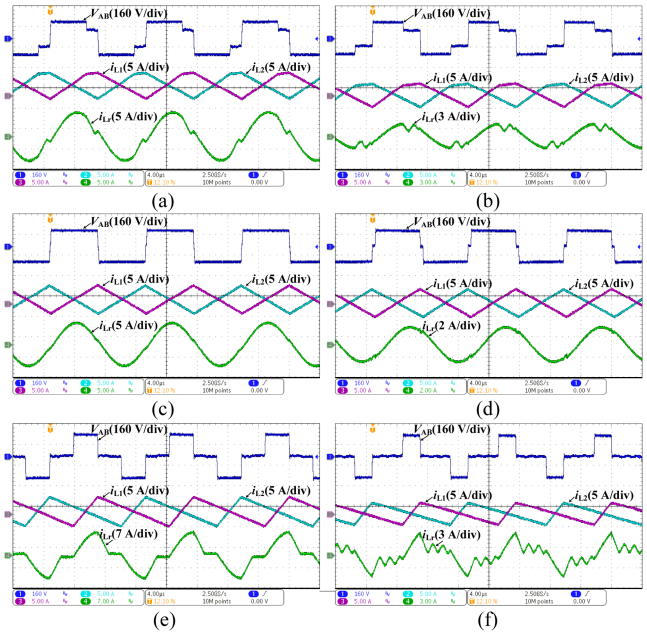

Fig. 15. Tested results of input inductor currents and resonant stage. (a) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 400 W. (b) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 80 W. (c) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 400 W. (d) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 80 W. (e) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 400 W. (f) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 80 W.

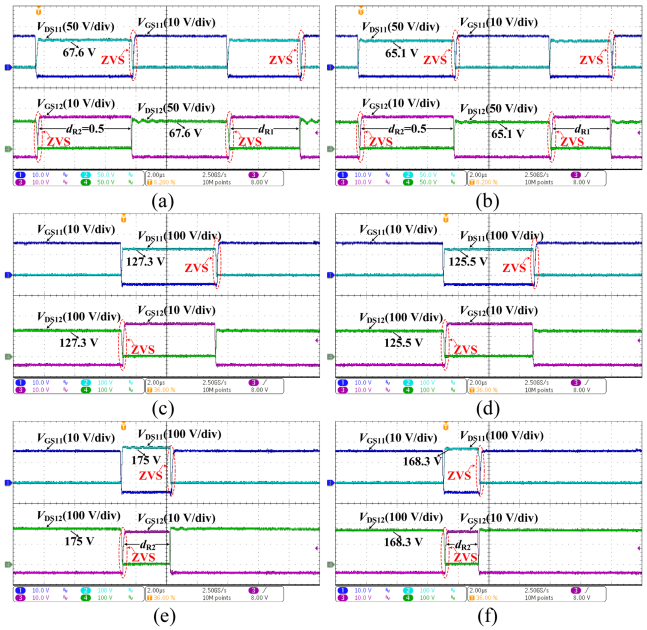

Fig. 16. ZVS waveforms of switches S_{11} and S_{12}. (a) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 400 W. (b) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 80 W. (c) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 400 W. (d) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 80 W. (e) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 400 W. (f) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 80 W.

Fig. 19(a)–(d) display the dynamic waveforms of input voltage changes in HVG and LVG modes, respectively. As illustrated in Fig. 18(a)–(d), when the input voltage changes between 80 and 140 V in HVG mode at full load, neither the current $i_{\rm Lr}$ nor the voltage $V_{\rm AB}$ exhibits spikes. The HBM capacitor voltages vary in the same trend and have equal steady-state values,

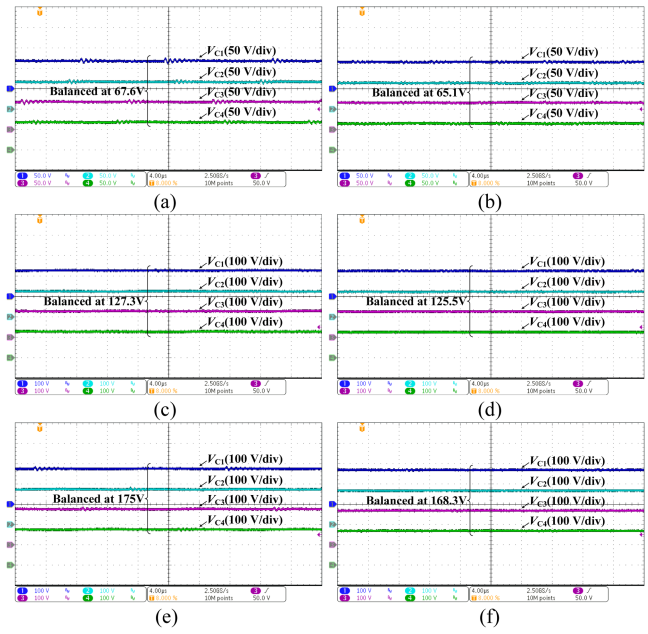

Fig. 17. Experimental waveforms of HBM capacitor voltages. (a) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 400 W. (b) $V_{\rm in}$ = 75 V, $P_{\rm o}$ = 80 W. (c) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 400 W. (d) $V_{\rm in}$ = 188 V, $P_{\rm o}$ = 80 W. (e) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 400 W. (f) $V_{\rm in}$ = 300 V, $P_{\rm o}$ = 80 W.

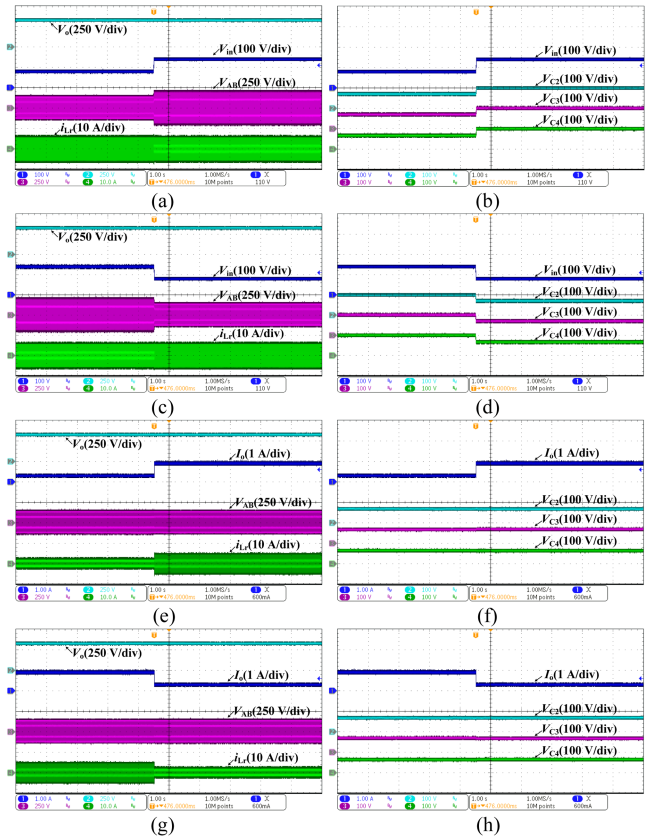

Fig. 18. Dynamic waveforms of the DMIDC operating in HVG mode when the input voltage or output load changes. (a), (b) For changing the input voltage from 80 V to 140 V. (c), (d) For changing the input voltage from 140 V to 80 V. (e), (f) For changing the load from 100 W to 300 W. (g), (h) For changing the load from 300 W to 100 W.

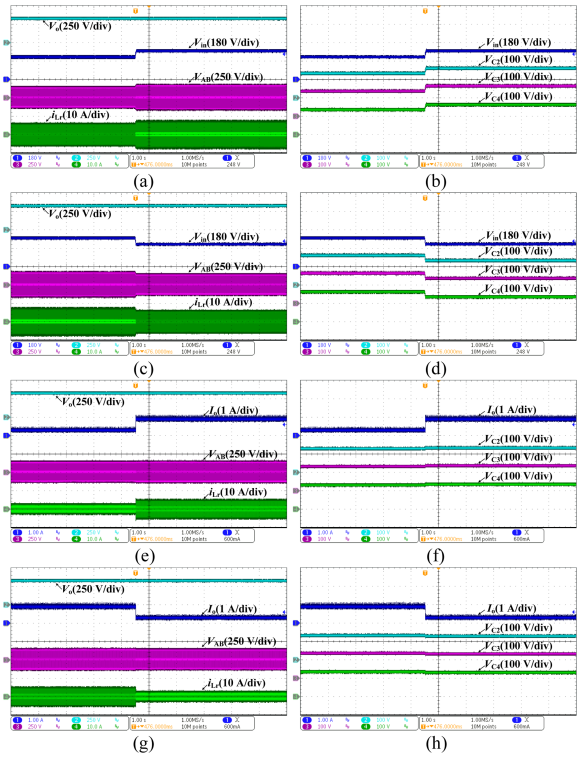

Fig. 19. Dynamic waveforms of the DMIDC operating in LVG mode when the input voltage or output load changes. (a), (b) For changing the input voltage from 220 V to 280 V. (c), (d) For changing the input voltage from 280 V to 220 V. (e), (f) For changing the load from 100 W to 300 W. (g), (h) For changing the load from 300 W to 100 W.

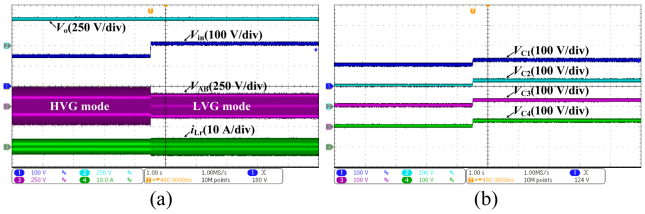

Fig. 20. Dynamic waveforms of mode transition from HVG (150 V) to LVG (210 V). (a) $V_{\rm in}$, $V_{\rm o}$, $V_{\rm AB}$, and $i_{\rm Lr}$. (b) $V_{\rm C1}$, $V_{\rm C2}$, $V_{\rm C3}$, and $V_{\rm C4}$.

indicating that voltage balance is achieved. Similarly, as shown in Fig. 19(a)–(d), when the input voltage changes between 220 and 280 V in LVG mode at full load, the HBM capacitor voltages also change consistently, implying that voltage balance is also achieved.

Furthermore, the dynamic waveforms of load changes in HVG and LVG modes are shown in Figs. 18(e)–(h) and 19(e)–(h), respectively. As can be seen in Figs. 18(e)–(h) and 19(e)–(h),when the load changes between 100 and 300 W in HVG and LVG modes, the HBM capacitor voltages are balanced as well in both dynamic state and steady-state. Through the abovementioned analysis, the proposed DMIDC can operate stably in HVG and LVG modes, and achieve self-balancing of HBM capacitor voltages in both modes when the input voltage or load changes.

Figs. 20 and 21 show the dynamic waveforms of mode transition between HVG mode (150 V) and LVG mode (210 V). As can be seen in Figs. 20(a) and 21(a), when the proposed

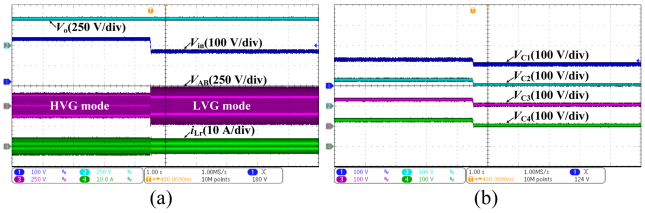

Fig. 21. Dynamic waveforms of mode transition from LVG (210 V) to HVG (150 V). (a) $V_{\rm in}$, $V_{\rm o}$, $V_{\rm AB}$, and $i_{\rm Lr}$. (b) $V_{\rm C1}$, $V_{\rm C2}$, $V_{\rm C3}$, and $V_{\rm C4}$.

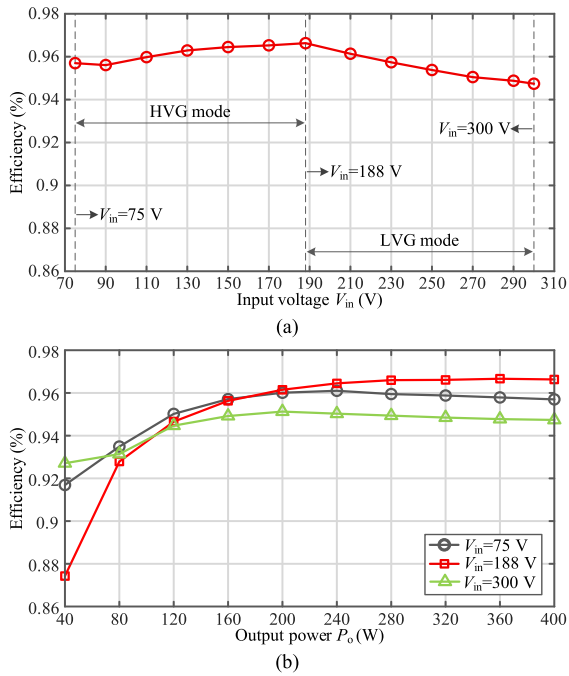

Fig. 22. Efficiency under different input and power levels. (a) Efficiency under different inputs at rated power. (b) Efficiency under different powers.

DMIDC converter transitions from HVG mode to LVG mode and from LVG mode to HVG mode, there are no spikes in the resonant current $i_{\rm Lr}$ and the input voltage $V_{\rm AB}$ of the resonant tank, which indicates that DMIDC can achieve smooth mode transition within a wide input voltage range under the circulant duty cycle modulation strategy. Moreover, when this converter steps between HVG and LVG modes, it only needs to control the total duty cycle $d_{\rm T}$ as a single variable without the need for an additional input voltage sampling circuit. Meanwhile, the HBM capacitor voltages $V_{\rm C1}$–$V_{\rm C4}$ maintain the same trend of change during the $V_{\rm in}$ step, as shown in Figs. 20(b) and 21(b). From this, it can be seen that the inherent balance performance of the HBM capacitor voltages $V_{\rm C1}$–$V_{\rm C4}$ can be well achieved both in steady-state and during the transition between HVG mode and LVG mode.

Fig. 22 shows the efficiency curves of the proposed DMIDC measured at rated power (full load) over a wide input voltage range, as well as efficiency curves measured over a wide power range at 75 V, 188 V, and 300 V inputs. As seen, the efficiency of the proposed DMIDC at full load with 300 V input is lower than that at 75 V input. Moreover, due to the smaller conduction

TABLE III
COMPARISON AMONG DIFFERENT CONVERTERS

Topology	This work	[15]	[16]	[17]	[18]	[20]
Switches	8	4	6	6	8	8
Diodes	4	2	2	6	8	2
Inductors	3	3	2	2	3	3
Transformers	1	1	1	2	2	1
Working mode	2	1	2	3	2	1
Control complexity	FFCDC (Simple)	PWM (Simple)	PWM+PFM (Complex)	PWM+PFM (Complex)	PSM+PFM (Complex)	FFCPS (Simple)
Control degrees of freedom	1	1	2	2	2	1
Input/output voltage	75–300 V / 330 V	120–240 V / 24 V	24–64 V / 375 V	50–300 V / 50 V	200–800 V / 200 V	80–120 V / 400 V
Rated Power	400 W	600 W	470 W	250 W	1000 W	400 W
Input voltage range K_r (K_r=V_{inmax}/V_{inmin})	4 (Extra wide)	2 (Wide)	2.7 (Extra wide)	6 (Extra wide)	4 (Extra wide)	1.5 (Wide)
Input current ripple	Small	Small	Small	Large	Large	Zero
Gain-Load characteristic	Good (Weakly dependent load)	Poor (Highly dependent load)	Poor (Highly dependent load)	Poor (Highly dependent load)	Poor (Highly dependent load)	Poor (Highly dependent load)
Switches voltage stress	$\frac{V_{in}}{2-d_T}<V_{in}$ (Low)	$\frac{V_{in}}{1-d}>V_{in}$ (High)	$\frac{V_{in}}{1-d}>V_{in}$ (High)	V_{in} (Medium)	$\frac{V_{in}}{2}$ (Low)	V_{in} (Medium)

FFCDC, PFM, PWM, PSM, and FFCPS are, respectively, referred to as fixed-frequency circulant duty cycle modulation, pulse frequency modulation, pulsewidth modulation, phase-shift modulation, and fixed-frequency circulant phase-shift modulation, respectively.
d is the duty cycle of boost circuit in each converter.

and switching losses at 188 V input, its efficiency is higher than that at full load with 75 V and 300 V inputs.

B. Performance Comparison and Analysis

Table III shows a qualitative comparison between the proposed converter and other existing wide voltage range resonant converters. The comparison focuses on component count, working mode, control complexity, control degrees of freedom, input/output voltage, rated power, input voltage range K_r ($K_r = V_{inmax}/V_{inmin}$), input current ripple, gain-load characteristic, and switches voltage stress. When comparing the performance, the "gain-load characteristic" is evaluated by "good" or "poor". Among them, "good gain-load characteristic" is referred to the changes in load (quality factor Q) have little impact on voltage gain, i.e., there is a weak dependence between voltage gain and load.

As seen, the control strategy of the structure in [20] is simple and the converter can achieve zero input current ripple. However, this scheme has only one working mode, a large phase-shift angle must be introduced when the converter operates in the extra wide input range, making it difficult to achieve ZVS over an extra wide input range. The converters in [16], [17], and [18] have multiple working modes and good ZVS performance in a wide gain range. However, they have multiple control degrees of freedom, which leads to complex control strategies. The control scheme in [15] is simple, but the switches are subjected to high voltage stress and have poor gain-load characteristics. For the proposed DMIDC, it not only has only one control degree of freedom and simple control scheme, but also has moderate component count, good ZVS performance in a wide gain range, low voltage stress, and good gain-load characteristics.

In addition, to make fair comparisons of the relevant power density, costs, and losses, virtual prototypes of the proposed DMIDC topology and some competitive topologies are designed and simulated based on the same design specifications. Table IV shows the detailed parameters along with the calculated power density, costs distribution, and losses distribution for these virtual hardware prototype. The power density is equal to output power P_o / volume and its unit is W/cm^3. According to the cost of available components in [26], the costs distribution of different structures can be obtained. Combining the loss models in [27] and [28] and the details of each topology in Table IV, the losses distribution for different schemes can be evaluated.

It can be seen from Table IV that the total losses of the converter in [20] with a single working mode is the largest because of the large conduction and switching losses generated when operating over a wide voltage range. The conventional single-stage boost-*LLC* converter in [15] also has only one working mode, and its structure is the simplest and the cost is the lowest. On the other hand, the output clamp capacitor of the interleaved boost circuit is subjected to large voltage stress when the converter operates over a wide voltage range. Therefore, high-voltage clamp capacitors are required in this converter, which results in its power density being the lowest. The converters in [17] and [18] can select different working modes according to the input voltage range. However, when the converters in [17] and [18] operate in a wide voltage range, their switching frequencies vary in a large range, resulting in a large volume of magnetic components. Compared with the existing wide range resonant converters mentioned above, the proposed DMIDC adopts fixed-frequency circulant duty cycle control, which can achieve high power density, high efficiency, and moderate cost. This is because the DMIDC significantly

TABLE IV
COMPARISON OF DESIGN SPECIFICATIONS, POWER DENSITY, COSTS, AND LOSSES FOR DIFFERENT CONVERTERS

Topology		This work	[15]	[17]	[18]	[20]
Voltage range		Input: 75–300 V Output: 330 V (400 W)	Input: 75–300 V Output: 330 V (400 W)	Input: 75–300 V Output: 330 V (400 W)	Input:75–300 V Output:330 V (400 W)	Input:75–300 V Output:330 V (400 W)
Frequency	Switching	80 kHz	80 kHz	43.6–129 kHz	44.1–80.9 kHz	80 kHz
	Resonant	80 kHz	80 kHz	80 kHz	80 kHz	80 kHz
Switches		**5.3432 cm^3 / 26.2240 $**	**2.6716 cm^3 / 9.8384 $**	**4.0074 cm^3 / 13.7664 $**	**5.3432 cm^3 / 26.2240 $**	**5.3432 cm^3 / 18.3552 $**
		8 × IPP200N25N3 (250 V, 64 A)	4 × IPP60R080P7 (650 V, 37 A)	6 × IPP50R140CP (550 V, 23 A)	8 × IPP200N25N3 (250 V, 64 A)	8 × IPP50R140CP (550 V, 23 A)
Diodes		**2.6716 cm^3 / 11.8400 $**	**1.3358 cm^3 / 10.9576 $**	**4.0074 cm^3 / 17.7600 $**	**5.3432 cm^3 / 23.6800 $**	**1.3358 cm^3 / 5.9200 $**
		4 × C3D10060A (600 V, 14.5 A)	2 × C4D10120A (1200 V, 16 A)	6 × C3D10060A (600 V, 14.5 A)	8 × C3D10060A (600 V, 14.5 A)	2 × C3D10060A (600 V, 14.5 A)
Transformer (E core and litz wire)		**22.9003 cm^3 / 6.3320 $**	**22.9003 cm^3 / 6.3320 $**	**45.8006 cm^3 / 12.6640 $**	**31.9354 cm^3 / 9.7640 $**	**22.9003 cm^3 / 6.3320 $**
		Core: EE43/10/28-3C95 Primary winding: 150 × 0.1 mm, 12 turns Secondary winding: 50 × 0.1 mm, 32 turns Core size: 43.2/27.9/19.0 mm (Length/Width/Height)	Core: EE43/10/28-3C95 Primary winding: 50 × 0.1 mm, 36 turns 2 × Secondary winding: 35 × 0.1 mm, 32 turns Core size: 43.2/27.9/19.0 mm (Length/Width/Height)	2 × Core: EE43/10/28-3C95 Primary: 100 × 0.1 mm, 18 turns Secondary: 45 × 0.1 mm, 30 turns 2 × Core size: 43.2/27.9/19.0 mm (Length/Width/Height)	2 × Core: EE38/8/25-3C95 Primary: 160 × 0.1 mm, 18 turns Secondary: 25 × 0.1 mm, 40 turns 2 × Core size: 38.1/25.4/16.5 mm (Length/Width/Height)	Core: EE43/10/28-3C95 Primary winding: 130 × 0.1 mm, 13 turns Secondary winding: 100 × 0.1 mm, 15 turns Core size: 43.2/27.9/19.0 mm (Length/Width/Height)
Inductor (E core and litz wire)		**16.3968 cm^3 / 7.1920 $**	**31.9354 cm^3 / 9.7640 $**	/	**28.6803 cm^3 / 5.6286 $**	**31.9354 cm^3 / 9.7640 $**
		a. 2 × Core: EE32/6/20-3C95 Winding: 90 × 0.1 mm, 14 turns (53.3 μH) 2 × Core size: 31.8/20.3/12.7 mm (Length/Width/Height)	a. 2 × Core: EE38/8/25-3C95 Winding: 90 × 0.1 mm, 19 turns (129.1 μH) 2 × Core size: 38.1/25.4/16.5 mm (Length/Width/Height)		a. Core: EE47/20/16-3C95 Winding: 140 × 0.1 mm, 31 turns (163.0 μH) 2 × Core size: 46.9/19.6/15.6 mm (Length/Width/Height)	a. 2 × Core: EE38/8/25-3C95 Winding: 160 × 0.1 mm, 9 turns (32.6 μH) 2 × Core size: 38.1/25.4/16.5 mm (Length/Width/Height)
		15.9677 cm^3 / 4.8820 $	**8.1984 cm^3 / 3.5960 $**	**16.3968 cm^3 / 7.1920 $**	**31.9354 cm^3 / 9.7640 $**	**15.9677 cm^3 / 4.8820 $**
		b. Core: EE38/8/25-3C95 Winding: 170 × 0.1 mm, 12 turns (41.79 μH) Core size: 38.1/25.4/16.5 mm (Length/Width/Height)	b. Core: EE32/6/20-3C95 Winding: 60 × 0.1 mm, 10 turns (41.79 μH) Core size: 31.8/20.3/12.7 mm (Length/Width/Height)	b. 2 × Core: EE32/6/20-3C95 Winding: 100 × 0.1 mm, 12 turns (41.79 μH) 2 × Core size: 31.8/20.3/12.7 mm (Length/Width/Height)	b. 2 × Core: EE38/8/25-3C95 Winding: 240 × 0.1 mm, 10 turns (41.79 μH) 2 × Core size: 38.1/25.4/16.5 mm (Length/Width/Height)	b. Core: EE38/8/25-3C95 Winding: 120 × 0.1 mm, 13 turns (41.79 μH) Core size: 38.1/25.4/16.5 mm (Length/Width/Height)
Capacitor	Resonant	**0.1528 cm^3 / 2.8408 $**	**0.1528 cm^3 / 2.8408 $**	**23.9320 cm^3 / 16.0164 $**	**23.9320 cm^3 / 16.0164 $**	**0.1528 cm^3 / 2.8408 $**
		250 V AC/47 nF 250 V AC/33 nF 250 V AC/10 nF 250 V AC/4.7 nF	250 V AC/47 nF 250 V AC/33 nF 250 V AC/10 nF 250 V AC/4.7 nF	2 × 400 V AC/80 nF (4 × 20 nF) 2 × 400 V AC/10 nF 2 × 400 V AC/4.7 nF	2 × 400 V AC/80 nF (4×20 nF) 2 × 400 V AC/10 nF 2 × 400 V AC/4.7 nF	250 V AC/47 nF 250 V AC/33 nF 250 V AC/10 nF 250 V AC/4.7 nF
	HBM / Clamp	**HBM: 1.7100 cm^3 / 16.1380 $**	**Clamp: 66.7480 cm^3 / 10.9798 $**	/	**Clamp: 1.9380 cm^3 / 17.6700 $**	**HBM: 3.3000 cm^3 / 49.3014 $**
		4 × 250 V DC/11 μF (5 × 2.2 μF)	600 V DC/44 μF (2 × 22 μF)		2 × 250 V DC/22 µF (10 × 2.2 µF)	4 × 450 V DC/11 μF (5 × 2.2 μF)
	Voltage-doubler	/	/	/	/	**Voltage-doubler: 1.7100 cm^3 / 16.1380 $**
						2 × 250 V DC/22 μF (10 × 2.2 μF)
Total Volumes (cm^3)		**65.1424 cm^3**	**133.9423 cm^3**	**94.1442 cm^3**	**129.1075 cm^3**	**82.6452 cm^3**
Total Costs ($)		**75.4488 $**	**54.3086 $**	**67.3988 $**	**108.7470 $**	**113.5334 $**
Losses at 188 V input (W)	Switching	3.6739 W	6.7398 W	3.9667 W	0.8490 W	9.4950 W
	Conduction	1.8563 W	3.5413 W	2.9110 W	0.6504 W	38.1006 W
	Transformer	2.5762 W	4.4478 W	4.5302 W	7.2244 W	3.9289 W
	Inductor	2.2016 W	5.0528 W	0.8076 W	1.3863 W	3.8813 W
	Diode	2.2858 W	1.1657 W	2.3146 W	2.1969 W	3.1367 W
Total Losses (W)		**12.5938 W**	**20.9474 W**	**14.5301 W**	**12.3070 W**	**58.5425 W**
Power density (W/cm^3)		**6.1404 W/cm^3**	**2.9864 W/cm^3**	**4.2488 W/cm^3**	**3.0982 W/cm^3**	**4.8400 W/cm^3**

diminishes the size of high-voltage capacitors and magnetic components that account for a large proportion of the total system volumes as well as switching devices with lower voltage ratings and better characteristics can be used.

V. Conclusion

In this article, a DMIDC converter with wide voltage gain is proposed. The proposed DMIDC converter can operate in different modes according to the value of the total duty cycle of the lower switching devices in the same bridge arm, thereby expanding the voltage gain range. Since the proposed scheme has only a single control variable of total duty cycle and its switching frequency is fixed, this is not only beneficial to achieving smooth transitions of different voltage gain modes but also to the design of magnetic components. In addition, the proposed converter has both good gain-load characteristics and low voltage stress on the primary switches compared to other wide range resonant converters. Also, it has the advantages of ZVS of all switching devices, high efficiency, and self-balancing of the HBM capacitor voltages. Finally, the experimental results validate the correctness and effectiveness of the proposed DMIDC converter.

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