# Compact Design of PCB-Based Planar Capacitive Voltage Measurement System for WBG Devices

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***Abstract*—Compact and accurate online monitoring of the voltage switching characteristics of wide-bandgap devices is crucial for the safe operation of power converters. The voltage measurement system based on printed circuit board (PCB) planar capacitors offers advantages in miniaturization, making it suitable for integration into converters. However, the front-end planar capacitive voltage divider (PCVD) faces the problems of balancing integration level with measurement accuracy and insufficient gain in the low-frequency band. To address these issues, this article proposes a multiobjective optimization method for the PCVD and a pulse-sampling compensation (PSC) method to suppress low-frequency distortion. First, the performance difference in size between the PCVD and traditional voltage dividers is compared, clearly demonstrating the miniaturization advantages of the PCVD. Second, the physical size model and measurement error models of the PCVD are established to derive the Pareto front of multiobjective optimization and guide PCVD parameter design. Third, a PSC method is proposed to suppress low-frequency distortion based on the analysis of the time-domain distortion characteristics of the output voltage. Finally, a ±2 kV PCB-based planar capacitive voltage measurement system is developed. This system achieves an upper bandwidth limit of 940 MHz and compact dimensions of 48 mm × 35 mm, validating the effectiveness of the proposed multiobjective optimization method. Furthermore, the effectiveness of the PSC method is verified using a half-bridge converter prototype integrated with the measurement system. Experimental results demonstrate that the compensated output voltage exhibits no significant distortion, and the maximum measurement error is 1.87%.**

***Index Terms*—Planar capacitor, system size, voltage measurement, wide-bandgap (WBG) device.**

## I. Introduction

WIDE-BANDGAP (WBG) devices with superior electrical and thermal performance have become enabling components for high-efficiency, high-power-density power electronic conversion systems, such as photovoltaic inverters [1], electric vehicle drivetrains [2], and aircraft electric propulsion systems [3]. Online monitoring of WBG device voltage switching characteristics is critical for voltage spike detection, aging prediction, and junction temperature estimation [4], [5], [6], [7]. However, for high-power-density converters, online monitoring of WBG devices poses significant challenges to the integration level, galvanically isolated capability, and measurement bandwidth [8] of the measurement system.

Currently, researchers have proposed various voltage-sensing techniques, which are primarily classified into nonisolated and isolated measurements. Among nonisolated measurements, Garrido et al. [9] proposed a solution combining passive high-impedance probes with traditional dividers to extend the measurement range. However, the introduced voltage divider decreases the system integration level. A single-ended probe based on printed circuit board (PCB) planar capacitors was proposed in [10]. Utilizing the superior interlayer insulation of PCB, this probe demonstrates a significant size advantage over conventional solutions. Nevertheless, its bandwidth is limited to 206 MHz due to transmission line parasitic inductance, and there is a problem of insufficient gain in the low-frequency band. Furthermore, nonisolated measurement requires shared reference potentials between the measurement system and the measured signal. Simultaneous measurements of signals with disparate reference potentials cause ground conflicts, creating short-circuit risks. These factors limit nonisolated techniques in WBG device voltage sensing applications.

For isolated measurements, Niklaus et al. [11] proposed a digital optical isolation measurement system. The addition of common-mode chokes and an auxiliary charging circuit at the analog front-end enabled this system to achieve a common-mode rejection ratio (CMRR) exceeding 100 dB within a frequency range of 100 MHz. However, limited by the sampling rate of the analog-to-digital converter (ADC), the system bandwidth merely reached 130 MHz. The authors in [12] and [13], respectively, employed digital isolation chips and wireless transmission technology to achieve galvanic isolation. However, both systems are also constrained by insufficient sampling rates of the ADCs. As a result, the system bandwidth in [12] only reaches 1 MHz, and the data transmission rate of the system in [13] is limited. Moreover, the introduction of the digital control unit decreased the integration level of the measurement system. In [14], a high-voltage differential probe achieving

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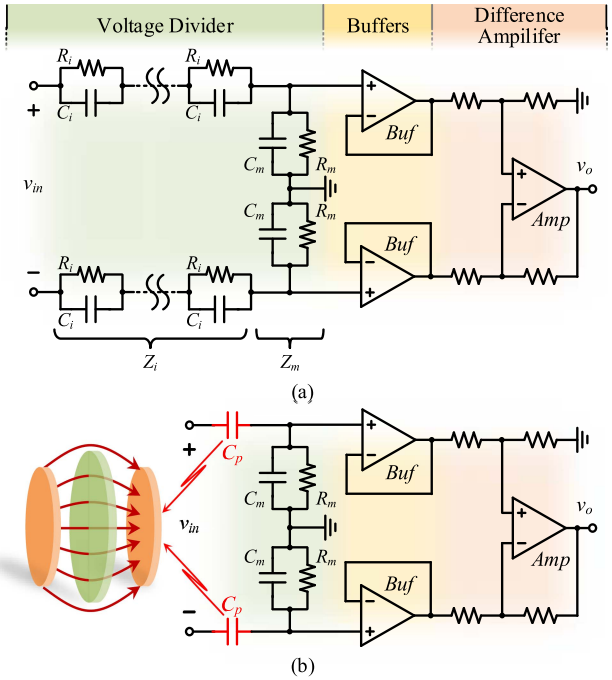


Fig. 1. (a) Traditional differential measurement system. (b) PCB-based planar capacitive voltage measurement system.

0.2% frequency-response flatness below 2 MHz was developed through the integration of frequency-response correction circuits. However, the introduced low-pass filter limited the system bandwidth to 20 MHz. Wang et al. [15] proposed a transmission line voltage divider (TLVD) achieving GHz-level bandwidth, which effectively suppressed bandwidth limitations caused by multilayer ceramic capacitors (MLCCs) parasitic effects and PCB coupling effects by substituting MLCCs with metal parallel plates. However, since the metal parallel plates exhibit a significantly larger size than MLCCs, this leads to a decrease in the integration level of the voltage divider.

The abovementioned analysis indicates that current research primarily focuses on the galvanically isolated capability and bandwidth performance of measurement systems, while the assessment of their physical size has received relatively less attention, thereby constraining the development of compact measurement systems. Among various isolation techniques, wireless transmission and digital isolation technologies require high-performance ADCs and field-programmable gate arrays (FPGAs) to achieve high-speed digital signal transmission, which significantly increases the power consumption and cost of the measurement system. In contrast, the differential measurement technique with floating measurement capability demonstrates higher economic efficiency and lower complexity. However, the front-end of differential measurement systems commonly employs a traditional voltage divider structure, as illustrated in Fig. 1(a). This structure incorporates numerous passive components, limiting the system integration level. Therefore, this article modifies the planar capacitive voltage divider (PCVD) in [10] from single-ended to a differential configuration, as illustrated in Fig. 1(b). To address the challenges of balancing physical size with measurement accuracy and mitigating low-frequency distortion in the PCVD, this article makes the following contributions.

1) A multiobjective optimization method for the PCVD that systematically resolves the trade-offs between physical size and measurement accuracy.
2) A pulse-sampling compensation (PSC) method to effectively suppress output voltage waveform distortion caused by insufficient low-frequency gain in the PCVD.

The remainder of this article is structured as follows. Section II provides a comparative analysis of the factors influencing the sizes of the traditional voltage divider and the PCVD, clearly demonstrating the miniaturization advantages of the PCVD. Section III first establishes the physical size model and measurement error models of the PCVD to derive the feasible performance space and the Pareto front of multiobjective optimization. Subsequently, a solution with a relatively high marginal rate of return is selected from the Pareto front to guide the parameter design of the PCVD. Section IV introduces the PSC method to suppress low-frequency distortion, based on the analysis of the time-domain distortion characteristics of the output voltage. Section V experimentally validates both the compact size and the wide bandwidth of the developed measurement system. Additionally, the effectiveness of the PSC method is validated using a half-bridge converter prototype integrated with the measurement system. Finally, Section VI concludes this article.

## II. Transmission Characteristics and Integration Advantages of PCVD

The differential measurement system comprises three core components: the voltage divider, the buffers, and the differential amplifier, as illustrated in Fig. 1. Among these components, the buffers performing impedance matching and the differential amplifier performing differential-to-single-ended signal conversion both can employ high-speed operational amplifiers with compact packaging and bandwidth exceeding the system target bandwidth to attain satisfactory performance. The voltage divider, in addition to providing precise attenuation of the measured signal, must also withstand high voltage, resulting in it occupying a large proportion of the system size. This section compares the performance differences in size between the PCVD and the traditional voltage divider to demonstrate the advantages of the PCVD in miniaturization.

### A. Limitation in Traditional Voltage Divider Integration

The traditional differential voltage divider is composed of $2N$ identical resistance-capacitance (RC) units $Z_i$ and two identical RC units $Z_m$ connected in series, as illustrated in Fig. 1(a). The resistance network attenuates primarily low-frequency signals, while the capacitance network attenuates primarily high-frequency signals. To increase the bandwidth of the voltage divider, surface-mounted devices with low parasitic parameters are typically selected for the RC components [9]. Furthermore, a highly symmetrical layout enables precise matching of the impedance and frequency response between the signal ground and the two input ports, thus enhancing the CMRR. Therefore, the typical layout diagram of the traditional voltage divider is

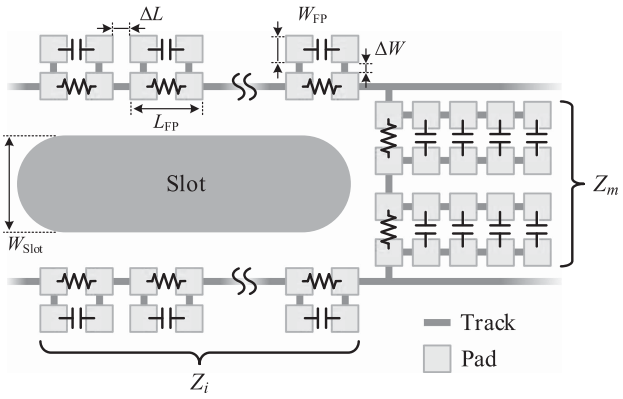


Fig. 2. Typical layout diagram of the traditional voltage divider.

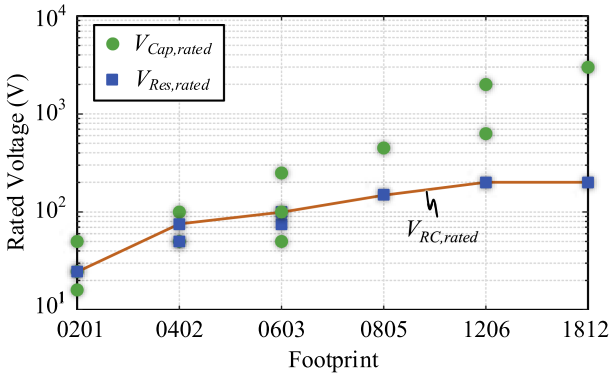


Fig. 3. Rated voltages of surface-mounted RC components.

illustrated in Fig. 2. The following are explanations for this figure.

1) $L_{FP}$ and $W_{FP}$ denote the length and width of the RC component footprint, respectively. $\Delta L$ and $\Delta W$ denote the length and width intervals between footprints, respectively.
2) The closer to the input port, the larger the voltage difference between the two symmetrically arranged $Z_i$. To enhance the creepage distance, an isolation slot of width $W_{Slot}$ is incorporated between paired $Z_i$.
3) Since the unit $Z_m$ withstands only signal-level voltages (within ±5 V), small-sized packages (e.g., 0402 footprint) satisfy its voltage-withstand requirements. Conversely, the series-connected $Z_i$ must withstand the majority of the input voltage. To minimize the number of series units while satisfying the voltage-withstand constraint, $Z_i$ typically operates near its rated voltage. Fig. 3 presents the rated voltages of different surface-mounted RC components, which exceed the signal-level voltages.
4) To decrease the load effect of the voltage divider on the device under test (DUT) and the influence of the parasitic capacitance in resistors, the typical value of the capacitor $C_i$ is several picofarads [16]. The capacitance value of $C_m$ (typically in the hundreds of picofarads) is substantially greater than that of $C_i$ to ensure that the voltage across $Z_i$ is much higher than that across

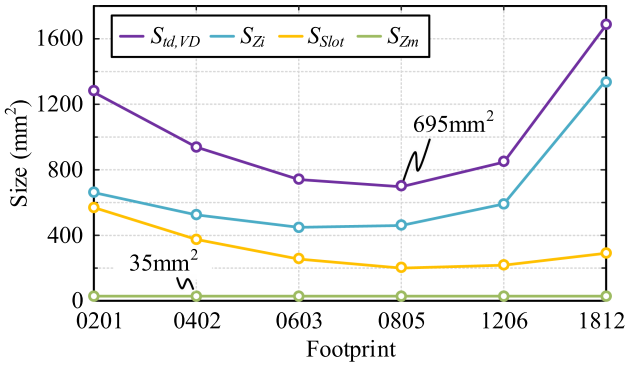


Fig. 4. Physical sizes of the traditional voltage divider.

$Z_m$. However, high-capacitance capacitors exhibit lower self-resonant frequencies, which can limit the bandwidth of the voltage divider [15]. Therefore, $C_m$ is typically implemented through parallel combinations of multiple low-capacitance MLCCs, enhancing the equivalent self-resonant frequency. As illustrated in Fig. 2, this example employs a four-capacitor parallel configuration. The total voltage divider size ($S_{td,VD}$) is determined by the size of $Z_i$ ($S_{Zi}$), the size of $Z_m$ ($S_{Zm}$), and the size of the isolation slot ($S_{Slot}$), expressed as follows:

$$\begin{aligned} S_{td,VD} &= S_{Zi} + S_{Zm} + S_{Slot} \\ &= (Num_{Ri} + Num_{Ci}) \cdot (L_{FP} + \Delta L) \cdot (W_{FP} + \Delta W) \\ &\quad + (Num_{Rm} + Num_{Cm}) \cdot (L_{FP,0402} + \Delta L) \\ &\quad \cdot (W_{FP,0402} + \Delta W) \\ &\quad + \frac{Num_{Ri}}{2} \cdot (L_{FP} + \Delta L) \cdot W_{Slot} \end{aligned} \tag{1}$$

$$\begin{cases} Num_{Ri} = Num_{Ci} = ceil\left(\frac{K|V_{MR}|}{V_{RC,rated}}\right) \\ Num_{Rm} = 1, Num_{Cm} = 4 \\ V_{RC,rated} = \min[\max(V_{Res,rated}), \max(V_{Cap,rated})] \end{cases} \tag{2}$$

where $Num_{Ri}$, $Num_{Ci}$, $Num_{Rm}$, and $Num_{Cm}$ denote the quantities of $R_i$, $C_i$, $R_m$, and $C_m$, respectively. $V_{MR}$ is the voltage measurement range, $K$ is the safety voltage margin coefficient, and ceil is the ceiling function. $L_{FP,0402}$ and $W_{FP,0402}$ are the length and width of the 0402 footprint, respectively. $V_{Res,rated}$ and $V_{Cap,rated}$ are the rated voltage values of the resistor and capacitor, respectively. Considering that the drain-source voltage of current mainstream WBG devices reaches 1.7 kV, the voltage measurement range $V_{MR}$ is set to ±2 kV. For a safety voltage margin coefficient $K = 1.5$, slot width $W_{Slot} = 5$ mm, and footprint intervals $\Delta L = \Delta W = 1$ mm, Fig. 4 shows the sizes of the traditional voltage divider for different footprints. It can be seen that in the high-voltage WBG applications, constrained by the relatively low rated voltages of surface-mounted components, the voltage divider needs to be assembled by multiple components connected in series. Additionally, sufficient creepage distance must be maintained between components. These factors collectively result in a large physical size (exceeding

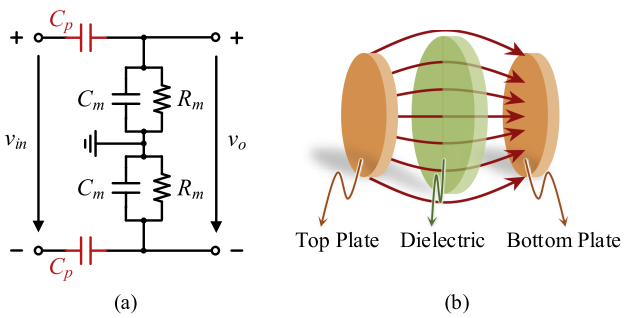


Fig. 5. (a) PCVD circuit. (b) Schematic diagram of a planar capacitor.

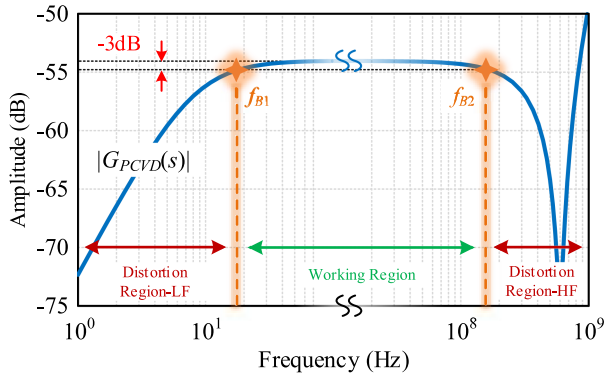


Fig. 6. Schematic diagram of the frequency response curve of the PCVD.

695 mm$^2$), posing significant integration challenges for measurement systems.

### *B. Transmission Characteristics and Size Influencing Factors of the PCVD*

By removing the 2$N$ surface-mounted resistors $R_i$ that withstand high voltage in the traditional voltage divider and replacing the corresponding surface-mounted capacitors $C_i$ with a pair of PCB planar capacitors $C_p$, the PCVD is formed, as illustrated in Fig. 5. Neglecting component parasitic parameters, the transfer function $G_{PCVD}(s)$ from the output terminal to the input terminal of the PCVD can be expressed as follows:

$$G_{PCVD}(s) = \frac{v_o(s)}{v_{in}(s)} = \frac{sR_mC_p}{sR_m(C_p + C_m) + 1}. \quad (3)$$

There exists a cut-off frequency $f_{B1}$ for $G_{PCVD}(s)$, which is expressed as follows:

$$f_{B1} = \frac{1}{2\pi R_m(C_p + C_m)}. \quad (4)$$

Therefore, the transmission characteristics of the PCVD are divided into three regions: the low-frequency distortion region, the high-frequency distortion region, and the working region. The Bode diagram of the PCVD is illustrated in Fig. 6.

1) Low-frequency distortion region (the signal frequency $f < f_{B1}$). In this region, the impedance of $C_m$ is greater than that of $R_m$. The PCVD can be approximately equivalent to a series circuit of $R_m$ and $C_p$, and (3) can be simplified to (5). The gain $|G_{PCVD}(s)|$ is directly proportional to the frequency. This implies that the gain of the PCVD exhibits frequency dependence.

$$G_{PCVD}(s) \approx sR_mC_p \quad (f < f_{B1}). \quad (5)$$

2) High-frequency distortion region ($f > f_{B2}$). In this region, the signal frequency $f$ approaches or exceeds the capacitor's self-resonant frequency, causing the capacitor to no longer exhibit ideal capacitive impedance behavior. This results in a change in the gain of the PCVD. Here, $f_{B2}$ is defined as the frequency corresponding to a gain attenuation of $-3$ dB caused by the change in capacitor characteristics.
3) Working region ($f_{B1} < f < f_{B2}$). In this region, the impedance of $C_m$ is less than that of $R_m$. The PCVD can be approximately equivalent to the series circuit of $C_m$ and $C_p$, and (3) can be simplified to (6). The amplitude of $G_{PCVD}(s)$ is equal to the reciprocal of the attenuation ratio $M$. This implies that the gain of the PCVD is independent of frequency. The frequency range covered by this region is the measurement bandwidth of the PCVD. To accurately capture the switching characteristics of WBG devices, the lower cut-off frequency $f_{B1}$ should be much lower than the switching frequency of the device, while the upper cut-off frequency $f_{B2}$ should be much higher than that switching frequency.

$$G_{PCVD}(s) \approx \frac{C_p}{C_m + C_p} = \frac{1}{M}(f_{B1}<f<f_{B2}). \quad (6)$$

In terms of physical size, the PCVD exhibits obvious advantages compared to the traditional voltage divider. On one hand, owing to the outstanding insulating properties of the PCB interlayer dielectric, the planar capacitor $C_p$ can withstand voltages up to tens of thousands of volts. Consequently, $C_p$ can withstand the rated operating voltage of WBG devices without series connections. Moreover, embedding the capacitor plates within PCB inner layers can effectively reduce the required insulation distance from adjacent components. On the other hand, removing resistors $R_i$ eliminates the constraint imposed by resistor parasitic capacitance on the minimum capacitance of $C_p$ [16], enabling $C_p$ to be designed with substantially lower capacitance than $C_i$. Since the capacitor plate size is positively correlated with the capacitance, reducing the capacitance of $C_p$ directly contributes to reducing the PCVD size. Theoretically, as the capacitance of $C_p$ approaches zero, the plate size also approaches zero. In this case, the PCVD size is dominated by units $Z_m$, which occupy 35 mm$^2$, as illustrated in Fig. 4.

In conclusion, compared to the traditional voltage divider (with the smallest size of 695 mm$^2$), the PCVD that replaces the $Z_i$ units with PCB planar capacitors exhibits a significant advantage in physical size. However, existing designs have not systematically evaluated trade-offs among the physical size, measurement bandwidth, and measurement accuracy of the PCVD. To address this shortcoming, the next section proposes a multiobjective optimization method for the PCVD.

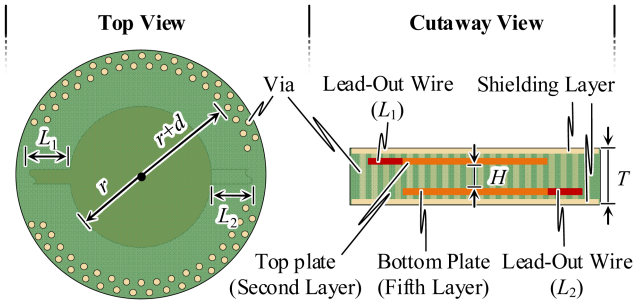


Fig. 7. Schematic diagram of physical structure parameters of the planar capacitor.

## III. Optimization Method of PCVD Parameters

The PCVD measurement error is composed of three factors: the capacitance deviation of the planar capacitor, the input offset error of the buffers, and the low-frequency distortion compensation error. To maximize the PCVD integration level, it is essential to minimize the physical size of the planar capacitor $C_p$ as much as possible. However, this reduction mainly leads to an increase in the capacitance value deviation component of the measurement error. To resolve the conflicting requirements (size vs accuracy), this section proposes a multiobjective optimization method. By establishing the physical size model and error models of the PCVD, the feasible performance space and the Pareto front of multiobjective optimization can be obtained. Subsequently, a solution with a relatively high marginal rate of return is selected from the Pareto front to guide the parameter design of the PCVD.

### A. Objective Functions and Constraints

The planar capacitor employs circular plates to mitigate the edge field concentration effect. Its physical structure parameters are defined in Fig. 7. Taking the plate radius $r$ as the design variable, the optimization objectives are to minimize the relative measurement error $v^*_{error}(r)$ and the physical size $S_{PCVD}(r)$. This optimization is subject to two crucial constraints. First, any design with a relative measurement error exceeding 5% is deemed invalid as it does not meet the accuracy requirements of the system. Second, the system bandwidth must be greater than 500 MHz to accurately measure the switching characteristics of WBG devices [17]. Overall, the multiobjective optimization problem of the PCVD can be expressed as follows:

$$\begin{aligned} \min F(r) &= [v^*_{error}(r), S_{PCVD}(r)] \\ \text{s. t.} \quad & v^*_{error}(r) < 5\%; \\ & BW_{PCVD} > 500\ \text{MHz} \end{aligned} \tag{7}$$

where $F(r)$ denotes the objective vector. From the analysis in Section II, it can be known that the upper limit of the PCVD bandwidth is determined by the lowest resonant frequency of the planar capacitor $C_p$ and the capacitor $C_m$. The resonant frequency of $C_m$ can be obtained from its datasheet. For $C_p$, accurate modeling of its parasitic inductance is challenging. Thus, its resonant frequency needs to be extracted by the finite-element method (FEM). It should be noted that the parasitic inductances of plate lead-out wires $L_1$ and $L_2$ are incorporated into the total parasitic inductance of $C_p$.

### B. Model Construction

*1) Model of Relative Measurement Error: Capacitance deviation:* considering the edge effect, the capacitance value of a circular planar capacitor can be approximated as follows [18]:

$$C_p(r) = \frac{\varepsilon_0\varepsilon_r\pi r^2}{H} + \varepsilon_0\varepsilon_r r \cdot \left(\ln\frac{16\pi r}{H} - 1\right) \tag{8}$$

where $\varepsilon_0$ denotes the vacuum permittivity, $\varepsilon_r$ denotes the relative permittivity of the PCB dielectric, and $H$ denotes the distance between the plates. To reduce the capacitance of $C_p$ (thereby increasing the self-resonant frequency), $H$ is set to the maximum value allowed between the inner layers of the PCB. Moreover, with the attenuation ratio $M$ remaining unchanged, reducing the capacitance of $C_p$ simultaneously decreases the capacitance of $C_m$.

The capacitance deviation $\Delta C_p$ caused by the wire-diameter tolerance ($\Delta l = 0.01$ mm) in the PCB manufacturing process can be expressed as follows:

$$\begin{aligned} \Delta C_p(r) &= C_p(r+\Delta l) - C_p(r) \\ &= \frac{\varepsilon_0\varepsilon_r\pi}{H}\cdot(2r\Delta l + \Delta l^2) + \varepsilon_0\varepsilon_r r\ln\frac{r+\Delta l}{r} \\ &\quad + \varepsilon_0\varepsilon_r\Delta l\cdot\left(\ln\frac{16\pi(r+\Delta l)}{H} - 1\right). \end{aligned} \tag{9}$$

Then, the relative measurement error $v^*_{ec}$ caused by the capacitance deviation of the planar capacitor can be expressed as follows:

$$v^*_{ec}(r) = \frac{MC_p(r) + M\Delta C_p(r)}{MC_p(r) + \Delta C_p(r)} - 1. \tag{10}$$

*Offset error:* the input terminals of an operational amplifier generally connect to the base of a bipolar junction transistor (BJT) or the gate of a field effect transistor (FET). The base current of BJT and the gate leakage current of FET are collectively termed input bias current $i_B$, as illustrated in Fig. 8(a). When this current flows through resistor $R_m$, a voltage drop $v_B$ is generated, which can be expressed as follows:

$$v_B = i_B R_m. \tag{11}$$

Transistor manufacturing tolerances cause input bias current mismatch between buffers. The relative measurement error $v^*_{ei}$ caused by the bias current mismatch can be expressed as follows:

$$v^*_{ei} = \frac{(i_{B1} - i_{B2})R_m M}{v_{in}} \tag{12}$$

where $v_{in}$ denotes the input voltage. To evaluate the maximum possible error, the bias currents $i_{B1}$ and $i_{B2}$ are, respectively, set to their maximum and minimum values. Additionally, the mismatch of the base-emitter voltage of BJT or the threshold voltage of FET results in a voltage difference between the two input terminals of a buffer. The voltage difference is defined as input offset voltage $v_{OS}$, as illustrated in Fig. 8(b). The

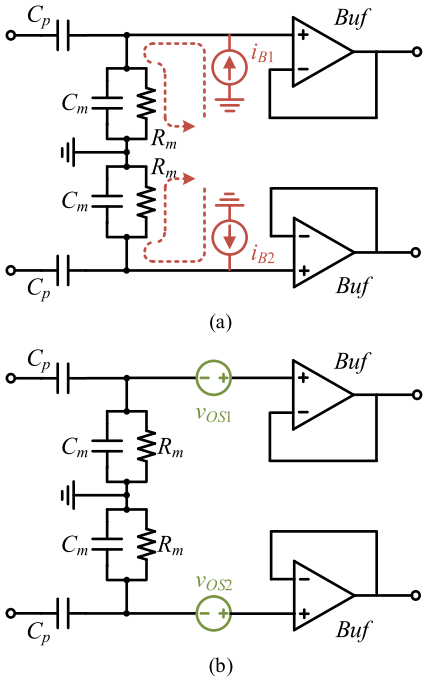


Fig. 8. (a) Equivalent circuit of buffer input bias current. (b) Equivalent circuit of buffer input offset voltage.

relative measurement error $v_{ev}^*$ caused by the offset voltage can be expressed as follows:

$$v_{ev}^* = \frac{(v_{OS1} - v_{OS2})M}{v_{in}}. \tag{13}$$

Similarly, offset voltages $v_{OS1}$ and $v_{OS2}$ are, respectively, set to their maximum and minimum values to evaluate the maximum possible error. As indicated in (12) and (13), reducing $M$ can decrease the offset error caused by the buffers. However, this leads to an increase in the amplitude of the PCVD output signal. High-speed operational amplifiers typically operate with a power supply of ±5 V. It is necessary to ensure that the dynamic range of signals remains within the linear operating region of the amplifier. Considering these factors, it is appropriate to set the attenuation ratio $M$ at 500 for the PCVD with a ±2 kV measurement range. Furthermore, the adoption of precision high-speed operational amplifiers can further reduce the offset error. Single-channel operational amplifiers from TI that are unity-gain stable and feature a bandwidth greater than 1 GHz were screened, and their key parameters are listed in Table I. Based on the PCVD transmission characteristics described in Section II, the lower cut-off frequency $f_{B1} = 1/2\pi MR_mC_p$ should be significantly lower than the switching frequency. Therefore, for the capacitance of $C_p$ on the order of picofarads, the resistance of $R_m$ should be in the megohm range. When the resistance of $R_m$ is 1 MΩ, a bias current of merely 1 $\mu$A can cause an error of 1 V, which is unacceptable. Therefore, the OPA859 with low bias current (±5 pA) and low offset voltage (±5 mV) was selected as the buffer.

*Low-frequency distortion compensation error:* the relative compensation error $v_{ep}^*$ from the PSC method proposed in Section IV can be expressed as follows:

TABLE I
KEY PARAMETERS OF HIGH-SPEED OPERATIONAL AMPLIFIERS FROM TI

| Model | Bandwidth | Max $i_B$ | Max $v_{OS}$ |
|---|---|---|---|
| OPA859 [19] | 1.8 GHz | 5 pA | 5 mV |
| OPA856 | 1.1 GHz | 20 µA | 1.5 mV |
| OPA693 | 1.4 GHz | 54 µA | 2.5 mV |
| OPA694 | 1.5 GHz | 38 µA | 4.1 mV |
| OPA695 | 1.7 GHz | 70 µA | 4 mV |
| BUF602 | 1 GHz | 8.5 µA | 38 mV |
| BUF802 | 3.1 GHz | 220 pA | 900 mV |
| LMH6702 | 1.7 GHz | 34 µA | 6 mV |
| LMH6703 | 1.8 GHz | 44 µA | 9 mV |
| LMH6559 | 1.75 GHz | 14 µA | 25 mV |
| THS4211 | 1 GHz | 8 µA | 14 mV |
| THS4215 | 1 GHz | 8 µA | 14 mV |
| THS4271 | 1.4 GHz | 18 µA | 12 mV |
| THS4275 | 1.4 GHz | 8 µA | 12 mV |
| THS4304 | 1 GHz | 20 µA | 6 mV |

$$v_{ep}^*(r) = \frac{1 - e^{-\frac{1}{2f_{sw}R_mMC_p(r)}}}{2} \tag{14}$$

where $f_{sw}$ denotes the switching frequency. The detailed derivation and explanation of this expression will be presented in Section IV. As can be inferred from (14), the relative compensation error $v_{ep}^*$ is negatively correlated with the switching frequency $f_{sw}$. To evaluate the maximum possible error, this article chooses the lower limit of the switching frequency commonly employed in practical applications of SiC MOSFETs ($f_{sw} = 20$ kHz) as the analysis case [20]. Furthermore, the compensation error $v_{ep}^*$ is negatively correlated with $R_m$. However, (12) shows that the error $v_{ei}^*$ caused by bias currents is positively correlated with $R_m$. By differentiating the sum of the two errors, (15) can be obtained. The sum of the errors first decreases and then increases over $R_m \in (0, +\infty)$. Therefore, there exists an optimal value $R_{m0}$ that minimizes the sum of the errors. This value can be obtained by numerical methods.

$$\frac{dv_{ei}^* + v_{ep}^*}{dR_m} = \frac{(i_{B1} - i_{B2})M}{v_{in}} - \frac{e^{-\frac{T_{sw}}{2R_mMC_p}}}{2} \cdot \frac{T_{sw}}{2R_m^2MC_p}. \tag{15}$$

In summary, the total relative measurement error $v_{error}^*(r)$ can be expressed as follows:

$$v_{error}^*(r) = v_{ec}^*(r) + v_{ei}^* + v_{ev}^* + v_{ep}^*(r). \tag{16}$$

*2) Model of Physical Size:* To enhance the noise immunity of planar capacitors, shielding layers are added to the outside of the plates and interconnected through vias [10]. Since the plates are positioned in the PCB inner layers, a safety insulation distance $d = 1$ mm between plate edges and shielding vias is sufficient, as shown in Fig. 7. Fig. 9 shows the layout diagram of the PCVD, where $D$ denotes the horizontal distance between the two planar capacitors. Since the shielding vias at the plate edges are at the same potential, $D$ is set to 1 mm in this design. Similar to traditional divider modeling, the capacitor $C_m$ comprises

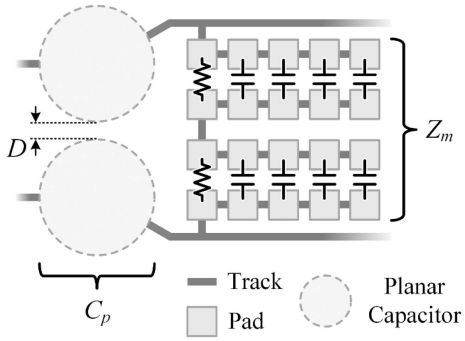


Fig. 9. PCVD layout diagram.

four MLCCs in parallel. Therefore, the PCVD size ($S_{PCVD}$) is determined by the size of the planar capacitors ($S_{Cp}$), and the size of the units $Z_m$ ($S_{Zm}$), expressed as (17). It should be noted that the geometric dimensions of the planar capacitor are calculated using a square that is tangent to the plate edge, since the part outside the ring within the square is an invalid region and cannot be employed for component layout.

$$\begin{aligned} S_{PCVD} &= S_{Cp} + S_{Zm} \\ &= [4(r+d)+D]\cdot 2(r+d) \\ &\quad + (Num_{Rm} + Num_{Cm})\cdot(L_{FP,0402} + \Delta L) \\ &\quad \cdot (W_{FP,0402} + \Delta W). \end{aligned} \tag{17}$$

### C. Performance Space

Fig. 10 illustrates the flowchart for the parameter design optimization of the PCVD, with its execution steps as follows.

1) Define the system specifications (input and output voltage ranges), constraint conditions (lower bandwidth limit and upper error limit), and the design variable (plate radius *r*).
2) Perform a parametric sweep of the plate radius *r* over the range of 0–10 mm with a step size of 0.01 mm to ensure calculation accuracy.
3) Substitute the swept value into the two objective functions (16) and (17) to compute their values, and evaluate whether the corresponding design scheme meets the constraints.
4) Output the schemes that satisfy the constraints. For those that do not, adjust the value of the radius *r* and repeat the objective function calculation and constraint evaluation.

The results of the parametric sweep are illustrated in Fig. 11(a): the total relative measurement error $v^*_{error}(r)$ exhibits a negative correlation with *r*, whereas the physical size $S_{PCVD}(r)$ shows a positive correlation with *r*. This implies that adjusting the value of *r* cannot simultaneously achieve the dual objectives of "minimizing $v^*_{error}(r)$ and $S_{PCVD}(r)$." In other words, each value of *r* corresponds to a Pareto optimal solution. The set of objective vectors $F(r)$ corresponding to all optimal solutions that meet the constraint conditions forms the Pareto front, as illustrated in Fig. 11(b).

In multiobjective optimization problems, the knee point on the Pareto front is generally considered to be the point at which

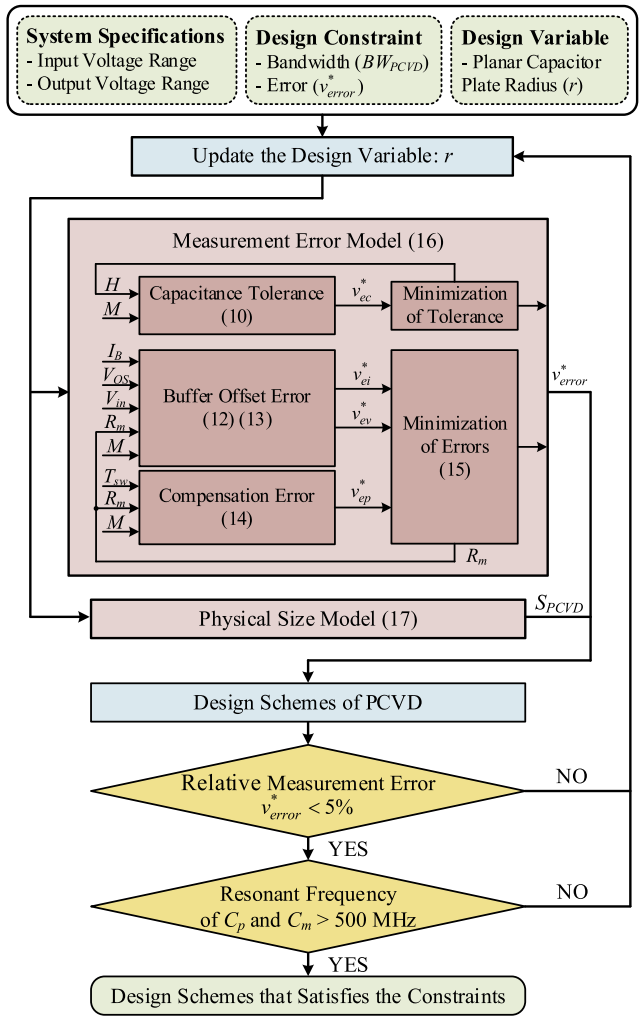


Fig. 10. Flowchart of the PCVD parameter design optimization.

the marginal rate of return is maximized. This article adopts the knee point definition and identification method proposed in [21], with the specific steps as follows:

First, identify the two extreme points on the Pareto front: Extreme Point 1 (corresponding to the maximum measurement error) and Extreme Point 2 (corresponding to the minimum measurement bandwidth). Second, connect these two extreme points to form an extreme line, which can be expressed as follows:

$$y - kx - b = 0 \tag{18}$$

where *x*, *y*, *k*, and *b* denote the physical size, relative measurement error, slope of the extreme line, and intercept of the line, respectively. Ultimately, the vertical distances from each point on the Pareto front to this extreme line are calculated using the following equation:

$$d_i = \frac{|y_i - kx_i - b|}{\sqrt{1+k^2}} \tag{19}$$

where $x_i$, $y_i$, and $d_i$ denote the physical size, relative measurement error, and vertical distance to the extreme line of

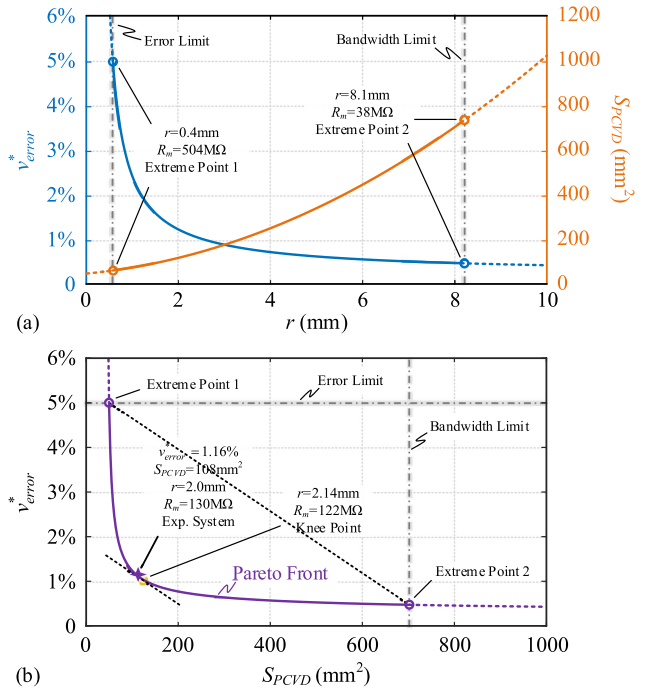


Fig. 11. (a) Relationship curve between the design variable (plate radius $r$) and the objective functions [relative measurement error $v^*_{error}(r)$ and physical size $S_{PCVD}(r)$]. (b) Feasible performance space of the PCVD.

TABLE II
PHYSICAL STRUCTURE PARAMETERS OF THE PLANAR CAPACITOR

| Parameters | Value |
|---|---|
| Number of layers | 6 |
| Relative permittivity ($\varepsilon_r$) | 4.6 |
| Loss tangent ($\tan\delta$) | 0.018 |
| Board thickness (T) | 1.92 mm |
| Plate radius ($r$) | 2 mm |
| Plate spacing ($H$) | 1.36 mm |
| Lead-out wire length ($L_1$) | 10 mm (Width: 0.762 mm) |
| Lead-out wire length ($L_2$) | 2 mm (Width: 0.762 mm) |
| Via-to-edge distance($d$) | 1 mm |

the $i$th point on the Pareto front, respectively. The point with the maximum distance to the extreme line is identified as the knee point, which is marked by a yellow circle in Fig. 11(b) for clarity. At this knee point, the plate radius $r = 2.14$ mm, the relative measurement $v^*_{error}(r) = 1.11\%$, and the physical size $S_{PCVD}(r) = 115$ mm$^2$. Under the premise of ensuring no significant impact on the overall system performance and considering the convenience of engineering design, this article selects the design scheme with a radius $r = 2$ mm (near the knee point) to guide the PCVD design. The corresponding objective function values are $v^*_{error}(r) = 1.16\%$ and $S_{PCVD}(r) = 108$ mm$^2$. Based on this design scheme, the physical structure parameters of the planar capacitor are listed in Table II, and the component parameters and core characteristic parameters of the PCVD are summarized in Table III. It can be seen from Table III that the resonant frequency of the planar capacitor $C_p$ is 2.4 GHz, while that of the capacitor $C_m$ is 1 GHz. Therefore, the upper bandwidth limit of the measurement system is constrained to within 1 GHz.

TABLE III
COMPONENT PARAMETERS AND CHARACTERISTIC PARAMETERS OF THE PCVD

| Parameters | | Value |
|---|---|---|
| Planar capacitor ($C_p$) | Capacitance | 0.316 pF |
| | ESL | 13.77 nH |
| | ESR | 19.18 mΩ |
| | Resonant frequency | 2.4 GHz |
| Capacitor ($C_m$) | Capacitance | 156 pF=(4×39pF) CGA2B2C0G1H390J05 0BA (TDK) [22] |
| | Resonant frequency | 1 GHz |
| Resistor ($R_m$) | | 130 MΩ |
| Buf OPA859 | Bias current ($i_B$) | ±5 pA |
| | Offset voltage ($v_{OS}$) | ±5 mV |
| Attenuation ratio ($M$) | | 500:1 |
| Cut-off frequency ($f_{B1}$) | | 7.8 Hz |
| Relative error ($v^*_{error}$) | | 1.16% |
| Physical size ($S_{PCVD}$) | | 108 mm$^2$ |

## IV. LOW-FREQUENCY DISTORTION PSC METHOD

Compared with the traditional voltage divider, the PCVD that substitutes the RC units $Z_i$ with PCB planar capacitors shows significant advantages in terms of physical size. However, removing the resistor $R_i$ also results in low-frequency gain droop, as illustrated in Fig. 6. This section first analyzes the time-domain characteristics of the WBG device's drain-source voltage after passing through the PCVD. Based on this analysis, a PSC method is proposed, which can effectively suppress distortion under both Pulse Width Modulation (PWM) and Sinusoidal Pulse Width Modulation (SPWM) strategies and exhibits universality. Finally, the physical size of the introduced components and the compensation error of this method are analyzed.

### A. Analysis of Low-Frequency Distortion Characteristics

As the focus of this section is to analyze the impact of the PCVD on low-frequency components of the drain-source voltage $v_{ds}$, the switching transient process and high-frequency ringing are neglected. An ideal switching waveform is adopted to substitute for the actual drain-source voltage waveform [22]. For the power device operating under the PWM strategy, its drain-source voltage waveform is substituted with an ideal PWM waveform, as illustrated in Fig. 12(a). Fourier analysis reveals that the PWM wave contains a dc component and carrier harmonic components, as illustrated in Fig. 12(b). The dc component located in the low-frequency distortion region is defined as the low-frequency component $v_{ds1,LF}(t)$. It can be expressed as follows:

$$v_{ds1,LF}(t) = (1-d)v_{DC} \tag{20}$$

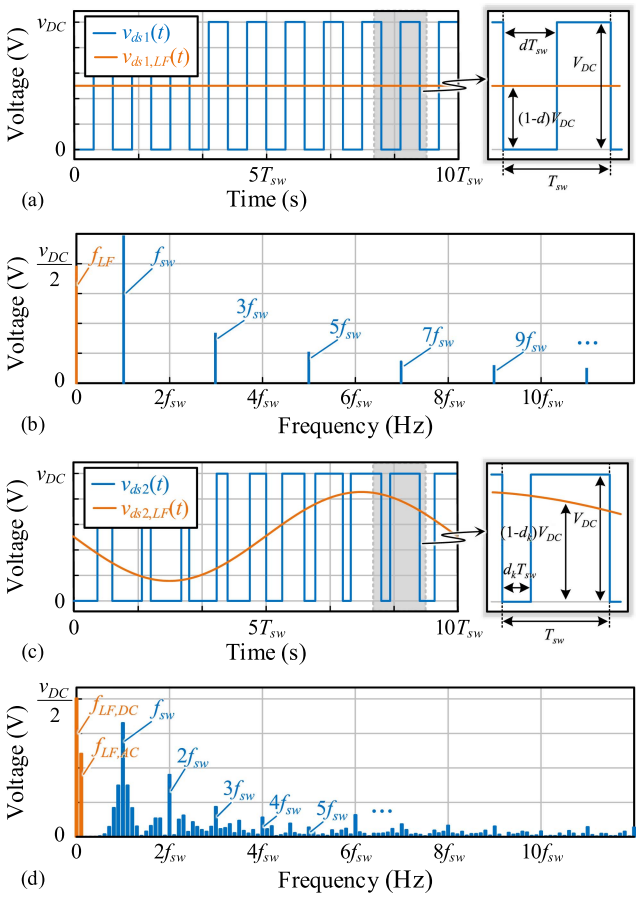


Fig. 12. (a) PWM wave and (b) its spectrum. (c) SPWM wave and (d) its spectrum.

where $v_{dc}$ and $d$ denote the dc-link voltage and the on-state duty cycle, respectively. When the input is the low-frequency component $v_{ds1,LF}(t)$, the $s$-domain expression $v_{o1,LF}(s)$ of the PCVD output voltage is

$$v_{o1,LF}(s)=v_{ds1,LF}(s)\cdot G_{PCVD}(s)=\frac{(1-d)v_{DC}R_mC_p}{sR_m(C_p+C_m)+1}. \tag{21}$$

By performing the inverse Laplace transform on $v_{o1,LF}(s)$, the time-domain expression $v_{o1,LF}(t)$ is obtained. It can be expressed as follows:

$$v_{o1,LF}(t)=\frac{(1-d)v_{DC}}{M}\cdot e^{-\frac{t}{R_m(C_p+C_m)}} \tag{22}$$

where $M$ denotes the attenuation ratio. It can be known from (22) that after the low-frequency component is attenuated by a factor of $M$, its value still decreases exponentially with time and finally approaches zero. The distortion amount $\Delta v_{o1,LF}(t)$ can be expressed as follows:

$$\Delta v_{o1,LF}(t)=\frac{(1-d)v_{DC}}{M}\cdot\left(1-e^{-\frac{t}{R_m(C_p+C_m)}}\right). \tag{23}$$

Next, an analysis is conducted on the time-domain characteristics of the PCVD output voltage when the input is the PWM wave. The $s$-domain expression $v_{ds1}(s)$ of the PWM wave is

$$v_{ds1}(s)=v_{DC}\cdot\frac{e^{-dT_{sw}s}-e^{-T_{sw}s}}{s}\cdot\frac{1}{1-e^{-T_{sw}s}} \tag{24}$$

where $T_{sw}$ denotes the switching period. Then, the $s$-domain expression $v_{o1}(s)$ of the PCVD output voltage is

$$\begin{aligned}v_{o1}(s)&=v_{ds1}(s)\cdot G_{PCVD}(s)\\&=\frac{e^{-dT_{sw}s}-e^{-T_{sw}s}}{1-e^{-T_{sw}s}}\cdot\frac{v_{DC}R_mC_p}{sR_m(C_p+C_m)+1}.\end{aligned} \tag{25}$$

Applying the inverse Laplace transform to (25) yields the time-domain output voltage $v_{o1}(t)$, which can be expressed as follows:

$$\begin{aligned}v_{o1}(t)=&\frac{v_{DC}}{M}\cdot\sum_{n=0}^{+\infty}\delta(t-nT_{sw})\\&*\left[e^{-\frac{t-dT_{sw}}{R_m(C_p+C_m)}}\cdot\varepsilon(t-dT_{sw})-e^{-\frac{t-T_{sw}}{R_m(C_p+C_m)}}\cdot\varepsilon(t-T_{sw})\right]\end{aligned} \tag{26}$$

where $\delta(t\text{-}nT_{sw})$, $\varepsilon(t\text{-}dT_{sw})$, and $\varepsilon(t\text{-}T_{sw})$, respectively, denote the unit impulse function with a delay of $nT_{sw}$, the unit step function with a delay of $dT_{sw}$, and the unit step function with a delay of $T_{sw}$. The symbol "$*$" denotes convolution. The output voltage is divided into two components: the on-state voltage $v_{o1,on}(t)$ and the off-state voltage $v_{o1,off}(t)$. Then the output voltage during the $k$th switching period is

$$\begin{aligned}v_{o1,on}(t)=&\frac{v_{DC}}{M}\cdot\frac{e^{\frac{dT_{sw}}{R_m(C_p+C_m)}}-e^{\frac{T_{sw}}{R_m(C_p+C_m)}}}{1-e^{\frac{T_{sw}}{R_m(C_p+C_m)}}}\\&\cdot\left(e^{-\frac{t}{R_m(C_p+C_m)}}-e^{-\frac{t-kT_{sw}}{R_m(C_p+C_m)}}\right)\end{aligned} \tag{27}$$

$$v_{o1,off}(t)=v_{out1,on}(t)+\frac{v_{DC}}{M}\cdot e^{-\frac{t-(k+d)T_{sw}}{R_m(C_p+C_m)}}. \tag{28}$$

Since the cut-off frequency $f_{B1}=1/2\pi R_m(C_p+C_m)$ of the PCVD is much lower than the switching frequency $f_{sw}$, the on-state voltage $v_{o1,on}(t)$ can be simplified as follows:

$$\begin{aligned}v_{o1,on}(t)&\approx\frac{(1-d)v_{DC}}{M}\cdot\left(e^{-\frac{t}{R_m(C_p+C_m)}}-1\right)\\&\approx-\Delta v_{o1,LF}(t).\end{aligned} \tag{29}$$

From (29), it can be seen that the on-state voltage $v_{o1,on}(t)$ is approximately equal to the negative of the low-frequency distortion amount $\Delta v_{o1,LF}(t)$. This provides a theoretical foundation for low-frequency distortion compensation.

For the power device operating under the SPWM strategy, its drain-source voltage waveform is substituted with an ideal SPWM waveform, as illustrated in Fig. 12(c). The expression $d(t)$ for the on-state duty cycle is

$$d(t)=0.5+m\sin(w_ot) \tag{30}$$

where $m$ and $w_o$, respectively, denote the amplitude and angular frequency of the fundamental component in the modulated wave.

Double Fourier analysis of the SPWM wave reveals that it contains a dc component, a fundamental component, carrier harmonic components, and groups of sideband harmonic components around the carrier [24], as illustrated in Fig. 12(d). The dc and fundamental components located in the low-frequency

distortion region are defined as the low-frequency component $v_{ds2,LF}(t)$, which can be expressed as follows:

$$v_{ds2,LF}(t) = [1 - d(t)]v_{DC} = 0.5v_{DC} - mv_{DC}\sin(wt) \tag{31}$$

When the input is the low-frequency component $v_{ds2,LF}(t)$, the PCVD output voltage $v_{o2,LF}(t)$ in the time domain is (32) shown at the bottom of this page. Then the distortion amount $\Delta v_{o2,LF}(t)$ can be expressed as (33) shown at the bottom of this page.

Next, an analysis is conducted on the time-domain characteristics of the PCVD output voltage when the input is the SPWM wave. In order to facilitate the Laplace transformation, the duty cycle within each switching period is considered as a constant. This method is the Regular Sampling Pulse Width Modulation that is extensively employed in engineering. In this method, the modulating wave is sampled once within each carrier period, and the sampled value is taken as the duty cycle of the current carrier period. For sufficiently high carrier ratios, the difference between the regular sampling method and the natural sampling method can be neglected. Considering that most power electronic converters satisfy the condition of a high carrier ratio, this simplification is reasonable. Then the on-state duty cycle $d_k$ of the $k$th switching period can be expressed as (34). The $s$-domain expression $v_{ds2}(s)$ of the SPWM wave can be expressed as (35).

$$d_k = 0.5 + m\sin(w_o \cdot kT_{sw}) \tag{34}$$

$$v_{ds2}(s) = v_{DC} \cdot \sum_{n=0}^{+\infty} \frac{e^{-(n+d_n)T_{sw}s} - e^{-(n+1)T_{sw}s}}{s}. \tag{35}$$

The time-domain output voltage $v_{o2}(t)$ can be expressed as follows:

$$v_{o2}(t) = \frac{v_{DC}}{M} \cdot \sum_{n=0}^{+\infty} \{e^{-\frac{t-(n+d_n)T_{sw}}{R_m(C_p+C_m)}} \cdot \varepsilon[t-(n+d_n)T_{sw}] - e^{-\frac{t-(n+1)T_{sw}}{R_m(C_p+C_m)}} \cdot \varepsilon[t-(n+1)T_{sw}]\} \tag{36}$$

where $\varepsilon[t\text{-}(n+d_n)T_{sw}]$ and $\varepsilon[t\text{-}(n+1)T_{sw}]$, respectively, denote the unit step function with a delay of $(n+d_n)T_{sw}$ and the unit step function with a delay of $(n+1)T_{sw}$. The output voltage is divided into two components: the on-state voltage $v_{o2,on}(t)$ and the off-state voltage $v_{o2,off}(t)$. Then the output voltage during the $k$th switching period is

$$v_{o2,on}(t) = \frac{v_{DC}C_p}{C_p+C_m} \cdot e^{-\frac{t}{R_m(C_p+C_m)}} \cdot \sum_{n=0}^{k-1} (e^{\frac{(n+d_n)T_{sw}}{R_m(C_p+C_m)}} - e^{\frac{(n+1)T_{sw}}{R_m(C_p+C_m)}}) \tag{37}$$

$$v_{o2,off}(t) = v_{o2,on}(t) + \frac{v_{DC}C_p}{C_p+C_m} \cdot e^{-\frac{t-(k+d_k)T_{sw}}{R_m(C_p+C_m)}}. \tag{38}$$

Fig. 13(b) plots the waveforms of the output voltage $v_{o2}(t)$ and the negative of the low-frequency distortion amount $\Delta v_{o2,LF}(t)$ based on the time-domain expressions. It can be seen that the on-state voltage $v_{o2,on}(t)$ is approximately equal to the negative of the low-frequency distortion amount $\Delta v_{o2,LF}(t)$. This distortion characteristic is consistent with the PWM strategy.

In three-phase systems, a common-mode component $e(t)$ is typically superimposed on the sinusoidal modulation wave to improve the utilization efficiency of the dc voltage. The common-mode components should cancel each other out in the three-phase load to ensure that the sinusoidal characteristics of the output voltage remain unaffected. Therefore, the common-mode component is typically composed of dc components, third harmonics, and integer multiple harmonic components. For instance, in the Third Harmonic Injection Pulse Width

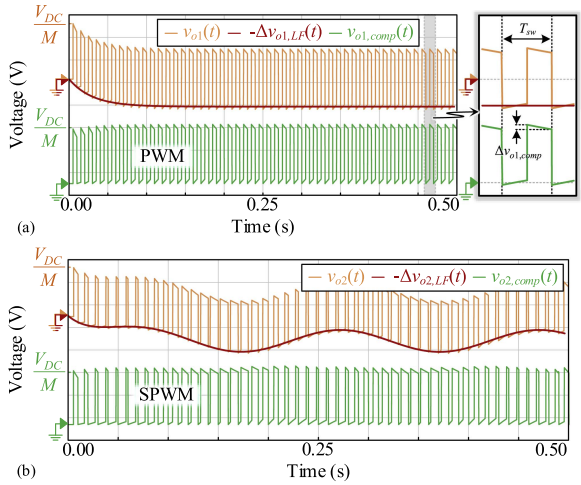


Fig. 13. Waveforms of the uncompensated output voltage (orange), the negative of the low-frequency distortion component (dark red), and the compensated output voltage (green) under input conditions of (a) the PWM wave and (b) the SPWM wave.

$$v_{o2,LF}(t) = \frac{v_{DC}}{M} \cdot \left\{ \left( \frac{1}{2} + \frac{mwR_m(C_p+C_m)}{w^2R_m^2(C_p+C_m)^2+1} \right) \cdot e^{-\frac{t}{R_m(C_p+C_m)}} - \frac{mwR_m(C_p+C_m)}{w^2R_m^2(C_p+C_m)^2+1} \cdot [\cos(wt) + wR_m(C_p+C_m)\sin(wt)] \right\} \tag{32}$$

$$\Delta v_{o2,LF}(t) = \frac{v_{DC}}{M} \cdot \left\{ \frac{1}{2} - \left( \frac{1}{2} + \frac{mwR_m(C_p+C_m)}{w^2R_m^2(C_p+C_m)^2+1} \right) e^{-\frac{t}{R_m(C_p+C_m)}} - m\sin(wt) + \frac{mwR_m(C_p+C_m)}{w^2R_m^2(C_p+C_m)^2+1} \cdot [\cos(wt) + wR_m(C_p+C_m)\sin(wt)] \right\}. \tag{33}$$

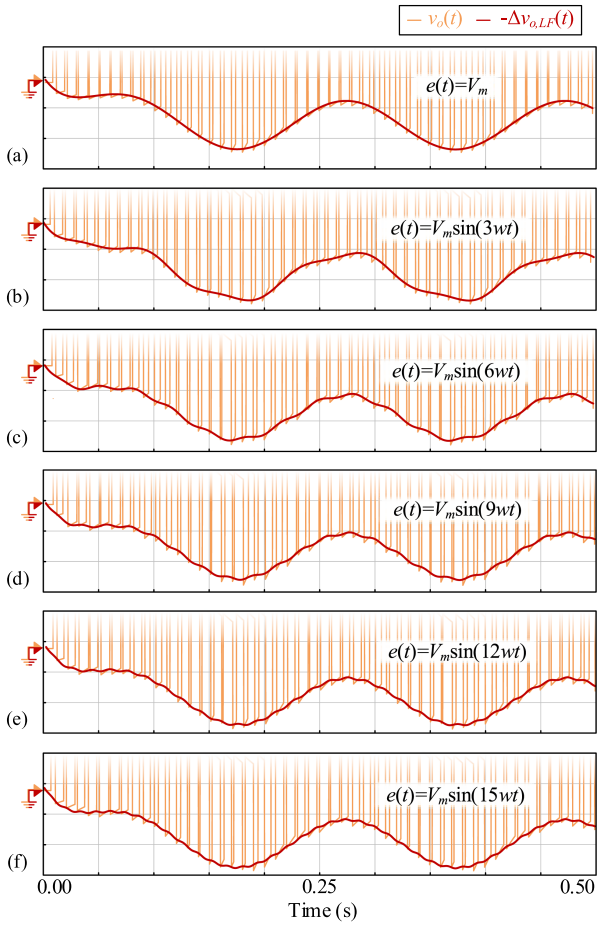


Fig. 14. Waveforms of the uncompensated output voltage (orange) and the negative of the low-frequency distortion component (dark red) when the drain-source voltage [obtained under the modulation strategy of injecting (a) DC component, (b) third harmonic component, (c) sixth harmonic component, (d) ninth harmonic component, (e) twelfth harmonic component, and (f) fifteenth harmonic component into the sinusoidal modulation wave] serves as the input of the PCVD.

Modulation (THPWM) strategy, the third harmonic component is injected into the sinusoidal modulation wave. The Space Vector Pulse Width Modulation (SVPWM) strategy can be considered equivalent to a carrier-based PWM strategy that injects a common-mode component into the sinusoidal modulation wave [25]. For the classic SVPWM strategy, the common-mode component mainly includes the third harmonic, ninth harmonic, and fifteenth harmonic components. Fig. 14 shows the waveforms of the PCVD output voltage $v_o(t)$ and the negative of the low-frequency distortion component $\Delta v_{o,LF}(t)$ under the modulation strategy of injecting different harmonic components into the sinusoidal modulation wave. It can be seen from the figure that regardless of the frequency of the injected harmonics, the distortion characteristic that "the on-state voltage $v_{o,on}(t)$ is approximately equal to the negative of the low-frequency distortion $\Delta v_{o,LF}(t)$" is satisfied.

### B. Operational Principle of PSC Method

The abovementioned theoretical analysis demonstrates that under the strategies of PWM, SPWM, and injection of common-mode components, the value of the PCVD output voltage during the on-state stage is approximately equal to the negative of the low-frequency distortion amount. Based on this conclusion, the PSC method is proposed: within each switching period, the on-state output voltage $v_{o,on}(t)$ is sampled by a trigger pulse and used as the compensation amount $v_{o,offset}(t)$ for the current switching period. Then, the compensation amount $v_{o,offset}(t)$ is subtracted from the original output voltage $v_o(t)$, yielding the compensated voltage $v_{o,comp}(t)$.

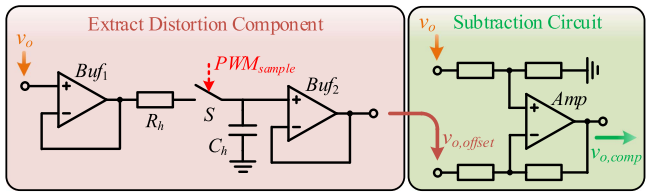


Fig. 15. Schematic diagram of the compensation circuit.

The schematic diagram of the compensation circuit is illustrated in Fig. 15. It is composed of an input buffer $Buf_1$, a sampling switch $S$, a damping resistor $R_h$, a hold capacitor $C_h$, an output buffer $Buf_2$, and a subtraction circuit. The input buffer $Buf_1$ is introduced to attain a high input impedance for the compensation circuit, so as to reduce the loading effect of the compensation circuit on the original output voltage $v_o(t)$. When the DUT is fully on-state stage, the sampling pulse $PWM_{sample}$ drives the sampling switch $S$ to close, and the hold capacitor $C_h$ starts to charge. It is crucial to note that after the DUT completes the turn-ON process, its drain-source voltage will be accompanied by a ringing with a decaying amplitude [26]. Under operating scenarios featuring high switching frequencies or low on-state duty cycle, if waiting for the ringing to completely decay (which usually lasts for several microseconds), the available sampling time will be insufficient. If the sampling switch $S$ is closed before the ringing completely decays, the sampled voltage will contain this ringing component, thereby degrading the compensation effectiveness. To suppress ringing, a damping resistor $R_h$ is inserted in series within the sampling loop, forming a first-order RC low-pass filter together with the hold capacitor $C_h$. Furthermore, while efficiently filtering out ringing, to minimize the charging time of the hold capacitor $C_h$, the cut-off frequency of the filter is set to one-tenth of the ringing frequency. After the charging process lasts for five RC time constants, the switch $S$ is opened, and the circuit enters the hold stage. To reduce the charge leakage on the capacitor $C_h$ during the hold stage, the sampling voltage needs to pass through an output buffer $Buf_2$. The output of $Buf_2$ is the compensation amount $v_{o,offset}(t)$. Finally, by means of a subtraction circuit, the compensation amount $v_{o,offset}(t)$ is subtracted from the original output voltage $v_o(t)$, yielding the compensated voltage $v_{o,comp}(t)$.

### C. Physical Size of Compensation Circuit

The component models and package dimensions employed in the compensation circuit are listed in Table IV. The buffer

TABLE IV
PACKAGE AND DIMENSIONS OF KEY COMPONENTS IN THE COMPENSATION CIRCUIT

| Model | Package | Dimension |
|---|---|---|
| OPA859 | WSON-8 | 2 mm×2 mm |
| LMH6703 | SOIC-8 | 4.9 mm×3.9 mm |
| TMUX6202 | WQFN-8 | 3 mm×2 mm |

uses the WSON-8 packaged OPA859, with dimensions of 2 mm × 2 mm; the differential amplifier uses the SOIC-8 packaged LMH6703, with dimensions of 4.9 mm × 3.9 mm; the sampling switch $S$ uses the WQFN-8 packaged TMUX6202, with dimensions of 3 mm × 2 mm. A 100 nF high-frequency decoupling capacitor in a 0402 package and a 10 $\mu$F low-frequency decoupling capacitor in an 0805 package are each placed adjacent to the power supply pins of the buffer, the differential amplifier, and the sampling switch. The resistor $R_h$, the hold capacitor $C_h$, and the four precision resistors in the subtraction circuit are all surface-mounted devices in 0402 package. In summary, the physical size of the compensation circuit is approximately 80 mm$^2$. Therefore, the total physical size of the PCVD, including the compensation circuit, is 188 mm$^2$, which is still significantly smaller than that of traditional voltage dividers (695 mm$^2$).

### D. Analysis of Compensation Error

The proposed compensation method exhibits two error sources: First, (29) is a simplified result. That is to say, the on-state output voltage $v_{o1,on}(t)$ is extremely close to the negative of the distortion amount $\Delta v_{o1,LF}(t)$, yet the two are not completely identical. Second, the distortion amount $\Delta v_{o1,LF}(t)$ is a time-varying amount. However, the compensation method samples the on-state output voltage $v_{o1,on}(t)$ at a certain moment and applies it as the compensation amount throughout the entire switching period. Taking the buck converter as an example, the magnitude of the compensation error is quantitatively analyzed. The compensated output voltage $v_{o1,comp}(t)$ in the $k$th switching period is

$$v_{o1,on,comp}(t) = \frac{(1-d)v_{DC}}{M} \cdot \left(1 - e^{-\frac{t-kT_{sw}}{R_m(C_p+C_m)}}\right) \quad (39)$$

$$v_{o1,off,comp}(t) = \frac{(1-d)v_{DC}}{M} \cdot \left(1 - e^{-\frac{t-kT_{sw}}{R_m(C_p+C_m)}}\right) + \frac{v_{DC}}{M} \cdot e^{-\frac{t-(k+d)T_{sw}}{R_m(C_p+C_m)}}. \quad (40)$$

It can be observed from (39) and (40) that the compensated voltage during the on-state and off-state stages still contains exponential terms, which do not coincide with the constant values of the ideal PWM wave. When the on-state duty cycle is equal to 50%, the amplitude of the voltage variation reaches its maximum value, which can be expressed as follows:

$$\Delta v_{o1,comp} \approx \frac{v_{DC}}{2M} \cdot \left(1 - e^{-\frac{T_{sw}}{2R_m(C_p+C_m)}}\right). \quad (41)$$

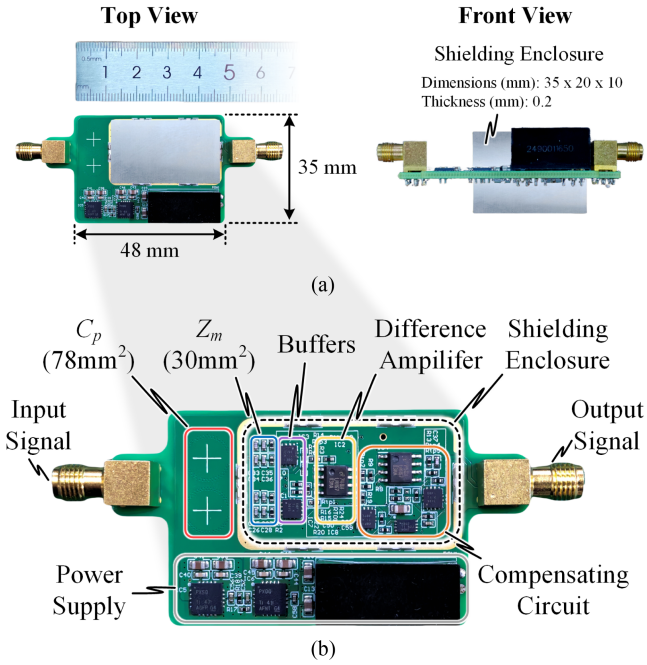


Fig. 16. (a) Size diagram of the hardware prototype for the performance. (b) Relevant circuit blocks are highlighted.

Then, the relative compensation error $v_{ep}^*$ can be expressed as follows:

$$v_{ep}^* = \frac{\Delta v_{o1,comp}}{\frac{v_{DC}}{M}} = \frac{1 - e^{-\frac{1}{2f_{sw}R_m(C_p+C_m)}}}{2}. \quad (42)$$

Since the cut-off frequency $f_{B1} = 1/2\pi R_m(C_p+C_m)$ of the PCVD is much lower than the switching frequency $f_{sw}$, the relative compensation error $v_{ep}^*$ is extremely small. According to the PCVD design parameters in Section III, the calculated relative compensation error $v_{ep}^*$ is merely 0.06%.

## V. EXPERIMENTAL VALIDATION

This section validates the performance of the designed measurement system and the proposed PSC method through experiments.

### A. Validation of PCVD Performance

Fig. 16 shows the prototype of the developed measurement system based on the parameters listed in Tables II and III. Its physical dimensions are merely 48 mm × 35 mm. To further highlight the high integration advantage of the developed measurement system, a size comparison is conducted between it and the differential probe designed in [15]. To ensure the fairness of the comparison, the scope of size comparison is confined to the voltage divider unit (including the additional size occupied by the proposed low-frequency compensation circuit). The sizes of other system units, such as buffers, differential circuits, and power supply circuits, are assumed to be identical and are not included in the comparison scope. Fig. 17 presents the comparison results of the sizes occupied by both on the

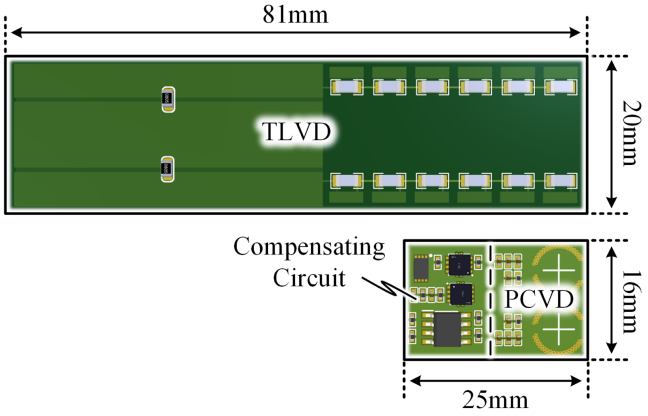


Fig. 17. 3D diagram of the dimensional comparison between the PCVD with the compensation circuit and the TLVD.

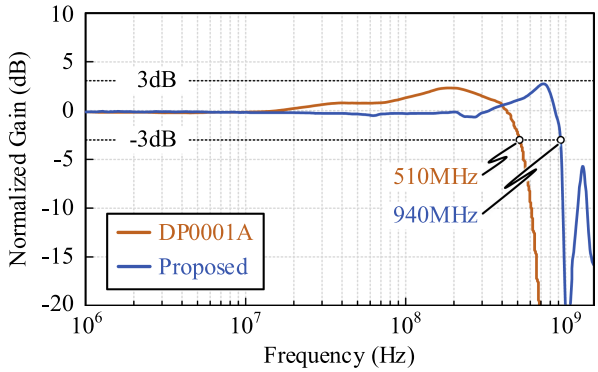


Fig. 18. Normalized frequency responses of the developed measurement system and Keysight DP0001A.

PCB from a 3D perspective. The total size of the PCVD and the compensation circuit in this design is reduced by 75% compared to that of the TLVD in the literature. The comparison results validate the advantage of the PCB-based planar capacitive voltage measurement system in terms of physical size. It should be noted that the total size of the PCVD and the compensation circuit on the PCB is larger than the theoretically calculated value in Part C of Section IV. This is mainly caused by two factors: First, the theoretical calculations did not account for the essential spacing between the components of the compensation circuit. Second, the components of both the compensation circuit and the PCVD require a clustered layout strategy to reduce the impact of parasitic parameters. This implies that there exists a relatively optimal placement relationship among the components, rather than random placement. Consequently, the size occupied on the PCB is greater than the theoretically calculated value.

For the frequency response of the measurement system in the high-frequency band (ranging from 1 MHz to 1.5 GHz), Fig. 18 presents the test results obtained by using the vector network analyzer (VNA) Keysight E5063A. The test data indicate that the developed system achieves an upper bandwidth limit of 940 MHz, outperforming the commercial probe Keysight DP0001A with a bandwidth of 510 MHz. In addition, the frequency response of the system exhibits a resonant peak at

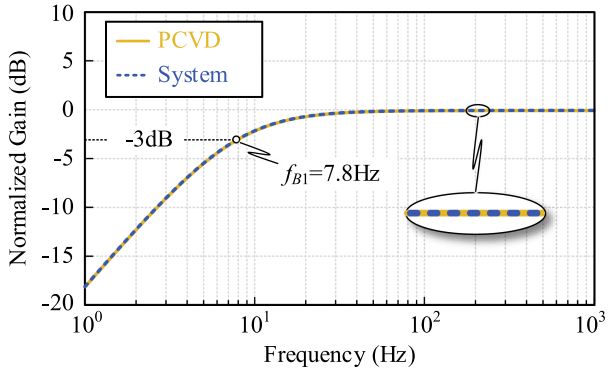


Fig. 19. Normalized frequency responses of the developed measurement system without low-frequency compensation and the PCVD in the low-frequency band, which are derived from calculations.

1 GHz. This frequency corresponds to the resonant point of the capacitor $C_m$, which is consistent with the aforementioned analysis results.

For the frequency response of the system in the low-frequency band (near the PCVD cut-off frequency $f_{B1}$), two aspects require special clarification: First, the proposed low-frequency compensation method is designed for the scenario of measuring the drain-source voltage of the device and is not applicable to all waveform types (e.g., sinusoidal waves). It essentially performs bias compensation on the distorted output voltage, without modifying the inherent gain droop characteristic of the PCVD in the low-frequency band. Second, since the minimum measurement frequency of the VNA E5063A is 100 kHz, the response in this low-frequency band cannot be directly measured. However, within the low-frequency band, both the closed-loop gain of the buffer and the differential circuit can remain stable at unity gain, and the parasitic parameters (resistor/capacitor parasitics, wiring inductance, component pin-to-ground capacitance) can be neglected. Thus, the low-frequency response of the measurement system is predominantly determined by the low-frequency characteristics of the PCVD and can be calculated through the transfer function $G_{PCVD}(s)$. Fig. 19 shows the frequency response curve of the developed measurement system in the low-frequency band without low-frequency compensation.

The CMRR is another crucial performance parameter of the differential measurement system. It is mainly constrained by two key factors: one is the symmetry of the two sets of input voltage dividers (i.e., PCVD) and the two buffers, while the other is the matching accuracy of the differential matching resistors in the differential amplifier circuit and the CMRR of the differential amplifier itself [22], [27]. Fig. 20 compares the CMRR of the developed measurement system with that of DP0001A. It can be seen that, limited by the CMRR of the used differential amplifier LMH6703 (blue dashed line), the CMRR of this system reaches only 40 dB in the low-frequency band. Moreover, near 20 MHz, it exhibits a $-20$ dB/decade attenuation trend along with the CMRR characteristics of LMH6703. This common-mode rejection ability has a relatively minor impact on measuring the drain-source voltage of the upper switch in the half-bridge circuit (i.e., where the magnitude of the differential voltage is

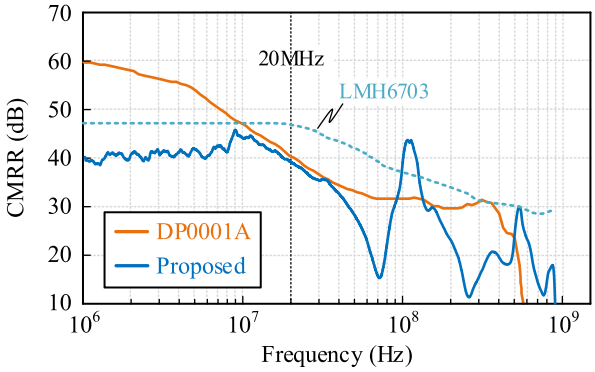


Fig. 20. CMRR of the developed measurement system and Keysight DP0001A.

comparable to that of the common-mode voltage). Nevertheless, for measuring the drive voltage of the upper switch (i.e., where the magnitude of the differential voltage is far smaller than that of the common-mode voltage), the impact is significant, and a differential amplifier with higher common-mode rejection capability needs to be replaced.

### B. Validation of PSC Method

To validate the proposed low-frequency distortion compensation method, a half-bridge SiC converter (Microchip MSCSM120HRM052NG) integrated with the measurement system was developed, as illustrated in Fig. 21. In the experiment, a 6-GHz bandwidth oscilloscope Keysight MXR608A with a sampling rate of 16-GSa/s was employed for signal acquisition to ensure the measurement accuracy. Under the operating conditions of a switching frequency of 100 kHz and a dc voltage of 800 V, the converter operates, respectively, with PWM, SPWM, THPWM, and SVPWM modulation strategies. The waveforms of the drain-source voltage of the upper switch $S_1$ measured by the developed system and the commercial probe DP0001A are presented in Figs. 22 –24. Specifically, the green waveforms denote the measurement results of the developed system, the blue waveforms represent those of DP0001A, and the dark red waveforms are the results obtained after low-pass filtering of the waveforms measured by DP0001A (i.e., low-frequency components in the drain-source voltage).

When no low-frequency distortion compensation is applied to the measurement system, the experimental results are presented in Fig. 22. Due to the insufficient gain of the PCVD in the low-frequency band, the output voltage waveforms of the system exhibit obvious distortion under four modulation strategies.

Following the implementation of low-frequency distortion compensation, the experimental results are illustrated in Figs. 23 and 24. In Fig. 23, the measurement waveforms of the compensated system and DP0001A are presented on the oscilloscope with an identical vertical scale and vertical offset. It can be observed that under all four modulation strategies, the measurement waveforms of both are basically coincident, thereby verifying the effectiveness of the PSC method. In Fig. 24, the vertical offsets of the two are set to different values (50 and −150 V, respectively) to improve the visibility of the measurement waveform of DP0001A (the bottom waveform).

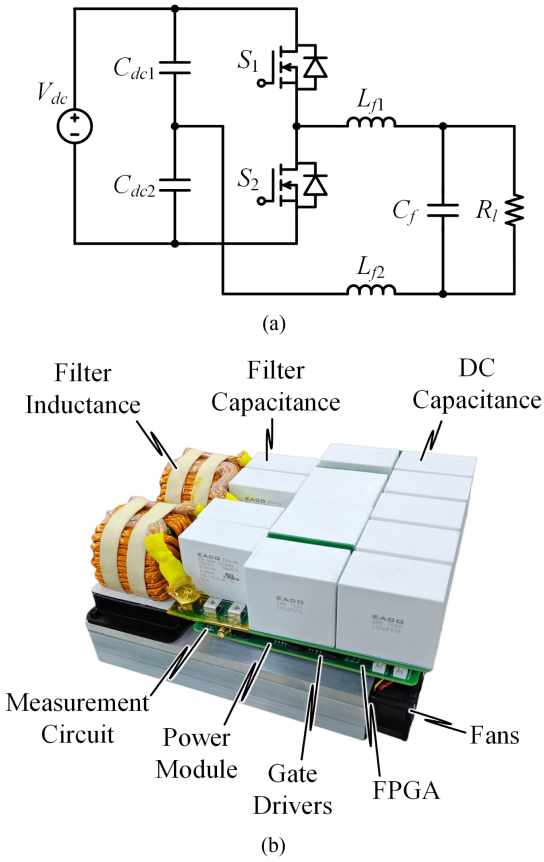


Fig. 21. (a) Half-bridge converter topology. (b) Picture of the half-bridge converter integrated with measurement systems.

### C. Comparison of Switching Transient Voltages and Verification of Measurement Errors

Fig. 25 (with the same vertical offset) and Fig. 26 (with different vertical offsets) comparatively show the waveforms of the transient voltages of the upper and lower switches ($S_1$ and $S_2$) simultaneously measured by the developed system and DP0001A (with a measurement error of 0.35%) at a switching frequency of 100 kHz. As observed in Fig. 25, the waveforms from both measurement devices basically overlap in the voltage transition edge part and the high-frequency ringing part. The maximum voltage deviation is 15 V, corresponding to a relative error of 1.87%. Fig. 27 shows the measurement results at a switching frequency of 20 kHz. The maximum voltage deviation is merely 13 V, corresponding to a relative error of 1.63%. These experimental results validate that the developed differential measurement system has the galvanically isolated capability and that the proposed multiobjective design optimization method is effective.

### D. Structural Optimization of PCVD

In addition to the two innovative contributions of the multiobjective design optimization method and the PSC method, the

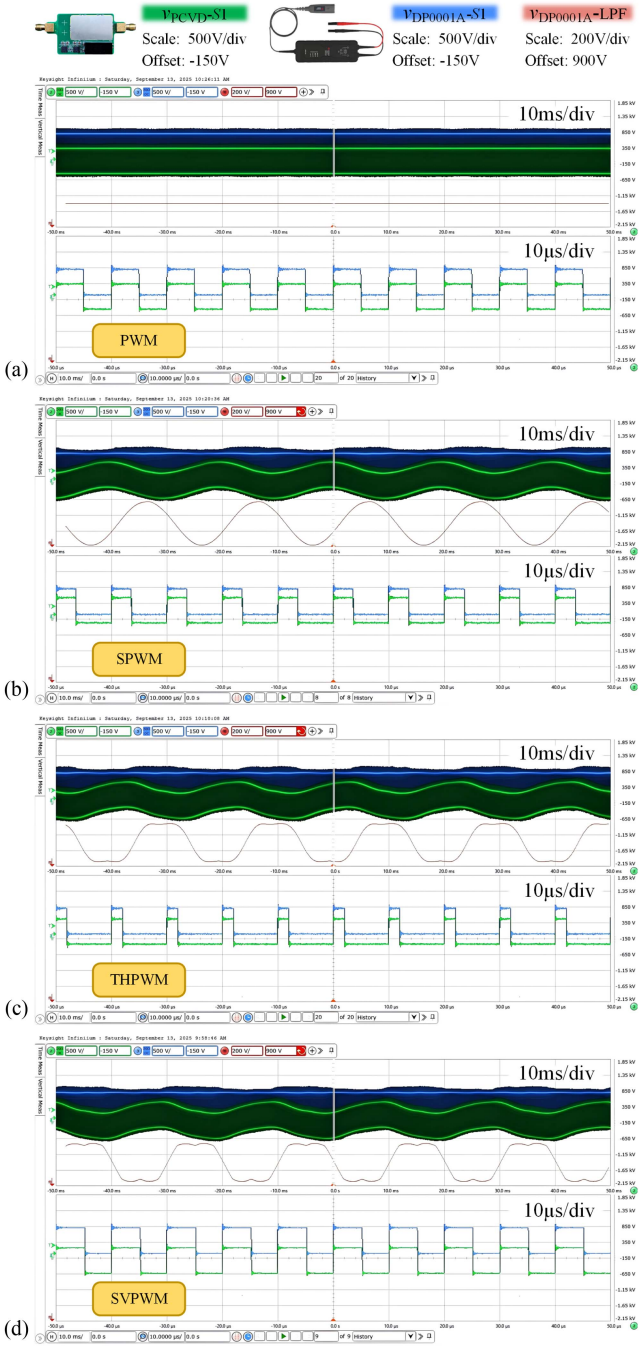


Fig. 22. Comparison of drain-source voltage waveforms of the upper switching device $S_1$ measured by the uncompensated measurement system (green) and DP0001A (blue) when the power converter operates under (a) PWM, (b) SPWM, (c) THPWM, and (d) SVPWM control strategies.

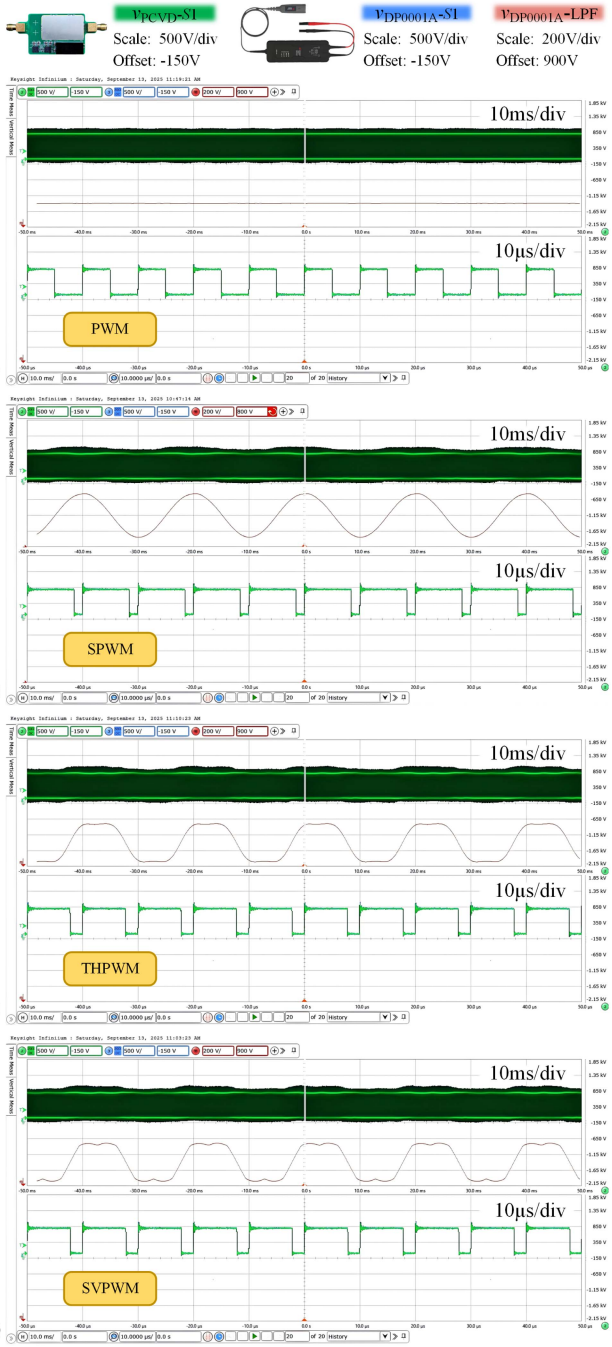


Fig. 23. Comparison of drain-source voltage waveforms of the upper switching device $S_1$ measured by the compensated measurement system (green) and DP0001A (blue) when the power converter operates under (a) PWM, (b) SPWM, (c) THPWM, and (d) SVPWM control strategies. Note that the vertical offsets of the waveforms are the same.

PCVD designed in this article has also been optimized at the hardware level compared with the reference scheme in [10].

*1) Topology Optimization:* In this article, a differential-structured PCVD is employed to substitute for the single-ended structure in the reference scheme, endowing the measurement system with the galvanically isolated capability, as shown in Fig. 1(b). This design is applicable to the simultaneous measurement of multiple signals with different reference potentials.

*2) Planar Capacitor Optimization:* Regarding the planar capacitor $C_p$, when the plate radius and the length of the leads are held constant, its parasitic inductance remains essentially unchanged. To enhance the self-resonant frequency of capacitor $C_p$, it is essential to minimize its capacitance. Simultaneously, since the capacitance of $C_m$ will decrease synchronously with the reduction of $C_p$, the self-resonant frequency of $C_m$ will correspondingly increase. This effectively broadens the upper

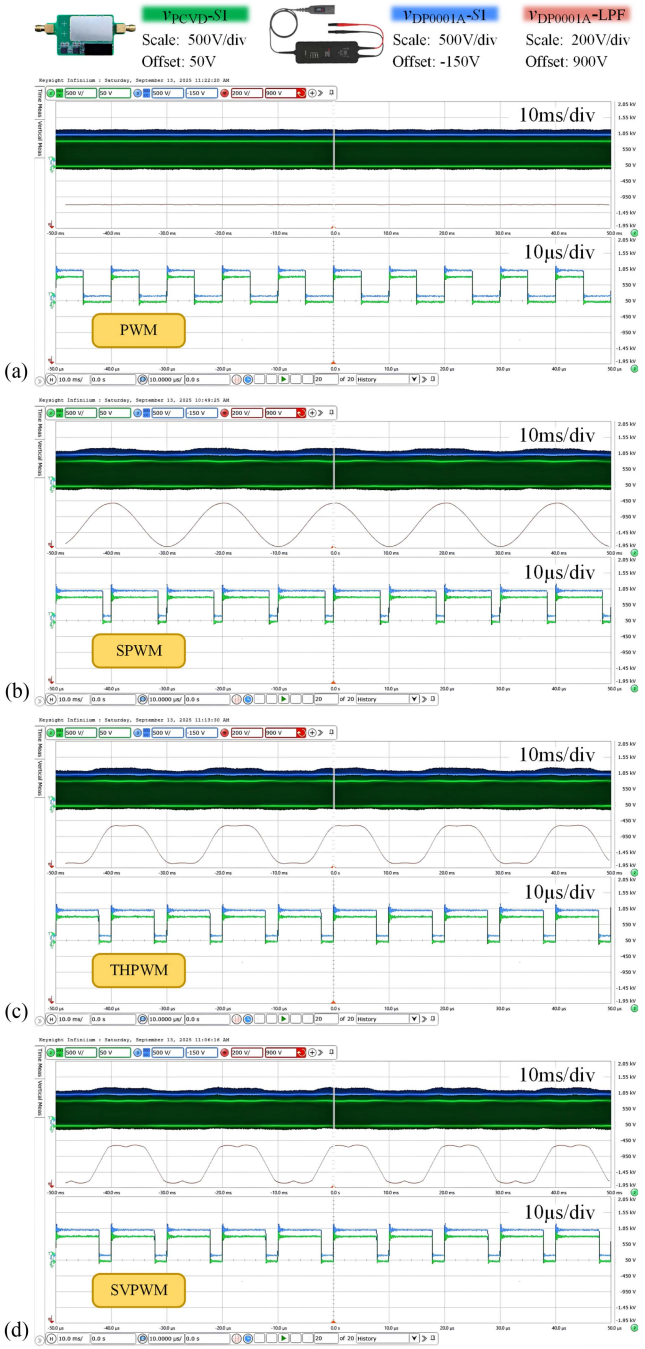


Fig. 24. Comparison of drain-source voltage waveforms of the upper switching device $S_1$ measured by the compensated measurement system (green) and DP0001A (blue) when the power converter operates under (a) PWM, (b) SPWM, (c) THPWM, and (d) SVPWM control strategies. Note that the vertical offsets of the waveforms are different.

limit of the bandwidth of the PCVD. As can be seen from (8), increasing the plate spacing $H$ is an effective approach to reducing the capacitance of $C_p$. In this article, a six-layer PCB with a thickness of 1.92 mm was utilized. The plates of the planar capacitor were, respectively, placed on the second and fifth layers (shielding layers were placed on the top and bottom layers). Meanwhile, the PCB lamination structure was optimized

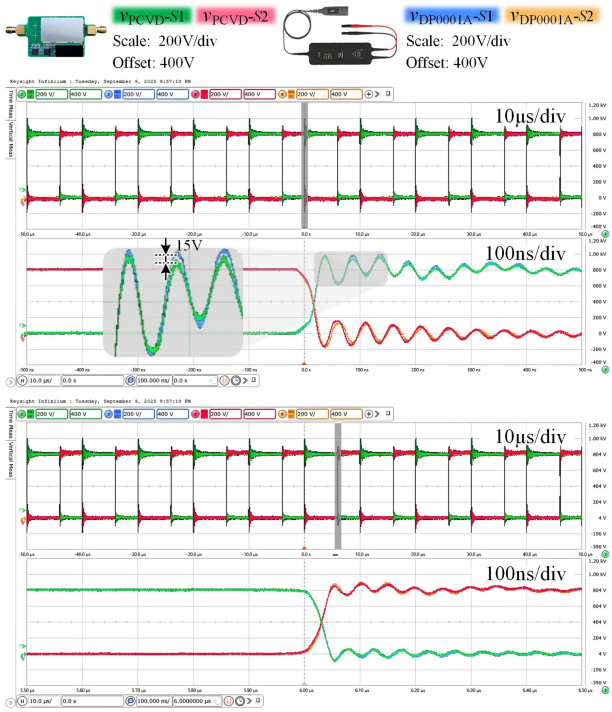


Fig. 25. Switching transient voltage waveforms measured by the compensated measurement system (green for $S_1$, pink for $S_2$) and DP0001A (blue for $S_1$, yellow for $S_2$) at a switching frequency of 100 kHz. (a) $S_1$ is turned OFF, and $S_2$ is turned ON. (b) $S_1$ is turned ON, and $S_2$ is turned OFF. Note that the vertical offsets of the waveforms are the same.

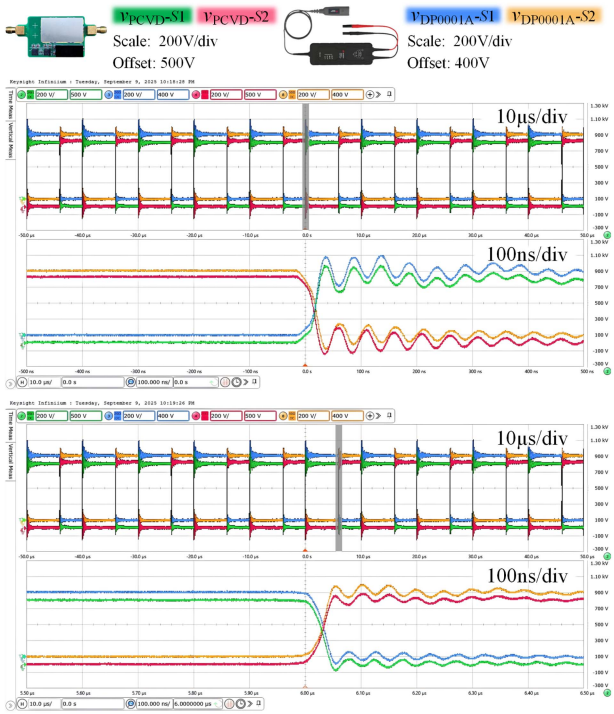


Fig. 26. Switching transient voltage waveforms measured by the compensated measurement system (green for $S_1$, pink for $S_2$) and DP0001A (blue for $S_1$, yellow for $S_2$) at a switching frequency of 100 kHz. (a) $S_1$ is turned OFF, and $S_2$ is turned ON. (b) $S_1$ is turned ON, and $S_2$ is turned OFF. Note that the vertical offsets of the waveforms are different.

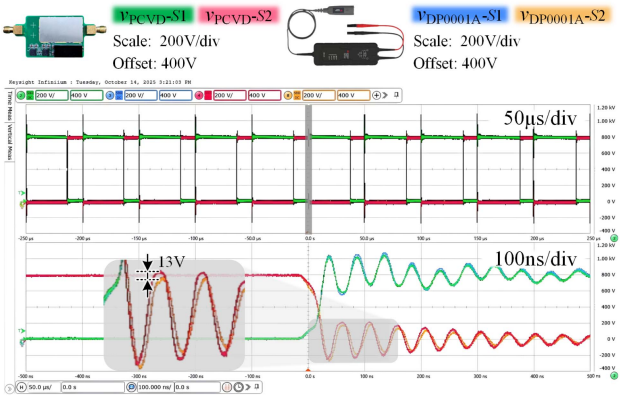


Fig. 27. Switching transient voltage waveforms measured by the compensated measurement system (green for $S_1$, pink for $S_2$) and DP0001A (blue for $S_1$, yellow for $S_2$) at a switching frequency of 20 kHz. Note that the vertical offsets of the waveforms are the same.

to maximize the distance between the second layer and fifth layer ($H = 1.36$ mm) on the premise that the interlayer insulation performance meets measurement requirements. Based on this, with the same plate radius, the capacitance of the planar capacitor designed in this article is 0.316 pF, which is smaller than 0.456 pF designed in the reference scheme.

*3) Layout Optimization:* In the reference scheme, the planar capacitor $C_p$ is connected to the impedance unit $Z_m$ via a transmission line with a length of 20 cm. This transmission line introduces relatively large parasitic inductance into the circuit. As a result, the resonant frequency formed by it and the planar capacitor is decreased, thereby limiting the upper bandwidth of the system. In this article, both the impedance unit $Z_m$ and the planar capacitor $C_p$ are integrated onto the same PCB, and a short and wide trace (length 2 mm, width 0.762 mm) is employed to connect them. This not only reduces the parasitic inductance but also enhances the compactness of the PCVD. The improvement in performance has been validated through experimental results. In the reference scheme, the frequency response of the measurement system presents the first resonant peak at around 350 MHz, restricting the system bandwidth to merely 206 MHz. In contrast, the frequency response of the measurement system developed in this article presents the first resonant peak at around 1 GHz, and the system bandwidth reaches 940 MHz, as presented in Fig. 18.

## VI. Conclusion

This article addresses the dual challenges existing in the PCB-based planar capacitive voltage measurement system: the difficulty in synergistically optimizing the integration level and measurement accuracy, as well as the insufficient gain in the low-frequency range. A multiobjective optimization method and a PSC method are proposed. First, the physical size model and measurement error models of the PCVD are established to derive the Pareto front for multiobjective optimization. Then, a Pareto optimal solution (relative measurement error $v^*_{error}(r) = 1.16\%$, physical size $S_{PCVD}(r) = 108$ mm$^2$) is selected to guide the PCVD parameter design. Second, based on the quantitative analysis of output voltage distortion characteristics in the time domain, the PSC method is proposed. This method can reduce the low-frequency distortion of the voltage to 0.06%. The experimental results demonstrate that the developed measurement system achieves an upper bandwidth limit of 940 MHz and compact dimensions of 48 mm $\times$ 35 mm. Moreover, the compensated output voltage waveform shows a 1.87% deviation from reference probe measurements. These results confirm the effectiveness of the multiobjective design optimization method and the PSC method.

## References

[1] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless PV inverter with GaN AC switches," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7474–7488, Aug. 2019, doi: 10.1109/TPEL.2018.2878586.

[2] D. Cittanti, E. Vico, and I. R. Bojoi, "New FOM-based performance evaluation of 600/650 V SiC and GaN semiconductors for next-generation EV drives," *IEEE Access*, vol. 10, pp. 51693–51707, 2022, doi: 10.1109/ACCESS.2022.3174777.

[3] D. Wang et al., "Multilevel inverters for electric aircraft applications: Current status and future trends," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 2, pp. 3258–3282, Jun. 2024, doi: 10.1109/TTE.2023.3296284.

[4] P. Nayak and K. Hatua, "Active gate driving technique for a 1200 V SiC MOSFET to minimize detrimental effects of parasitic inductance in the converter layout," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1622–1633, Mar./Apr. 2018, doi: 10.1109/TIA.2017.2780175.

[5] H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder, and M. Zefran, "Closed-loop control of switching transition of SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 782–788.

[6] M. Du, F. Liu, J. Yin, C. Dong, and Z. Ouyang, "Junction temperature correction method for SiC MOSFET based on turn-off oscillation frequency of drain-source voltage," *IEEE Trans. Electron Devices*, vol. 71, no. 10, pp. 6208–6215, Oct. 2024, doi: 10.1109/TED.2024.3438673.

[7] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, "Condition monitoring: A decade of proposed techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 4, pp. 22–36, Dec. 2015, doi: 10.1109/MIE.2015.2481564.

[8] P. Sun et al., "Focuses and concerns of dynamic test for wide bandgap device: A questionnaire-based survey," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15522–15534, Dec. 2023, doi: 10.1109/TPEL.2023.3312563.

[9] D. Garrido, I. Baraia-Etxaburu, J. Arza, and M. Barrenetxea, "Simple and affordable method for fast transient measurements of SiC devices," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2933–2942, Mar. 2020, doi: 10.1109/TPEL.2019.2924358.

[10] Z. Xin, X. Liu, X. Li, and J. Kang, "An electric field probe with high immunity for SiC MOSFET switching voltage measurement," *IEEE Sensors J.*, vol. 23, no. 7, pp. 7008–7016, Apr. 2023, doi: 10.1109/JSEN.2023.3248874.

[11] P. S. Niklaus, R. Bonetti, C. Stäger, J. W. Kolar, and D. Bortis, "High-bandwidth isolated voltage measurements with very high common mode rejection ratio for WBG power converters," *IEEE Open J. Power Electron.*, vol. 3, pp. 651–664, 2022, doi: 10.1109/OJPEL.2022.3208693.

[12] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "A digital isolated high voltage probe for measurements in power electronics," in *Proc. IEEE 27th Int. Symp. Ind. Electron.*, 2018, pp. 791–796.

[13] Y. Lobsiger, G. Ortiz, D. Bortis, and J. W. Kolar, "Concept and experimental evaluation of a novel DC-100MHz wireless oscilloscope," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 1309–1316.

[14] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "Development of a differential voltage probe for measurements in automotive electric drives," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2335–2343, Mar. 2017, doi: 10.1109/TIE.2016.2626374.

[15] Y. Wang et al., "High-bandwidth differential voltage probe for accurate switching characterization of WBG devices," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 12545–12557, Oct. 2024, doi: 10.1109/TPEL.2024.3401011.

[16] C. Yang et al., "A low-cost high-performance voltage sensing circuit with proactive parameter design compensation network for SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 11532–11543, Nov. 2021, doi: 10.1109/TIE.2020.3034864.

[17] Y. Wang, Z. Zeng, T. Long, P. Sun, L. Wang, and M. Zou, "Impedance-matching shunt: Current sensor with ultrahigh bandwidth and extremely low parasitics for wide-bandgap device," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11528–11533, Oct. 2022, doi: 10.1109/TPEL.2022.3175973.
[18] H. Nishiyama and M. Nakamura, "Capacitance of disk capacitors," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 16, no. 3, pp. 360–366, May 1993, doi: 10.1109/33.232065.
[19] T. Instruments, "OPA859 1.8 GHz unity-gain bandwidth, 3.3 nV/√Hz, FET input amplifier," 2018. [Online]. Available: https://www.ti.com/product/OPA859
[20] M. Buffolo et al., "Review and outlook on GaN and SiC power devices: Industrial state-of-the-art, applications, and perspectives," *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1344–1355, Mar. 2024, doi: 10.1109/TED.2023.3346369.
[21] J. Zou, Q. Li, S. Yang, H. Bai, and J. Zheng, "A prediction strategy based on center points and knee points for evolutionary dynamic multi-objective optimization," *Appl. Soft Comput.*, vol. 61, pp. 806–818, Dec. 2017, doi: 10.1016/j.asoc.2017.08.004.
[22] P. S. Niklaus, D. Bortis, and J. W. Kolar, "Next generation measurement systems with high common-mode rejection," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, 2018, pp. 1–8.
[23] T. D. Kagaku, "CGA2B2C0G1H390J050BA characteristic table," 2016. [Online]. Available: https://product.tdk.cn/system/files/dam/doc/product/capacitor/ceramic/mlcc/charasheet/cga2b2c0g1h390j050ba.pdf
[24] D. G. Holmes and A. L. Thomas, "Modulation of one inverter phase leg," in *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003, pp. 95–153.
[25] Z. Keliang and W. Danwei, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis [three-phase inverters]," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002, doi: 10.1109/41.982262.
[26] Y. Wei, Q. Xu, J. Hu, B. Xu, H. Wei, and G. Liu, "A hard-switching loss calculation method for SiC MOSFETs without current sensors," in *Proc. CPSS IEEE Int. Symp. Energy Storage Convers.*, 2024, pp. 1004–1010.
[27] R. Pallas-Areny and J. G. Webster, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 4, pp. 669–676, Aug. 1991, doi: 10.1109/19.85332.

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