Class Φ Resonant Gate Driver With Waveform Shaping for SiC-Based VHF Power Conversion

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***Abstract*—Driving Silicon Carbide (SiC) MOSFETs at high frequencies presents significant challenges due to their high input gate capacitance and required voltage swing. In this article, we propose a design method for a Class Φ resonant gate driver topology, implemented on an SiC device in a 6.78-MHz Class E inverter power stage. The topology is modeled using state-space analysis for performance optimization and gate voltage profile shaping. Experimental results demonstrate significant advantages compared to conventional hard-switched half-bridge gate drivers, including lower gate driver power consumption and higher power device drain efficiency. Further optimization of the magnetic components of the gate driver resulted in a further reduction both in size and power consumption, achieving an 8.6-fold reduction in gate driving power compared to the conventional half-bridge gate driver. In addition, the experimental setup shows improved efficiency of the power stage, which correlates to a 8.8-W (25.9%) reduction in loss in the power device when driven by the resonant gate driver.**

***Index Terms*—Resonant gate driver (RGD), silicon carbide (SiC), soft switching.**

I. Introduction

RESONANT power converter topologies enable efficient high-power operation at high switching frequencies (≥1 MHz) [1] resulting in higher gravimetric and volumetric power density [2]. In addition, recent advances in wide band-gap (WBG) devices, such as gallium nitride and silicon carbide (SiC), have further enabled the improvement of the performance metrics of these converters [3]. Good gate driver performance in such demanding conditions is essential for minimizing the switching and conduction losses of power transistors. However, driving the gate of these devices becomes a challenging task as the input capacitance of the power device, C_{iss}, has to be charged and discharged in short time intervals to ensure that the device turn-ON and turn-OFF transients are not significant portions of a switching period [4].

The most conventionally used gate driver topology is the half-bridge or Class D gate driver, which is popular because of its simplicity [5] but with the drawbacks of hard-switching and high-side driving [1]. A candidate high-frequency alternative is a Class E-type gate driver topology, but this has the drawback of complex tuning, low bandwidth, and limited duty cycle control. In this article, we propose a Class Φ resonant gate driver (RGD) solution, which removes some of the deficiencies with the Class E approach to enable efficient high frequency driving. The Class Φ circuit, although more complicated than the basic Class E, offers more optimal gate voltage shaping properties and more degrees of freedom for tuning [6]. Also, the Class E-type gate drivers offer the advantage of only using a single low-side transistor, reduced switching losses, and soft waveform transitions. Table I summarizes the key differences between a hard-switched (HSW), half-bridge topology and the one we propose.

TABLE I
Comparison of Gate Driver Topologies

Attributes	Proposed Class Φ gate drivers	Conventional gate drivers
Num. of devices	1	2
Num. of passives	4	0
High-side driving	No	Yes
Waveshape control	Yes	No
Variable duty cycle	Limited	Flexible
Bandwidth	Limited	High
Input voltage	Low	High
Num. of supplies	1	2
Power efficiency	Very high	Low
Design	Complicated	Straightforward

Fundamental work on the design of a gate driver using the Class Φ topology is described in [7], [8], and [9], which have been enhanced in this work. The analyses presented in these work use a first order approximation in the mathematical formulation of the circuit behavior. As established in [10], first order analysis generally results in poor accuracy in Class Φ converters especially due to the current through ϕ-branch consisting of multiple harmonics. Furthermore, this work extends the design of the gate driver to be more generalized by formulating a solution for any duty cycle rather than a fixed 0.5 as done in [7].

We briefly compare the work done on RGD in the literature to what we present in this article. The attributes compared between the various works are the switching frequency, the number of devices (both switches and diodes) and passives in the topology (which correlate to complexity of the topology), the gate driving

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TABLE II
LITERATURE REVIEW OF RGD

Refs.	f_S (MHz)	No. of devices	No. of passives	Power loss reduction (%)	Power level (W)	Power device FoM (10^{-3})
[13]	0.36	4	2	90.3	1000	56.7
[14]	0.5	4	1	45	-	40
[15]	0.5	4	3	76	960	24.8
[16]	1	4	1	24.8	50	45
[17]	1	5	2	10.1	56	3
[18]	1	5	2	64.8	50	5.05
This work	**6.78**	**1**	**4**	**88.3**	**≈10000**	**77.2***
[19]	13.56	3	1	-	4.7	32.5
[20]	13.56	4	1	60	78	127*
[21]	12–15	3	3	82.4	1200	144*
[22]	20	2	3	60	32	78.6

loss reduction found compared to conventional gate drivers, and the power level of the power stage as well as an additional figure of merit (FoM) representing the load for the gate driver. This FoM is defined as

$$\text{FoM} = C_{iss} \cdot V_{GS} \cdot f_S = Q_g \cdot f_S \tag{1}$$

where C_{iss} is the input gate capacitance, V_{GS} is the peak gate voltage required, and f_S is the driving frequency. A higher FoM refers to a harder to drive load for the gate driver. This can be simplified by incorporating the gate charge, Q_g, as it is the product of C_{iss} and V_{GS}. The collation of data is shown in Table II and has been based upon the review done in [11] as well as other relevant work. The metrics achieved in this work (shown in bold) are compared with those in the literature, with the best performance for each metric highlighted in green. The FoMs noted with an asterisk (∗) show cases where the power device is SiC. SiC devices tend to have high internal gate resistance [12] (3.5 Ω for the device chosen in this article), which increases the challenges in gate driving beyond the FoM used here.

This article first uses state-space representation combined with complete analytic expressions to obtain solutions for any duty cycle for a simplified lumped gate element of C_{iss}. The circuit component values derived from the above tuning stage are then used as the starting point for further optimization of the gate driver on a modified topology. This tuning stage achieves higher robustness to variable C_{iss} (Miller effect and device-to-device variations) and gate parasitics, such as internal gate resistance, R_g, and gate inductance due to packaging, L_g. The design is then experimentally validated on a single ended 6.78 MHz Class E inverter power stage designed for a power output of 10 kW (assuming a 50 Ω ac load), where the performance of the gate driving circuit and power device losses are compared to a commercially available high-speed half-bridge gate driver. Finally, we discuss these results and comment on possible future work.

II. ANALYSIS OF SIMPLIFIED CIRCUIT MODEL

A. Gate Driver Topology

The circuit diagram of a Class Φ gate driver is shown in Fig. 1, where V_{dd} is the input dc voltage source, S is the switching

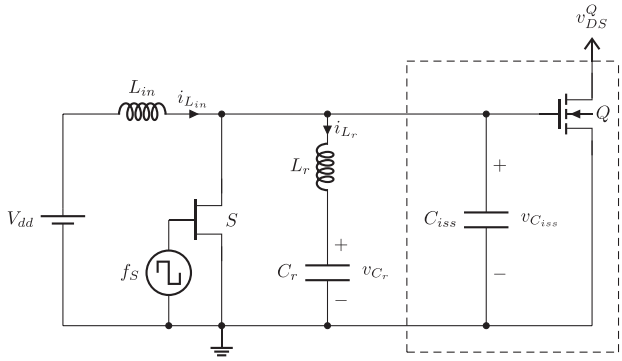

Fig. 1. Circuit diagram of the proposed Class Φ gate driver supplied by V_{dd} driving the gate of the main power device Q. The overall input capacitance of Q is modeled as C_{iss}, which represents the capacitive load of the gate driver.

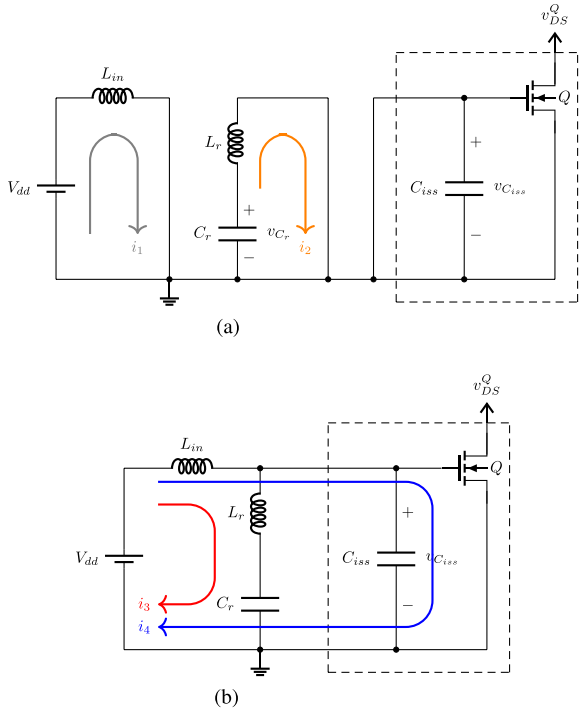

Fig. 2. Equivalent circuit states when switch S is turned ON (top) or turned OFF (bottom), which shows the Class E operation of the circuit. The voltage $v_{C_{iss}}$ is the gate voltage of the power device Q. In the case where S is switched ON, $v_{C_{iss}} = 0$ V. (a) S switched ON. (b) S switched OFF.

device of the gate driver circuit, L_{in} is the input choke, L_r and C_r form a resonant branch in parallel with S, and C_{iss} is the gate capacitance of the power device (Q), which is the load of the gate driver. The difference between the Class Φ inverter in [10] and the Class Φ gate driver topology is that the load network of the inverter is removed in the gate driver circuit and replaced with power device input capacitance, C_{iss}. The frequency of the input signal of the gate driver f_S is the same as the switching frequency of the power device (Q), and the duty cycle of S is the complementary of that of Q.

Fig. 2 shows the equivalent circuits during each switching period, when S is switched ON and switched OFF. When S is switched ON, $i_1 = i_{L_{\text{in}}}$ (given by a linear ramp as the inductor

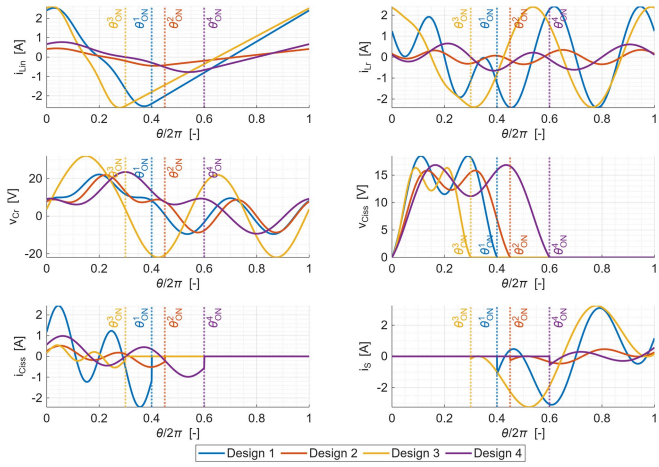

Fig. 3. Indicative waveforms of the voltages and currents of the passives in the circuit showing the mode of operation of the gate driver. These are results for various designs derived from the analytical solution for the gate driver for the topology in Fig. 1. The input parameters for these designs are given in Table III.

TABLE III
PARAMETERS FOR VARIOUS GATE DRIVER DESIGNS

Input Parameters	Design 1	Design 2	Design 3	Design 4	Units
f_S	6.78	3	1	13.56	MHz
D_Q	0.4	0.45	0.3	0.6	-
C_{iss}	1.5	1	2	0.5	nF
V_{dd}	5	5	3.3	7	V
Output Parameters					
L_{in}	91.9	1098	458.3	154.4	nH
L_r	30.5	401.7	659.1	77.02	nH
C_r	1.94	0.62	7.8	0.322	nF

has a constant voltage across it) and $i_2 = -i_{L_r}$, which is a sinusoid at the resonant frequency of L_rC_r. The capacitor C_{iss} is discharged completely and there is no voltage across it and hence the gate of the power device, Q. When S is switched OFF, there is a more complicated network of passives. The current $i_3 = i_{L_r}$ and $i_4 = i_{L_{in}} - i_{L_r}$. The current through C_{iss}, i_4, shapes the voltage across it and hence the gate voltage profile. The following subsections describe the methodology for obtaining the analytical solution for the circuit. Fig. 3 shows indicative waveforms for the gate driver topology, as shown in Fig. 1. The waveforms shown are for four different designs with the parameters, as shown in Table III. The circuit values for these waveforms are derived through an analytical method that will be detailed in this section and shows that our method can be used to design a Class Φ RGD for various power device input capacitance with differing duty cycle, switching frequency, input voltage, etc. The switching angle of the switching device of the gate driver (S) is shown by the dotted line in Fig. 3, highlighting that zero-voltage Switching (ZVS) has been achieved in all cases.

The circuit analysis of Fig. 1 is carried out by assuming that S is an ideal switch, i.e., $i_S = 0$ during $\theta^+_{\text{OFF}} \leq \theta \leq \theta^-_{\text{ON}}$ and $v_{C_{iss}} = 0$ when $\theta^+_{\text{ON}} \leq \theta \leq \theta^-_{\text{OFF}}$. This condition also means that the discharge of C_{iss} is instantaneous, so there is zero current through the shunt capacitor during turn-ON. We must clarify that in this section, switching timings refer to the switching device of the gate driver S and not the power transistor Q, unless explicitly stated otherwise. Consequently, to this convention, $\theta^+_{\text{OFF}} = 0$, $\theta^-_{\text{OFF}} = 2\pi$, and $\theta_{\text{ON}} = 2\pi D_Q$, where D_Q is the duty cycle of Q. In addition, the input capacitance of the power device Q, which is dependent on v^Q_{DS}, is assumed to be constant.

B. State Equations During Turn-On

Applying Kirchhoff's voltage law (KVL) to the input branch during turn-ON results in the differential equation

$$\omega L_{\text{in}} \frac{\mathrm{d}i^{\text{ON}}_{L_{\text{in}}}(\theta)}{\mathrm{d}\theta} = V_{dd} \tag{2}$$

where ω is $2\pi f_S$, where f_S is the switching frequency. The normalized solution is

$$\frac{i^{\text{ON}}_{L_{\text{in}}}(\theta)}{\lambda} = \theta + A_1 \tag{3}$$

where A_1 is boundary-dependent constant and

$$\lambda = \frac{V_{dd}}{\omega L_{\text{in}}}. \tag{4}$$

Combining KVL and Kirchhoff's current law (KCL) in ϕ-branch during turn-ON produces ϕ-branch inductor current state equation

$$-\omega^2 L_r C_r \frac{\mathrm{d}^2 i^{\text{ON}}_{L_r}(\theta)}{\mathrm{d}\theta^2} = i^{\text{ON}}_{L_r}(\theta) \tag{5}$$

whose normalized solution is given by the relation

$$\frac{i^{\text{ON}}_{L_r}(\theta)}{\lambda} = A_2 \cos(\tau_r\theta) + A_3 \sin(\tau_r\theta) \tag{6}$$

where $A_{2,3}$ are boundary parameters and

$$\tau_r = \frac{1}{\omega\sqrt{L_rC_r}}. \tag{7}$$

Applying (6) to

$$v^{\text{ON}}_{C_r}(\theta) = -\omega L_r \frac{\mathrm{d}i^{\text{ON}}_{L_r}(\theta)}{\mathrm{d}\theta} \tag{8}$$

gives

$$\frac{v^{\text{ON}}_{C_r}(\theta)}{V_{dd}} = -k^2 \left(\frac{n}{\tau_r}\right)^2 \frac{\mathrm{d}}{\mathrm{d}\theta} \frac{i^{\text{ON}}_{L_r}(\theta)}{\lambda} \tag{9}$$

where

$$k = \frac{C_{iss}}{C_r} \tag{10}$$

$$n = \frac{1}{\omega\sqrt{L_{\text{in}}C_{iss}}} \tag{11}$$

$$\frac{\mathrm{d}}{\mathrm{d}\theta} \frac{i^{\text{ON}}_{l_r}(\theta)}{\lambda} = \tau_r \left[A_3 \cos(\tau_r\theta) - A_2 \sin(\tau_r\theta)\right]. \tag{12}$$

C. State Equations During Turn-Off

Solving the circuit, as shown in Fig. 1, using KVL and KCL so that ϕ-branch inductor current is the only independent state

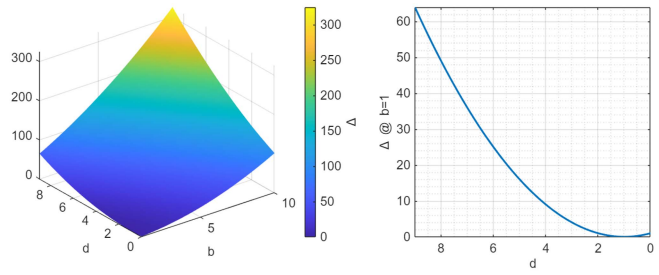

Fig. 4. Surface plot of (18) (left) and line curve of (18) at $b = 1$ (right).

variable during turn-OFF produces the following fourth-order differential equation

$$V_{dd} = \omega^3 L_{\text{in}} C_{iss} L_r \frac{\mathrm{d}^3 i_{l_r}^{\text{OFF}}(\theta)}{\mathrm{d}\theta^3} + \omega\left(L_{\text{in}} + L_r + \frac{L_{\text{in}} C_{iss}}{C_r}\right)\frac{\mathrm{d} i_{l_r}^{\text{OFF}}(\theta)}{\mathrm{d}\theta} + \frac{1}{\omega C_r}\int_{\theta_{\text{OFF}}}^{\theta} i_{L_r}^{\text{OFF}}(\theta)\,\mathrm{d}\theta + v_{C_r}(\theta_{\text{OFF}}). \tag{13}$$

The Laplace transformation of i_{L_r} from (13) is a rational function whose denominator is a fourth-degree polynomial

$$D(s) = as^4 + (b + ac)s^2 + c \tag{14}$$

where

$$a = L_{\text{in}} C_{iss} \tag{15}$$

$$b = \frac{L_{\text{in}}}{L_r} + 1 \tag{16}$$

$$c = \frac{1}{L_r C_r}. \tag{17}$$

The discriminant of (14) with respect to s^2 is

$$\Delta_{s^2} = (b + d)^2 - 4d \tag{18}$$

where

$$d = ac. \tag{19}$$

By definition, $b > 1$ from (16) and $d > 0$ from (19), since the inductances and capacitances are always positive. As a result, (18) is always positive, with its minimum limit at $b = 1$, as shown in Fig. 4. Consequently, (14) has four purely imaginary roots, and thus, the analytic expression of the inverse Laplace transform of (13) is

$$\frac{i_{L_r}^{\text{OFF}}(\theta)}{\lambda} = \sum_{i=1}^{2}\left[\left(A_4 + \frac{A_5}{\tau_i^2}\right)\cos(\tau_i\theta) + \frac{1}{\tau_i}\left(\frac{A_6}{\tau_i} + A_7\right)\sin(\tau_i\theta)\right] \tag{20}$$

where $A_{4,5,6,7}$ are again boundary-dependent parameters and

$$\tau_1 = \left\{\frac{1}{2}\left[\tau_r^2\left(\frac{1}{k} + 1\right) + n^2\right] - \sqrt{\frac{1}{4}\left[\tau_r^2\left(\frac{1}{k} + 1\right) + n^2\right]^2 - (n\tau_r)^2}\right\}^{\frac{1}{2}} \tag{21}$$

$$\tau_2 = \frac{n\tau_r}{\tau_1}. \tag{22}$$

The rest of the normalized state variables equations can be directly derived from (20) and are given as follows:

$$\frac{i_{L_{\text{in}}}^{\text{OFF}}(\theta)}{\lambda} = (1 + k)\frac{i_{L_r}^{\text{OFF}}(\theta)}{\lambda} + \frac{k}{\tau_r^2}\frac{\mathrm{d}^2}{\mathrm{d}\theta^2}\frac{i_{L_r}^{\text{OFF}}(\theta)}{\lambda} \tag{23}$$

$$\frac{v_{C_r}^{\text{OFF}}(\theta)}{V_{dd}} = 1 - \frac{k}{\tau_r^2}\frac{\mathrm{d}^3}{\mathrm{d}\theta^3}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} - \left[1 + k\left(1 + \frac{n^2}{\tau_r^2}\right)\right]\frac{\mathrm{d}}{\mathrm{d}\theta}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} \tag{24}$$

$$\frac{v_{C_{iss}}^{\text{OFF}}(\theta)}{V_{dd}} = 1 - (1 + k)\frac{\mathrm{d}}{\mathrm{d}\theta}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} - \frac{k}{\tau_r^2}\frac{\mathrm{d}^3}{\mathrm{d}\theta^3}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} \tag{25}$$

where

$$\frac{\mathrm{d}}{\mathrm{d}\theta}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} = \sum_{i=1}^{2}\left[\left(\frac{A_6}{\tau_i^2} + A_7\right)\cos(\tau_i\theta) - \left(\tau_i A_4 + \frac{A_5}{\tau_i}\right)\sin(\tau_i\theta)\right] \tag{26}$$

$$\frac{\mathrm{d}^2}{\mathrm{d}\theta^2}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} = -\sum_{i=1}^{2}\left[\left(\tau_i^2 A_4 + A_5\right)\cos(\tau_i\theta) + \left(\frac{A_6}{\tau_i} + \tau_i A_7\right)\sin(\tau_i\theta)\right] \tag{27}$$

$$\frac{\mathrm{d}^3}{\mathrm{d}\theta^3}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda} = \sum_{i=1}^{2}\left[\tau_i\left(\tau_i^2 A_4 + A_5\right)\sin(\tau_i\theta) - \left(A_6 + \tau_i^2 A_7\right)\cos(\tau_i\theta)\right]. \tag{28}$$

D. Solving Boundary Conditions

After deriving the exact analytic expressions of the state variables of the RGD, as shown in Fig. 1, during the two states of the transistor, we need to set the boundary continuation conditions for calculating the parameters $A_{1,2,\ldots,7}$. These conditions rise from the fact that there cannot be abrupt changes and discontinuities in inductor currents and capacitor voltages during the transitions of the transistor conduction states. The only exception to this rule is the voltage across the input capacitance of the power device Q, which acts as a shunt capacitor to S. Since the transistor is modeled as an ideal short during turn-ON, it can theoretically support infinite discharge current, which corresponds to a discontinuity in the voltage of C_{iss}, unless ZVS conditions are applied.

Setting the boundary continuation conditions of the state signals at turn-OFF and turn-ON produces the following linear system of equation where $c_r^{\text{OFF}} = \cos(\tau_r\theta_{\text{OFF}}^-)$, $s_r^{\text{OFF}} = \sin(\tau_r\theta_{\text{OFF}}^-)$,

$c_r^{\text{ON}} = \cos(\tau_r\theta_{\text{ON}})$, $s_r^{\text{ON}} = \sin(\tau_r\theta_{\text{ON}})$, $c_i^{\text{ON}} = \cos(\tau_i\theta_{\text{ON}})$, and $s_i^{\text{ON}} = \sin(\tau_i\theta_{\text{ON}})$:

$$\mathbf{a} = \mathbf{B}^{-1}\mathbf{c} \tag{29}$$

where (31), shown at the bottom of this page.

$$\mathbf{a} = \begin{bmatrix} A_1 & A_2 & A_3 & A_4 & A_5 & A_6 & A_7 \end{bmatrix}^T \tag{30}$$

$$\mathbf{c} = \begin{bmatrix} \theta_{\text{OFF}}^- & 1 & 0 & 1 & \theta_{\text{ON}} & 0 & 1 \end{bmatrix}^T. \tag{32}$$

E. Solving the Differential Equations

In order to create a design process, we first map all the parameters of the state equations to the inputs and constraint conditions of our method. Then, the component values of Fig. 1 can be directly computed by the state equation parameters. The successful application of the design method relies heavily on the careful mathematical formulation of this inverse problem.

The main design parameters used as inputs to our tuning algorithm of the Class Φ gate driver are dictated by the requirements of the power stage circuit, namely, the switching frequency, f_S, the duty cycle of Q, D_Q, and the input capacitance of Q, C_{iss}. The duty cycle of the gate driver is related to the duty cycle of the power transistor through the relation

$$D_S = 1 - D_Q. \tag{33}$$

Furthermore, we decide to use the supply voltage V_{dd} as a design input of choice, since it may be convenient to set it to a value that already exists on the printed circuit board (PCB), and thus minimize the number of different power supplies needed.

The switching frequency sets the value of ω and the duty cycle sets the turn-ON angle. The supply voltage sets the power level, and turns all the normalized state equations to their absolute

$$\mathbf{B} = \begin{bmatrix} -1 & 0 & 0 & 2+2k-\frac{k}{\tau_r^2}\sum_{i=1}^{2}\tau_i^2 \\ 0 & 0 & 0 & 0 \\ 0 & c_r^{\text{OFF}} & s_r^{\text{OFF}} & -2 \\ 0 & \frac{kn^2}{\tau_r}s_r^{\text{OFF}} & -\frac{kn^2}{\tau_r}c_r^{\text{OFF}} & 0 \\ -1 & 0 & 0 & \sum_{i=1}^{2}\left(1+k-\frac{k\tau_i^2}{\tau_r^2}\right)c_i^{\text{ON}} \\ 0 & c_r^{\text{ON}} & s_r^{\text{ON}} & -\sum_{i=1}^{2}c_i^{\text{ON}} \\ 0 & \frac{kn^2}{\tau_r}s_r^{\text{ON}} & -\frac{kn^2}{\tau_r}c_r^{\text{ON}} & \frac{k}{\tau_r^2}\sum_{i=1}^{2}\tau_i\left(\tau_i^2-\tau_r^2-\frac{\tau_r^2}{k}-n^2\right)s_i^{\text{ON}} \end{bmatrix}$$

$$\begin{bmatrix} (1+k)\sum_{i=1}^{2}\frac{1}{\tau_i^2}-\frac{2k}{\tau_r^2} & 0 & 0 \\ 0 & (1+k)\sum_{i=1}^{2}\frac{1}{\tau_i^2}-\frac{2k}{\tau_r^2} & 2+2k-\frac{k}{\tau_r^2}\sum_{i=1}^{2}\tau_i^2 \\ -\sum_{i=1}^{2}\frac{1}{\tau_i^2} & 0 & 0 \\ 0 & \left(1+k+\frac{kn^2}{\tau_r^2}\right)\sum_{i=1}^{2}\frac{1}{\tau_i^2}-\frac{2k}{\tau_r^2} & 2\left(1+k+\frac{kn^2}{\tau_r^2}\right)-\frac{k}{\tau_r^2}\sum_{i=1}^{2}\tau_i^2 \\ \sum_{i=1}^{2}\left(\frac{1+k}{\tau_i^2}-\frac{k}{\tau_r^2}\right)c_i^{\text{ON}} & \sum_{i=1}^{2}\left(\frac{1+k}{\tau_i^3}-\frac{k}{\tau_r^2\tau_i}\right)s_i^{\text{ON}} & \sum_{i=1}^{2}\left(\frac{1+k}{\tau_i}-\frac{k\tau_i}{\tau_r^2}\right)s_i^{\text{ON}} \\ -\sum_{i=1}^{2}\frac{1}{\tau_i^2}c_i^{\text{ON}} & -\sum_{i=1}^{2}\frac{1}{\tau_i^3}s_i^{\text{ON}} & -\sum_{i=1}^{2}\frac{1}{\tau_i}s_i^{\text{ON}} \\ \frac{k}{\tau_r^2}\sum_{i=1}^{2}\left(\tau_i-\frac{\frac{\tau_r^2}{k}+\tau_r^2+n^2}{\tau_i}\right)s_i^{\text{ON}} & \frac{k}{\tau_r^2}\sum_{i=1}^{2}\left(\frac{\frac{\tau_r^2}{k}+\tau_r^2+n^2}{\tau_i^2}-1\right)c_i^{\text{ON}} & \frac{k}{\tau_r^2}\sum_{i=1}^{2}\left(\frac{\tau_r^2}{k}+\tau_r^2+n^2-\tau_i^2\right)c_i^{\text{ON}} \end{bmatrix}. \tag{31}$$

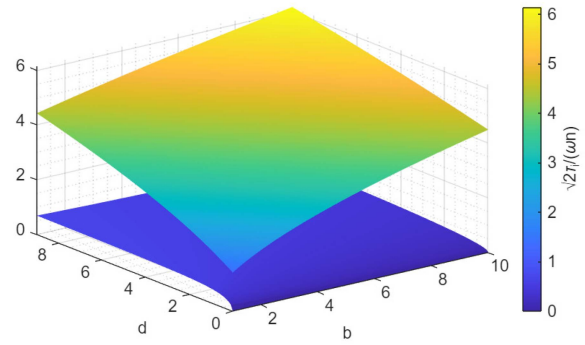

Fig. 5. Surface plots of normalized (21) (bottom) and (22) (top) with respect to (16) and (19).

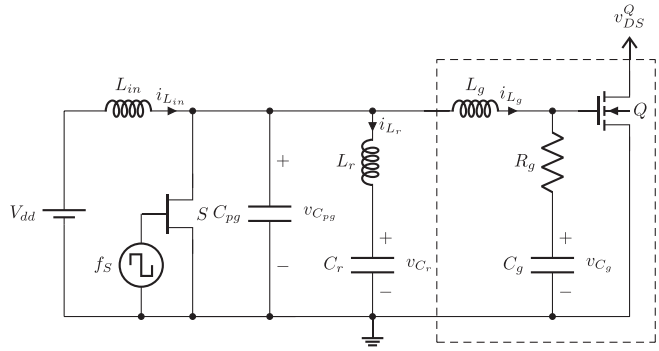

Fig. 6. Circuit diagram of the updated topology of the Class Φ gate driver. The gate of Q is modeled as a series lumped C_g, L_g, and R_g, as well as, a parallel capacitor C_{pg} is introduced to the topology.

values. From this point, the remaining unknowns of the circuit are the values of the four passive energy storing components. Since the input capacitance of the power device is provided as an input parameter, we have to define three more constraint conditions in order to calculate the remaining components.

Given that the gate driver is a Class E type inverter with shunt capacitance, an unavoidable and straight-forward design condition is ZVS, otherwise high efficiency operation will not be achieved. This condition is mathematically defined from (25) as follows:

$$\frac{V_{DS}^{\text{OFF}}}{V_{dd}} = (1+k)\left.\frac{\mathrm{d}}{\mathrm{d}\theta}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda}\right|_{\theta=\theta_{\text{ON}}} - \left.\frac{k}{\tau_r^2}\frac{\mathrm{d}^3}{\mathrm{d}\theta^3}\frac{i_{L_R}^{\text{OFF}}(\theta)}{\lambda}\right|_{\theta=\theta_{\text{ON}}} \tag{34}$$

where V_{DS}^{OFF} is the required value of the drain voltage at turn-ON. For ZVS, V_{DS}^{OFF} should be set to zero, but our method allows for circuit designs at any value of $v_{C_{iss}}(\theta_{\text{ON}})$.

From (25), we can notice that the harmonic content of the gate voltage of the power transistor has two components, i.e., τ_1 and τ_2, normalized to the switching frequency. From this observation, we decide to form the remaining two design conditions based on the frequency domain of the gate signal. As explained in [8], the gate signal best approximating a square wave for the circuit, as shown in in Fig. 1, is a Class Φ_2 gate driver that includes the first and third harmonics at zero phase, along with a dc component.

In Fig. 5, we plot the normalized surface of τ_1 and τ_2 with respect to b and d, where we can observe that $\tau_2 > \tau_1$ for any combination of (b, d). The same conclusion can be made by analyzing (21) and then applying the conclusions to (22). Hence, in order to obtain a square gate voltage signal, we need to set (21) to represent the first harmonic and (22) the third harmonic. However, our method still works for any combination of (τ_1, τ_2).

Since (14) is a quadratic equation with respect to s^2 and (14) is positive, there is a special relation for the sum and the product of its roots. The product relation is given by (22), and the sum is the following:

$$\tau_1^2 + \tau_2^2 = n^2 + \tau_r^2\left(1+\frac{1}{k}\right). \tag{35}$$

These two equations form the final two conditions needed for solving the inverse problem of designing a Class Φ gate driver.

As mentioned previously, the best approximation of a square voltage gate signal using a Class Φ gate driver is achieved with ϕ-branch resonating at the second harmonic and ideally the remaining first and third harmonic contents of the output being in phase. However, in practice, this requirement may be too strict to produce a real circuit solution, and therefore, we introduce relaxation parameters to the definitions of the harmonic content of the gate voltage. Mathematically, for a Class Φ_2 gate driver, this condition is set by

$$\tau_1 = \frac{r_1}{2D_Q} \tag{36}$$

$$\tau_2 = 3r_2\tau_1 \tag{37}$$

where $r_{1,2}$ are the relaxation parameters set as inputs to the design method.

III. Optimization on Modified Gate Driver Circuit

The analytical solution developed on the simplified model in the previous section allows for the component values of the passives to be derived easily. In this section, a few modifications are made to the circuit topology, as shown in Fig. 6, to make the design more robust toward gate parasitics as well as power stage operation. This allows for accurate waveform shaping to be performed through an iterative optimization tool.

A. Modified Gate Model

The model of the gate is enriched to include the parasitic gate resistance, R_g, and gate inductance, L_g, as well as a dynamic gate capacitance, C_g, which is now a function of the switching angle, θ, and takes into account the Miller effect.

The gate inductance parameter, L_g, represents the sum of the internal gate inductance itself and any parasitic inductance in the driving loop from S to the gate of Q. The parasitic inductance should be minimized by means of layout as much as possible. Practically, zero gate inductance is impossible; however, since this is a design parameter for our circuit, even relatively high values can be absorbed without negative impact to the operation

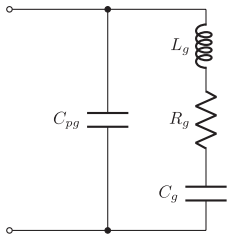

Fig. 7. Gate network with C_{pg} included to dominate the effects of the gate parasitics such that the impedance network that the gate driver is designed for is still capacitive in nature.

of the gate driver. In our experimental example in Section V, the impedance of L_g is 11.5% of R_g and 1.3% of C_g. The effect of L_g in a Class Φ gate driver is nontrivial as it can potentially change the current in the output branch. This corresponds to a large di_{L_g}/dt into the gate, which produces a spike in v^Q_{GS}, as shown by

$$v^Q_{GS} = v_{C_g} + R_g i_{L_g} + L_g \frac{\mathrm{d}i_{L_g}}{\mathrm{dt}}. \tag{38}$$

The other addition to the model is related to C_{iss} being a function of the drain voltage and changing through the switching period. Furthermore, the Miller effect also causes the gate capacitance, C_g, to be highly variable through the switching period due to the high voltage gain (v^Q_{DS}/v^Q_{GS}) for an SiC device. The update of C_g to include the Miller effect is shown by

$$C_g(\theta) = C_{iss}(\theta) + \frac{v^Q_{DS}(\theta)}{v^Q_{GS}(\theta)} \cdot C_{rss}(\theta). \tag{39}$$

B. External Shunt Capacitance for Versatility

To reduce the effect of the parasitics of the gate, an addition is made to the topology of the gate driver, which improves the robustness of the design. A shunt capacitance is included, C_{pg}, which can dominate the effective network, as shown in Fig. 7. The equivalent input impedance relation of the network is shown in (40), and it can be seen in (41) that at high frequencies, the impedance of the network asymptotes toward that of C_{pg}, which means that the design of the gate driver will be closer to that in Fig. 1 with the design variable in the previous section, C_{iss}, now equivalent to the C_{pg} chosen

$$Z_{\text{in}}(s,\theta) = \frac{s^2 L_g C_g + s C_g R_g + 1}{s C_{pg} \cdot [s^2 L_g C_g + s R_g C_g + 1]} \tag{40}$$

$$\lim_{s\to\infty} Z_{\text{in}}(s,\theta) \approx \frac{1}{sC_{pg}}. \tag{41}$$

It is to be noted that C_{pg} includes the output capacitance of the switch S, C^S_{oss}, which varies with the drain voltage of S. The device parasitic can be absorbed in the choice of C_{pg} chosen by using a lower effective discrete capacitor.

C. Full State-Space Model

For accurate modeling of the steady-state time domain waveforms of the gate driver circuit, a state-space model of the circuit is developed on the updated topology, as shown in Fig. 6. The methodology resembles the state-space analysis for a Class EF inverter from [10] and the specific system and input matrices for our topology are given in the following:

$$\mathbf{A}_{\text{ON/OFF}} = \frac{1}{\omega} \cdot \text{diag}^{-1}(L_{\text{in}}, L_r, L_g, C_r, C_{pg}, C_g) \cdot \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & -R_g & 0 & 1 & -1 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & -1 & -1 & 0 & -\dfrac{1}{R_{ds}} & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{42}$$

$$\mathbf{B} = \frac{V_{dd}}{\omega \cdot L_{in}} \cdot \mathbf{e}_1 \tag{43}$$

$$\mathbf{X}(\theta) = \begin{bmatrix} i_{L_{\text{in}}}(\theta) & i_{L_r}(\theta) & i_{L_g}(\theta) & v_{C_r}(\theta) & v_{C_{pg}}(\theta) & v_{C_g}(\theta) \end{bmatrix}^T \tag{44}$$

where $\mathbf{e}_i$ represent a column vector with ith element being 1 and all other elements being 0. The $\mathbf{A}_{\text{ON/OFF}}$ matrix changes based upon the value of R_{ds} depending on whether the switch S is switched ON or OFF. The assumption made is that there is no transition time between the states. This state-space model representation can be used to calculate the waveforms of the node voltages and branch currents defined by the states, as well as solve for the boundary conditions. The solution is given by (46) shown at the bottom of the next page, with the boundary conditions given as follows:

$$\begin{bmatrix} \mathbf{X}(\theta_{\text{ON}}) \\ \mathbf{X}(\theta_{\text{OFF}}) \end{bmatrix} = \mathbf{C}^{-1}\mathbf{E} \tag{45}$$

where $\mathbf{C}^{-1}$ and $\mathbf{E}$ are given by (47) and (48) shown at the bottom of the next page.

D. Full State-Space Optimization

With the full state-space model derived, the drain waveform can be shaped as required by using an optimization algorithm. This allows the designer to obtain gate profiles for a certain switching speed and output slew rate as per the application to improve power device drain efficiency. Fig. 3 demonstrates examples with diverse gate profiles and $\mathrm{d}v/\mathrm{d}\theta$ rates (i.e., designs 1 and 3 are steeper than 2 and 4). With the given V_{dd} and gate parameters, L_g, R_g, and C_g, the parameters to be found are L_r, C_r, L_{in}, and C_{pg}. The starting value for the search algorithm is the result from Section II with $C_{pg} = C_{iss}$. The parameters to be found can be combined into two resonant pairs, $L_r C_r$ and $L_{\text{in}} C_{pg}$. Having each pair resonated at a different frequency, or changing the individual values for the same resonant frequency, allows for precise control of the drain waveform shape. This is done by using two normalized parameters, p_{Lr} and $p_{L\text{in}}$

$$L'_{\text{in}} = L_{\text{in}}/p_{L\text{in}} \tag{49}$$

$$L'_r = L_r \cdot p_{Lr} \tag{50}$$

$$C_r' = C_r/p_{Lr}. \tag{51}$$

The following weighted cost function is developed as there are three objectives and 2 degrees of freedom in the design:

$$\text{Cost, } J = \mathbf{W}\cdot\mathbf{R} \tag{52}$$

where $\mathbf{W} = \begin{bmatrix} W_1 & W_2 & W_3 \end{bmatrix}$ is the weighting matrix and

$$\mathbf{R} = \begin{bmatrix} \sqrt{\dfrac{\sum_{i=1}^{N_{\text{pt}}} |v_{C_{pg}}^{\text{array}}[i] - \mu_{\text{peak}}|^2}{N_{\text{pt}}-1}} \\ \left.\dfrac{\mathrm{d}v_{C_{pg}}(\theta)}{\mathrm{dt}}\right|_{\theta=0} + \left.\dfrac{\mathrm{d}v_{C_{pg}}(\theta)}{\mathrm{dt}}\right|_{\theta=\theta_{\text{ON}}} \\ v_{C_{pg}}(\theta_{\text{ON}}) \end{bmatrix} \tag{53}$$

where

$$\mu_{\text{peak}} = \frac{1}{N_{\text{pt}}}\sum_{i=1}^{N_{\text{pt}}} v_{C_{pg}i}. \tag{54}$$

The components of the $\mathbf{R}$ matrix define the drain voltage objectives to be minimized. The first term, $\mathbf{R}_{(1,1)}$, relates to the flatness of the peak gate voltage. Inherently, due to the superposition of two harmonics on the drain voltage, the flatness of the peak of the gate voltage can be manipulated by controlling the phase difference between the two harmonics. The characteristic third harmonic ripple in the drain voltage of a Class EF_2 should be minimized so that the gate voltage has as wide as possible flat peak, enabling the power device, Q, to have a lower channel resistance and higher drain efficiency. A standard deviation-based cost is attributed to this, where the array of discrete drain voltages calculated in the state-space analysis of S is arranged in a descending order, and the standard deviation is calculated for a number of points, N_{pt}.

The next term, $\mathbf{R}_{(2,1)}$, targets the reduction of the inductive spike, as discussed in Section III-A. This is achieved by equalizing the turn-ON and turn-OFF slope magnitudes of the gate waveform. The rate of change of the drain voltage of S is related to the current through the capacitor C_{pg} via the following relationship:

$$\frac{\mathrm{d}v_{C_{pg}}(\theta)}{\mathrm{d}\theta} = \frac{i_{C_{pg}}(\theta)}{C_{pg}}. \tag{55}$$

To represent the equality of the turn-ON and turn-OFF slopes, the currents should be

$$i_{C_{pg}}(\theta_{\text{OFF}}) = -i_{C_{pg}}(\theta_{\text{ON}}) \tag{56}$$

where the quantities can be defined using state variables

$$i_{C_{pg}}(\theta) = i_{L_{\text{in}}}(\theta) - \frac{v_{C_{pg}}(\theta)}{R_{ds}(\theta)} - i_{L_g}(\theta). \tag{57}$$

The third component, $\mathbf{R}_{(3,1)}$, defines the soft-switching of the gate driver device, S. Maintaining this would reduce the power loss of the gate driver; however, the design can also be made to hard-switch slightly to increase the turn-OFF slope of the gate profile of Q.

The cost function shown in this section is only one of many possible ones. The parameters chosen target key aspects of the waveform to provide sufficient shaping capabilities. This can be used as a tool to design the specific gate signal profile that would suit the power device, the most depending on the gate capacitance, parasitics, power stage topology, and specification.

IV. Numerical Example and Simulation Results

To implement and verify the design methodology developed so far, specific numerical values for the power device gate, and switching parameters are required. For this, the power stage has to be designed in terms of topology, switching frequency, and device positive duty cycle, as well as the power device itself chosen accordingly. The design methodology can then be used to find parameters for the passives of the RGD for this specific application. This section looks into utilizing the design methodology and verifying it on simulation program with integrated circuit emphasis (SPICE) simulation with the power stage to observe the behavior of the complete system.

A. Power Stage Design and Device Choice

The design of the gate driver has to be performed for a specific duty cycle, frequency, and input parameters of the power device, Q. In this article, we choose to drive an SiC power device at multi-MHz frequencies to evaluate the RGD. To implement a high-frequency power stage, we choose the topology to be a Class E inverter, as shown in Fig. 8, with Q chosen to be the C3M0065100J device which is a 1000 V, 65 mΩ SiC MOSFET developed by Wolfspeed. The reason for choosing this device was the relatively low-output capacitance C_{oss} of the device, which simplifies the design of the inverter as well as low $\tau_g =$

$$\mathbf{X}(\theta)|_{\theta^+_{\text{ON/OFF}} \le \theta \le \theta^-_{\text{OFF/ON}}} = \mathrm{e}^{\left(\theta-\theta^+_{\text{ON/OFF}}\right)\mathbf{A}_{\text{ON/OFF}}}\cdot\mathbf{X}\left(\theta_{\text{ON/OFF}}\right) + \mathbf{A}^{-1}_{\text{ON/OFF}}\cdot\left(\mathrm{e}^{\left(\theta-\theta^+_{\text{ON/OFF}}\right)\mathbf{A}_{\text{ON/OFF}}} - \mathbf{I}\right)\mathbf{B} \tag{46}$$

$$\mathbf{C}^{-1} = \begin{bmatrix} \left[\mathbf{I} - \mathrm{e}^{\left(\theta^-_{\text{ON}}-\theta_{\text{OFF}}\right)\mathbf{A}_{\text{OFF}}}\mathrm{e}^{\theta_{\text{OFF}}\mathbf{A}_{\text{ON}}}\right]^{-1} & \mathbf{0} \\ \mathbf{0} & \left[\mathbf{I} - \mathrm{e}^{\theta_{\text{OFF}}\mathbf{A}_{\text{OFF}}}\mathrm{e}^{\left(\theta^-_{\text{ON}}-\theta_{\text{OFF}}\right)\mathbf{A}_{\text{OFF}}}\right]^{-1} \end{bmatrix}\cdot\begin{bmatrix} \mathbf{I} & \mathrm{e}^{\left(\theta^-_{\text{ON}}-\theta_{\text{OFF}}\right)\mathbf{A}_{\text{OFF}}} \\ \mathrm{e}^{\theta_{\text{OFF}}\mathbf{A}_{\text{ON}}} & \mathbf{I} \end{bmatrix} \tag{47}$$

$$\mathbf{E} = \begin{bmatrix} \mathbf{A}^{-1}_{\text{OFF}}\left(\mathrm{e}^{\left(\theta^-_{\text{ON}}-\theta_{\text{OFF}}\right)\mathbf{A}_{\text{OFF}}} - \mathbf{I}\right)\mathbf{b} \\ \mathbf{A}^{-1}_{\text{ON}}\left(\mathrm{e}^{\theta_{\text{OFF}}\mathbf{A}_{\text{ON}}} - \mathbf{I}\right)\mathbf{b} \end{bmatrix}. \tag{48}$$

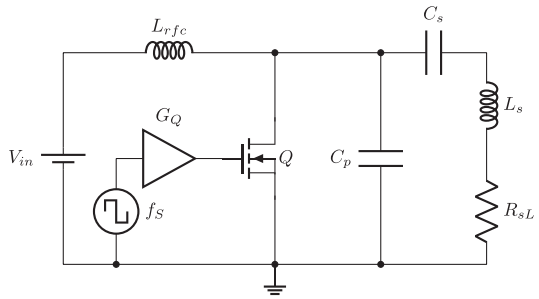

Fig. 8. Circuit diagram of the Class E power stage. The device Q is the Wolfspeed C3M0065100J SiC MOSFET and the gate driver G_Q is either a commercial SiC driver or the RGD.

R_gC_g constant, which means that the device can be driven more easily at high frequencies.

The power stage is designed to be operated at 6.78 MHz with $D_Q = 0.4$. Since the aim of the power stage is to allow for Q to be stressed with a high current and high drain voltage, the real load on the output branch is not consequential. Hence, to prevent the complication of dissipating the power through an RF ac load, a design choice was made to only have an undamped L_sC_s output resonant tank. In addition, to improve the thermal dissipation of Q, an insulated metal substrate (IMS) PCB is used as its thermal resistance is low due to a thinner and more effective dielectric. The thinner dielectric increases parasitic capacitance in the board layout, which can be an issue at high-frequency operation. The key parasitic capacitance for our case would be that between the drain copper area and the source (aluminium base is shorted to ground potential). This means that the capacitance has to be absorbed into the design of the circuit as C_p, and hence, a finite input choke is chosen to introduce a degree of freedom in the design of the power stage to allow for higher values of C_p to be tolerated for a given switching frequency [10].

B. Gate Driver Design Based on Power Device

With the design of the power stage, the parameters of the gate driver can be calculated. C_{pg} chosen to be 1.5 nF for this design as it would dominate the quoted input capacitance of Q from the datasheet. Fig. 9 shows waveforms obtained from the analytical approach of solving the simplified model with the inputs and outputs from the solver, as shown in Table IV. Fig. 10 shows the value of cost with iteration number and shows that the solver converges to a solution within the set tolerance after nine iterations. We compare the waveforms that our method obtains directly with what was available in the literature previously [7], [8], as shown in Fig. 9. It can be seen that our method of solving the state space is required, especially due to the waveform of i_{Lr}, which is composed of multiple frequencies. Assuming that this as a single harmonic, which is done in [7] and [8], would have been inaccurate. The first harmonic approximation (FHA) used in the literature obtains a nonideal gate profile. This is because the gate voltage dips below the threshold voltage of the device during the desired ON-state. Along with this, the gate

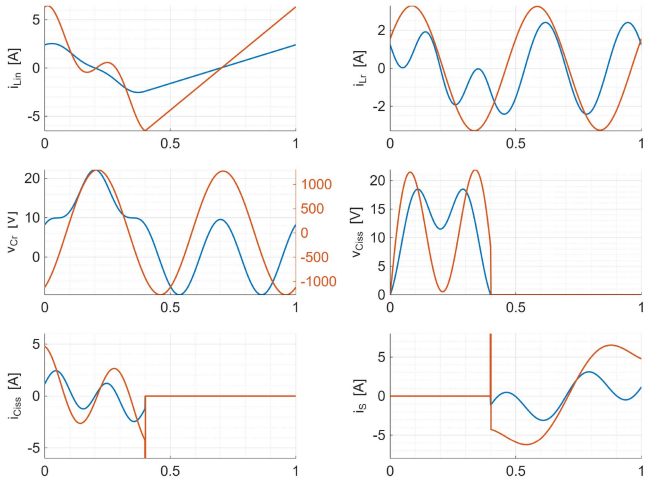

Fig. 9. Comparison of performance of the gate driver with parameters derived from our analytical method (blue) compared to the one in existing literature based on FHA [7], [8] (orange). The most important parameter to be noted is $v_{C_{iss}}$, which is the gate voltage. The plot of v_{C_r} has two axes as the scale of the voltages are two orders of magnitude different.

TABLE IV
PARAMETER VALUES OBTAINED FROM VARIOUS METHODS

Input Parameters	FHA [8]	Analytical	Full state-space	Units
f_S	6.78	6.78	6.78	MHz
D_Q	-	0.4	0.4	-
V_{dd}	-	5	5	V
C_{iss}	1	1.5	-	nF
a	0.278	-	-	-
τ_1	-	1	-	-
τ_2	-	1.3	-	-
N_{pt}	-	-	2000	-
$W_{1,2,3}$	-	-	1	-
R_g	-	-	2.6	Ω
L_g	-	-	7.14	nH
C_g	-	-	1	nF
Output parameters				
L_{in}	42.5	91.9	64.3	nH
C_{pg}	-	-	1.5	nF
L_r	4590	30.5	45.9	nH
C_r	0.03	1.94	1.29	nF

driver itself would have had high power losses as the switch, S, would hard-switch.

As discussed previously, this is a sufficiently good design point; however, the full state-space model developed incorporates more details of the gate parasitics, which allows for more precise tuning of the component values. Fig. 11 shows that relying on the values of the passive components from the analytical solution would not be possible due to the limitations of the model, which causes the circuit to be detuned. The component values obtained are used as the starting guess for the optimization algorithm with the cost function prescribed in (52). The values chosen for the parameters N_{pt} and $W_{1,2,3}$ are shown in Table IV along with the results from the retuning process. The optimization algorithm used is trust-region-dogleg implemented using the optimization toolbox in MATLAB. The

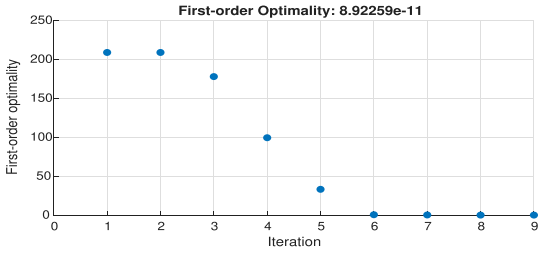

Fig. 10. First-order optimality cost function value with iteration number.

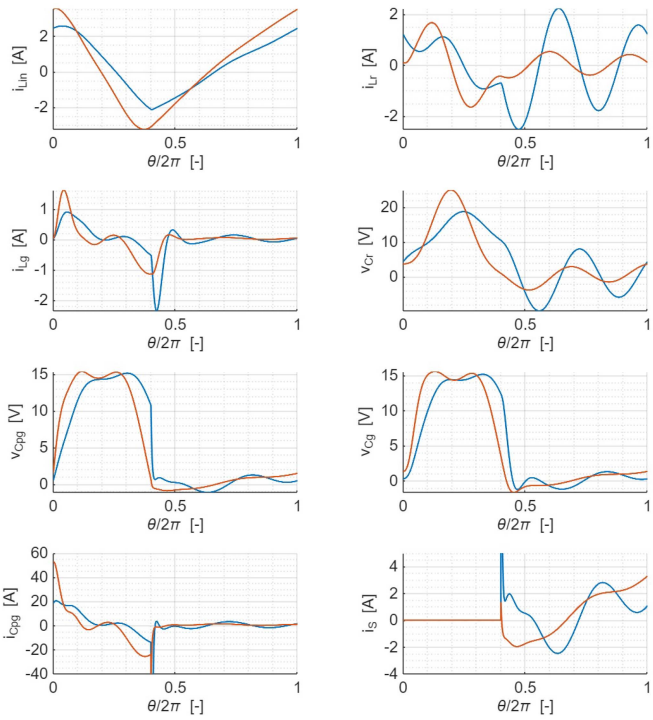

Fig. 11. Results from full state-space modeling with circuit parameters obtained from analytical solutions (blue) and those obtained by optimizing for the cost function described in (52) (orange). The most important parameter to be noted is $v_{C_{pg}}$, which is the gate voltage.

adjusted values of the components lead to a 30% difference in L_{in} required and a different pair of L_rC_r, which resonate at the same frequency. Fig. 12 shows the effects on the v_{Cpg} waveform as the parameters $p_{L\text{in}}$ and p_{Lr} are changed to show the degrees of freedom used to achieve the final waveform. Fig. 11 also shows the updated waveforms of the node voltages and branch currents.

C. SPICE Simulation

Due to the high operating frequency, and the nonlinear output capacitance of the devices, (C^Q_{oss} and C^S_{oss}) SPICE simulations are used to tune the resonant converters (power stage and gate driver) so that these parasitics are accounted for and absorbed in the discrete passive choices. Fig. 13 shows the drain current and voltage of Q, the input current, $i_{L_{rfc}}$, the output resonant tank current, i_{L_s}, and drain power loss, P^Q_{ds} for the RGD and HSW gate signal profiles.

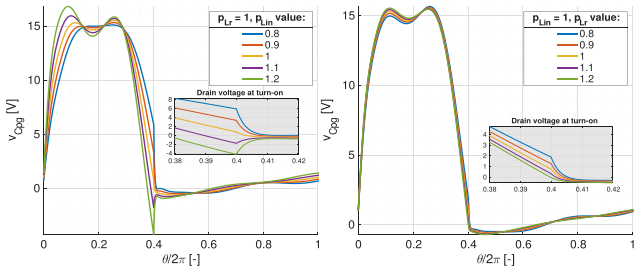

Fig. 12. Effect of normalized parameters, $p_{L\text{in}}$ and p_{Lr}, on the drain voltage of S (gate voltage of Q). These parameters can be effectively used to tune the waveform to enable soft-switching as well as control the shape (flatness) of the peak gate voltage. (a) Variation in $p_{L\text{in}}$. (b) Variation in p_{Lr}.

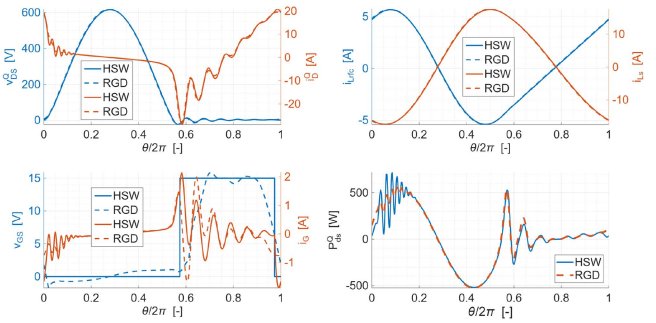

Fig. 13. Waveform comparison between RGD and HSW signal effect on the power stage, which shows that with an equivalent gate profile in terms of the duty cycle, the power stage performs the same.

It can be seen that the power stage matches exactly, with the drain voltage, input current and output branch current equivalent in both cases. The gate profiles have been matched for the effective gate duty cycle to ensure a fair comparison. The ringing on the drain current is seen to be lower when driven by the RGD due to the shape of the gate profile. This affects the transition through the resistive linear mode to saturation for the device (Q), which dampens the resonance effect. An interesting observation is the phase difference required for the different gate voltage waveform profiles to achieve the same drain waveform phase. It is easier to understand this by looking at the gate current, as shown in Fig. 13, where the spikes of the current align between the two gate signal profiles.

D. Robustness of Gate Driver to a Detuned Power Stage

For a Class E inverter, load variations can cause the resonant branch to be detuned, which would cause the power device, Q, to hard-switch or reverse conduct. This could be intentionally part of the design to tolerate large variations of load in open-loop, as described in [23]. This means that the gate driver should be able to operate effectively in these conditions as well.

To simulate the power stage being detuned, L_s is scaled from 90% to 130% of its nominal value (in steps of 10%). Fig. 14 shows the effect on the drain voltage and gate voltage by this. It can be seen that the effective gate voltage is similar with the switch S of the gate driver maintaining soft-switching operation and the desired duty cycle. There is a difference in ripple on the

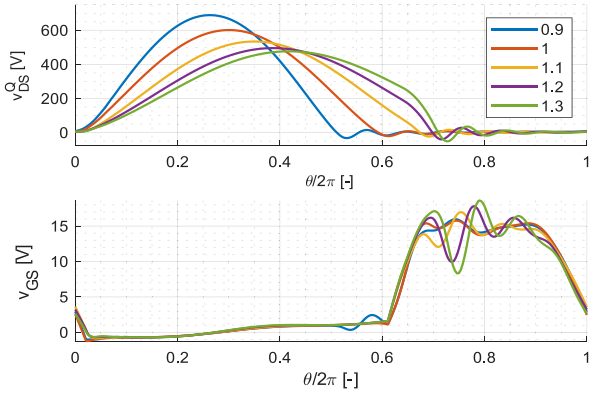

Fig. 14. Simulation waveforms showing how detuning the power stage [shown by the drain voltage of the power device (top)] affects the gate profile (bottom) produced by the RGD.

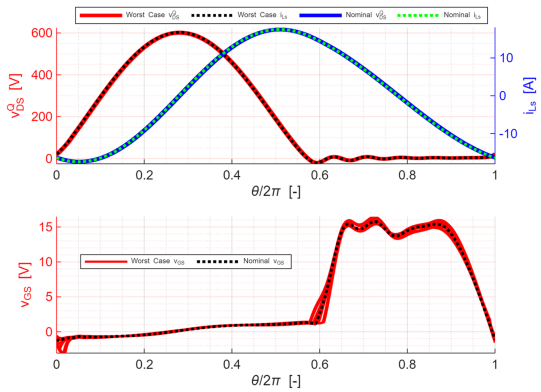

Fig. 15. Deviations on the gate driver and power stage circuit waveforms due to worst case variations on the RGD passives. There are 16 combinations of passives chosen.

gate profile and this is because of the high frequency ripple on the drain coupling to the gate via C_{gd}^{Q}. This phenomenon will be explored in more detail in Section V-C.

It is to be considered that the detuning of the power stage has been exaggerated as reverse conducting or hard-switching to the extent, as shown in Fig. 14, is not possible due to excessive power loss on the device. This can be considered as the absolute worst case scenario for the gate driver.

E. Worst Case Sensitivity Analysis to RGD Passives

As with resonant converters, the Class Φ gate driver is sensitive to choices in the passive components. The four passives in the gate drive circuit, L_{in}, L_r, C_{pg}, and C_r, can have variations due to manufacturing tolerances, layout parasitics, etc. It is important to investigate the effect of variations on these components on the gate profile as well as the performance of the Class E power stage.

We perform the worst case analysis simulation where we have a ±5% tolerance on the two inductors and ±1% on the two capacitors. There are 16 (2^N, where N is the number of parameters varied) combinations of all of the worst case deviations, which are plotted on Fig. 15 along with the nominal waveforms.

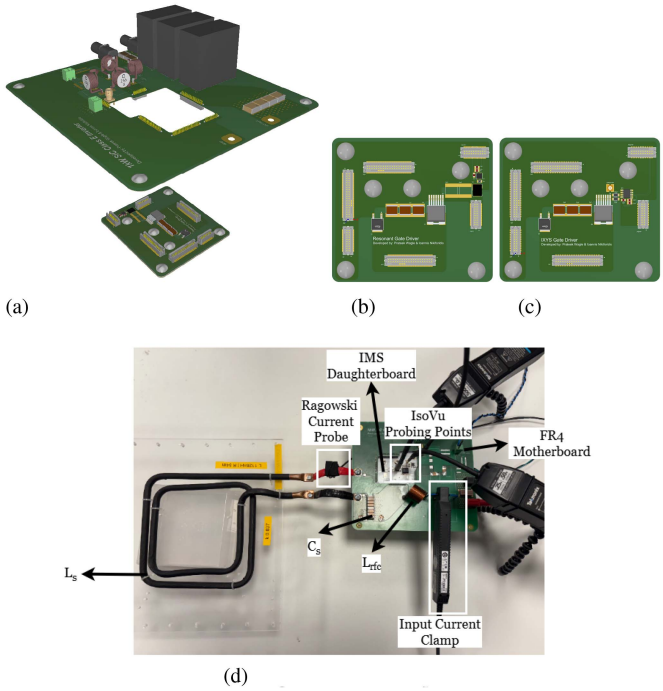

Fig. 16. Experimental setup pictures. (a) Render of the multiboard assembly with the mother and daughter board connected. (b) Top view of RGD IMS board. (c) Top view of HSW IMS board. (d) Experimental setup during testing, with the output coil (L_s) connected and modified input choke. (a) Complete multiboard assembly. (b) RGD IMS. (c) HSW IMS. (d) Experimental setup.

The effect on the power stage is minimal, with the drain voltage and current unaffected by the variations in the RGD circuit parameters. The gate profiles have a slightly different effective duty cycle, which means that in some cases, the power device reverse conducts or hard-switches. However, the variation in the effective duty cycle (threshold voltage crossing points) is ±0.025, which is negligible.

V. Experimental Validation and Results

A. Experimental Setup

To compare the RGD with a conventional off-the-shelf gate driver, identical power stages have to be designed to compare the performance of the power device, Q, and correlate any difference to the gate signal profile. Since the power stage is designed in the previous section to be operated with high frequency and high-amplitude currents to stress the power device, Q is placed on an IMS board. The IMS is connected to an FR4 motherboard, as shown in Fig. 16(a), which consists of the input decoupling capacitors (C_{in}), L_{rfc}, and C_s, and connectors for L_s, as well as for the input power and signal. The advantage of a multiboard setup is to share as many of the same components across the RGD and HSW implementation to equalize losses between the two power stages. As seen from Fig. 16(b) and (c), the drain node and interconnect positions are identical in the two IMS boards with differences only in the gate driving section. The HSW IMS gate driving section consists of the off-the-shelf gate driver with its decoupling capacitors while the RGD IMS gate

TABLE V
PARAMETER VALUES USED IN EXPERIMENTAL IMPLEMENTATION

Parameters	Values	Units
V_{dd}	5	V
V_{in}	≈ 210	V
C_{in}	1.28	μF
L_{rfc}	1.42	μH
$R_{L_{rfc}}$	497.7	mΩ
C_p^{eff}	925	pF
C_s	746.7	pF
L_s	1.16	μH
R_{L_s}	106.9	mΩ
L_{in}	61.3	nH
C_{pg}	1.4	nF
L_r	45.7	nH
C_r	1.297	nF

driving section has the switching element, S, and C_{pg}, with L_{in}, L_r, and C_r on the FR4 motherboard. The parasitic inductance on the gate loop is minimized by physically laying out S close to the gate pin of Q. In addition, bulk capacitors are used to make sure that the input current ripple is sourced from the bulk capacitance rather than the dc voltage source.

The measurements on the experimental setup are taken using a variety of voltage probes and current probes, which minimize additional circuit loading and provide sufficient bandwidth to analyze the waveforms. The drain and gate voltage of Q is measured using Tektronix IsoVu probes. The input choke current, i_{Lrfc}, is measured using a 30 A/100 MHz Agilent N2783A current probe and the output coil current, i_{Ls}, is measured using a 300 A/30 MHz Keysight N7042A Rogowski ac current probe due to the high-amplitude current. Fig. 16(d) shows the setup used with the probes attached to the circuit. Since the input voltage and current for both the power stage and gate driver are purely dc, the input power of both are measured using a Yokogawa WT332E 2-channel power meter. This has a sufficient accuracy for both power levels and allows convenient simultaneous acquisition of both metrics.

B. RGD and Power Stage Measurements

The passive component values used for the RGD and power stage in the experimental setup are shown in Table V. The RGD is sensitive to the values of the passives chosen, especially the inductances, L_{in} and L_r, which have small absolute values, and hence, parasitic inductance has to be taken into account. The inductances were therefore adjusted manually by increasing the spacing between the turns of copper of the Coilcraft 2014VS-66N and 1212VS-42N aircore inductors, reducing the inductance. Fig. 22(d) shows the gate signal profile obtained from the RGD. This is similar to the waveform expected from design work, with the expected duty cycle of $D_Q = 0.4$ and a peak $v_{GS}^Q = 15$ V achieved with an input voltage $V_{dd} = 5$ V. Fig. 22(a)–(c) shows the waveforms obtained from the power stage, which also match simulations.

The RGD consumes 0.8 W of power whilst the power stage takes 76.5 W when it is operating at maximum supply voltage. The power device reaches a steady-state temperature of 71.6 °C, which shows that the RGD works as intended in driving an SiC power stage at multi-MHz operating frequency.

C. Effect of C_{gd}^Q on RGD Waveform

When the device Q turns ON, a high frequency ringing is observed on the drain voltage due to the parasitic drain inductance and device output capacitance. This is coupled to the gate voltage waveform, through the C_{gd}^Q capacitance. The higher the ringing on the drain, the higher the resulting ringing on the gate voltage. The drain voltage of the power stage with a variety of input supply voltages is shown in Fig. 17(a), with detail of the ripple during turn-ON. The higher the peak drain voltage during turn-OFF, the higher the $\mathrm{d}V/\mathrm{d}t$ on the drain voltage, which, in turn, excites a higher amplitude ringing during turn-ON, despite having ZVS. It is observed that the higher amplitude of ringing on the drain, the higher the magnitude of the ringing on the gate waveform, which is shown in Fig. 17(b).

The reason for the phase difference in ripple voltage between the trials, as shown in Fig. 17(a) and (b), is due to C_{oss}^Q being dependent on v_{DS}^Q, which causes the drain voltage to have different zero-crossing points depending on the peak voltage reached. In addition, Fig. 18 shows that as the power stage input voltage increases, the power utilized by the gate driver reduces. This corroborates with the effect seen in SPICE simulations and occurs due to the different currents in S, C_{pg}, and the gate of Q affected by the high-frequency current injected through C_{gd}^Q.

D. Cored Versus Air-Core Magnetics for RGD

The majority of the power loss in the RGD gate drive circuit comes from conduction loss in S as well as the copper loss in the air-cored magnetic elements. The two magnetic elements of the gate driver circuit, i.e., ϕ-branch L_r and the finite input choke, L_{in}, have a high frequency, high-amplitude current though them. At high frequencies, the copper loss due to skin effect and proximity effect in the winding is significant [24], especially in air-core inductors where a high number of turns are needed to achieve the required inductance. However, our recent work in [25] shows that well-designed cored inductors in ϕ-branch yield performance benefits over their air-core counterparts. This should also be true for the finite input choke, which has a high current ripple component through it.

A reasonable and simple approximation to calculate the copper loss is by summing the ohmic loss of each frequency component of the current by the effective resistance of the winding of the inductor at the respective frequency. The dc resistance of a solenoid winding is given by [25]

$$R_{\text{dc}} = \frac{\rho N l_{\text{turn}}}{A_{\text{wire}}} \tag{58}$$

where ρ is the resistivity of the conductor, N is the number of turns on the winding, l_{turn} is the length of conductor used for a single turn, and A_{wire} is the cross-sectional area of the conductor. At high frequencies, the copper utilization decreases due to skin effect, and therefore, the ac resistance of the winding

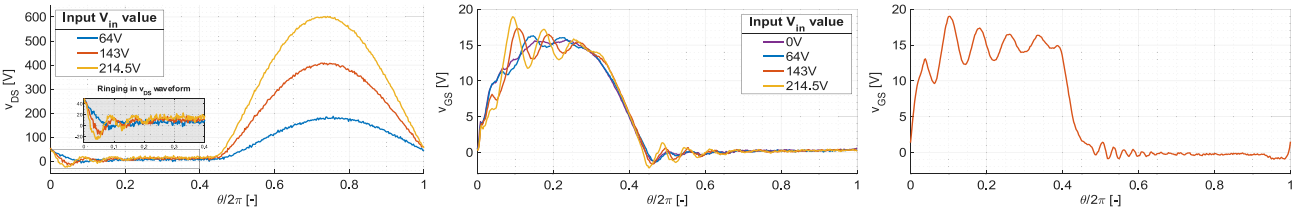

Fig. 17. Effect of v_{DS}^{Q} ringing on v_{GS}^{Q} waveform for different input voltages, which relates to the amount of ringing on the drain. (a) Drain waveform for various input voltages for RGD system. (b) Gate waveform for various input voltages for RGD system. The gate waveform is compared to the control, which is where the power stage is not running ($v_{DS}^{Q} = 0$). (c) Gate waveform for 143 V input voltage for the HSW system, which shows significant ringing at the limit of the specification of the maximum rating of the gate. (a) Drain voltage waveforms for RGD. (b) Ringing gate voltage waveforms for RGD. (c) Ringing gate voltage waveform for HSW.

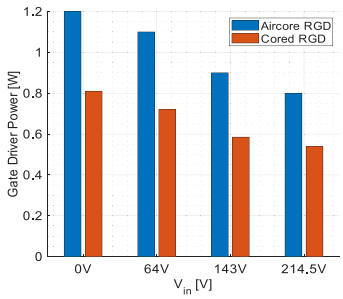

Fig. 18. Measured gate driver power consumption for RGD when the power stage is at various operating points (V_{in}). The HSW gate driver utilizes a consistent 4.65 W in all cases, with the first iteration of RGD with aircore magnetics utilising 0.8 W and the RGD with cored magnetics utilizing 0.54 W at the maximum operating point of the power stage.

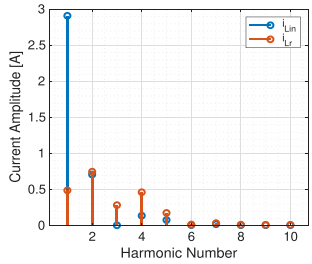

Fig. 19. Fourier coefficients of the first ten harmonics of the current through L_{in} and L_r showing the required harmonics for sufficient reconstruction and representation of the waveforms for copper and core loss calculations.

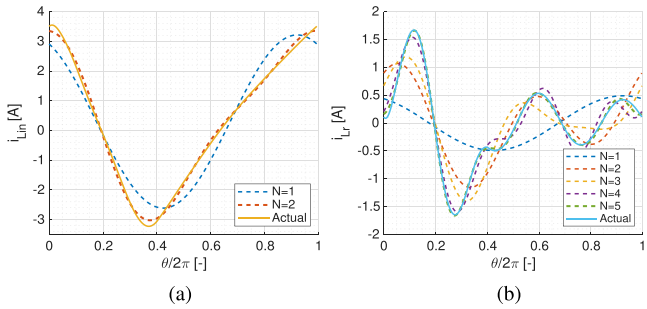

Fig. 20. Reconstruction of the current through the inductors of the gate driver using its harmonic content. Two harmonics are used for $i_{L\text{in}}$ and five are used for i_{Lr} to have a sufficiently high accuracy without introducing unnecessary computations. (a) $i_{L\text{in}}$ reconstruction. (b) i_{Lr} reconstruction.

is calculated by [24], [26]

$$R_{\text{ac},n} = R_{\text{dc}} \cdot \Delta_n \left(\frac{\sinh(2\Delta_n) + \sin(2\Delta_n)}{\cosh(2\Delta_n) - \cos(2\Delta_n)} \right) \tag{59}$$

where $\Delta_n = W/\delta_n$ for a rectangular wire, where W is the wire width; δ_n is the skin depth, where n is the frequency of the current; $\Delta_n \approx (\pi/4)^{3/4}\phi_{\text{wire}}/\delta_n$ for a round wire, where ϕ_{wire} is the diameter of the wire. The copper loss is given by

$$P_{\text{Cu}} = \frac{1}{2} \sum_{\forall n} I_n^2 R_{\text{ac},n}. \tag{60}$$

The core loss approximation for L_{in} and L_r is calculated by using the Steinmetz parameters, which provide a good approximation for power loss. The following equation is used to calculate the power loss density, which can be used to find the core loss of the structure [24]

$$P_v = \sum_{\forall n} P_{v,n} = \sum_{\forall n} k_n f_n^{\alpha_n} B_n^{\beta_n} \tag{61}$$

where k, α, and β are the Steinmetz parameters for the core material, for each frequency, n, and the flux, B_n, is

$$B_n = \frac{\mu_r \mu_0 N I_n}{l_c} \tag{62}$$

where I_n is the rms current at each frequency n, and l_c is the effective path length of the core. The core loss can be derived by using the effective volume of the core, V_e

$$P_{\text{core}} = P_v V_e. \tag{63}$$

The work in [25] and [27] shows that Fair-Rite 67 and Micrometals Mix-6 are suitable core materials for high-frequency inductors and will be used in this work. For L_{in}, a Fair-rite 67 planar EQ core is chosen (9567130302) while a Micrometals Mix-6 toroid (T50-6) is chosen for L_r. L_{in} has higher inductance and fewer harmonics compared to L_r, hence the difference in material choice. Fig. 19 shows the Fourier components of the currents through the inductors in a switching period. Using this, it was determined that two harmonics are sufficient to capture $i_{L\text{in}}$ whereas five harmonics are required for i_{Lr}. Fig. 20 shows the waveforms reconstructed using the Fourier components.

TABLE VI
CHARACTERIZATION OF INDUCTORS IN RGD

Parameters	L_{in}		L_r		Units
	2014VS-66N	F67 EQ Core	1212VS-42N	T50-6 Core	
μ_i	-	40	-	8.5	-
l_c	-	1.74	-	3.19	cm
V_e	-	0.348	-	0.358	cm^3
P_{Cu}	157.3	3.7	20.8	17.1	
P_{Core}	0	108.7	0	5.1	mW
P_{Total}	157.3	112.4	20.8	22.2	
L_{meas}	61.1	62.4	45.7	43.7	nH
Box vol.	2160	560	1680	2016	mm^3

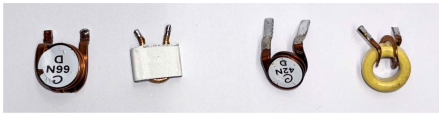

Fig. 21. Magnetic components from left to right: air-core L_{in} (2014VS-66N), cored L_{in} (F67 EQ Core), air-core L_r (1212VS-42N), and cored L_r (T50-6 Core).

The estimated copper and core losses in each of the magnetic structures are shown in Table VI along with the parameters used for the calculations.

The cored inductors are shown in Fig. 21 and built to match the inductance of the air-core inductors as closely as possible. An air-gap is introduced in between the EQ and I segments of the L_{in} structure to reduce the value of inductance to better match the requirement. The cored inductances are matched to within 2%–4.5% of the original value and are shown in Table VI. The box volume shown also indicates the benefits of utilizing a cored inductor, which allows for the magnetics to occupy a combined 67% of the volume of the air-core equivalent.

Fig. 18 shows a power improvement of 300 mW. which corresponds to a 32.5% improvement due to cored magnetics instead of air-core for the gate driver circuit. The gate waveform is slightly different, as shown in Fig. 22(d), and this is due to the core of L_r saturating slightly at full power, reducing the effective inductance value, which was matched at small signal. The measured power loss difference of the cored compared to air-core RGDs is higher than calculated. This is mainly due to the overestimation of core loss using the method in this article, as well as proximity effect being neglected in the air-core structures, which is not as significant in the cored structures due to the lower number of turns.

E. Power Stage Performance With an HSW Gate Driver

It is crucial to benchmark the performance of the RGD with a conventional gate profile to drive the SiC power MOSFETs. The authors in[28] and [29] utilize half-bridge drivers to synthesize the square wave gate profiles to drive SiC devices in the MHz region. In this article, we use an off-the-shelf high-speed gate driver, the IXYS IXDN614SI, which can source and sink up to 14 A of current. This gate driver was chosen after considering other suitable gate drivers that we have used at Megahertz in Class E/EF topologies previously, with a comparison of technical specifications, as shown in Table VII. The IXYS gate driver has the highest sink/source current capability amongst gate drivers in this class. With soft-switched circuits, the power device, Q, has the most efficient mode of operation when it does not reverse conduct or hard-switch [1], [30]. The most fair comparison is to drive the gate of Q with the duty cycle, which gives the power stage the highest efficiency for the HSW gate profile, as matching gate signals with different turn-ON and turn-OFF slopes is not straightforward.

TABLE VII
CANDIDATE COMMERCIAL GATE DRIVERS

Gate drivers	Sink/source current [A]	Rise/fall time [ns]	C/V (nF/V)
IXYS IXDN614SI	14/14	25/18	15/18
Infineon 1EDN7512G	4/8	6.5/4.5	1.8/12
TI UCC27512	4/8	8/7	1.8/12

Fig. 22(d) shows the comparison of the gate profiles used between the RGD and the HSW trials. These waveforms are taken with the power stage not active to measure the gate voltage without any C_{gd}^{Q} effects. The two different HSW gate profiles are with no gate resistor (IXYS0) and with a 1 Ω gate resistor (IXYS1). The gate profile closest to resembling an ideal square waveform is the IXYS0. The duty cycle, which produces the most efficient performance for Q with IXYS0, coincides with the effective duty cycle of the RGD when measured between crossing points at the nominal threshold voltage, V_{th} of Q, which indicates that the effective turn-ON portion of the switching period has been successfully matched. With the input current, i_{Lrfc}, the output branch current, i_{Ls}, and the drain voltage, v_{DS}^{Q}, matched, we can safely conclude that the power stage has also been fully matched. Consequently, the power loss in the passives, L_{rfc}, L_s, and C_s, and the attributed parasitics are also the same among the two trials. Since the current through L_{rfc} and L_s is matched, this means that the current flowing through the switching network $(Q \parallel C_p)$ is matched. The mean value of the drain voltage of Q over the switching period, $\overline{v_{DS}^{Q}}$, relates to the input dc voltage, V_{in}, to the inverter (assuming equal losses on the input choke). This means that the metric v_{DS}^{Q}/V_{in} shows how closely matched the effective off-period of Q is. Any differences in the dc input current I_{Lrfc} is then attributed to the losses in Q due to the different gate driving profile.

The work in [31] and [32] shows the correlation between conducted electromagnetic interference (EMI) and the voltage waveform of the switching node in an HSW circuit due to the current flowing in the commutation loop. For the HSW gate driver, this is true as pulses of current are taken by the gate driver. On the other hand, the input choke in the RGD inherently acts as a filter for conducted EMI. The radiated EMI from the gate driver is correlated to the switching waveform, which is the gate waveform. The fast Fourier transforms (FFTs) of the gate waveforms are taken up to the 29th harmonic (196.6 MHz) and shown in Fig. 22(e) where it can be seen that the RGD has a significantly lower magnitude of higher order harmonics compared to the HSW.

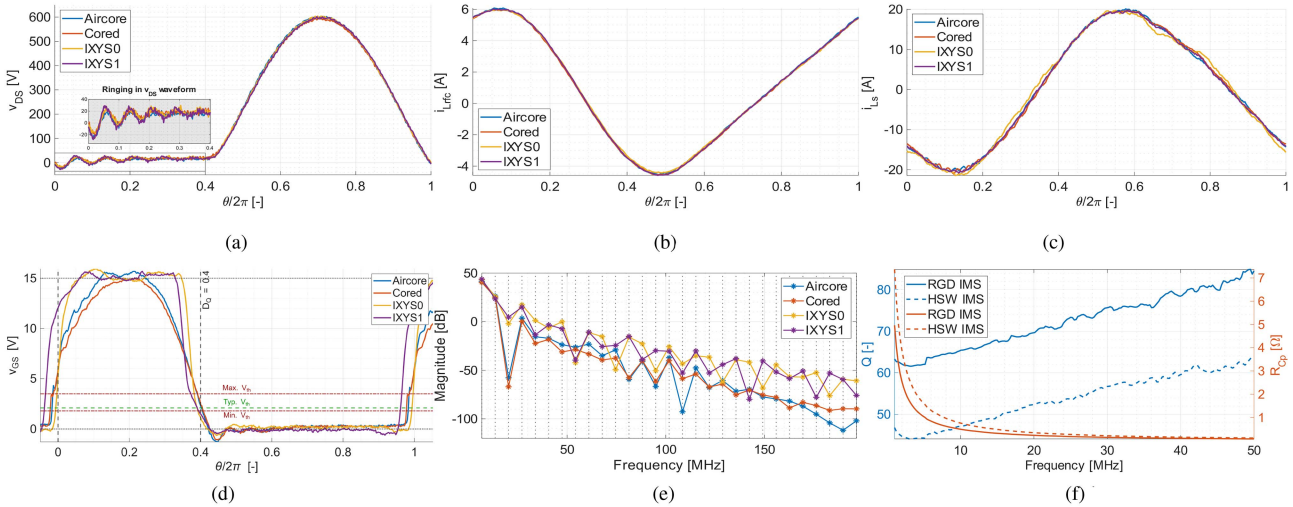

Fig. 22. Waveform comparison between the power stages for the Air-core RGD, Cored RGD, IXYS HSW (with 0 Ω gate resistor), and IXYS HSW (with 1 Ω gate resistor). (a) Drain voltage waveforms with equal peak voltage reached. The amplitude of the ringing during turn-ON of the device on the RGD test is lower. (b) Input current through finite choke showing similar AC ripple and slightly different DC component, which relates to power loss. (c) Current through the resonant tank L_sC_s with a peak of 20 A. (d) Gate voltage waveforms, showing same effective duty cycle of 40% at 6.78 MHz. (e) v_{GS}^{Q} waveform FFT results for the first 29 harmonics of the signal (≈200 MHz) for each gate signal profile. (f) Q factor and ESR measurements of the drain node to ground parasitic capacitance in the IMS boards for the RGD and HSW. (a) Drain voltage. (b) Input current. (c) Output branch current. (d) Gate voltage. (e) Gate FFT. (f) IMS parasitic.

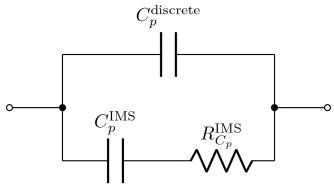

Fig. 23. Equivalent network of C_p, which consists of a high-Q discrete capacitor with the lossy IMS dielectric capacitance in parallel. The lossy capacitor is modeled as a series RC element.

F. Power Loss Comparison

Comparing the power loss in the power device is crucial as it gives a metric of comparison on device performance due to the gate signal profile. The power device loss computation can be done by removing all the known components of loss in the system and isolating the unknown components. The input power to the power stage can be broken down into the following components:

$$P_{\text{in}} = P_{Lrfc} + P_{Ls} + P_{Cs} + P_{Cp}^{\text{discrete}} + P_{Cp}^{\text{IMS}} + P_Q. \quad (64)$$

The losses in C_p are divided into two parts due to the paths for current to flow (i.e., the high-Q discrete C0G capacitors and the lossy IMS dielectric), as shown in Fig. 23. The loss calculation on L_{rfc}, L_s, and C_s is straightforward, but differentiating between the power loss through C_p and Q requires a more analytical approach. The values of the total capacitance in the network, $C_p^{\text{total}} = C_p^{\text{discrete}} + C_p^{\text{IMS}}$, are matched to achieve the same tuning. The rms current flowing through the network is the same given that the voltage across is the same, v_{DS}^{Q}, and the resistance R_{C_p} is negligible compared to the reactance of $X_{C_p^{\text{discrete}}}$ and $X_{C_p^{\text{IMS}}}$. The loss in the parasitic resistance of the IMS is then calculated, based on the same assumptions

$$P_{Cp}^{\text{IMS}} = \left(\frac{C_p^{\text{IMS}}}{C_p^{\text{total}}}\right)^2 \cdot (i_{Cp}^{\text{rms}})^2 \cdot R_{C_p} \quad (65)$$

where i_{Cp}^{rms} is the current flowing into the C_p network. The ratio of the power losses in the IMS is given by

$$\Delta_{j,k}^{\text{IMS}} = \frac{P_{Cp,j}^{\text{IMS}}}{P_{Cp,k}^{\text{IMS}}} = \frac{R_{C_p,j}(C_{p,j}^{\text{IMS}})^2}{R_{C_p,k}(C_{p,k}^{\text{IMS}})^2} = \frac{\text{Q}_k^{\text{IMS}} C_{p,j}^{\text{IMS}} \cdot \alpha}{\text{Q}_j^{\text{IMS}} C_{p,k}^{\text{IMS}}} \quad (66)$$

where Δ^{IMS} is the difference factor in the loss of the two IMS boards, Q^{IMS} is the quality factor of the IMS dielectric, j and k are the identification indices of the IMS board used, and α is the slack factor introduced to compensate for uncertainties in obtaining the quality factors. The loss difference between two power stages is compared, and subtracting the equal loss components within the circuit and substituting in (66) give

$$P_{\text{in},1} - P_{\text{in},2} = P_{Q,1} - P_{Q,2} + (1 - \Delta_{2,1}^{\text{IMS}}) \cdot P_{Cp,1}^{\text{IMS}}. \quad (67)$$

Fig. 22(f) shows the Q factors and equivalent series resistance (ESR) of the two IMS parasitic capacitances measured using a Keysight E4990 A Impedance Analyser with the 42941 A Probe Kit. Both IMS have similar capacitance, which are close to the expected value for the parameters of the dielectric (Ventec VT-4B7), with the relative permittivity being $\epsilon_r = 4.8$, effective area of the node, $A_e = 13.55\ \text{mm}^2$, and thickness of the dielectric being 150 µm. The loss tangent specified by the manufacturer also gives a Q-factor estimation at 1 MHz [33]. Both parameters are calculated as

$$C_p^{\text{IMS}} = \frac{\epsilon_0 \epsilon_r A_e}{d} = 384\text{pF} \quad (68)$$

$$\text{Q factor} = \frac{1}{\tan\delta} = 62.5. \quad (69)$$

TABLE VIII
MEASURED PARAMETERS FROM EXPERIMENTAL TESTS

Parameters	Air-core RGD	Cored RGD	IXYS [0 Ω]	IXYS [1 Ω]	Units
V_{in} (Power stage)	212.5	211.9	212.5	210.4	V
I_{Lrfc} (Power stage)	0.36	0.36	0.45	0.46	A
V_{dd} (Gate driver)	5	4.5	15	15	V
I_{Lin} (Gate driver)	0.16	0.12	0.31	0.31	A
v_{DS}^{Q}/V_{in}	2.83	2.82	2.84	2.86	–
Power stage power	76.5	76.3	95.6	96.8	W
Gate driver power	0.8	0.54	4.65	4.65	W

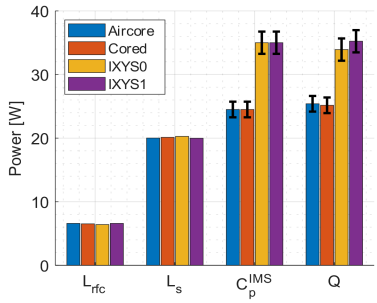

Fig. 24. Power breakdown estimations from measured parameters on the board along with error bars on the IMS and power device (Q) losses to include any worst case potential uncertainty in measurement.

It can be seen that the from the difference in the quality factors of the IMS, the losses on the dielectric have a factor of 0.7 on the RGD. With the slack factor α chosen to be 0.9 and 1.1, representing the maximum change of 5% uncertainty in the Q factor measurements that each IMS could present, the difference factor, Δ_P^{IMS}, is calculated to be between 0.56 and 0.84.

Table VIII shows the input parameters of the power stage and gate driving circuit. It can be seen that the power stages of RGD and HSW have approximately a 20 W difference, which is attributed to the difference in the power loss in Q and P_{Cp}^{IMS}. Using the current waveforms through L_{rfc} and L_s, the loss component from those can be estimated by calculating the rms current through each of their associated parasitic resistance. The loss through the discrete High-Q C0G capacitors used in C_s and C_p is not considered in this calculation. The reference value of the loss through the IMS capacitance (before adding the uncertainty factor) is estimated from the Q factor measured and the current through the capacitance from LTspice simulations. The current through that branch cannot be measured experimentally in this type of circuit at this high operating frequency, as the insertion inductance would load and detune the circuit. The simulated power loss quantities are $P_{Cp,\text{RGD}}^{\text{IMS}} = 24.8$ W and $P_{Cp,\text{HSW}}^{\text{IMS}} = 35$ W, which represent $\Delta_P^{\text{IMS}} = 0.7$ as expected.

Fig. 24 shows the power-stage loss breakdown, including the uncertainty error bars, according to the analysis above. Even though the chosen 5% error margin for the IMS quality factor is unrealistically high, the RGD always achieves lower losses on Q compared to the HSW counterparts. Numerically, the loss

Fig. 25. Thermal camera images of the RGD and HSW experiments with details on the power devices and the gate drivers. (a) The power device driven by the RGD gate signal profile reaches a steady-state temperature of 71.6 °C after 5 min of running. (b) The power device driven by the HSW gate signal profile surpasses 100 °C during transient, at which point the power stage is shut-down before reaching steady-stage. (c) The IXYS gate driver when driving the device Q at 6.78 MHz at a duty cycle of 0.4 reaches a steady-state temperature of 35.1 °C. (a) RGD Q. (b) IXYS Q. (c) IXYS gate driver.

difference in the power device with the slack factor is between

$$5.54\,\text{W} < \left[P_{Q,\text{RGD}} - P_{Q,\text{HSW}}\right] < 13.05\,\text{W}. \tag{70}$$

This shows that beyond the uncertainty of the measurements, there is an improvement in the power device drain efficiency when driven by the RGD gate waveform shape. This corroborates with the thermal measurements of the power stages. With identical cooling for the two IMS boards, and the thermal resistance network from the junction to ambient kept as similar as possible, the power stage with the RGD manages to operate in steady-state at the maximum power, whereas in the HSW trials, the device exceeded 100 °C even before reaching steady-stage. Fig. 25(a) and (b) shows the thermal data for both power stages. In addition, in Fig. 25(c), it can be seen that with the power stage switched OFF, the HSW gate driver still produces a lot of heat, which correlates to the high power consumption and inefficiency of the gate driver.

VI. DISCUSSION AND FUTURE WORK

The results from the experimental section show that, as expected, the RGD utilizes less power to drive the gate of the SiC power device at 6.78 MHz (i.e., 0.54 W by the RGD compared to the 4.65 W by the HSW gate driver, which represents 11.6% of the power). However, the power loss in Q is also lower when driven by the RGD gate profile, which is not accurately captured in simulation and not obvious or expected. Conventionally, a squarer gate profile is preferred as it lowers switching loss [34]. Indeed, previous research on driving SiC devices shows that waveform shaping during the turn-ON transition of the device reduces ringing on the drain voltage effectively quietening device operation [35], [36], [37] but increases switching loss. In those HSW, kHz examples, the high frequency ringing fully decays in a negligible portion of the switching period. The reduced ringing produces insignificant change in the conduction loss and is mainly reduced to maximize device rating utilization and improve electromagnetic compatibility.

With soft-switched circuits, on the other hand, the switching loss is no longer as significant, and slowing the device during turn ON and turn OFF does not increase switching losses. However, for multi-MHz systems, the ringing on the drain persists for a significant portion during conduction within a period, which

would correlate to power loss during the device's turn-ON period. This suggests that unlike their HSW counterparts, quietening the device in a soft-switched converter yields benefits to the drain efficiency of the device.

In this work, the gate driving profile for the RGD was tested with only a single design. However, the waveform can be shaped in different ways by redefining the cost function, (52), at the design stage. This can be tested in future work to observe how different gate profiles affect power device losses. Conventional waveform shaping circuits, such as in [37], can be used if the frequency of the power stage is low enough. However, producing waveforms with sufficient time-resolution for MHz operation (147.5 ns switching period in this case) is not trivial using existing methods. This, however, is not a limitation of the approach presented in this work, and high switching frequencies can easily be achieved.

The work in this article is carried out for a single frequency and single duty cycle. Liu et al.[21] used a technique on a similar type of gate driver where the input voltage is an actively controlled variable during operation to adjust the gate driver behavior. This can be put into the analytical model in Section II to find the best combination of passives and dynamic input voltage and duty cycle, D_S, to achieve a large range of possible operating points.

An extension to this work to improve its applicability and robustness in real-world scenarios would be to modify the topology to achieve isolated gate driving with the possibility of a negative voltage for turn-OFF. This has been briefly looked at in Appendix A. Furthermore, short circuit protection should be investigated in the same way as it is approached in conventional gate drivers. This is a commonly desired feature, which improves reliability and reduces cascaded faults. Experimental work to validate the improvements these provide is beyond the scope of this article.

VII. Conclusion

In this work, we demonstrate a fully analytical method of waveform shape design in a Class Φ RGD. A simplified circuit is used to generate initial solutions to seed an iterative solver run on a more detailed model. The full state-space model incorporates gate parasitics to enhance the accuracy of the design. When this design methodology is tested on a 6.78 MHz Class E power stage with a 30 A SiC device, the device switches as expected and the gate driving power requirements are significantly lower than those of an off-the-shelf high-speed, high-current gate driver. The following are the specific novelties and contributions that we have introduced to the literature.

1) Generalized design method for any duty cycle (compared to a fixed 50%) for such a topology.
2) Exact state-space analysis with closed form design equations, compared to simple first-order approximate solution existing in literature.
3) Included power device gate parasitics to the design procedure, which affect the operation significantly at multi-MHz frequencies (L_g, R_g).
4) Proposed circuit topology changes to absorb nonlinearities (C_{pg}).

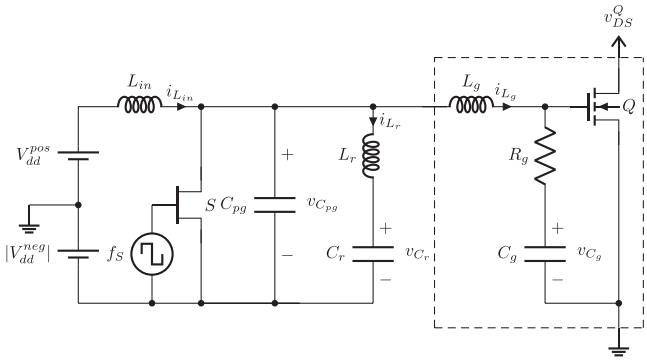

Fig. 26. Circuit diagram of a candidate Class Φ gate driver with split supplies to allow driving with both positive and negative voltages with respect to the Kelvin source of the power device.

5) Comprehensive comparison with the best-in-class, state-of-the-art conventional gate driver.
6) Tested in real-world high-power, high-frequency inverter, with a deliberately challenging power SiC device of choice to stress test the gate driver capabilities.
7) Included custom magnetics design for further efficiency improvement.

The Class Φ RGD proposed in this work also provides benefits, such as quietening the operation of the SiC device (reduced drain voltage ringing) and a single, lower input voltage supply to the gate driver (5 V compared to 15 V). Furthermore, the power device operates more efficiently with the gate profile from the RGD than with the off-the-shelf driver and hence shows significant promise for operating SiC devices at MHz in resonant converters.

Appendix A
Isolated Gate Driving with Negative Voltage

An isolated gate driver allows driving the power device referenced to the Kelvin source to improve performance in high $\mathrm{d}i/\mathrm{d}t$ applications. In addition, there are instances when the gate of the power device has to be driven with a negative voltage during turn-OFF to improve noise immunity, and the topology, as shown in Fig. A1, is a candidate solution for these. In this work, we do not delve further into experimental validation of this modified topology, which remains as future work. It is to be noted that the entire design flow in this isolated topology with split supplies has to be done by considering the effective input voltage ($|V_{dd}^{\text{neg}}| + V_{dd}^{\text{pos}}$) and the effective gate voltage swing required. These following steps have been performed to transform the design in Section IV-B for the one in Fig. A1.

1) Calculate the V_{in}, which would be required in Fig. 6 for the desired effective gate voltage swing.
   a) In this case, the operational gate-source voltage is chosen as −3/+15 V, which means that the swing required is 18 V. The effective input voltage is therefore 6 V.
2) Decide the split supplies to achieve the correct dc offset in the gate signal.
   a) The negative peak of the gate voltage is −3 V. which means that V_{dd}^{neg} is set as that voltage.

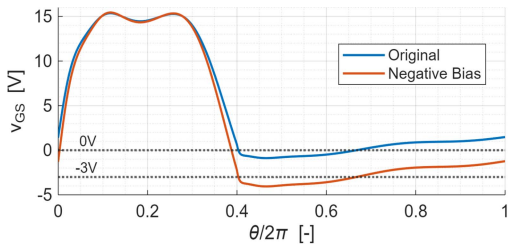

Fig. 27. Gate profiles of the original design for a swing from 0 to 15 V (blue) and the profile from the transformed topology in Fig. 26 to produce a swing from −3 to 15 V (orange).

b) The positive voltage source, V_{dd}^{pos}, is the remainder of the calculated input voltage, which is 3 V.

The gate profile of the original design (swing from 0 to 15 V) is transformed using the abovementioned method to produce a swing from −3 to +15 V. Fig. 27 shows the gate waveforms achieved. It is to be noted that S has to be driven with an isolated supply so that its gate signal is shifted by V_{dd}^{neg}.

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