Characterization and Minimization of Commutation Loop Inductance in Reconfigurable Battery Systems Using Magnetically Coupled Auxiliary Loops

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***Abstract*—This study presents a novel analysis of the commutation loop inductance in reconfigurable battery systems based on a half-bridge topology. The investigation considers variations in the number of series connected battery cells before being linked of the half-bridge. Based on these findings, three methods are explored to minimize loop inductance: 1) introducing magnetically coupled conductor/auxiliary loops to create a freewheeling path for the magnetization current, with parts of the auxiliary loop formed by sections of the power loop to achieve near-ideal coupling, 2) employing a solid copper shield as an alternative to auxiliary loops, and 3) optimizing the physical arrangement of the series connected battery cells. Experimental results show a reduction in loop inductance of up to 59% using the magnetically coupled auxiliary loop, and up to 66% with the solid copper shield.**

***Index Terms*—Half-bridge, loop inductance, reconfigurable battery systems (RBSs).**

I. Introduction

AN INCREASINGLY discussed approach to increase the efficiency of the electric drivetrain of battery electric vehicles is the utilization of reconfigurable battery systems (RBSs) to form a cascaded multilevel inverter (MLI). Research shows that MLIs have equal or even higher efficiency than conventional voltage source inverters with the MOSFETs based on silicon carbide (SiC) [1], [2], [3], [4], [5].

A prevalent challenge in power electronic systems, particularly in dc/dc converters, is the reduction in efficiency due to parasitic stray inductance. The overall efficiency of these systems is influenced by multiple factors, including transistor conduction and switching losses, PCB copper losses, as well as losses in diodes and inductors [6]. Switching losses, a significant contributor in modern converters, can be categorized into gate-drive, reverse-recovery, dead-time, and crossover losses, among others [7]. Crossover losses primarily stem from two sources: 1) the intrinsic device capacitances of the MOSFET and 2) parasitic circuit inductances, such as loop, common-source, and gate inductances [8].

The impact of these inductances on switching losses—and consequently on overall efficiency—varies significantly based on several parameters as follows [9], [10], [11], [12], [13]

1) The magnitude of the loop inductance.
2) The amplitude of the load current.
3) The switching frequency.

At higher switching frequencies, switching losses tend to dominate due to the increased frequency of voltage and current overlap during switching transitions, particularly in hard-switching designs. Conversely, at lower frequencies, conduction losses or inductor-related losses may become more significant. As an example, the work done in [6] shows that the SiC MOSFET switching losses account for 30.7% of the total losses at a switching frequency of 200 kHz.

One strategy to reduce the loop inductance is to reduce the enclosed area of the half-bridge and dc-link capacitor. In [14], it is shown that using a vertical lattice loop structure, which effectively reduces the enclosed area, halves the gate and power loop inductance. Similarly, Sun et al. [15] compared different printed circuit board (PCB) layouts and finds that the proposed design achieves a 44% reduction in power loop inductance compared to a conventional layout, which allowed to increase the maximum power capacity by 14%. Reusch et al. [16] performed a simulation-based investigation into the magnetic field intensity of layouts with and without a shield layer, demonstrating that the shield reduces field intensity and consequently decreases inductance by 25%. Measurements show an increase in efficiency of 1 percentage point (p.p.) at partial load. This suggests that inductance-related switching losses contribute approximately 40% of the total losses, assuming a linear relationship between inductance-related switching losses and inductance. Reusch et al. [17] extended their work by analyzing a conventional lateral loop with shield, a conventional vertical loop and an optimized vertical design for a Gallium-Nitride converter, evaluating them in terms of parasitic inductance, power losses, and efficiency. One interesting finding is that the lateral power loop with shield has higher losses than the conventional vertical power loop when both have the same loop inductance. This can be explained by additional losses in the shield layer (resistive

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losses due to eddy currents). Finally, the results for the optimized vertical design show that the optimized layout has a full load efficiency improvement of up to 1 p p. while the inductance has been lowered by 62%. Based on their specific application results, inductance-related switching losses account for about 12.9% of the total losses. Of particular interest is the study by Lim et al. [18], which examines the effect of a shield on a system-on-inductor substrate. Due to the inductors high magnetic permeability, the power loop inductance is significantly amplified. To mitigate this effect, a shield is placed between the system and the inductor, reducing the effective loop inductance from 0.74 to 0.17 nH and improving efficiency by up to 4 p p. under full load current conditions. These findings indicate that inductance-related switching losses represent roughly 32.2% of the total losses. The study by Moorthy et al. [19] achieves a reduction in loop inductance and voltage overshoot in a 135 kW SiC inverter by optimizing the busbar layout and incorporating decoupling capacitors. This approach results in a 42% decrease in loop inductance and up to a 7% reduction in voltage overshoot. Min et al. [20] proposed a 3-D lattice structure of the power path to achieve a higher flux cancellation. Results show a reduction in the switching energy of 9 p p. compared to the conventional structure. Zhao et al. [21] proposed an ultracompact gate driver for a 211 kW three-level inverter. Among others, they optimize the commutation path by combining PCB layers for low commutation inductance and busbars for low dc resistance. Meade et al. [7] demonstrated that, in their application, switching losses are reduced by approximately 75% when a wire-bond-free MOSFET package is used instead of discrete power devices. This is due to the much lower package inductance. This increases the overall system efficiency by 15–20 pp, indicating that inductance-related switching are estimated to contribute between 15% and 20% of the total losses. Hashimoto et al. [22] reported a 20% reduction in power losses achieved through a 44% decrease in parasitic inductance. This reduction was realized by mounting the dc-link capacitor directly on top of the half-bridge. Other studies that demonstrate reduced stray inductance through optimized layout and package designs include [23], [24], [25], [26], [27].

Summarizing the reviewed literature shows that various approaches have achieved reductions in loop inductance between 25% and 77% when compared to conventional designs. These reductions are directly linked to improvements in efficiency, which range from 1 to 20 pp. By combining the observed reductions in inductance with the corresponding efficiency improvements, the proportion of inductance-related switching losses within the overall losses can be estimated. This share has been found to lie within the range of 12.9%–40%. These findings clearly highlight the significant influence of circuit inductance on inverter performance and underline the importance of keeping it as low as possible in practical designs.

The research mentioned previously mostly focuses on inverters, where the entire system is integrated onto the PCB, allowing significant changes in stray inductance through modifications to the PCB layout. However, in RBS, altering the PCB layout results in only a minor change in stray inductance, as most of the spanned area (and inductance) results from the battery cell itself. The parasitic inductance is heavily influenced by the battery cells internal structure and casing. For cylindrical battery cells, this inductance typically falls within the range of a few hundred nanohenries. According to Landinger et al. [28], the parasitic inductance of a 2.6 Ah 18 650 cylindrical battery cell can be divided into three components, with the largest contribution, approximately 130–140 nH, originating from the current collector. In contrast, studies on prismatic battery cells have identified significantly lower parasitic inductance values, despite their larger physical size. For instance, Dai et al. [29] analyzed a 40 Ah prismatic battery cell across varying temperatures and reported a parasitic inductance ranging from 45 to 47 nH for a single battery cell. Similarly, Saidani et al. [30] observed a parasitic inductance of 80 nH for a 20 Ah hardcase battery cell. While it is difficult to get confirmation from the battery industry, it seems clear that the reduced inductance in prismatic battery cells can largely be attributed to their aluminum casings [31], [32], which have a relative permeability close to 1. In contrast, cylindrical battery cells often feature (nickel plated) steel casings [32], [33], [34], with relative permeabilities ranging from hundreds to thousands. Therefore, cylindrical battery cells exhibit higher parasitic inductance despite their smaller physical dimensions.

Nearly all the research mentioned focuses either on inverter systems implemented on a PCB or exclusively on the parasitic inductance of standalone battery cells. To the best of our knowledge, no studies have explored the parasitic loop inductance in RBS, which integrate a battery cell with a half-bridge implemented on a PCB. Moreover, no methods have been reported for minimizing stray inductance in such reconfigurable systems. Thus, this article presents a novel investigation for reducing commutation inductance in RBS. The key contributions of this work include the following.

1) Measurement of the commutation loop inductance in RBS, considering a varying number of series connected battery cells to achieve higher module voltages, as commonly practiced in cascaded MLIs.
2) Application and experimental validation of both existing and newly proposed methods for reducing inductance.

II. Methodology

A simplified circuit diagram of an RBS using a single battery cell linked to a half-bridge is depicted in Fig. 1(a). Here, Q_{hs} and Q_{ls} denote the high- and low-side switch, and U_{cell} represents the terminal voltage of the battery cell. Instead of using a half-bridge, a full-bridge [see Fig. 1(b)] or any other switching topologies, e.g., BM3 [35], M2SPC [36], or PECIN [37], can be utilized to form an RBS.

The RBS is not limited to having only one battery cell as energy storage medium but it can be combination of series and parallel connected battery cells, forming a battery module to achieve a higher output voltage or current.

In Fig. 1(c), a PCB that incorporates a half-bridge as switching topology is mounted on top of the prismatic battery cell. The aluminum casing from the prismatic battery cell is removed, giving access to the internal structure of the battery cell and showing the jelly roll, as well as the anode and the cathode current collector. In addition, the simplified circuit diagram

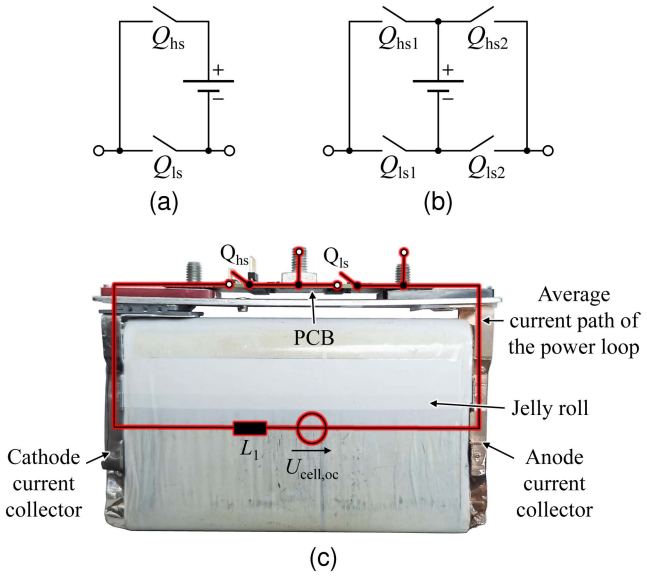

Fig. 1. Formation of an RBS using a conventional battery cell with a dedicated switching topology. (a) Half-bridge. (b) Full-bridge. (c) Shows the side view of an prismatic battery cell without aluminum casing with a PCB on top. Superimposed is the simplified circuit diagram of the half-bridge.

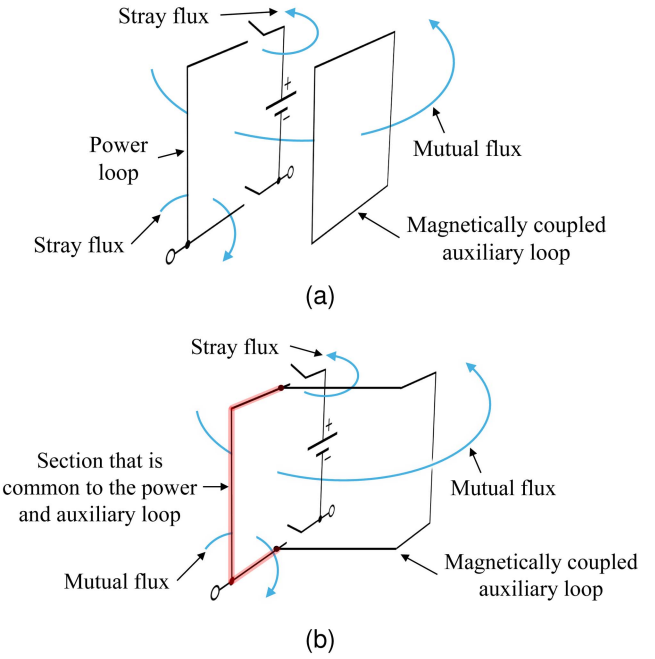

Fig. 2. Illustration of (a) a magnetically coupled auxiliary loop but electrically isolated from the power loop and (b) a magnetically coupled auxiliary loop where parts of the auxiliary loop (highlighted in red) is formed by using a section of the power loop.

of the half-bridge following the average current path (power loop) is superimposed. Here, $U_{\mathrm{cell,oc}}$ represents the open-circuit voltage of the battery cell, and L_1 the loop inductance of the power loop.

Lowering the parasitic loop inductance can be done in several ways as follows.

1) Remove nearby components and materials with high magnetic permeability from the loop.
2) Insert magnetically coupled auxiliary/conductor loops and shields. This provides a freewheel path for the magnetization current and allows for flux cancellation, which translates into a reduction in parasitic inductance.
3) Rearrange the associated components of the loop as well as the PCB layout to reduce the effective enclosed area or to achieve flux cancellation.

The last two methods are investigated in this work.

A. Implementing a Magnetically Coupled Auxiliary Loop

One method to reduce the effective inductance is to utilize the transformer principle, providing a freewheeling path for the magnetization current. By adding a magnetically coupled auxiliary loop as close as possible to the power loop, a transformer is formed. The auxiliary loop serves as the secondary side of the transformer. An illustration of such a configuration is shown in Fig. 2(a). The power and auxiliary loop share the mutual flux, which translates into a mutual inductance. Shorting the secondary side results in a low impedance freewheeling path for the magnetization current.

An interesting feature of this method is that the magnetically coupled auxiliary loop can be electrically connected to the power loop at two points, provided these points share the same electrical potential. This enables a portion of the power loop to serve as part of the magnetically coupled auxiliary loop. The underlying principle is illustrated in Fig. 2(b), where the red-highlighted section is common to both the power loop and the auxiliary loop. Doing so offers two main benefits compared to the approach shown in Fig. 2(a): 1) it reduces the amount of conductive material required to form the magnetically coupled auxiliary loop and 2) the portion of the magnetically coupled auxiliary loop formed using the power loop achieves an ideal coupling factor, as both loops share the same physical current-carrying conductor.

As previously noted, achieving high coupling factors requires placing the magnetically coupled auxiliary loop as close as possible to the power loop. Ideally, this loop is integrated directly into the jelly roll or casing of the battery cell during the manufacturing process. Fig. 3(a) depicts the front view of a prismatic battery cell with the focus on the jelly roll structure, while Fig. 3(b) presents one possible configuration in which the entire anode copper foil of the jelly roll, the anode current collector, the anode terminal, and the PCB trace from anode terminal to the source of the low-side MOSFET are utilized as a common section for both the power loop and the auxiliary loop. To close the magnetically coupled auxiliary loop, a copper wire is connected to the anode copper foil on the cathode (left) side, as shown in Fig. 3(b). This copper wire is then routed to the PCB, where it connects to a dedicated PCB trace positioned in close proximity to the PCB power path. The opposite end of the PCB trace is connected to the anode terminal (source contact of the low-side MOSFET). In this arrangement, the majority of the magnetically coupled auxiliary loop is formed using the anode current collector and anode copper foil. Care must be taken to

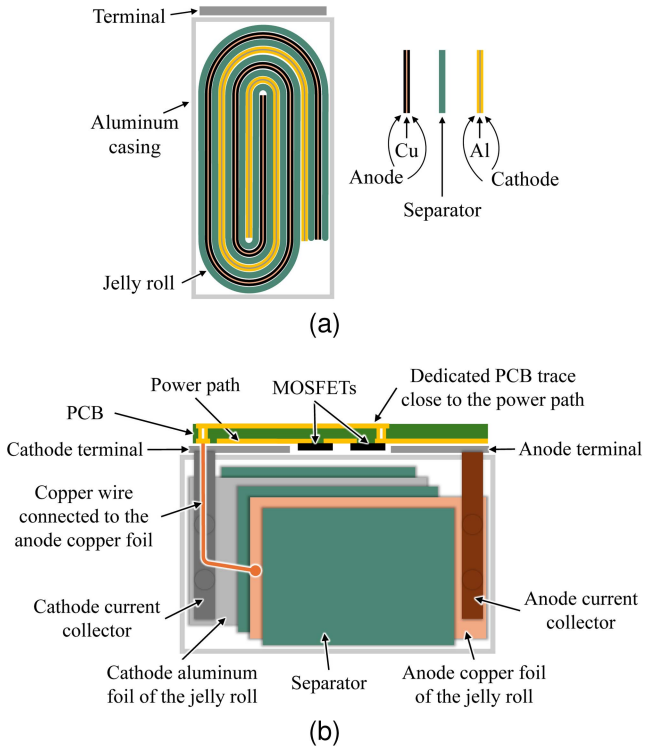

Fig. 3. Structural composition of the prismatic battery cell highlighting the jelly roll. (a) Cross section from the front view and (b) side view. In (b), the connection of the magnetically coupled auxiliary loop to the anode copper foil and to the PCB is shown.

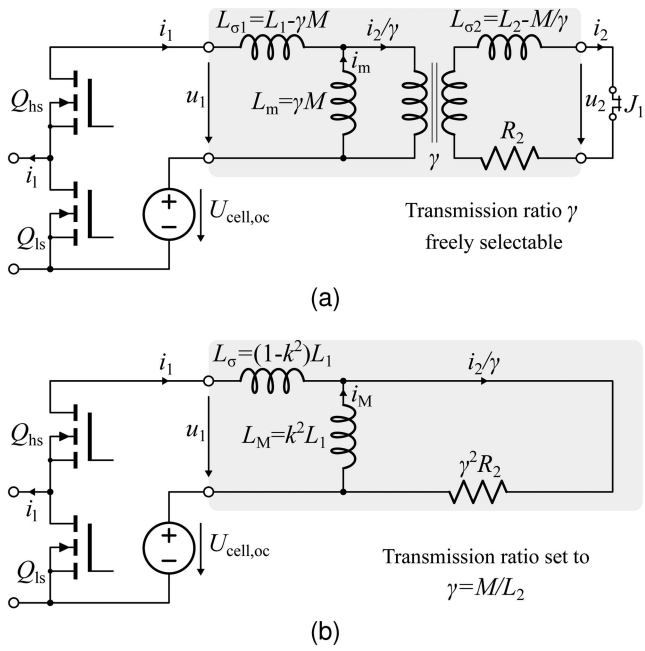

Fig. 4. Schematic representation of the half-bridge with a magnetically coupled auxiliary loop: (a) conventional ECM and (b) inverse Γ-ECM with secondary side transformed to primary side.

ensure that both the conductor and its insulation remain resistant to degradation caused by the battery cells electrolyte. A further improvement involves integrating the entire PCB directly into the battery casing. This leads to a reduced enclosed area of the power loop, resulting in a reduction of the loop inductance.

The magnetic and electric interaction of the power loop and the magnetically coupled auxiliary loop can be represented using an equivalent circuit model (ECM) in a T-shaped (T-ECM) configuration, see Fig. 4(a). The primary inductance $L_1 = L_{\sigma1} + L_\mathrm{m}$ is equal to the loop inductance, L_m is the magnetizing inductance, M the mutual inductance, L_2 is the secondary inductance, $L_{\sigma1}$ and $L_{\sigma2}$ are the primary and secondary leakage inductances, respectively. R_2 is the parasitic resistance of the secondary side. J_1 is a jumper inserted due advantages during measurements. The transmission ratio γ can be arbitrary chosen without affecting the transformer voltages u_1, u_2 or currents i_1, i_2. Typically, γ is set to $\gamma = L_1/L_2$ to closely align the ECM with the physical behavior of voltage, current and flux. However, if the physical representation is of lower priority, the ECM can be simplified. By setting $\gamma = M/L_2$ and introducing the coupling factor

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{1}$$

the diagram shown in Fig. 4(b) is derived [38, pp. 265–271]. The secondary stray inductance becomes zero. Since the secondary quantities u_2 and i_2 are irrelevant, R_2 and J_1 are transformed to the primary side, assuming J_1 is lossless. This results in an ideal transformer with a short-circuited secondary side, effectively eliminating the need for the ideal transformer itself, which is subsequently removed. This representation is commonly used during modeling of induction machines and is called inverse Γ-ECM (Gamma) [39, pp. 143–144]. It should be noted that the magnetic fluxes are no longer accurately represented by this ECM. Instead, they need to be corrected using γ, as highlighted in [40].

It becomes evident from Fig. 4(b), that in the case of no coupling $k = 0$, L_σ equals L_1, and L_m becomes zero. This scenario is equivalent to having no secondary side or to an open-circuit secondary side. Conversely, when ideal coupling exists ($k = 1$), the stray inductance becomes zero and L_M equals L_1. In this case, the apparent commutation loop inductance is zero and the magnetization current i_M has a freewheeling path over the resistance $\gamma^2 R_2$.

At this point, it is important to emphasize that even under the condition of ideal magnetic coupling—that is, when no stray inductance is present and the entire loop inductance is represented by the magnetizing inductance L_M—inductance-related switching losses remain unavoidable. The crucial difference is that these losses no longer occur in the MOSFET itself. Instead, the energy stored in L_M during turn-OFF is dissipated through the parasitic resistance $\gamma^2 R_2$ located in the secondary circuit. In other words, the physical location of the dissipation is altered: the MOSFET is relieved from a significant portion of switching stress. Furthermore, a reduction in inductance-related switching losses is achieved due to 1) less induced voltage that is being applied across the MOSFET during switching and 2) lower current commutation times in the cell current. Especially latter results

in less energy being provided by the cell during switching. Assuming the switching behavior of the MOSFET is strongly inductance-limited [11], the turn-OFF switching losses in accordance with Fig. 4(b) can be expressed as

$$E = \frac{1}{2} L_\sigma i_1^2 \left(1 + \frac{U_{\text{cell,oc}}}{U_{(\text{BR})\text{DSS}} - U_{\text{cell,oc}}}\right) \tag{2}$$

where $U_{(\text{BR})\text{DSS}}$ is the MOSFETs breakdown-voltage. The theoretical maximum percentagewise reduction can than reach up to $U_{\text{cell,oc}}/U_{(\text{BR})\text{DSS}} \cdot 100\%$.

Another opportunity for energy saving is provided by the freewheeling path for the magnetization current. In case of a shorted secondary side, the induced current will decay exponentially over time, governed by the time constant τ. Assuming $R_2 = N_2 R_{2\text{s}}$ and $\gamma = k\frac{N_1}{N_2}$, where N_1 and N_2 represent the number of primary and secondary turns, and $R_{2\text{s}}$ is the resistance of a single turn of the secondary side. The time constant τ can be expressed as

$$\tau = \frac{L_\text{m}}{\gamma^2 R_2} = N_2 \frac{L_1}{R_{2\text{s}}}. \tag{3}$$

The number of primary turns is set to $N_1 = 1$. As evident from (3), τ depends linearly on N_2. When the high-side switch is reactivated after being OFF for a time smaller than 5τ, the magnetization current (and flux) must rebuild from the level it decayed to during the off period. By realizing big time constants or small turn-OFF times, more flux remains and less energy must be provided to remagnetize the inductances at turn-ON.

Instead of using auxiliary loops, a continuous conducting plane (shield) can be utilized [16], [17]. The fundamental principle is the same as for auxiliary loops, but the induced currents (eddy currents) in the shield follow uncontrolled loops that form naturally whereas for auxiliary loops, the path of the current can be precisely controlled. The advantages of a shield compared to auxiliary loops are as follows.

1) Less knowledge about the shape of the magnetic field is required.
2) It's easier to achieve a higher coupling factor.
3) A lower impedance R_2 for the induced current.

Therefore, the magnetic flux will decay slower and less energy during turn-ON to remagnetize the inductance must be provided. The large aluminum casing of the battery cell inherently serves as an effective shield. It significantly reduces the loop inductance generated by the jelly roll and the current collector within the battery cell, as will be shown later.

B. Physical Rotation of the Battery Cells

When two or more battery cells are connected in series before being linked to the switching topology, the enclosed area and consequently the loop inductance increases. However, by arranging the series connected battery cells strategically, the enclosed area can be minimized. Fig. 5 schematically illustrates the half-bridge, where two battery cells connected in series are arranged in two configurations: first, with all positive terminals aligned on the same side, and second, with an alternating physical rotation of 180 °. In addition, the corresponding magnetic

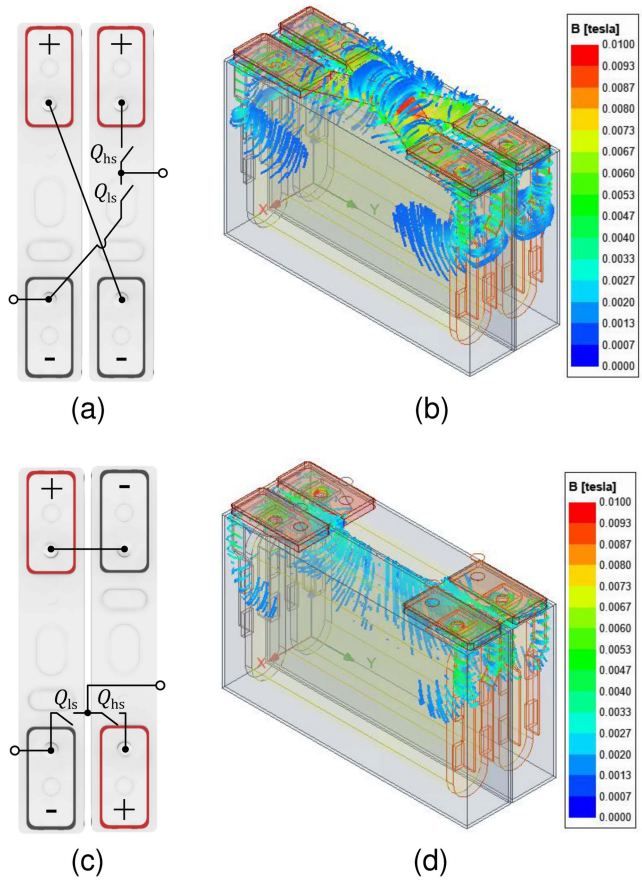

Fig. 5. Schematic representation of the half-bridge (a) without and (c) with physical rotation of two series connected battery cells from top view as well as FEM simulations of the magnetic field (b) without and (d) with physical rotation of the series connected battery cells.

flux is shown. The FEM simulations were performed with Ansys Maxwell at an excitation frequency of 1 MHz.

When all positive terminals are aligned on the same side, the magnetic flux in Fig. 5(b) spreads over a larger area, with more flux lines exhibiting higher amplitudes. The flux lines concentrate particularly on the current collectors of the battery cells and on the diagonal external busbars required for series connection. In contrast, when the battery cells are physically rotated, the magnetic flux becomes more localized, as shown in Fig. 5(d), and fewer flux lines reach high amplitudes. The area between the cell terminals is then almost free of flux.

Inductance extraction with Ansys Q3D at an excitation frequency of 1 MHz yields 59.6 nH for two series connected cells with all positive terminals on the same side. Rotating the cells reduces the inductance to 24.0 nH, corresponding to a decrease of 59.7%. This demonstrates that a favorable geometric arrangement—in this case, a simple physical rotation—can significantly lower the commutation loop inductance of an RBS.

It should be noted that Ansys Q3D accounts for the skin effect but not for eddy currents in the aluminum casing. As a result, the simulated inductance values are higher than those expected in practice.

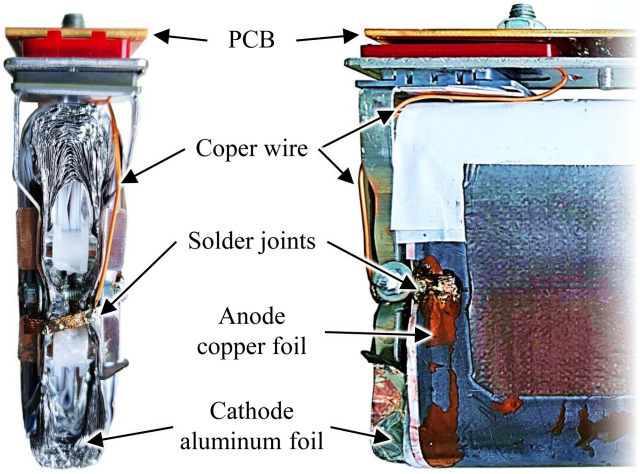

Fig. 6. Laboratory prototype of a battery cell without aluminum casing. A combination of power section and dedicated copper wire is used to build the magnetically coupled auxiliary loop.

III. Experimental Setup

Placing a magnetically coupled auxiliary loop directly adjacent to the power path inside a battery cell requires cutting open the cell casing, making it an irreversible and destructive modification. Since no commercially available battery cell includes this feature, the investigation of loop inductance reduction using an internal magnetically coupled auxiliary loop is therefore restricted to a single cell.

To further investigate the effect of magnetically coupled auxiliary loops under varying number of series connected battery cells, auxiliary loops outside the cell casing are used. For this purpose, dedicated copper traces in a PCB positioned as close as possible to the power path were employed. PCB traces were chosen because of two reasons. First, as the half-bridge topology is implemented on a PCB, it makes sense to use a dedicated copper trace on the same PCB to form the magnetically coupled auxiliary loop. This allows for close alignment of the magnetically coupled auxiliary loop on the power loop, which increases magnetic coupling. The second reason is that PCB copper traces are fixed in their geometry, which ensures highly reproducible results.

The following sections describe the experimental setup for 1) the single battery cell with an internal auxiliary loop and 2) the PCB prototypes when varying the numbers of series connected cells. Finally, the complete measurement setup is presented.

A. Battery Cell With Internal Magnetically Coupled Auxiliary Loop

To assess the effectiveness of a magnetically coupled auxiliary loop that 1) is placed directly alongside the battery cells power path (e.g., jelly roll and current collector) and 2) utilizes a section of this power path to form the magnetically coupled auxiliary loop, the aluminum casing of a battery cell is cut open on the top side and subsequently removed. The upper part of the casing, however, is left in place to provide sufficient mechanical stability for the jelly roll, the current collectors, and the terminals.

The magnetically coupled auxiliary loop is then formed. The elements shared by both the power loop and the magnetically coupled auxiliary loop include the following.

1) The anode terminal.
2) The anode current collector.
3) The anode copper foil.

To complete the magnetically coupled auxiliary loop, a copper wire is connected to the anode copper foil on the cathode side. This wire is then routed along the cathode current collector and beneath the cathode terminal toward the drain contact of the high-side MOSFET, where the opposite end of the wire is soldered. Special attention is given to routing process to ensure that the copper wire remains as close as possible to the power path, thereby maximizing magnetic coupling. Fig. 6 shows a photo of the laboratory prototype.

B. PCB Prototypes

The following PCB prototypes were constructed, incorporating both the power path and dedicated PCB traces that form the external magnetically coupled auxiliary loop.

1) Prototype A allows to connect a varying number of series connected battery cells without physical rotation. Furthermore, the PCB contains $N_2 = 4$ magnetically coupled auxiliary loops in PCB layer 2 and 3 to form the secondary side.
2) Prototype B allows series connected battery cells to be physically rotated alternatingly. Like prototype A, the PCB contains $N_2 = 4$ auxiliary loops to form the secondary side.
3) Prototype C allows to rotate series connected battery cells, just like prototype B. However, no auxiliary loops but a continuous copper plane over the whole PCB layer 2 and 3 is used to form a shield.

For all prototypes, the number of series connected battery cells n_{ser} is varied before being linked to the half-bridge. To keep the number of PCBs reasonable, prototypes with $n_{\text{ser}} = [1, 2, 3, 6]$ are constructed, resulting in 11 prototypes in total. For $n_{\text{ser}} = 1$, the differentiation between with and without rotation is obsolete. Thus, for $n_{\text{ser}} = 1$, only two prototypes A and C exist. Fig. 7(a)–(c) illustrates the structural layouts of prototypes A, B, and C, shown here for the case of $n_{\text{ser}} = 2$. The PCB consists of four layers. In order to achieve a better coupling factor, an additional PCB has been designed, specifically to capture the flux generated along the battery cells side. Fig. 7(d) illustrates the structural layout of the side PCB containing auxiliary loops while Fig. 7(e) shows the side PCB incorporating a shield. The optimal shape of the auxiliary loops in the side PCB has been determined in preceding experiments by trying different configurations crafted from rigid wire. Together with the auxiliary loops in prototype A and B, the transformers secondary side is completed. The PCB on the side of the battery cell in case of prototype C does not contain auxiliary loops. Instead, the PCB layers are completely poured with copper to form the shield, see Fig. 7(e).

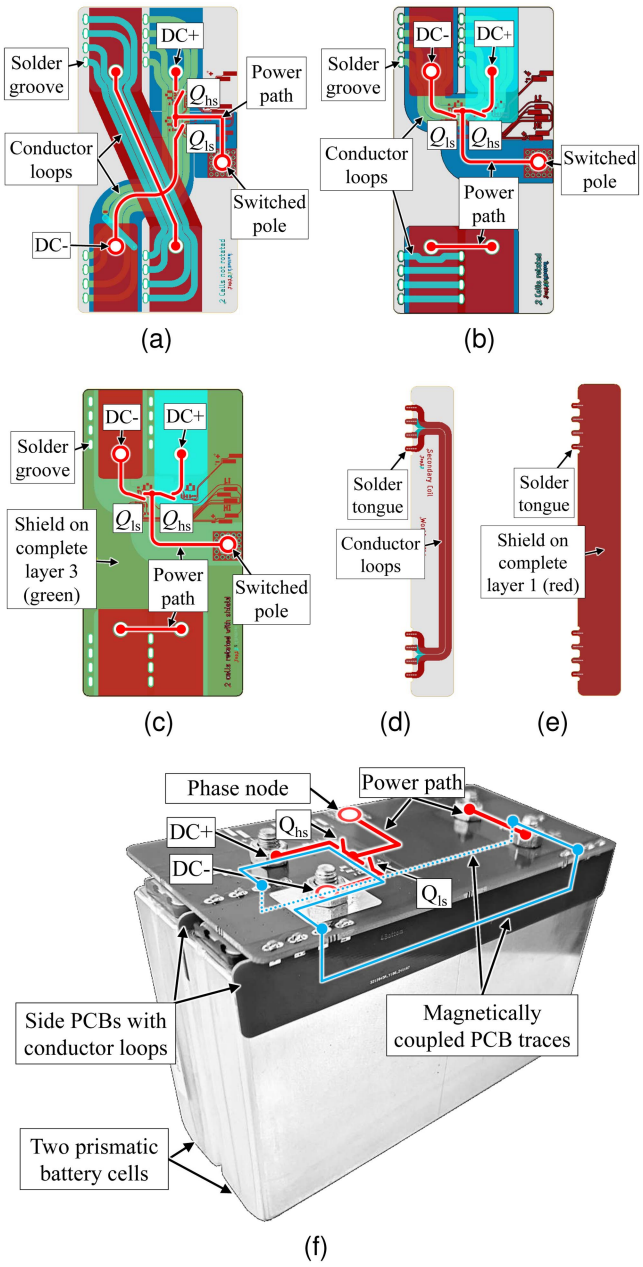

Fig. 7. Structural views of the prototypes with $n_{ser} = 2$. (a) Prototype A. (b) Prototype B. (c) Prototype C. (d) Side PCB with auxiliary loops. (e) Side PCB with shield. (f) Photograph of prototype B with $n_{ser} = 2$ mounted on two prismatic battery cells. The schematic power path is highlighted in red, and the magnetically coupled auxiliary loop is highlighted in blue.

The prototypes A, B, C, and the side PCBs are connected soldering the tongues and grooves, see Fig. 7(f). The secondary side can also be left open by removing the jumper J_1. This leads to the same results as if there were no secondary side at all for prototypes A and B.

C. Measurement Setup

The loop inductance is measured with a frequency response analyzer (FRA). The excitation and sense cables are connected to the drain and source pads of the desoldered high-side switch.

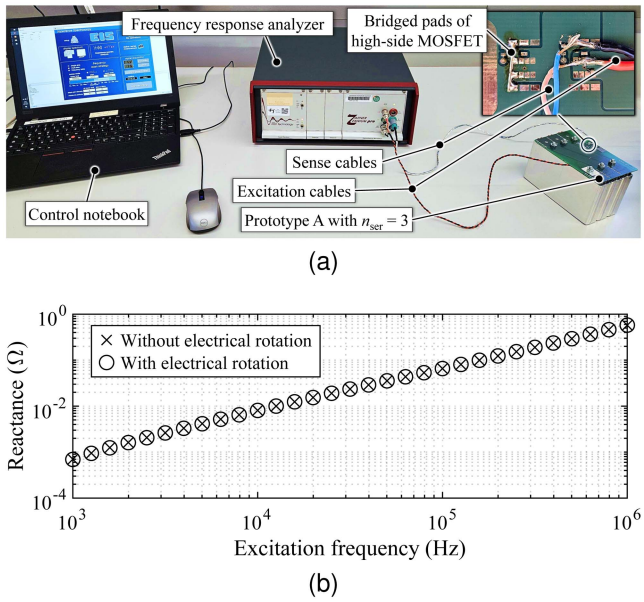

Fig. 8. (a) Picture of the complete test rig. (b) Comparison of the reactive behavior with and without electrical rotation for prototype A, $n_{ser} = 3$ and a controlled voltage of ± 15 V.

The power loop is closed by bridging the pads of the desoldered low-side switch. To measure the inductance without the secondary side, jumper J_1 is removed. When J_1 is closed, the loop inductance with shorted secondary side is measured. A picture of the complete test rig for $n_{ser} = 3$ is shown in Fig. 8(a).

To further obtain the coupling factor, L_2 along with M are measured. k can then be calculated according to (1). The procedure for measuring L_2 is identical to that of L_1, except that the excitation and sense wires are soldered to the pads of the jumper, while the primary side remains open. To measure M, the excitation wires are connected to the drain pads of Q_{ls} with Q_{hs} being bridged, and the sense wires are soldered to the pads of the desoldered jumper.

The utilized FRA *Zahner Zennium Pro* has a maximum controlled voltage of ± 5 V/± 15 V. As the resulting voltage for $n_{ser} = 6$ exceeds this limit, the following method is employed: the series connected battery cells are alternately electrically rotated. Therefore, the voltages of the battery cells are no longer added together; instead, the voltages of the electrically rotated battery cells are subtracted. For example, when $n_{ser} = 6$, three battery cells are electrically rotated. As a result, the measured dc voltage becomes zero when all battery cells exhibit the same state-of-charge. Two preceding measurements for $n_{ser} = 3$, conducted with and without electrical rotation, reveal no noteworthy difference in the reactive behavior, see Fig. 8(b). The reactance is measured by sweeping the excitation frequency from 1 kHz to 1 MHz with 10 measurements per decade. Using the electrical rotation, the resulting voltage for all prototypes is equal to or smaller than the voltage of a single battery cell, enabling the use of the low-voltage measurement range of ± 5 V, which offers the highest precision.

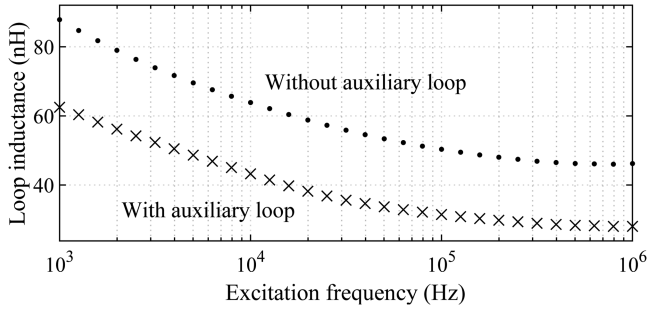

Fig. 9. Measured loop inductance of the half-bridge connected to a single battery cell without aluminum casing, with and without a magnetically coupled auxiliary loop.

IV. Results

A. Battery Cell With Internal Magnetically Coupled Auxiliary Loop

Fig. 9 shows the measured loop inductance for the case where a magnetically coupled auxiliary loop is positioned directly alongside the power path of the battery cell and PCB, with a section of this power path being also used as a part of the magnetically coupled auxiliary loop. For comparison, the loop inductance is also presented for the same configuration when the magnetically coupled auxiliary loop is left open (desoldered at one end). Both measurements were conducted without the aluminum casing of the battery cell.

As shown in Fig. 9, the measured loop inductance decreases with increasing excitation frequency and eventually converges to a stable value at high frequencies. This behavior arises because the loop inductance is composed of both internal and external inductance. The internal inductance results from flux linkage within the conductor and depends on frequency due to the skin and proximity effects, whereas the external inductance remains frequency independent [23]. At higher frequencies, the skin effect causes the current to concentrate near the conductor surface, driving the internal inductance toward zero. Consequently, only the external inductance remains significant at high frequencies.

For the configuration without a magnetically coupled auxiliary loop, the inductance decreases from 87.8 nH at 1 kHz to 46.2 nH at 1 MHz. In contrast, when a magnetically coupled auxiliary loop is included, the inductance is reduced from 62.5 nH at 1 kHz to 28.0 nH at 1 MHz.

A direct comparison of both cases highlights the effectiveness of the proposed strategy of introducing a magnetically coupled auxiliary loop. At 1 kHz, the absolute reduction reaches 25.3 nH, while at 1 MHz it amounts to 18.2 nH. In relative terms, this corresponds to reductions of 28.8% and 39.4%, respectively.

These results highlight the substantial benefits of implementing a magnetically coupled auxiliary loop that is tightly aligned with the power path and further incorporates a section of the power path itself into the loop.

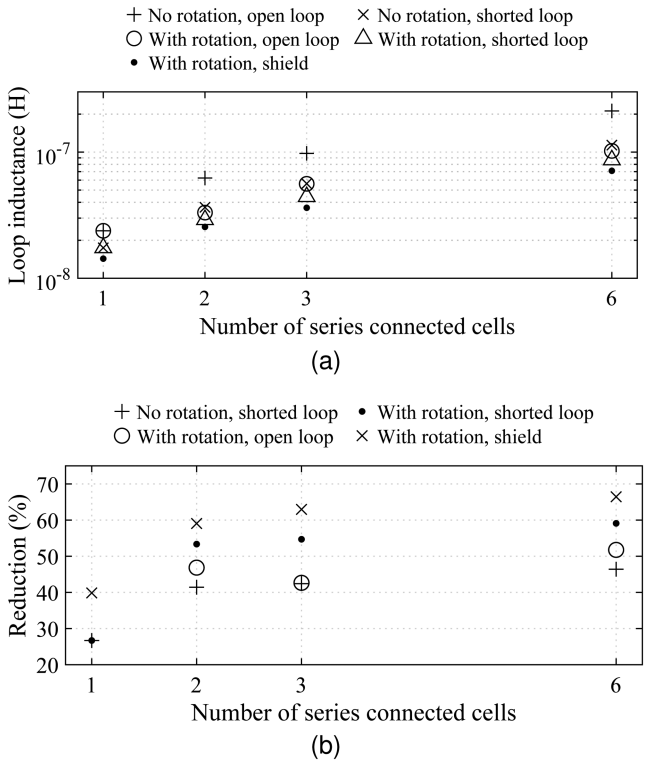

Fig. 10. (a) Measured loop inductance and (b) percentage reduction in loop inductance with respect to no rotation and open loop as a function of the number of series connected battery cells.

B. Series Connected Battery Cells With External Magnetically Coupled Auxiliary Loop

The inductances obtained for all configurations are summarized in Table I and visualized in Fig.10(a). For ease of comparison, the inductance at 1 MHz is used as a representative value of the overall inductive behavior. This is justified as the research in [10] demonstrates that this inductance value sufficiently represents the switching losses caused by the loop inductance in RBS. For better readability and clarity, the various prototypes explained in Section III-B are rewritten as follows.

1) Prototype A, J_1 not inserted $\rightarrow$ no rotation, open loop.
2) Prototype A, J_1 inserted $\rightarrow$ no rotation, shorted loop.
3) Prototype B, J_1 not inserted $\rightarrow$ with rotation, open loop.
4) Prototype B, J_1 inserted $\rightarrow$ with rotation, shorted loop.
5) Prototype C $\rightarrow$ with rotation, shield.

A visualization of the data in Fig.10(a) demonstrates that the loop inductance increases with increasing n_{ser}. Notably, the configuration with no rotation and open loop exhibits the highest loop inductance for any n_{ser}, which aligns with expectations since this configuration maximizes the effective enclosed area of the power path.

Following, a detailed comparison among the prototypes for $n_{\text{ser}} = 6$ is done as a representation for the overall behavior. For the configuration no rotation and no loop, the loop inductance amounts to 211.9 nH. Shorting the loop substantially reduces this inductance to 133.6 nH. A further reduction is achieved when

TABLE I
EXTRACTED LOOP INDUCTANCE INCLUDING THE UNCERTAINTY RANGE FOR DIFFERENT PROTOTYPES AND VARYING NUMBER OF SERIES CONNECTED BATTERY CELLS AT AN EXCITATION FREQUENCY OF 1 MHZ

	Loop inductance in nH for varying number of series connected battery cells			
	1	2	3	6
Prototype A, J_1 open	23.79 ± 0.14	62.37 ± 0.33	97.73 ± 0.51	211.9 ± 1.08
Prototype A, J_1 shorted	17.44 ± 0.10	36.52 ± 0.20	56.27 ± 0.30	113.6 ± 0.59
Prototype B, J_1 open	see Prototype A, J_1 open	33.15 ± 0.18	56.05 ± 0.30	102.2 ± 0.53
Prototype B, J_1 shorted	see Prototype A, J_1 shorted	29.09 ± 0.16	44.28 ± 0.24	86.67 ± 0.45
Prototype C	14.31 ± 0.09	25.53 ± 0.14	36.20 ± 0.20	71.09 ± 0.37

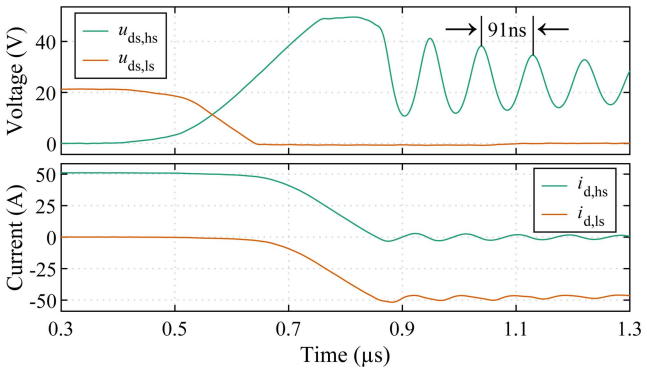

Fig. 11. Measured drain–source voltage (upper subplot) and drain currents (lower subplot) during the switching transition Q_{hs} OFFand Q_{ls} ON for $i_l = 50$ A and $n_{ser} = 6$.

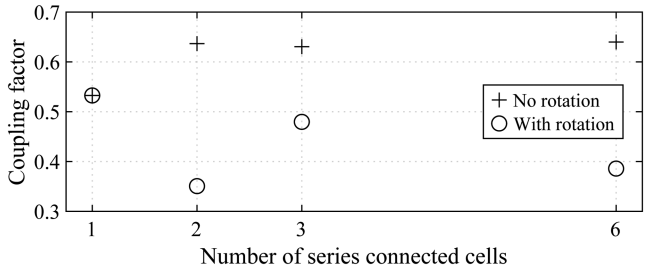

Fig. 12. Coupling factor for prototypes A and B as a function of the number of series connected battery cells.

rotating the series connected battery cells. With rotation and open loop, the loop inductance decreases to 102.2 nH, and by shorting the loop, it drops further to 86.67 nH. The lowest loop inductance is observed with rotation and shield, reducing the inductance to 71.09 nH.

Fig. 10(b) illustrates the percentage reduction in loop inductance as a function of n_{ser}, relative to the configuration without rotation and with an open loop. For the case without rotation but with a shorted loop, reductions between 27% and 46% are achieved. A particularly notable result is the 43%–52% reduction obtained by simply rotating the cells in the open-loop configuration. This highlights that physical rotation of series connected cells within an RBS—without additional measures—can nearly halve the loop inductance. Further reduction is possible by shortening the loop, lowering the inductance by approximately 27% at $n_{ser} = 1$ up to 59% at $n_{ser} = 6$. The biggest reduction is observed when rotating the battery cells and employing a shield, yielding an reduction of 40% at $n_{ser} = 1$ up to 66% at $n_{ser} = 6$. The largest reduction occurs when the battery cells are rotated and a shield is applied, achieving a decrease of 40% at $n_{ser} = 1$ up to 66% at $n_{ser} = 6$.

To validate the measured loop inductance of 102.2 nH for the configuration with rotation and open loop at $n_{ser} = 6$, drain–source voltages and drain currents were recorded during the switching transition Q_{hs} OFF to Q_{ls} ON at a load current of 50 A. The corresponding high-frequency oscillation period following turn-OFF was extracted from the measured waveforms, shown in Fig. 11. As observed, the oscillation period is $T_{osc} = 91$ ns.

Based on the method described in [41], the loop inductance is then calculated using

$$L_l = \frac{T_{osc}^2}{4\pi^2 C_{res}} \tag{4}$$

with

$$C_{res} = \frac{C_d C_s}{C_d + C_s} \tag{5}$$

and

$$C_d = C_{gd} + C_{ds} + C_{gd}C_{ds}/C_{gs} \tag{6}$$

$$C_s = C_{gs} + C_{ds} + C_{gs}C_{ds}/C_{gd}. \tag{7}$$

The gate–drain, drain–source, and gate–source capacitances of the MOSFET *IRL7472* are $C_{gd} = 1.47$ nF, $C_{ds} = 0.76$ nF, and $C_{gs} = 18.3$ nF, respectively. These values were obtained by evaluating the capacitance curves in the datasheet at 30 V. Using the extracted oscillation period, a loop inductance of $L_l \approx 98.9$ nH is determined. Compared to the 102.2 nH measured using the FRA, this results in a relative deviation of 3.2%, thereby validating the measurement approach.

Fig. 12 presents the calculated coupling factor for the configurations with and without rotation. While no rotation achieves coupling factors of 0.53–0.64, rotating the battery cells only achieves coupling factors of 0.35–0.53. In addition, low coupling factors are present when the number of series connected battery cells is even ($n_{ser} = [2; 6]$) and high k-values when the number of series connected battery cells is odd ($n_{ser} = [1; 3]$). This behavior arises from variations in the power path layout between even and odd n_{ser}. For odd n_{ser}, the path from the negative pole of the cell compound to the low-side switch is extended by

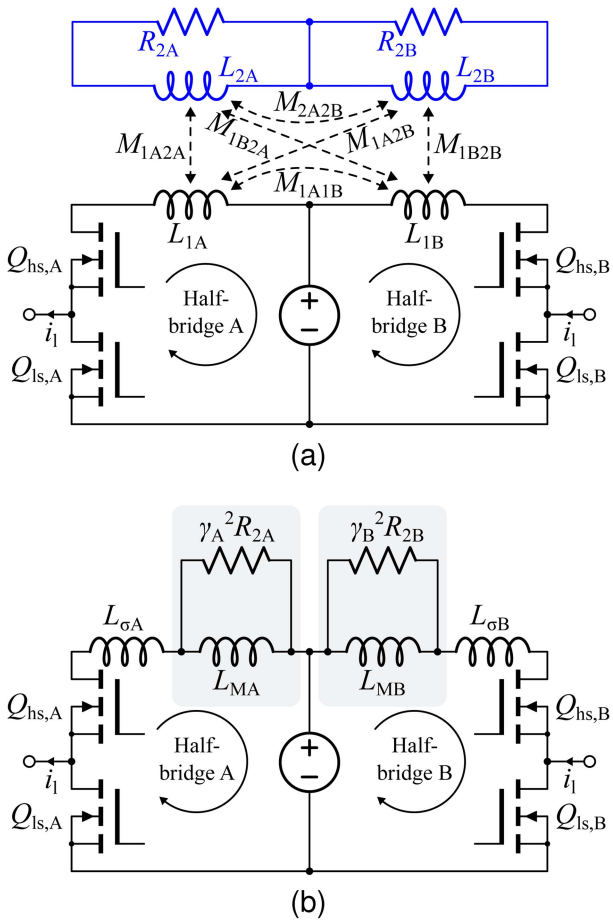

Fig. 13. Schematic representation of a full-bridge with two magnetically coupled auxiliary loops. (a) Conventional ECM and (b) simplified inverse Γ-ECM with secondary side transformed to primary side. The simplified ECM assumes negligible M_{1A1B}, M_{2A2B}, M_{1B2A}, and M_{1A2B}.

the distance between negative and positive pole of one battery cell. This extended path, implemented on the PCB, enables the secondary loop to remain in close proximity, resulting in strong coupling for this section of the loop.

V. Discussion on Broader Applicability

A. Other Switching Topologies

The broader applicability of magnetically coupled auxiliary loops to other switching topologies is discussed next, with a detailed investigation of the full-bridge. The underlying principle can be extended without restriction to other topologies, such as M2SPC [36], PECIN [37], or three-switch structures, such as BM3 [35].

As pointed out in [42], the full-bridge consists of two half-bridges A and B in parallel, see Fig. 13(a). This results in two power loops and consequently in two loop inductances L_{1A} and L_{1B}. Thus, two magnetically coupled auxiliary loops, highlighted in blue in Fig. 13(a), are added. Depending on the physical arrangement of the two power loops and the two magnetically coupled auxiliary loops, cross coupling between the two power loops and between the two magnetically coupled auxiliary loops as well as diagonal cross coupling may occur, resulting in a total number of six mutual inductances and consequently to six transformers. However, if the magnetically coupled auxiliary loops are aligned very closely to the power loop, achieving high coupling factors, the ECM can be simplified in such a way, that the number of mutual inductances (and thus transformers) is equal to the number of power loops. In that way, the mutual inductances M_{1A1B}, M_{2A2B}, M_{1A2B}, M_{1B2A} are negligible compared to M_{1A2A} and M_{1B2B}. Than, the conventional ECM shown in Fig. 13(b) can be simplified and transformed into the Γ-ECM illustrated in Fig. 13(b). The strategy is the same as discussed in Section II-A with the difference, that not one but two transformers are present. Here, L_{MA} and L_{MB} are the magnetizing inductances whose current has a freewheeling path over the (shorted) auxiliary loop with transferred resistance $\gamma_A^2 R_{2A}$ and $\gamma_B^2 R_{2B}$, respectively.

An additional simplification can be done if most of the loop inductance can be attributed to the battery cell while half-bridge A and B are physically located very close to each other (e.g., they are integrated in a module). In such a application, it is sufficient to use only one magnetically coupled auxiliary loop that is closely aligned with the power path of the battery cell and the full-bridge module. This results into only one transformer and the Γ-ECM used for the half-bridge in Fig. 4(b) can be used.

B. Other Battery Cell Types

So far, this article has focused on prismatic battery cells. However, the proposed methods are equally applicable to other formats, e.g., cylindrical or pouch cells. The main challenge then becomes an engineering task of how to construct the battery cells and RBS.

Fig. 14 shows a cross section of a cylindrical cell with an integrated half-bridge. The jelly roll, composed of anode, separator, and cathode, is wound around the mandrel. A PCB-based half-bridge connects to both anode and cathode leads on the positive side of the cell, thereby inherently reducing the loop inductance. Further reduction is achieved by placing a dedicated wire along the mandrel, connecting its ends to the anode lead on the positive side and to the negative terminal. This way, a part of the magnetically coupled auxiliary loop is formed by using the anode lead of the power loop, as discussed in Fig. 2(b). Depending on wire stiffness, the mandrel can even be replaced by the wire. In addition, the wire lowers dc conduction losses when the low-side switch is ON, as the current splits between the anode lead and the wire.

Adapting the magnetically coupled auxiliary loop to other battery types follows the same principle: identify the longest section of the power loop with equal potential and use it as part of the auxiliary loop. In a second step, complete the loop by placing an added wire as close as possible to the remaining section of the power loop.

C. Implications on Electromagnetic Interference (EMI)

In power electronic inverters, EMI coupling occurs either through conduction or radiation, mainly determined by the

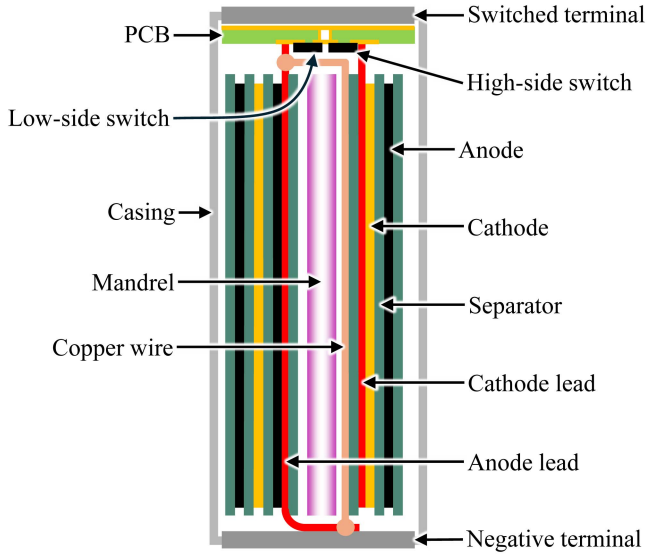

Fig. 14. Cross-section of a cylindrical battery cell with an integrated half-bridge. A copper conductor is additionally included, connecting the negative terminal to the cathode lead on the positive terminals side, thereby completing the magnetically coupled auxiliary loop.

harmonic content of the switching transition and the distance between the noise source and the victim [43], [44].

Fast current transients through parasitic inductances cause voltage overshoots and resonances with parasitic device capacitances, producing high-frequency conducted noise. Under capacitance-limited switching conditions [11], reducing the loop inductance lowers the induced voltage and consequently EMI [19], [23], [45]. Conversely, under inductance-limited switching, a smaller loop inductance increases current slew rate. Thus, two opposing effects occur—higher $\mathrm{d}i/\mathrm{d}t$ but lower inductance—with the dominant one depending on the application and operation point. Umetani et al. [46] demonstrated that the induced voltage spike exhibits a local minimum at an intermediate inductance value and a global minimum at zero inductance, with a local maximum in between. This suggests that although reducing inductance is usually beneficial, there may exist application-specific optimal values balancing EMI mitigation and switching losses. Which effect dominates is application-dependent; nevertheless, minimizing loop area and inductance is generally more beneficial.

When the battery cells are physically rotated, the enclosed area—and therefore the loop inductance—decreases. However, this also increases the current and magnetic flux gradients. In contrast, the behavior differs for magnetically coupled auxiliary loops. Similar to the physical rotation of series-connected battery cells, introducing magnetically coupled auxiliary loops reduces the loop inductance and increases the current gradients under inductance-limited switching. Unlike physical rotation, though, the magnetic flux gradient does not necessarily rise, as it depends on the coupling factor. While stray inductance still produces steep field gradients, the flux associated with the magnetizing inductance decays more gradually, governed by the time constant defined in (3). Consequently, the resulting field exhibits reduced harmonic content. Overall, magnetically coupled loops are more effective at reducing both inductance and EMI compared to geometric optimization alone, particularly when a solid shield is used, since it supports eddy currents that counteract radiated EMI.

VI. Conclusion

This article examines loop inductance in RBSs with a variable number of series-connected battery cells. Three approaches for reducing inductance are explored as follows.

1) Strategic orientation of the series-connected cells.
2) A novel method using a magnetically coupled auxiliary loop placed near the power loop to provide a freewheeling path for the magnetization current.
3) The addition of a solid copper shield.

Part of the auxiliary loop is implemented through a section of the power loop itself, enabling near-ideal coupling. Experimental validation with a single battery cell shows a relative inductance reduction of 39.4%. When combined with an optimized physical arrangement of the series-connected cells, the reduction reaches up to 52%. The greatest improvement is achieved by combining strategic orientation with the solid copper shield, lowering the inductance by as much as 66%. Finally, the broader applicability of the proposed techniques to other switching topologies and battery cell types is discussed. Future work will focus on integrating a rectifier at the secondary coil terminals to capture the transferred energy, preventing its dissipation as heat in the secondary resistance.

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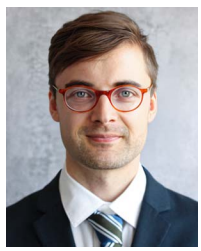

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