Bidirectional Isolated DC–DC Converter With Power Active Allocation Strategy for Single-Cell BESS

Jiahao Wang, Dongyuan Qiu, *Senior Member, IEEE*, Yangbin Zeng, *Member, IEEE*, Bo Zhang, *Fellow, IEEE*, and Yukun Chen

***Abstract*—This article proposes a low-voltage-side parallel high-voltage-side series isolated bidirectional dc–dc converter for single-cell battery energy storage systems, addressing the critical challenges of high voltage gain requirements and low-voltage/high-current operation. Two parallel staggered shunt boost units are used on the low-voltage side to reduce the current ripple and the current stress. The voltage gain is further increased by applying an isolation capacitor on the high-voltage side, which enables the converter to accomplish high-gain boosting without a high transformer turns ratio. Since switches with different performance are used in the two parallel branches to achieve cost efficiency, this article further proposes a power active allocation strategy (PAAS) for the proposed converter. Despite the mixed use of switches with different conduction and switching characteristics, the proposed strategy dynamically optimizes the branch current allocation through duty cycle control while regulating the output voltage, thus improving the overall system efficiency, particularly enhancing efficiency under light-load conditions. Finally, a 250 W prototype with 3.2 V/48 V is built to verify the working principle of the proposed converter, and the overall efficiency is improved by an average of 1.22% after adopting the PAAS.**

***Index Terms*—High voltage gain, input-parallel output-series, isolated bidirectional dc–dc converter, power active allocation, single-cell battery.**

I. Introduction

BATTERY energy storage systems (BESSs) are pivotal for the energy transition, widely used in electric vehicles, data centers, and communication base stations [1], [2]. Currently, high-power demands are met by connecting multiple cells in series/parallel, but inherent performance inconsistencies degrade battery lifespan and safety [3]. The adoption of high-capacity single cells is driven by requirements for lower integration costs and higher safety standards. Serving as the essential energy transfer interface between battery and load, bidirectional dc–dc converters must overcome the challenges of high voltage gain and high current tolerance to effectively work with low-voltage single-cell configurations. Thus, high-gain bidirectional converters are essential for optimizing large-capacity single-cell performance.

Bidirectional high-gain dc–dc converters can be classified into isolated and nonisolated types based on electrical isolation between input and output. Nonisolated converters typically employ coupled inductors, switched capacitors, voltage multipliers, or cascaded topologies for voltage boosting [4], [5], [6], [7]. However, their voltage gain is practically limited by both topologies and parasitic parameters, while switch rating boundaries also challenge their use in high gain and high power applications. In contrast, isolated bidirectional dc–dc converters (IBDCs) utilize a high-frequency transformer to provide electrical isolation, improving operational safety. Additionally, the transformer turns ratio serves as an extra control parameter, expanding the voltage regulation range to accommodate varying battery voltage levels. This makes IBDCs particularly suitable for BESSs requiring high voltage gains (e.g., >10) during charging/discharging [8].

Extensive research efforts have been devoted to IBDCs in recent years. While bidirectional forward [9], flyback [10], and push-pull [11], [12] converters, derived from non-isolated topologies with incorporated transformers, feature simplified control schemes and reduced switch counts, they exhibit inherent limitations. Forward and flyback converters suffer from low transformer utilization due to unidirectional excitation, restricting them to small/medium-power applications. Push-pull configurations require switches to withstand twice the operating voltage during turn-OFF, limiting their use to low-voltage scenarios. Alternatively, full-bridge-based IBDCs, such as dual active bridge [13], [14], series/parallel resonant [15], LLC [16], [17], [18], and CLLC [19], [20], [21] converters, adjust voltage gain via transformer turns ratio. However, in boost mode, the voltage of magnetic inductance equals the input voltage [22], requiring high turns ratios for ultralow-voltage single cells, which increases size and cost. Moreover, leakage inductance introduces voltage spikes, current ripple, and resonant frequency reduction, resulting in degraded output waveform quality and compromised system performance. A parallel resonant IBDC in [23] employs interleaving techniques to reduce current ripple, while a voltage doubler on the high-voltage side multiplies the output voltage by a factor of two, eliminating the need for a high turns ratio transformer. But its practical implementation suffers from strict resonant tuning and excessive low-side switch stress, limiting its use in ultralow-voltage, high-current single-cell scenarios. A

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The authors are with the School of Electric Power, South China University of Technology, Guangzhou 510640, China. (e-mail: 202321014714@mail.scut.edu.cn; epdyqiu@scut.edu.cn; epybzeng@scut.edu.cn; epbzhang@scut.edu.cn; 202320113885@mail.scut.edu.cn).

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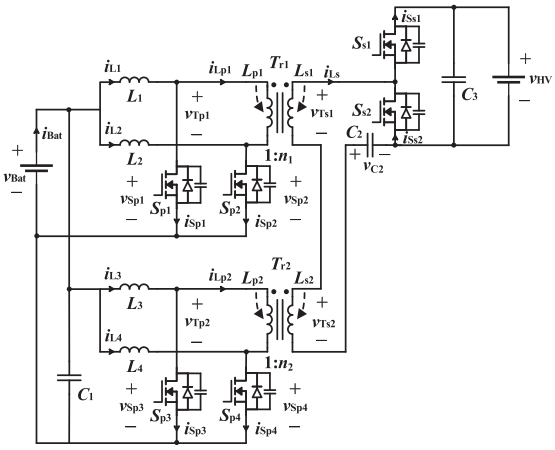


Fig. 1. Schematic diagram of the proposed LPHS-IBDC.

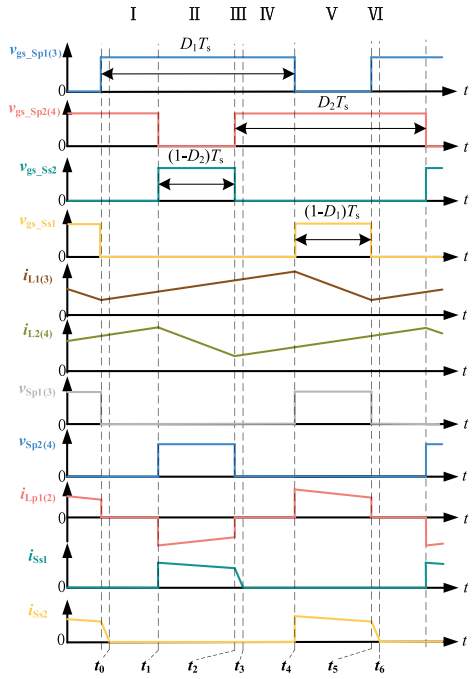


Fig. 2. Key waveforms of the LPHS-IBDC operating in the discharge-boost mode.

critical challenge in such applications is efficiency optimization, heavily influenced by switching device performance (e.g., ON-resistance, switching speed). While superior switching devices improve efficiency, their higher cost creates a tradeoff between performance and affordability.

For high step-up applications, the input-parallel output-series configuration is commonly employed to enhance both the voltage boosting capability and the power level of the system [24]. Accordingly, a low-voltage-side parallel and high-voltage-side series isolated bidirectional dc–dc converter (LPHS-IBDC) is proposed to specifically meet the demanding requirements of single-cell battery applications. The parallel low-voltage-side configuration enables current sharing across multiple branches, significantly enhancing current-handling capability, while the series high-voltage-side connection inherently doubles the voltage gain, collectively addressing both the high-current and high-gain needs of single-cell charging/discharging operations. While the LPHS topology reduces current stress through multibranch sharing and achieves the required voltage gain with reduced turns ratio, its multiple switches contribute substantially to system cost. To address this cost challenge without compromising performance, the design combines high-performance and cost-effective switches across distinct branches. Furthermore, a power active allocation strategy (PAAS) is proposed for this mixed-switch implementation, biasing current toward switches with superior characteristics through duty cycle optimization to achieve a favorable balance between efficiency and cost. Finally, an experimental prototype with 3.2 V on the low-voltage side and 48 V on the high-voltage side and a rated power of 250 W was built to experimentally verify the theoretical analysis.

II. Operation Principle of the Proposed LPHS-IBDC

The proposed LPHS-IBDC is illustrated in Fig. 1. The low-voltage side includes a single-cell battery voltage v_{Bat} and capacitor C_1, while the high-voltage side consists of high voltage v_{HV} and capacitor C_3. Two isolated transformers Tr_1 and Tr_2 with 1:n turns ratios ($n\geq 1$) provide galvanic isolation and voltage transformation between the low-voltage and high-voltage stages. The low-voltage side features two interleaved parallel branches, consisting of inductors L_1-L_4, switches S_{p1}-S_{p4}. The transformer secondaries and a dc-blocking capacitor C_2 form the input to a high-voltage-side half-bridge composed of switches S_{s1} and S_{s2}. The current flow arrows in Fig. 1 define the reference directions for the branch and inductor currents used in the subsequent analysis.

Gate signals for S_{p1}, S_{p3} and S_{p2}, S_{p4} share duty cycles D_1 and D_2 ($0.5< D_1, D_2 <1$), respectively, with 180° phase interleaving. For analytical convenience, S_{s1} and S_{s2} are assumed to operate complementarily to S_{p2}, S_{p4} and S_{p1}, S_{p3}, with duty cycles 1-D_2 and 1-D_1. In practice, slight dead times from complementarity enable ZVS through body diode conduction. These short intervals are negligible in steady-state analysis. When S_{s1} is on, C_2 doubles the voltage of secondary winding. Thus, the voltage gain can be doubled by connecting C_2 in series with the half-bridge converter. This allows lower transformer turns ratios, reducing converter size. The topology supports both discharge-boost mode and charge-buck mode.

A. Discharge-Boost Mode

The operating waveforms of the proposed LPHS-IBDC in the discharge-boost mode are illustrated in Fig. 2. One complete switching period can be divided into six operating stages. In this mode, a pure resistive load R_L is used on the high-voltage side to absorb the output power. Fig. 3 illustrates the three main equivalent circuits in discharge-boost mode, where the colored current loops (red, green, and blue) depict the actual instantaneous flow of the circuit currents during that specific stage, while black arrows maintain the established reference

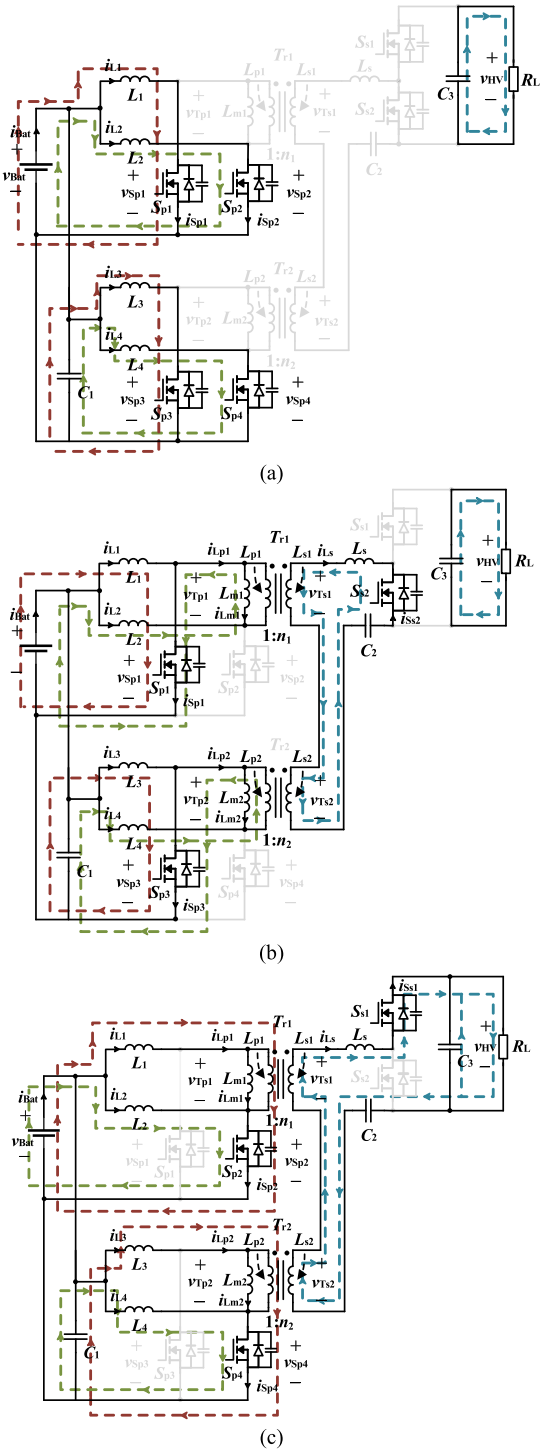


Fig. 3. Three main equivalent circuits of the LPHS-IBDC operating in the discharge-boost mode. (a) Stage I and Stage IV. (b) Stage II. (c) Stage V.

directions. Each of the six operating stages is analyzed in detail below.

1) *Stage* I [t_0–t_1]: During this interval, the low-voltage side switches S_{p1}-S_{p4} turn ON, while the high-voltage side switches S_{s1} and S_{s2} remain OFF. As shown in Fig. 3(a), v_{Bat} and C_1 charge inductors L_1 to L_4 through the low-voltage side switches, causing the inductor currents i_{L1} to i_{L4} to increase linearly. The voltage across the excitation inductance L_{m1} and L_{m2} of transformers Tr_1 and Tr_2 is zero. The low-voltage side switches S_{p1}-S_{p4} are fully on, while the high-voltage side switches S_{s1} and S_{s2} block a voltage of $v_{HV}/2$. Meanwhile, C_3 supplies energy to the load R_L. This stage ends at $t = t_1$, when S_{p2} and S_{p4} are turned OFF and S_{s2} is turned ON.
2) *Stage* II [t_1–t_2]: During this interval, S_{p1}, S_{p3}, and S_{s2} are ON, while S_{p2}, S_{p4}, and S_{s1} are OFF. As shown in Fig. 3(b), L_1 and L_3 continue charging from v_{Bat} and C_1, with i_{L1} and i_{L3} increasing linearly. Meanwhile, L_2 and L_4 transfer energy through Tr_1 and Tr_2 to C_2, causing i_{L2} and i_{L4} to decrease linearly. C_3 continues supplying energy to the load. This stage ends at $t = t_2$, when S_{s2} turns OFF and S_{p2} and S_{p4} turn ON.
3) *Stage* III [t_2–t_3]: During this interval, S_{p1}–S_{p4} are ON, while S_{s1} and S_{s2} are OFF. The energy previously stored in leakage inductance L_s by Tr_1 and Tr_2 is discharged through the antiparallel diode of S_{s2}. This stage ends at $t = t_3$, once the energy in L_s is fully released.
4) *Stage* IV [t_3–t_4]: During this interval, S_{p1}–S_{p4} are ON, while S_{s1} and S_{s2} remain OFF. The equivalent circuit is identical to that in stage I, as shown in Fig. 3(a). This stage ends at $t = t_4$, when S_{p1} and S_{p3} turn OFF and S_{s1} turns ON.
5) Stage V [t_4–t_5]: During this interval, S_{p2}, S_{p4}, and S_{s1} are ON, while S_{p1}, S_{p3}, and S_{s2} are OFF. The equivalent circuit is shown in Fig. 3(c). Inductors L_2 and L_4 continue to store energy from v_{Bat} and C_1, with i_{L2} and i_{L4} increasing linearly. Meanwhile, i_{L1} and i_{L3} decrease linearly as the energy stored in L_1 and L_3, along with that from the isolation capacitor C_2, is delivered to C_3 and R_L via Tr_1 and Tr_2. This stage ends at $t = t_5$, when S_{s1} turns OFF and S_{p1} and S_{p3} turn ON.
6) *Stage* VI [t_5–t_6]: During this interval, S_{p1}-S_{p4} are turned ON, while S_{s1} and S_{s2} remain OFF. The energy previously stored in L_s is discharged through the antiparallel diode of S_{s1}. This stage ends at $t = t_6$, once the energy in L_s is fully released.

B. Charge-Buck Mode

The operating waveform of the proposed LPHS-IBDC in charge-buck mode is illustrated in Fig. 4 and can also be divided into six stages within a complete switching cycle. During this mode, the load is a single-cell with constant voltage v_{Bat}, and the charging power is determined by the charging current i_{Bat}. Fig. 5 illustrates the three main equivalent circuits in charge-buck mode. Similar to the analysis of the discharge-boost mode, the actual current paths in Fig. 5 are illustrated by colored loops, with black arrows indicating the reference directions. The six operating stages are analyzed as follows.

1) *Stage* I [t_0–t_1]: During this interval, S_{s1} turns ON and S_{s2} turns OFF, while S_{p2} and S_{p4} are conducting and S_{p1} and S_{p3} are OFF. As shown in Fig. 5(a), v_{HV} and capacitor C_3 deliver energy to L_1, L_3, C_1, and v_{Bat} through Tr_1 and Tr_2, while also charging C_2. The voltage across S_{s2} is clamped to v_{HV}, with i_{L1} and i_{L3} increasing linearly while i_{L2} and i_{L4} decrease linearly as L_2 and L_4 discharge to C_1 and

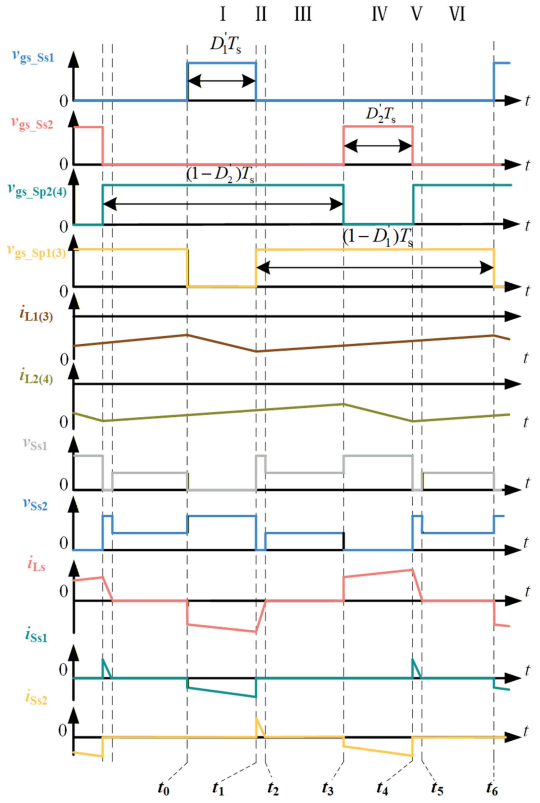


Fig. 4. Key waveforms of the LPHS-IBDC operating in the charge-buck mode.

v_{Bat}. This stage ends at $t = t_1$, when S_{s1} turns OFF and S_{p1} and S_{p3} turn ON.

2) *Stage* II [t_1–t_2]: During this interval, S_{p1}–S_{p4} are turned ON, while S_{s1} and S_{s2} are OFF. The energy previously stored in L_s discharges through S_{s2}'s body diode. This stage ends at $t = t_2$ when L_s is fully discharged.
3) *Stage* III [t_2–t_3]: During this interval, S_{p1}–S_{p4} are turned ON, while S_{s1} and S_{s2} remain OFF. The equivalent circuit is shown in Fig. 5(b), where L_1–L_4 discharge to C_1 and v_{Bat}, causing i_{L1}–i_{L4} to decrease linearly. The cutoff voltages of S_{s1} and S_{s2} are both $v_{\mathrm{HV}}/2$. This stage ends at $t = t_3$, when S_{s2} conducts and S_{p2} and S_{p4} turn OFF.
4) *Stage* IV [t_3–t_4]: During this interval, S_{s2} turns ON and S_{s1} turns OFF, while S_{p1} and S_{p3} conduct and S_{p2} and S_{p4} remain OFF. The equivalent circuit is shown in Fig. 5(c), where the energy stored in C_2 transfers to L_2, L_4, C_1, and v_{Bat} via Tr_1 and Tr_2. The voltage across S_{s1} is clamped to v_{HV}, with i_{L2} and i_{L4} increasing linearly while i_{L1} and i_{L3} decrease linearly as L_1 and L_3 discharge to C_1 and v_{Bat}. The stage ends at $t = t_4$, when S_{s2} turns OFF and S_{p2} and S_{p4} turn ON.
5) *Stage* V [t_4–t_5]: During this interval, S_{p1} to S_{p4} turn ON, while S_{s1} and S_{s2} remain OFF. The energy previously stored in L_s discharges through S_{s1}'s body diode. The stage ends at $t = t_5$ when L_s is fully discharged.
6) *Stage* VI [t_5–t_6]: The equivalent circuit is identical to that of mode III, as shown in Fig. 5(b). This stage ends at $t = t_6$, when S_{s1} turns ON and S_{p1} and S_{p3} turn OFF.

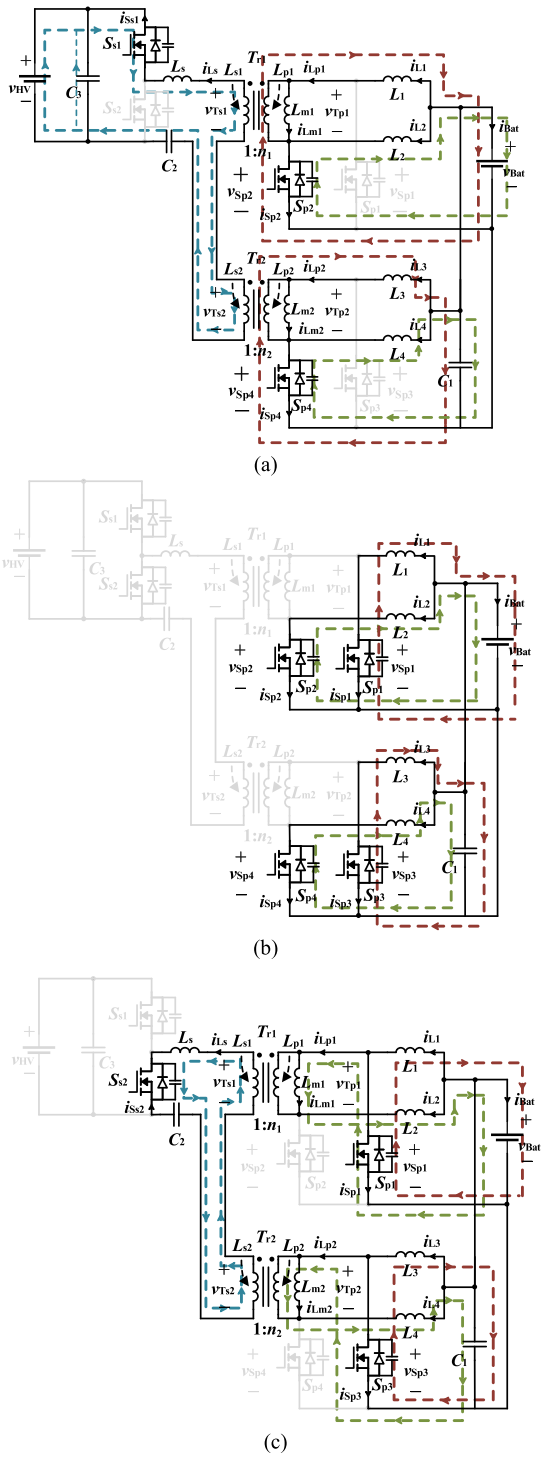


Fig. 5. Three main equivalent circuits of the LPHS-IBDC operating in the charge-buck mode. (a) Stage I. (b) Stage III and stage VI. (c) Stage IV.

III. Steady-State Analysis of the Proposed LPHS-IBDC

To achieve cost reduction, the design intentionally incorporates both high-performance switches with superior conduction/switching characteristics and cost-optimized switches with compromised performance. The converter features two paired low-side switch groups (S_{p1}/S_{p3} and S_{p2}/S_{p4}) sharing common

gate signals, with one pair utilizing performance-optimized devices and the other employing cost-reduced alternatives. The proposed active power distribution strategy aims to optimally allocate power between these two distinct switch-pair branches, thereby enhancing overall converter efficiency.

In order to enable this power allocation, a detailed steady-state analysis is first carried out to explicitly derive the relationship between branch currents and the duty cycles D_1 and D_2 under a given resistive load R_L. These analytical expressions reveal how varying D_1 and D_2 directly affect the current sharing between branches. Based on these results, the losses of each component, including MOSFET conduction and switching losses, inductor copper and core losses, transformer copper and core losses, and capacitor ESR losses, are calculated as explicit functions of D_1, D_2, and R_L. This comprehensive loss modeling establishes a quantitative link between control parameters and converter efficiency. Consequently, it forms the mathematical foundation for dynamically adjusting the duty cycles to actively allocate power in a way that minimizes overall losses and optimizes efficiency.

From Figs. 3 and 5, it can be observed that the equivalent circuits of the main operating phases in both discharge boost and charge buck modes correspond to each other based on the switching states of the high- and low-voltage sides. The analysis methods are essentially identical, with the primary difference being the direction of power flow. Therefore, the discharge-boost mode is selected as a representative case for establishing the converter's large-signal model.

Before proceeding with the steady-state analysis, the following assumptions are made to simplify the state equations.

1) The gate signals for high- and low-voltage side switches are complementary. The switching period T_s is much longer than both the ZVS transition time caused by antiparallel diodes and the diode conduction period for transformer energy release.
2) All switches are considered ideal with zero on-resistance and infinite off-resistance; The output capacitance of MOSFETs is neglected; Inductors are sufficiently large to ensure continuous conduction mode (CCM); capacitors are large enough that their voltage ripple is negligible; Transformers are treated as ideal, with leakage and magnetizing inductances addressed separately during the detailed power loss analysis.
3) Since the goal is to establish the relationship between branch currents and duty cycles D_1 and D_2, all other parameters are kept constant. The two parallel branches on the low-voltage side are structurally symmetrical, therefore $i_{L1} = i_{L3}$, $i_{L2} = i_{L4}$. Specifically, low-voltage side inductors are equal ($L_1 = L_2 = L_3 = L_4$), transformer turns ratios are the same ($n_1 = n_2$), and magnetizing inductances are equal ($L_{m1} = L_{m2}$).

The selected state variables for the state-space model include the inductor currents i_{L1} to i_{L4} of each branch, the transformer magnetizing currents i_{Lm1} and i_{Lm2}, the isolated capacitor voltage v_{C2}, and the high-voltage side capacitor voltage v_{C3}. The input variable is the single-cell voltage V_{Bat}. Based on these definitions, the state equations corresponding to the four main operating modes within one switching cycle T_s are formulated.

A. Stage I, Stage IV

From the previous analysis, it is evident that stages I and IV share identical equivalent circuits. Therefore, their state equations are combined. According to Fig. 2, the total duration of these two stages within one switching cycle T_s is $(D_1+D_2-1)T_s$. As shown in Fig. 3(a), during this period, switches S_{p1} to S_{p4} are conducting, and the battery voltage V_{Bat} is directly applied across inductors L_1 to L_4. In this interval, the inductor currents i_{Ly} ($y = 1, 2, 3, 4$) change linearly, and the slopes are as

$$\frac{di_{\mathrm{Ly}}}{dt} = \frac{v_{\mathrm{Ly}}}{L} = \frac{V_{\mathrm{Bat}}}{L}. \tag{1}$$

The high-voltage side capacitor C_3 supplies energy to the load R_L, and the slope of its voltage v_{C3} can be expressed as

$$\frac{dv_{\mathrm{C3}}}{dt} = \frac{i_{\mathrm{C3}}}{C_3} = -\frac{V_{\mathrm{HV}}}{R_L C_3}. \tag{2}$$

By combining (1) and (2), the corresponding state equation in this mode can be derived as $\dot{x} = A_1 x + B_1 V_i$ and must be satisfied by

$$\begin{aligned} \dot{x} &= \frac{d}{dx}\begin{bmatrix} i_{\mathrm{L1}} & i_{\mathrm{L2}} & i_{\mathrm{L3}} & i_{\mathrm{L4}} & i_{\mathrm{Lm1}} & i_{\mathrm{Lm2}} & v_{\mathrm{C3}} & v_{\mathrm{C2}} \end{bmatrix}^T \\ x &= \begin{bmatrix} i_{\mathrm{L1}} & i_{\mathrm{L2}} & i_{\mathrm{L3}} & i_{\mathrm{L4}} & i_{\mathrm{Lm1}} & i_{\mathrm{Lm2}} & v_{\mathrm{C3}} & v_{\mathrm{C2}} \end{bmatrix}^T \\ V_i &= V_{\mathrm{Bat}}. \end{aligned} \tag{3}$$

A_1 and B_1 are shown in Appendix (A1).

B. Stage II

According to Fig. 2, the duration of stage II within one switching cycle T_s is $(1\text{-}D_2)T_s$. As shown in Fig. 3(b), during this stage, S_{p1}, S_{p3}, and S_{s2} are turned ON, while S_{p2}, S_{p4}, and S_{s1} remain OFF. The battery voltage V_{Bat} continues to charge inductors L_1 and L_3 directly, and the state equations for these two branches are identical to those in stage I. Simultaneously, inductors L_2 and L_4 transfer energy through transformers Tr_1 and Tr_2 to C_2. In this interval, currents i_{L2}, i_{L4} decrease linearly, and the slopes are as

$$\frac{di_{\mathrm{L2}}}{dt} = \frac{di_{\mathrm{L4}}}{dt} = \frac{v_{\mathrm{Tp}} + V_{\mathrm{Bat}}}{L} = -\frac{v_{\mathrm{C2}}}{2nL} + \frac{V_{\mathrm{Bat}}}{L}. \tag{4}$$

The voltage across the transformer excitation inductance is denoted as v_{Tp}. Accordingly, the slopes of excitation currents i_{Lm1} and i_{Lm2} follows:

$$\frac{di_{\mathrm{Lm1}}}{dt} = \frac{di_{\mathrm{Lm2}}}{dt} = \frac{v_{\mathrm{Tp}}}{L_{\mathrm{m}}} = -\frac{v_{\mathrm{C2}}}{2nL_{\mathrm{m}}}. \tag{5}$$

The high-voltage side capacitor C_3 continues to supply energy to the load R_L, so its state equation remains unchanged. Meanwhile, the transformer secondary charges the isolation capacitor, and the slope of the voltage across the isolation capacitor v_{C2} can be obtained as

$$\frac{dv_{\mathrm{C2}}}{dt} = \frac{i_{\mathrm{C2}}}{C_2} = \frac{i_{\mathrm{L2}} + i_{\mathrm{L4}} + i_{\mathrm{Lm1}} + i_{\mathrm{Lm2}}}{2nC_2}. \tag{6}$$

By combining (4), (5), and (6), the corresponding state equation in this mode can be derived as $\dot{x} = A_2 x + B_2 V_i$ and must be satisfied by $B_2 = B_1$ and A_2 is shown in Appendix (A1).

C. Stage V

According to Fig. 2, the duration of Stage V within one switching cycle T_s is $(1–D_1)T_s$. As shown in Fig. 3(c), S_{p2}, S_{p4}, and S_{s1} are turned ON, while S_{p1}, S_{p3}, and S_{s2} are turned OFF. The battery voltage V_{Bat} is directly applied to inductors L_2 and L_4 for charging, and the state equations for I_{L2} and I_{L4} remain the same as in stage I. Meanwhile, L_1 and L_3 transfer energy through Tr_1 and Tr_2, together with the isolation capacitor C_2, to charge the high-voltage side capacitor C_3 and supply power to the load R_L. In this interval, currents i_{L2}, i_{L4} decrease linearly, and the slopes are as

$$\frac{di_{\mathrm{L1}}}{dt}=\frac{di_{L3}}{dt}=\frac{-v_{Tp}+V_{Bat}}{L}=\frac{-v_{\mathrm{C3}}+v_{\mathrm{C2}}}{2nL}+\frac{V_{\mathrm{Bat}}}{L} \tag{7}$$

the slopes of excitation currents i_{Lm1} and i_{Lm2} follows:

$$\frac{di_{\mathrm{Lm1}}}{dt}=\frac{di_{\mathrm{Lm2}}}{dt}=\frac{v_{Tp}}{L_m}=\frac{v_{\mathrm{C3}}-v_{\mathrm{C2}}}{2nL_m} \tag{8}$$

the slope of the voltage across the high-voltage side capacitor v_{C3} can be expressed as

$$\frac{dv_{\mathrm{C3}}}{dt}=\frac{i_{\mathrm{C3}}}{C_3}=\frac{i_{Ls}-i_{RL}}{C_3}=\frac{i_{\mathrm{L1}}+i_{L3}-i_{\mathrm{Lm1}}-i_{\mathrm{Lm2}}}{2nC_3}-\frac{v_{\mathrm{C3}}}{RC_3} \tag{9}$$

the slope of the voltage across the isolation capacitor v_{C2} can be obtained as

$$\frac{dv_{\mathrm{C2}}}{dt}=\frac{i_{\mathrm{C2}}}{C_2}=\frac{-i_{Ls}}{2nC_2}=\frac{-i_{\mathrm{L1}}-i_{L3}+i_{\mathrm{Lm1}}+i_{\mathrm{Lm2}}}{2nC_2}. \tag{10}$$

By combining (7), (8), (9) and (10), the corresponding state equation in this mode can be derived as $\dot{x}=A_3x+B_3V_i$ and must be satisfied by $B_3=B_1$ and A_3 is shown in Appendix (A1).

Based on the state equations derived for each operating phase, the state-space averaging method is applied by weighting each phase's contribution according to its duration within one switching period. As a result, the averaged system matrices A and B are obtained, as expressed in Appendix (A2).

According to the steady-state condition of the converter, the system of equations can be expressed as

$$AX+BV_i=0. \tag{11}$$

For the converter to operate in steady state, the average time derivative of the state vector must be zero. Applying this condition to (11), yields the steady-state relationships for the average value of the voltage state variable (V_{Bat}, $V_{C,2}$ and V_{C3}), which must satisfy

$$\begin{cases}\frac{1-D_1}{-2nL}V_{\mathrm{C3}}+\frac{1-D_1}{2nL}V_{\mathrm{C2}}+\frac{1}{L}V_{\mathrm{Bat}}=0\\ \frac{1-D_1}{-2nL}V_{\mathrm{C2}}+\frac{1}{L}V_{\mathrm{Bat}}=0\end{cases}. \tag{12}$$

Solving (12) results in

$$\begin{cases}V_{\mathrm{HV}}=V_{\mathrm{C3}}=\left(\frac{2n}{1-D_1}+\frac{2n}{1-D_2}\right)V_{\mathrm{Bat}}\\ V_{\mathrm{C2}}=\frac{2n}{1-D_2}V_{\mathrm{Bat}}\end{cases}. \tag{13}$$

Under stead-state conditions, the solution to (11) also requires that the average values of the current state variables (I_{L1}, I_{L2}, $I_{L3,}$ and I_{L4}) satisfy

$$\begin{cases}\frac{1-D_1}{2nC_3}I_{\mathrm{L1}}+\frac{1-D_1}{2nC_3}I_{L3}-\frac{1}{R_LC_3}V_{\mathrm{C3}}=0\\ -\frac{1-D_1}{2nC_2}I_{\mathrm{L1}}+\frac{1-D_2}{2nC_2}I_{\mathrm{L2}}-\frac{1-D_1}{2nC_2}I_{L3}+\frac{1-D_2}{2nC_2}I_{\mathrm{L4}}=0\end{cases}. \tag{14}$$

Considering that $I_{L1}=I_{L3}$ and $I_{L2}=I_{L4}$, the steady-state inductor currents value is given by

$$\begin{cases}I_{\mathrm{L1}}=I_{L3}=\frac{nV_{\mathrm{HV}}}{(1-D_1)R_L}\\ I_{\mathrm{L2}}=I_{\mathrm{L4}}=\frac{nV_{\mathrm{HV}}}{(1-D_2)R_L}\end{cases}. \tag{15}$$

The steady-state analysis presented above is only valid under the CCM. Therefore, it is necessary to further analyze the boundary conditions of the proposed converter. Assuming that $D_1<D_2$, when the LPHS-IBDC operates in the boundary conduction mode (BCM), the minimum average current must equal the boundary average current

$$I_{\mathrm{L\_min}}=\frac{nV_{\mathrm{HV}}}{(1-D_1)R_L}=\frac{\Delta I_L}{2}. \tag{16}$$

Based on the preceding analysis of stage I and stage IV, the inductor current rises continuously during the turn-ON time D_1T_s of switches S_{p1} and S_{p3}. Consequently, the ripple of the inductor current ΔI_L can be expressed as

$$\Delta I_L=\frac{V_{\mathrm{Bat}}D_1T_s}{L}. \tag{17}$$

By combining (16) and (17), the necessary condition for the LPHS-IBDC to operate in BCM can be derived as

$$\frac{nV_{\mathrm{HV}}}{(1-D_1)R_L}=\frac{V_{\mathrm{Bat}}D_1T_s}{2L}. \tag{18}$$

To ensure the LPHS-IBDC operates in CCM, (13) is substituted into (18), from which the necessary condition that load resistance R_{L} must satisfy can be derived

$$R_L<\frac{4n^2(2-D_1-D_2)L}{(1-D_1)^2(1-D_2)D_1T_s}. \tag{19}$$

If $D_1=D_2=D$, (19) can be simplified as

$$R_L<\frac{8n^2L}{(1-D)^2DT_s}. \tag{20}$$

The operating boundary of LPHS-IBDC between CCM and discontinuous conduction mode (DCM) is shown in Fig. 6. As Fig. 6 illustrates, a larger inductance leads to a smaller current ripple, which consequently expands the CCM region. Furthermore, a larger duty cycle D results in a higher output voltage. Under the same load condition, this higher voltage yields a larger inductor current, thereby making the converter less likely to enter the DCM region.

The equivalent circuits of the main stages in the charging mode correspond one-to-one with those in the discharging mode, and their state-space equations are essentially the same. Therefore, a detailed analysis is omitted.

A comparison between the proposed converter and other high-gain IBDCs is given in Table I. The table summarizes key characteristics including the number of components, voltage gain, power density, voltage stress on both high- and low-voltage side switches, the maximum current stress on the low-voltage

TABLE I
COMPARISON OF IBDCS

Topologies	N_S	N_C	N_L	N_T	Voltage stress of the switches primary; secondary	Current stress of the switches	Power density	Voltage Gain V_{HV}/V_{LV}	Controlling complexity
Wu et al. [12]	7	1	1	1	$2V_{LV}/(2\text{-}D)$; V_{HV}	I_{LV}	Medium	nD	Complex
Tang et al. [21]	8	2	2	1	V_{LV}; V_{HV}	I_{LV}	Medium	nD	Complex
Chen et al. [26]	4	2	0	1	$2V_{LV}$; $2V_{HV}$	I_{LV}	High	$nD/(1\text{-}D)$	Normal
Wu and Ke [27]	6	3	0	1	$V_{LV}/(1\text{-}D)$; V_{HV}	I_{LV}	Medium	$n/(1\text{-}D)^2$	Complex
Wu and Pan [28]	4	4	0	1	$V_{LV}/(1\text{-}D)$; V_{HV}	I_{LV}	Medium	$n/(1\text{-}D)$	Normal
Liang and Lee [29]	4	1	2	1	$V_{LV}/(1\text{-}D)$; V_{HV}	$I_{LV}/2$	Medium-High	$2n/(1\text{-}D)$	Normal
Tseng et al. [30]	6	4	2	1	$V_{LV}/(1\text{-}D)$; V_{HV}	$I_{LV}/2$	Medium	$2n/(1\text{-}D)$	Complex
Kothapalli et al. [31]	6	5	0	2	$V_{LV}/(1\text{-}D)$; $V_{HV}/2$	$I_{LV}/2$	Medium	$2n/D(1\text{-}D)$	Complex
Proposed	6	1	4	2	$V_{LV}/(1\text{-}D)$; V_{HV}	$I_{LV}/4$	Medium-High	$4n/(1\text{-}D)$*	Normal

Notes: N_S denotes the number of switches, N_C denotes number of capacitors, N_L denotes the number of inductors, N_T denotes the number of transformers;
*: D_1=D_2=D

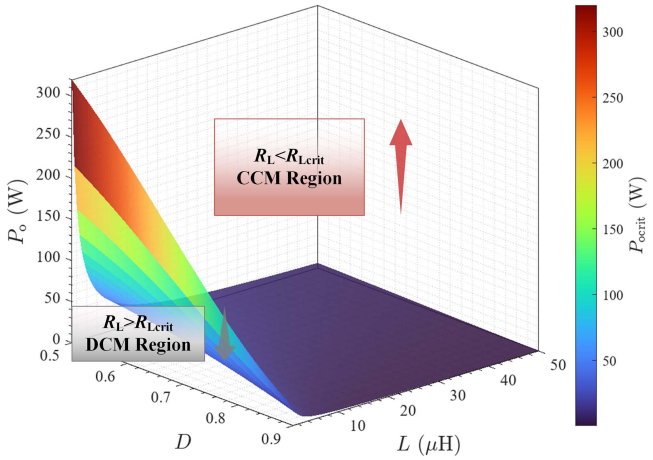


Fig. 6. Operating boundary of LPHS-IBDC between CCM and DCM.

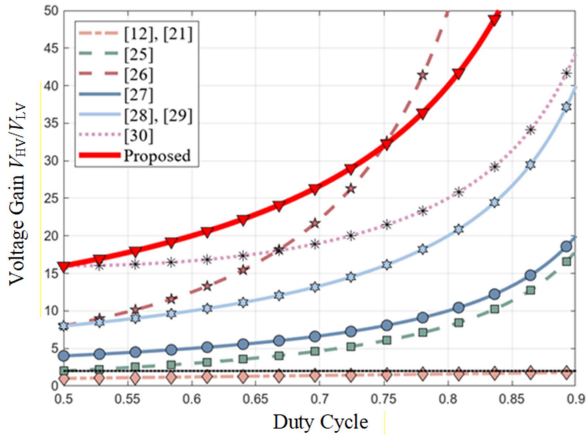


Fig. 7. Voltage gain comparison of different IBDCs with turns ratio $n = 2$.

side switches and controlling complexity. As given in Table I, the proposed LPHS-IBDC employs fewer capacitors and benefits from a simplified control system realization, owing to the common ground on the low-voltage side and the requirement of only four PWM control signals for all switches.

Although four inductors and two transformers are required due to the dual-branch structure, the current sharing inherent to this design provides substantial benefits. Each magnetic element and low-voltage side switch carries only one-fourth of the total current stress ($I_{LV}/4$), compared to conventional single-branch topologies. This significant current reduction translates directly into two major advantages:

1) *Magnetics and Density*: The lower stress allows for a significant downsizing of core cross-section and winding gauge per magnetic element. Consequently, the total magnetic volume is comparable to that of single-branch topologies while simultaneously offering lower conduction loss and improved thermal distribution, leading to a favorable power density.
2) *Switches and Cost*: More importantly, the substantial reduction in the RMS current through each low-voltage side switch not only improves efficiency but also critically enables the use of lower-current-rated (and thus lower-cost) switching devices.

Moreover, as illustrated in Fig. 7, when the transformer turns ratio is fixed at $n = 2$, the converter achieves a high voltage gain without the need for an excessively large duty cycle. These combined characteristics—reduced component stress, lower component cost, and high gain capability—make the proposed topology particularly well-suited for single-cell charging and discharging applications, which demand both high voltage gain and sustained high current levels on the low-voltage side.

IV. PAAS OF THE PROPOSED LPHS-IBDC

The following analysis examines the correlation between the major converter losses and the established state variables. These losses primarily originate from the conduction and switching behavior of the MOSFETs, the copper and core losses of the inductors and transformers, as well as the ESR-related losses of the capacitors.

A. Switching Device Losses

Switching device losses include conduction, switching, and gate driving losses of the MOSFETs. Conduction loss arises from the ON-state resistance of the devices, while switching loss is associated with the nonideal transitions during turn-ON and turn-OFF. Gate driving loss, resulting from the repeated charging and discharging of the MOSFET gate capacitance, is

also taken into account. The corresponding RMS and average current stresses, derived in Section III, form the basis of the quantitative evaluation.

The conduction loss $P_{\rm on}$ of the MOSFET can be expressed as

$$P_{\rm on} = {I_{\rm DS}}^2 R_{\rm ds(on)} D \tag{21}$$

where $I_{\rm DS}$ represents the value of the drain-source current $i_{\rm DS}$ when the MOSFET is fully turned ON, $R_{\rm ds(on)}$ is the on-state resistance, and D is the duty cycle within one switching period. Assuming that during both turn-ON and turn-OFF processes, the variations of $V_{\rm DS}$ and $I_{\rm DS}$ occur simultaneously and are completed synchronously.

The switching loss $P_{\rm sw}$ of the MOSFET can be estimated as

$$P_{\rm sw} = \frac{1}{6} V_{\rm DS} I_{\rm DS} (t_r + t_f) f_s \tag{22}$$

where $V_{\rm DS}$ represents the drain-source voltage when the MOSFET is fully turned OFF, t_r is the rise time during which $i_{\rm DS}$ increases from zero to the $I_{\rm DS}$, t_f is the fall time during which $i_{\rm DS}$ decreases from $I_{\rm DS}$ to zero.

The gate driving loss $P_{\rm dr}$ of the MOSFET can be estimated as

$$P_{\rm dr} = V_{\rm GS} Q_g f_s \tag{23}$$

where $V_{\rm GS}$ represents the drive voltage of the MOSFET , and Q_g is the total gate charge of the MOSFET.

Let the inductor current of the low-voltage side branch corresponding to duty cycle D_1 be I_{D1}, with the ON-resistance of the MOSFETs $R_{\rm on1}$, rise time t_{r1}, the fall time is t_{f1} and the total gate charge is Q_{g1}. Similarly, for the branch corresponding to D_2, the corresponding parameters are $I_{\rm D2}$, $R_{\rm on1}$, t_{r2}, t_{f2}, and Q_{g2}. On the high-voltage side, the parameters for the upper and lower switches are characterized by $R_{\rm on3}$, t_{r3}, t_{f3}, and Q_{g3} and by $R_{\rm on4}$, t_{r4}, t_{f4}, and Q_{g4}, respectively.

From Fig. 3(c), combined with (13), the drain-source voltage $V_{\rm DS1}$ of the low-voltage side MOSFETs with duty cycle D_1 (i.e., $S_{\rm p1}$ and $S_{\rm p3}$) during turn-OFF can be expressed as

$$\begin{aligned} V_{\rm DS1} &= \frac{1}{2n}(V_{\rm HV} - V_{\rm C2}) = \frac{1}{2n} \cdot \frac{2n}{1-D_1} V_{\rm Bat} \\ &= \frac{1}{1-D_1} V_{\rm Bat}. \end{aligned} \tag{24}$$

Considering that the drain-source currents of $S_{\rm p1}$ and $S_{\rm p3}$ satisfy $I_{\rm DS1} = I_{D1}$ in stages I and IV, and $I_{\rm DS1} = I_{D1} + I_{\rm D2}$ in stage II, the main losses of $S_{\rm p1}$ and $S_{\rm p3}$ can be estimated as the sum of conduction loss and switching loss

$$\begin{aligned} P_{\rm Sp1,3} &= 2I_{D1}^2 R_{\rm on1}(D_1 + D_2 - 1) + 2(I_{D1} + I_{D2})^2 \\ &\quad \times R_{\rm on1}(1 - D_2) \\ &\quad + \frac{1}{6}\frac{1}{1-D_1} V_{\rm Bat} I_{D1}(t_{r1} + t_{f1}) f_s + V_{\rm GS} Q_{g1} f_s. \end{aligned} \tag{25}$$

From Fig. 3(b), combined with (13), the drain-source voltage $V_{\rm DS2}$ of the low-voltage side MOSFETs with D_2 (i.e., $S_{\rm p2}$ and $S_{\rm p4}$) during turn-OFF can be expressed as

$$V_{\rm DS2} = \frac{1}{2n} V_{\rm C2} = \frac{1}{2n} \cdot \frac{2n}{1-D_2} V_{\rm Bat} = \frac{1}{1-D_2} V_{\rm Bat}. \tag{26}$$

Considering that $i_{\rm DS}$ of $S_{\rm p2}$ and $S_{\rm p4}$ satisfy $I_{\rm DS2} = I_{\rm D2}$ in stages I and IV, and $I_{\rm DS2} = I_{D1} + I_{\rm D2}$ in stage V, the main losses of $S_{\rm p2}$ and $S_{\rm p4}$ can be estimated as

$$\begin{aligned} P_{\rm Sp2,4} &= 2I_{D2}^2 R_{\rm on2}(D_1 + {\rm D}_2 - 1) + 2(I_{D1} + I_{D2})^2 \\ &\quad \times R_{\rm on2}(1 - D_1) \\ &\quad + \frac{1}{6}\frac{1}{1-D_2} V_{\rm Bat} I_{D2}(t_{r2} + t_{f2}) f_s + V_{\rm GS} Q_{g2} f_s. \end{aligned} \tag{27}$$

Based on the previous analysis, when transitioning from stage IV to stage V, the upper switch $S_{\rm s1}$ on the high-voltage side conducts. Before conduction, the drain-source voltage of $S_{\rm s1}$ satisfies $V_{\rm DS3} = V_{\rm HV}/2$. After conduction, the drain-source current satisfies $I_{\rm DS3} = I_{\rm D1}/n$. Therefore, the main losses of $S_{\rm s1}$ can be estimated as

$$\begin{aligned} P_{\rm Ss1} &= \frac{1}{n^2} I_{\rm D1}^2 R_{\rm on3}(1 - D_1) + \frac{1}{12n} V_{\rm HV} I_{D1}(t_{r3} + t_{f3}) f_s \\ &\quad + V_{\rm GS} Q_{g3} f_s. \end{aligned} \tag{28}$$

Similarly, the main losses of $S_{\rm s2}$ can be estimated as

$$\begin{aligned} P_{\rm Ss2} &= \frac{1}{n^2} I_{\rm D2}^2 R_{\rm on4}(1 - D_2) + \frac{1}{12n} V_{\rm HV} I_{D2}(t_{r4} + t_{f4}) f_s \\ &\quad + V_{\rm GS} Q_{g4} f_s. \end{aligned} \tag{29}$$

B. Inductor Losses

Inductor losses are primarily composed of winding loss $P_{L\rm win}$ caused by winding resistance and core loss $P_{L\rm core}$ due to alternating flux.

The major loss P_L of inductor can be expressed as

$$P_L = {I_L}^2 R_w + k_1 {f_s}^{\alpha_1} V_L {B_L}^{\beta_1} \tag{30}$$

where I_L represents the RMS current passing through the inductor, R_w is the winding resistance of the inductor, parameters k_1, α_1, and β_1 are coefficients of the magnetic core material, V_L is the volume of the inductor core, and B_L is determined by the peak-to-peak current ripple.

Assuming the four inductors on the low-voltage side are completely identical, with consistent parameters R_w, k_1, α_1, β_1, $V_{\rm L}$, and B_L, the branch inductor current corresponds to duty cycle D_1, and D_2 remains I_{D1} and $I_{\rm D2}$, then the main loss of inductor L_1 and L_3 can be estimated as

$$P_{\rm L1,3} = 2I_{D1}^2 R_w + 2k_1 {f_s}^{\alpha_1} V_L {B_L}^{\beta_1} \tag{31}$$

the main loss of inductor L_2 and L_4 can be estimated as

$$P_{\rm L2,4} = 2I_{D2}^2 R_w + 2k_1 {f_s}^{\alpha_1} V_L {B_L}^{\beta_1}. \tag{32}$$

C. Transformer Losses

Transformer losses primarily consist of winding loss $P_{T\rm win}$ in the windings and core loss $P_{T\rm core}$ induced by alternating magnetic flux.

The major loss P_T of inductor can be expressed as

$$P_T = {I_T}^2 R_T + k_2 {f_s}^{\alpha_2} V_T {B_T}^{\beta_2} \tag{33}$$

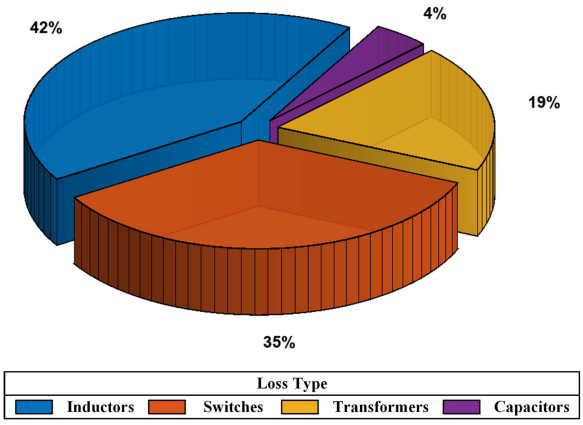


Fig. 8. Loss distribution of the proposed LPHS-IBDC.

where I_T denotes the RMS current of the transformer windings, R_T is the equivalent winding resistance, k_2, α_2, and β_2 are coefficients associated with the magnetic core material, V_T is the volume of the transformer core, and B_T is determined by the applied voltage and the switching frequency.

Assuming a symmetrical configuration and an identical core structure, the transformer experiences equal flux excitation in both half cycles, and the winding currents are determined by the duty cycles D_1 and D_2. Accordingly, the primary and secondary copper losses can be evaluated based on their respective RMS currents, while the total core loss is uniformly distributed across the magnetic core. Therefore, the main loss of transformers can be estimated as

$$P_T = 2I_{D1}^2 R_T(1-D_1) + 2I_{D2}^2 R_T(1-D_2) + 2k_2 {f_s}^{\alpha_2} V_T {B_T}^{\beta_2}. \tag{34}$$

D. Capacitor Losses

Capacitor losses are mainly attributed to the equivalent series resistance (ESR) associated with the capacitor.

The major loss P_C of the capacitor can be expressed as

$$P_C = I_C^2 R_C \tag{35}$$

where I_C denotes the RMS current flowing through the capacitor, R_T represents the ESR of the device, the main loss of capacitors can be estimated as

$$P_C = \frac{1}{n^2} I_{D1}^2 R_C(1-D_1) + \frac{1}{n^2} I_{D2}^2 R_C(1-D_2). \tag{36}$$

Based on the above analysis, by substituting the steady-state parameters of the converter under rated power, the theoretical loss values of the converter can be calculated. The proportion of losses in each part of the converter is shown in Fig. 8. As shown in Fig. 8, while inductor losses constitute the largest portion, switching device losses still account for more than one-third of the total loss. Since these losses are highly dependent on current distribution and device characteristics, their reduction presents a significant opportunity for improving efficiency.

The overall converter performance is directly governed by the combined loss components, which are closely correlated with the branch current distribution. Utilizing this correlation, actively allocating the load current among switches with varying performance characteristics is an effective method to balance system cost and efficiency. The proposed active power allocation strategy is specifically developed to leverage this principle. Under the constraint of maintaining continuous inductor current, this strategy establishes the minimization of the overall power loss as its primary optimization objective. This objective directly addresses the dependence of power loss on current distribution, thereby forming the basis for the proposed active power allocation strategy, the analysis and derivation of which are detailed in the following section.

The total predicted conduction and switching losses $P_{\rm loss}$ of the converter's MOSFETs can be deduced as

$$\begin{aligned} P_{\rm loss} &= P_{\rm Sp1,3} + P_{\rm Sp2,4} + P_{\rm Ss1} + P_{Ss2} + P_L + P_T + P_C \\ &= \frac{2K_{R1}K_{\rm I}^2 + K_{R2}K_{\rm I}^2 + K_{R3}K_{\rm I}^2 + K_{U3}K_{\rm I}}{1-D_1} \\ &\quad + \frac{2K_{R2}K_{\rm I}^2 + K_{R1}K_{\rm I}^2 + K_{R4}K_{\rm I}^2 + K_{U4}K_{\rm I}}{1-D_2} \\ &\quad + \frac{K_{U1}K_{\rm I} + K_l K_{\rm I}^2}{(1-D_1)^2} + \frac{K_{U2}K_{\rm I} + K_l K_{\rm I}^2}{(1-D_2)^2} \\ &\quad + \frac{D_1(K_{R1}K_{\rm I}^2)}{(1-D_1)^2} + \frac{D_2(K_{R2}K_{\rm I}^2)}{(1-D_2)^2} + A \\ &\text{s.t.} \begin{cases} \left(\frac{2n}{1-D_1} + \frac{2n}{1-D_2}\right) V_{\rm Bat} = \frac{V_{\rm HV}}{k} \\ 0.5 < D_1, D_2 < 1 \end{cases} \end{aligned} \tag{37}$$

where k<1 represents the non-ideal coefficient introduced to refine (13), $K_{\rm I} = nV_{\rm HV}/R_L$, $K_{R1} = 2R_{\rm on1}$, $K_{R2} = 2R_{\rm on2}$, $K_{R3} = (R_{\rm on3}+R_C)/n^2+2R_T$, $K_{\rm R4} = (R_{\rm on4}+R_C)/n^2+2R_T$, $K_l = 2R_w$, $K_{U1} = V_{\rm Bat}f_s(t_{r1}+t_{f1})/6$, $K_{U2} = V_{\rm Bat}f_s(t_{r2}+t_{f2})/6$, $K_{U3} = V_{\rm HV}f_s(t_{r3}+t_{f3})/(12n)$, $K_{U4} = V_{\rm HV}f_s(t_{r4}+t_{f4})/(12n)$, and A is the constant loss term, including losses that are less sensitive to the branch currents I_{D1} and $I_{\rm D2}$, such as gate drive losses and the core losses of the inductor and transformer.

From (37), the relationship between the duty cycles D_1 and D_2 of different branches and the total loss $P_{\rm loss}$ can be obtained. This relationship is illustrated in Fig. 9. According to Fig. 9, there exists an optimal combination of duty cycles D_1 and D_2 that minimizes $P_{\rm loss}$, providing a basis for active current distribution to improve converter efficiency.

Equation (37) can be reduced as

$$\begin{aligned} P_{\rm loss} &= (K_1+K_3)x_1^2 + (K_2+K_4)x_2^2 + (K_5-K_3)x_1 \\ &\quad + (K_6-K_4)x_2 \\ &\text{s.t.} \begin{cases} x_1 + x_2 = \frac{V_{\rm HV}}{2nkV_{\rm Bat}} = S \\ x_1, x_2 > 2 \end{cases} \end{aligned} \tag{38}$$

where $x_1 = 1/(1\text{-}D_1)$, $x_2 = 1/(1\text{-}D_2)$, $K_1 = K_{\rm U1}K_{\rm I}$, $K_2 = K_{\rm U2}K_{\rm I}$, $K_3 = K_{\rm on1}K_{\rm I}^2$, $K_4 = K_{\rm on2}K_{\rm I}^2$, $K_5 = K_{\rm on2}K_{\rm I}^2+K_{\rm on3}K_{\rm I}^2+2K_{\rm on1}K_{\rm I}^2+K_{\rm U3}K_{\rm I}$, $K_6 = K_{\rm on1}K_{\rm I}^2+K_{\rm on4}K_{\rm I}^2+2K_{\rm on2}K_{\rm I}^2+K_{\rm U4}K_{\rm I}$.

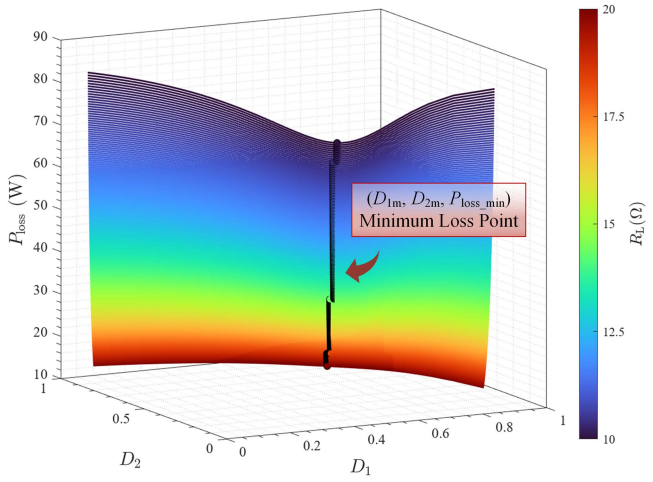


Fig. 9. Relationship curves among P_{loss}, D_1 and D_2.

Substituting the first constraint of (38) into the attrition equation yields

$$P_{\text{loss}} = (K_1+K_2+K_3+K_4)x_1^2+(K_5-K_6-K_3+K_4)x_1 - 2S(K_2+K_4)x_1+(K_2+K_4)S^2+(K_6-K_4)S. \tag{39}$$

Equation (39) is a quadratic equation, so the combinations of x_1 and x_2, i.e., the duty cycles D_1 and D_2 of the different branches, that minimize the estimated main losses of the MOSFET can be determined as follows:

$$x_1 = -\frac{K_1-K_2-K_5+K_6-2S(K_4+K_6)}{2(K_3+K_4+K_5+K_6)}$$
$$x_2 = \frac{K_1-K_2-K_5+K_6+2S(K_3+K_5)}{2(K_3+K_4+K_5+K_6)}. \tag{40}$$

From the above theoretical analysis, it can be concluded that selecting an appropriate combination of duty cycles D_1 and D_2, along with actively distributing power among different branches, can minimize the overall losses of the converter. Furthermore, when the performance disparity among the switching devices is more pronounced, the converter exhibits a more significant improvement in efficiency.

V. Experimental Verification

The typical voltage of commercially available single cells is approximately 3.2 V, while the supply voltage for dc loads such as two-wheeled electric vehicles and residential energy storage systems is generally 48 V. Therefore, an experimental prototype with a low-voltage side of 3.2 V (V_{LV}) and a high-voltage side of 48 V (V_{HV}), as illustrated in Fig. 10, has been constructed to validate the operating principle of the proposed LPHS-IBDC and to evaluate the impact of the proposed active power control strategy on converter efficiency. The corresponding experimental parameters are given in Table II.

The experimental waveforms of the converter operating in discharge-boost mode under full load conditions ($P_o = 250$W, $V_{\text{LV}} = 3.2$ V, and $V_{\text{HV}} = 48$ V) are shown in Fig. 11, while those in buck mode are presented in Fig. 12.

Fig. 11(a) shows the gate-source voltages v_{gs_Sp1} and v_{gs_Sp2}, and the drain-source voltages v_{ds_Sp1} and v_{ds_Sp2} of the low-voltage side switches S_{p1}, S_{p3} and S_{p2}, S_{p4}, respectively. Fig. 11(b) presents the gate-source voltages v_{gs_Ss1} and v_{gs_Ss2}, as well as the drain-source voltages v_{ds_Ss1} and v_{ds_Ss2} of the high-voltage side switches S_{s1} and S_{s2}. Fig. 11(c) shows the transformer primary-side voltage v_{Tp1}, the high-voltage bus voltage v_{HV}, and the voltage across the high-voltage side isolation capacitor v_{C2}. From Fig. 11(a) and (b), it can be observed that S_{p1}, S_{p3} and S_{p2}, S_{p4} operate in an interleaved manner, and the gate signals v_{gs_Sp1} and $v_{\text{gs\_Sp2}}$ are complementary to v_{gs_Ss1} and v_{gs_Ss2}. As shown in Fig. 9(a) and (c), during the turn-OFF period, the effective values of v_{ds_Sp1} and v_{ds_Sp2} are equal to the transformer primary-side voltage v_{Tp1}, which is $V_{\text{HV}}/4n$. The effective voltage of the high-voltage side isolation capacitor v_{C2} is equal to $V_{\text{HV}}/2$, which agrees with the theoretical analysis.

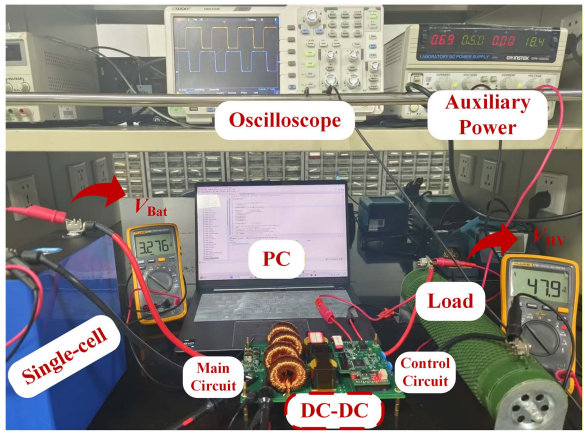


Fig. 10. Experimental prototype of the proposed LPHS-IBDC.

TABLE II
Experimental Parameters of the LPHS-IBDC Prototype

Parameters	Value
Single-cell battery voltage V_{Bat}	3.2 V
High-side voltage V_{HV}	48 V
Rating Power P_{n}	250 W
Switching frequency f_{s}	50 kHz
Transformer turns ratio n	1.5
Excitation inductance L_{m1}, L_{m2}	20 μH
Leakage inductance L_{s1}, L_{s2}	200 nH
Inductors L_1-L_4	15 uH
Capacitor C_1	600 μF
Isolation capacitor C_2	4 μF
Capacitor C_3	100 μF
Low-voltage side switches S_{p1}, S_{p3}	HYG011N04LS1TA (USD 0.61/unit) $R_{on1} = 0.9$ mΩ@10 V; $t_{r1} = 72$ ns; $t_{f1} = 92$ ns
Low-voltage side switches S_{p2}, S_{p4}	FDBL0065N40 (USD 4.73/unit) $R_{on2} = 0.5$ mΩ@10 V; $t_{r2} = 82$ ns; $t_{f2} = 52$ ns
High-voltage side switches S_{s1}, S_{s2}	IPB048N15N5 (USD 3.11/unit) $R_{on3}/R_{on3} = 4.8$ mΩ@10 V; $t_{r3}/t_{r4} = 5.3$ ns; $t_{f3}/t_{f4} = 4.5$ ns

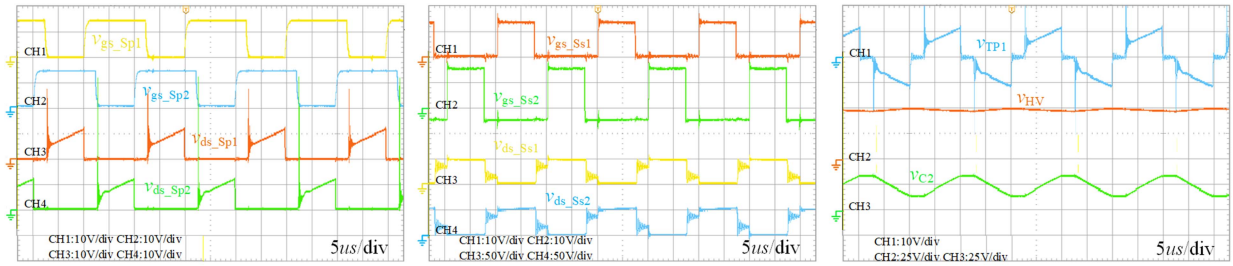


Fig. 11. Experimental waveforms of the converter operating in discharge boost mode at $P_o = 250$ W. (a) $v_{\rm gs}$ and $v_{\rm ds}$ of $S_{\rm p1}$ and $S_{\rm p2}$. (b) $v_{\rm gs}$ and $v_{\rm ds}$ of $S_{\rm s1}$ and $S_{\rm s2}$. (c) $v_{\rm Tp1}$, $v_{\rm HV}$ and $v_{\rm C2}$.

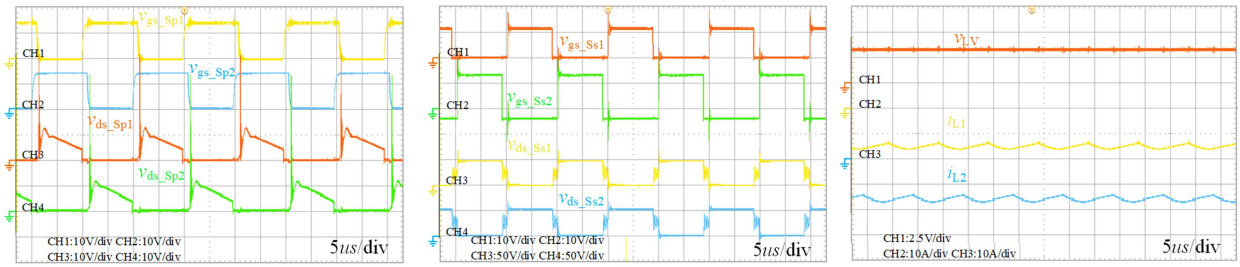


Fig. 12. Experimental waveforms of the converter operating in charge buck mode at $P_o = 250$ W. (a) $v_{\rm gs}$ and $v_{\rm ds}$ of $S_{\rm p1}$ and $S_{\rm p2}$. (b) $v_{\rm gs}$ and $v_{\rm ds}$ of $S_{\rm s1}$ and $S_{\rm s2}$. (c) $v_{\rm LV}$, $i_{\rm L1}$ and $i_{\rm L2}$.

Due to the large current on the low-voltage side, the high *di/dt* during switching-OFF causes noticeable voltage spikes on the drain-source voltages of the low-voltage side switches as shown in Figs. 11(a) and 12(a). These spikes contribute slightly to additional switching losses, but remain within the safe voltage margin considered during device selection. Although the leakage inductance is exceptionally small compared to the magnetizing inductance (1% as detailed in Table II), its stored energy can resonate with the device parasitic capacitances during turn-OFF, leading to the observed overshoot in $v_{\rm ds}$ waveforms. It is also noted that in Fig. 11(b), due to the junction capacitance of $S_{\rm s1}$ and S_{s3}, high-frequency oscillations appear in v_{ds_Ss1} and v_{ds_Ss2} during the turn-OFF process. Future optimization will focus on transformer design enhancements to further reduce leakage inductance. This includes optimization of the sector winding layout, investigation into magnetic integration techniques, and the potential adoption of planar transformer structures. These measures are expected to effectively suppress voltage spikes and further enhance the long-term reliability of the converter [32].

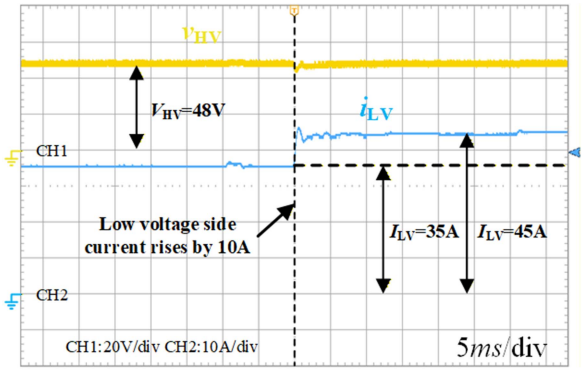
Fig. 12(a) shows v_{gs_Sp1} and v_{gs_Sp2}, as well as v_{ds_Sp1} and v_{ds_Sp2} of switches $S_{\rm p1}$, $S_{\rm p3}$ and $S_{\rm p2}$, $S_{\rm p4}$ during charging. Fig. 12(b) presents v_{gs_Ss1} and v_{gs_Ss2}, along with v_{ds_Ss1} and v_{ds_Ss2} of switches $S_{\rm s1}$ and $S_{\rm s2}$. Fig. 12(c) illustrates the waveforms of the low-voltage side output voltage $v_{\rm LV}$ and the inductor currents i_{L1} and i_{L2}. As shown in Fig. 12(c), the converter steps down the high-side 48 to 3.2 V to charge a single cell. The interleaved inductor currents i_{L1} and i_{L2} help to reduce the ripple in the charging current. Meanwhile, the average values of the inductor currents satisfy the relationship $I_{L1} = I_{L2} = I_{L3} = I_{L4} = I_{\rm Bat}/4 = P/(4v_{\rm LV})$, indicating balanced current sharing among the branches.

By designing the requisite sampling circuits and implementing a voltage closed-loop control program, the converter achieved a stable 48 V output voltage. Fig. 13(a) and (b) illustrate the dynamic response waveform of the output voltage during sudden load changes under this closed-loop operation.

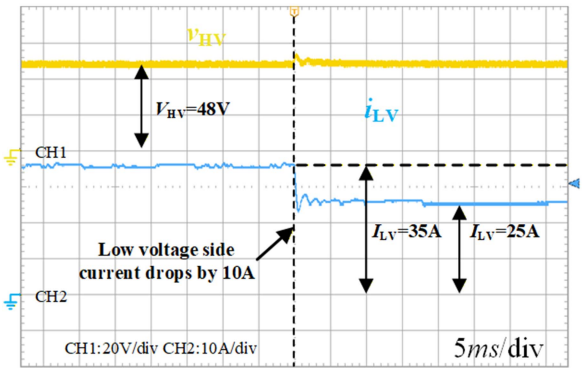
To verify the effectiveness of the PAAS in improving converter efficiency and its cost-effectiveness, different low-voltage side MOSFETs were strategically selected for implementation, as given in Table II. Specifically, the FDBL0065N40 utilized for switches $S_{\rm p2}$ and $S_{\rm p4}$ exhibits significantly superior conduction and switching performance compared to the HYG011N04LS1TA utilized for switches $S_{\rm p1}$ and $S_{\rm p3}$, despite sharing the same nominal ratings (40 V rated voltage and 300 A rated current). However, its higher unit price, which significantly increases overall material costs, motivates the adoption of a mixed-device implementation.

This mixed-device approach achieves a substantial cost reduction, which is visually confirmed by the cost distribution pie charts in Fig. 14. These charts illustrate the detailed breakdown of the total bill of materials cost, specifically showing the cost share of major components, such as the auxiliary power supply, gate drivers, capacitors, inductors, transformers, and switching devices. The total material cost decreases from USD 43.87 (uniform device configuration) to USD 35.63 (mixed device configuration), yielding an 18.78% reduction. Crucially, the cost share of the switching devices, which was the largest component, dropped from 58% before mixing to 47% after mixing, thereby freeing up budget for other critical components or further system-level optimization.

Furthermore, by actively controlling the duty cycles based on the characteristics of each device, the power flow in different



(a)



(b)

Fig. 13. Dynamic response waveform of V_{HV} during sudden load changes. (a) Load current rises. (b) Load current drops.

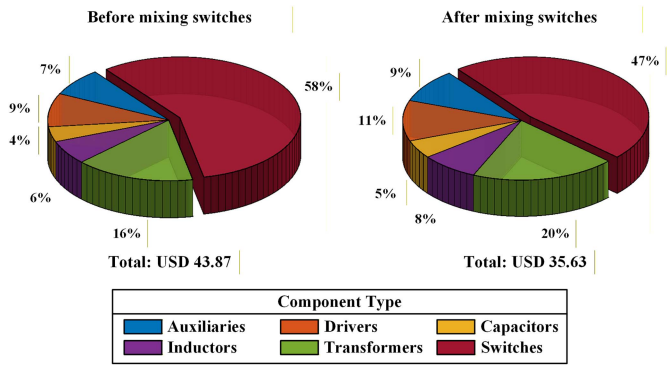


Fig. 14. Cost distribution of LPHS-IBDC.

branches can be dynamically allocated. This method effectively reduces the overall switching and conduction losses of MOSFETs, thereby improving the converter's overall efficiency while operating under the mixed-device structure.

With the V_{Bat} maintained at 3.2 V and the V_{HV} maintained at 48 V, the duty cycles of the MOSFETs and the corresponding converter efficiencies at various power levels are given in Table III. Fig. 15 illustrates the effectiveness of the proposed active power allocation strategy in distributing the load across different branches under rated power conditions. Specifically, the duty cycle D_1 of MOSFET S_{p1} is smaller than the duty cycle D_2 of S_{p2}, leading to a higher RMS inductor current in the

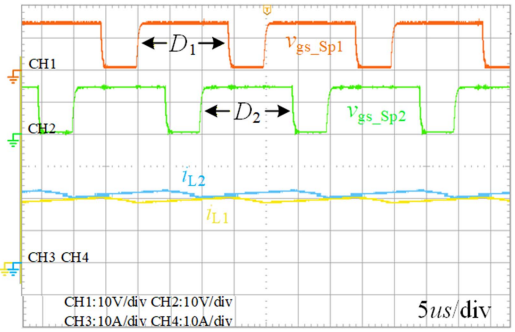


Fig. 15. Key waveforms of the converter with PAAS.

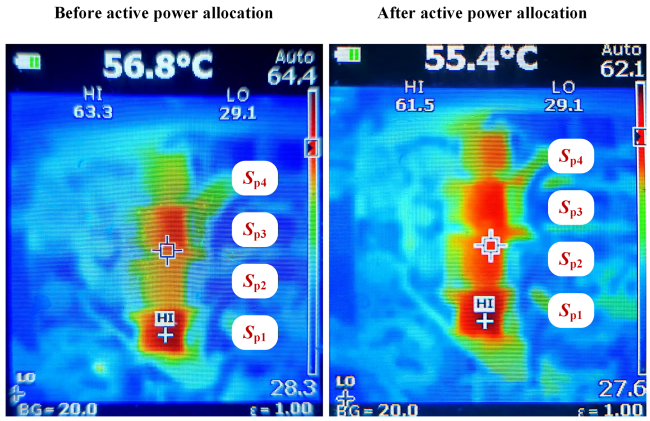


Fig. 16. Switch temperature distribution with and without PAAS.

branch containing S_{p2}. Consequently, the conduction current of the MOSFET associated with I_{L2} is greater than that of I_{L1}.

This active power distribution directly contributes to thermal management, as evidenced by the thermal images presented in Fig. 16. Before applying the active allocation strategy, the temperatures of switches were notably uneven, the lower-performance switches S_{p1} and S_{p3} generated significantly more heat, resulting in higher temperatures. Crucially, after implementing the active power allocation strategy, the temperature distribution across the switches becomes significantly more uniform. By diverting a larger current through the superior performing switches S_{p2} and S_{p4}, the heat generated on the different MOSFETs becomes more closely matched. Therefore, the proposed active power allocation strategy serves as an effective loss and thermal equalization scheme for the mixed-device converter.

To evaluate the efficiency improvement provided by the proposed active power allocation strategy, the converter efficiency was measured at five discrete power levels ranging from 50 W to 250 W. The resulting efficiency curves for the three operational modes are detailed in Fig. 17, with specific numerical data given in Table III. As demonstrated in Fig. 17, the introduction of lower-performance MOSFETs in the mixed-device topology initially led to a substantial average efficiency degradation of 2.77%, primarily caused by the resulting increase in conduction and switching losses. However, following the implementation

TABLE III
EFFICIENCY COMPARISON WITH AND WITHOUT PAAS

		Uniform Device Configuration		Mixed Device Configuration				
				Without PAAS		With PAAS		
Power	I_{Bat_max}	$D_1 = D_2$	Efficiency	$D_1 = D_2$	Efficiency	D_1	D_2	Efficiency
50 W	22.8 A	0.60	75.10%	0.60	68.60%	0.595	0.613	71.40%
100 W	36.0 A	0.61	89.50%	0.61	86.91%	0.602	0.618	88.10%
150 W	52.1 A	0.63	91.26%	0.63	89.95%	0.619	0.636	90.40%
200 W	70.5 A	0.66	89.95%	0.667	88.67%	0.656	0.672	89.37%
250 W	92.2 A	0.72	86.86%	0.73	84.70%	0.722	0.734	85.66%

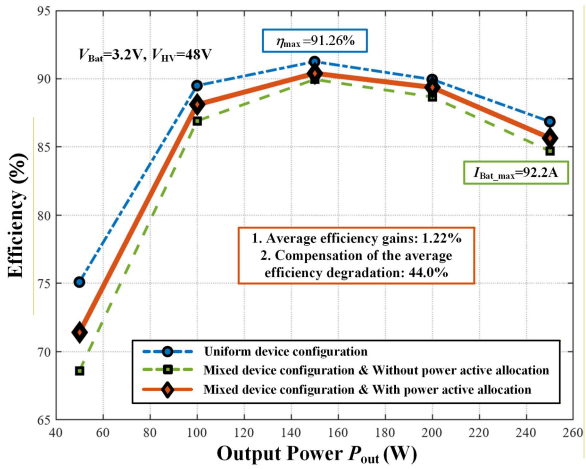


Fig. 17. Efficiency comparison of the converter with and without PAAS.

of the active power allocation strategy, the overall converter efficiency increased by an average of 1.22% compared to the unoptimized mixed topology. Quantitative results demonstrate that the active allocation approach compensates for 44.0% of the efficiency degradation resulting from the use of heterogeneous devices (44.0% = 1.22%/2.77%). This result rigorously validates the effectiveness of the proposed strategy in recovering and optimizing the efficiency performance of switch device mixing topologies.

VI. CONCLUSION

In this article, a low-voltage-side parallel high-voltage-side series LPHS-IBDC for single battery cell applications is proposed. The proposed topology offers high voltage gain, a lower required transformer turns ratio, and significantly reduced RMS current in both the low-voltage side switches and magnetic elements, making it well-suited for low-voltage, high-current scenarios such as single-cell charging and discharging. This substantial reduction in RMS current not only improves efficiency but also directly lowers the cost of the converter by allowing the selection of lower-current-rated switches, while simultaneously enhancing power density through the downsizing of individual magnetic elements. Furthermore, a PAAS is introduced as a key measure to compensate for the mixed use of high-performance and cost-optimized switches. By dynamically redistributing the branch power through duty cycle modulation, the strategy mitigates the additional conduction and switching losses caused by the lower-performance devices, thereby recovering part of the efficiency that would otherwise be lost. Experimental results validate both the feasibility of the proposed topology and the effectiveness of the power allocation strategy, demonstrating an average efficiency improvement of 1.22%. The proposed active allocation strategy yields a 44.0% compensation for the average efficiency degradation caused by device mixing, achieving this recovery relative to the high-performance benchmark peak efficiency of 91.26%.

APPENDIX

$$A_1 = \begin{bmatrix} 0 & \dots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & \frac{-1}{R_L C_3} & 0 \\ 0 & \dots & 0 & 0 & 0 \end{bmatrix},$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL_m} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL_m} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_L C_3} & 0 \\ 0 & \frac{1}{2nC_2} & 0 & \frac{1}{2nC_2} & \frac{1}{2nC_2} & \frac{1}{2nC_2} & 0 & 0 \end{bmatrix},$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL} & \frac{1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{2nL} & \frac{1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2nL_m} & \frac{-1}{2nL_m} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2nL_m} & \frac{-1}{2nL_m} \\ \frac{1}{2nC_3} & 0 & \frac{1}{2nC_3} & 0 & \frac{-1}{2nC_3} & \frac{-1}{2nC_3} & \frac{-1}{R_L C_3} & 0 \\ \frac{-1}{2nC_2} & 0 & \frac{-1}{2nC_2} & 0 & \frac{1}{2nC_2} & \frac{1}{2nC_2} & 0 & 0 \end{bmatrix},$$

$$B_1 = B_2 = B_3 == \begin{bmatrix} \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad \text{(A1)}$$

$$A = (D_1 + D_2 - 1)A_1 + (1 - D_1)A_2 + (1 - D_2)$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_1}{-2nL} & \frac{1-D_1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_2}{-2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_1}{-2nL} & \frac{1-D_1}{2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_2}{-2nL} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_1}{2nL_m} & \frac{1-D_1+1-D_2}{-2nL_m} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_1}{2nL_m} & \frac{1-D_1+1-D_2}{-2nL_m} \\ \frac{1-D_1}{2nC_3} & 0 & \frac{1-D_1}{2nC_3} & 0 & \frac{1-D_1}{-2nC_3} & \frac{1-D_1}{-2nC_3} & \frac{-1}{R_L C_3} & 0 \\ \frac{1-D_1}{-2nC_2} & \frac{1-D_2}{2nC_2} & \frac{1-D_1}{-2nC_2} & \frac{1-D_2}{2nC_2} & \frac{1-D_1+1-D_2}{2nC_2} & \frac{1-D_1+1-D_2}{2nC_2} & 0 & 0 \end{bmatrix}.$$

$$B = (D_1 + D_2 - 1)B_1 + (1 - D_1)B_2 + (1 - D_2)B_3 = \begin{bmatrix} \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad \text{(A2)}$$

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Jiahao Wang was born in Shenzhen, China, in 2001. He received the B.S. degree in electrical engineering and automation in 2023 from South China University of Technology, Guangzhou, China, where he is currently working toward the M.S. degree in power electronics with the School of Electric Power Engineering

His research interests include high gain bidirectional dc–dc converters and electric spring applications.

Dongyuan Qiu (Senior Member, IEEE) was born in China, in 1972. She received the B.Sc. and M.Sc. degrees in automation from the South China University of Technology, Guangzhou, China, in 1994 and 1997, respectively, and the Ph.D. degree in electronic engineering from the City University of Hong Kong, Kowloon, Hong Kong, in 2002.

She is currently a Professor with the School of Electric Power, South China University of Technology. She has authored or co-authored 5 books, and more than 200 papers and holds more than 100 patents. Her research interests include wireless power transfer, fault diagnosis, and sneak circuit analysis of power electronic systems.

Dr. Qiu is an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS.

Yangbin Zeng (Member, IEEE) received the B.Sc. degree in building electrical and intelligent from Xiangtan University, Xiangtan, China, in 2015, and the Ph.D. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2021.

From 2021 to 2024, he was a Post-Doctoral Researcher with the Department of Electrical Engineering, Tsinghua University, Beijing, China. From 2023 to 2024, he was a Post-Doctoral Researcher at the City University of Hong Kong, Hong Kong, SAR of China. He is currently an Associate Professor with the School of Electric Power, South China University of Technology, Guangzhou, China. His current research interests include real-time simulation, power router, and soft-switching techniques.

Bo Zhang (Fellow, IEEE) was born in Shanghai, China, in 1962. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1982, the M.S. degree in power electronics from Southwest Jiaotong University, Chengdu China, in 1988, and the Ph.D. degree in power electronics from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1994.

He is currently a Professor with the School of Electric Power, South China University of Technology, Guangzhou, China. He has authored or co-authored more than 600 papers and held more than 230 patents. He has authored 12 monographs. His research interests include nonlinear analysis and control of power electronics, wireless power transfer technology and ac drives.

Yukun Chen was born in Fujian, China, in 2001. He received the B.E. degree in electrical engineering and automation from Fuzhou University, Fujian, China, in 2023. He is currently working toward the M.S. degree in power electronics with the School of Electric Power Engineering, South China University of Technology, Guangzhou, China.

His research interests include power electronic converters and fractional order dc–dc converter.