Analytical Thermal Modeling and Arrangement Optimization Design Method for Hybrid Capacitor Banks Considering Thermal Transient and PCB Mounting Modes

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***Abstract*—Accurate and rapid thermal distribution acquisition is essential for the reliability assessment and enhancement of hybrid capacitor banks (HCBs). Current thermal models lack transient temperature estimation capability and do not account for effects of capacitor types and printed circuit board (PCB) mounting modes, which increases errors in estimating HCB temperature and lifetime. Therefore, this article proposes a transient analytical thermal modeling method for HCBs. First, the equivalent thermal capacitance is incorporated into the steady-state state-space equations, enabling the model to describe transient thermal processes. Subsequently, shape-specific factors are incorporated into the thermal model to characterize the thermal coupling relationships between different types of capacitors. Furthermore, PCB mounting is integrated into the thermal model, enhancing its applicability to operational conditions. Finally, a staggered arrangement optimization design method for uniform thermal distribution is proposed, which mitigates premature aging caused by temperature imbalances. It is verified that the proposed thermal model reduces the temperature error to less than 5%, and the proposed optimal arrangement design method increases the lifetime of the E-cap by 12.1%.**

***Index Terms*—Arrangement optimization, hybrid capacitors bank (HCB), printed circuit board (PCB), reliability, thermal network model.**

I. Introduction

HIGH power converters have been widely used in energy conversion systems such as renewable energy generation [1], [2], electric vehicles [3], and railways [4]. In these converters, an individual capacitor in the dc-link is insufficient to effectively filter voltage ripple, balance input-output power transients, and maintain stable bus voltage. Therefore, capacitor banks consisting of multiple capacitors connected in series and/or parallel configurations have been proposed for the dc-link [5], [6]. Today, capacitor banks are generally categorized into two types, that is, homogeneous electrolytic capacitor banks and hybrid capacitor banks (HCBs). HCBs are composed of multiple types of capacitor (e.g., electrolytic and film capacitors) and offer more advantages than electrolytic capacitor banks, such as highly stable capacitance (exhibiting only 1% variation within the 1 MHz range [7]), high power density, wide operational frequency band, and low cost [8], [9], [10]. However, HCBs are failure-prone under thermal stress, leading to reduced system reliability. Improving the reliability of HCBs through monitoring, assessment, and thermal analysis, as well as optimizing their arrangement design is a significant research topic that has attracted increasing attention in high-power conversion [11], [12], [13], [14], [15].

Electrical and thermal stress analysis is critical for precisely assessing the reliability of HCBs [4], [16]. In fact, electrical stress is readily quantified via the ripple current root mean square (RMS) value [17]. However, compared with electrolytic capacitor banks, effective methods for rapid and precise calculation of thermal stress in HCBs are still lacking. Moreover, thermal analysis in HCBs is more complex than in traditional banks because disparate power losses arise from different types of capacitors, combined with thermal coupling among multiple uneven heat sources. In addition, modeling HCB thermal stress cannot be treated as a linear superposition of individual capacitor effects. Furthermore, variations in cooling conditions, capacitor types, and packaging geometries result in complex uneven heat distribution, which leads to differential degradation rates among capacitors, and this uneven heat distribution adversely affect thermal stress. Therefore, it is significant to accurately and rapidly analyze the thermal distribution for assessing the reliability of HCBs.

Currently, the main methods for analyzing the thermal distribution of capacitor banks are the direct temperature measurement method [18], [19], the finite-element method (FEM) [20], [21], and the thermal network model method [9], [13]. The direct temperature measurement method is more accurate than other methods and can capture real-time features by using testing devices such as thermocouples and infrared thermal cameras. However, this method increases testing costs and intrusively

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modifies capacitor packaging. The FEM is applied to capacitor banks, using simulation software such as COMSOL or ANSYS, to obtain temperature distributions. Although the FEM provides high accuracy in thermal simulations, it is often computationally expensive [22], [23]. To address this limitation, model order reduction (MOR) techniques have been developed. In power electronics applications, MOR techniques compress high-order, strongly coupled models into low-dimensional surrogate models to enable fast analysis and embedded implementation [24], [25], [26]. For thermal estimation of power devices, the FEM is often combined with MOR to achieve computationally efficient and accurate simulations [27], [28]. For instance, the snapshot-based proper orthogonal decomposition method presented in [27] transforms a three-dimensional FEM model into a circuit-compatible multidomain thermal network, achieving less than 5% temperature error compared with transient FEM while greatly improving computation speed. In [28] projection or moment-matching techniques are employed to reduce the degrees of freedom by several orders of magnitude, thereby enabling real-time virtual thermal sensing. However, most of the aforementioned applications remain focused on the device level. At the system level, variations in operating conditions necessitate reconstructing the reduced-order matrices for new state, as the previously reduced model cannot be directly reused [29]. This process introduces substantial additional computational overhead. Furthermore, many FEM simulation tools lack precise circuit models [30], limiting their applicability for electro–thermal analysis in system-level reliability assessment of capacitor banks. Therefore, a thermal estimation methodology is needed that simultaneously ensures high accuracy, computational efficiency, and electro–thermal–aging coupling capability [16].

The thermal network modeling approach can be seamlessly integrated with circuit simulators, providing a rapid, noninvasive temperature estimation suitable for many application fields [4], [7], [16], [31], [32], [33], [34], [35]. In [4], [7], [16], and [31], thermal models are presented to rapidly and accurately estimate capacitor core temperatures for reliability assessment under mission profiles. In physics-of-failure-based online condition monitoring [32], thermal models provide real-time temperature estimation data to capacitor degradation models for state-of-health estimation. In [34], the thermal stress of supercapacitors in MMC systems is optimized using a designed thermal model. In [35], the thermal stress is used as part of a battery–supercapacitor thermal management control strategy. However, traditional models based on simplified one-dimensional thermal networks are unable to accurately characterize the thermal coupling in electrolytic capacitor banks due to neglecting the thermal resistance coupling among capacitors [22], [36].

In order to accurately characterize the thermal coupling distribution of homogeneous electrolytic capacitor banks, Wang and H. Wang [22] proposed a state-space analytical thermal model that improves temperature estimation accuracy by considering the thermal resistance coupling among capacitors. However, it cannot accurately estimate the thermal distribution of an electrolytic capacitor bank under varying cooling conditions. To address this limitation, Lv et al. [23] proposed an analytical thermal model that incorporates electrolytic capacitor aging and thermal–fluid field coupling between the capacitors and the external environment. This model is capable of calculating the thermal distribution of capacitor banks under both cooling and aging conditions.

Capacitors are surface-mounted on PCB substrates, therefore neglecting PCB thermal coupling in thermal models may introduce significant estimation inaccuracies [22]. However, few prior studies have considered this critical factor.

Today, most research predominantly focuses on steady-state thermal modeling of capacitor banks, and no comprehensive analytical framework for transient thermal processes currently exists. In power electronic converters with continuous load transients, thermal stress on capacitors is elevated, and analyzing transient performance becomes essential. The thermal model proposed in [37] considers capacitor temperature dynamics, facilitating reliability-oriented capacitor bank design. However, the coupling effect between capacitors must be further considered to improve the accuracy of thermal estimation. In summary, some results have been reported on thermal modeling of electrolytic capacitor banks, whereas few studies have addressed HCBs.

In addition, effective thermal matching design is an important prerequisite for improving capacitor bank reliability. Usually, the capacitor bank is arranged in-line, which causes severe uneven temperature distribution among capacitors, leading to rapid aging and premature failure of individual units. To solve this problem, a thermal matching method is proposed in [22] that equalizes thermal stress across the capacitor bank by adjusting capacitance and loads. This approach does not alter the arrangement topology but relies on selecting capacitor thermal lifetime characteristics or adjusting loads, which increases complexity. A staggered arrangement for homogeneous electrolytic capacitor banks is proposed in [23], which reduces temperature differences among capacitors and is relatively easy to implement. However, presents only a fixed staggered layout and lacks a systematic design methodology applicable to other cases, especially for HCBs. For HCBs with two different capacitor types, the staggered arrangement offers greater design flexibility but also increased complexity due to inherent disparities in geometric dimensions, volumetric characteristics, and loss mechanisms between the heterogeneous capacitors. In general, optimizing the staggered layout is essential for enhancing the operational reliability of HCBs, and this issue is investigated in this article.

To characterize thermal distributions and mitigate uneven thermal effects in HCBs, this article proposes an analytical thermal modeling method and a layout optimization design method. The main contributions are as follows.

1) The article derives a transient analytical thermal model and extends the applicability of analytical thermal models to enable thermal analysis of transient processes in HCBs.
2) A coupled thermal model of HCBs is established using shape factor–integrated composite thermal resistance networks, which are applicable to capacitor banks with identical or diverse configurations under complex operating conditions.

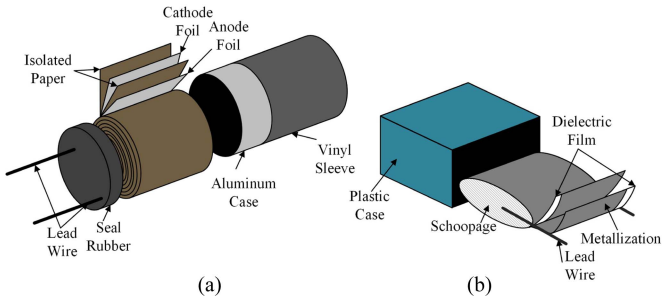


Fig. 1. Capacitor structure. (a) E-cap. (b) F-cap.

3) An optimal arrangement design methodology is developed, utilizing the proposed thermal model to mitigate capacitor aging caused by uneven temperature distribution.

The rest of this article is organized as follows: In Section II, the reliability of HCBs is analyzed. In Section III, a transient analytical thermal modeling method accounting for HCB heterogeneity and PCB mounting modes is proposed. Section IV verifies the steady-state and transient thermal properties of the proposed model. Section V proposes the optimal arrangement design method for HCBs. Section VI discusses the impact of aging effects and compares different thermal modeling and design methods. Finally, Section VII concludes this article.

II. Reliability Analysis for HCB

To illustrate the thermal model for HCB, this section introduces fundamental concepts of power loss analysis and reliability evaluation under aging conditions.

A. Capacitor Structure

A 450 V/390 μF E-cap and a 450 V/7.5 μF F-cap, shown in Fig. 1, are used as representative examples. The E-cap is cylindrical external geometry, with an internal wound multilayer structure comprising aluminum foil electrodes and an aluminum oxide dielectric [4]. The external shape of the F-cap is hexahedron, and its internal structure consists of two metalized polypropylene dielectric films wound together. The metalized electrode is in electrical contact with the metal spraying end to form an external electrical circuit [20]. The different material configurations and structural distributions of the two capacitor types result in distinct electrical characteristics, reliability, and thermal properties.

B. HCB Power Loss Analysis

The power loss P_{loss} of a capacitor is calculated using its ESR and the RMS value of its ripple current I_{rms} as follows:

$$P_{\text{loss}} = I_{\text{rms}}^2 \text{ESR}_i \tag{1}$$

where ESR_i is frequency-dependent resistor and the variation of ESR is related to capacitor types. The ESR values of both E-cap and F-cap decrease with increasing frequency, as shown in Fig. 2.

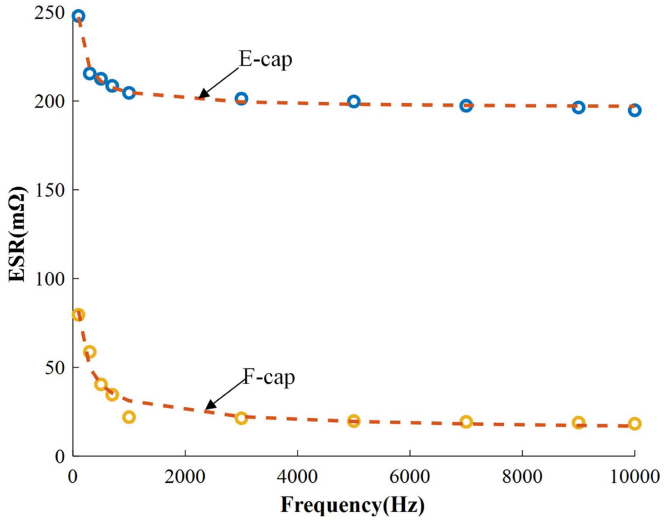


Fig. 2. Relationship between ESR and frequency of E-cap and F-cap.

C. HCB Reliability

During prolonged operation, internal capacitor material parameters gradually degrade, resulting in increases in both ESR and capacitance (C), which in turn increase power dissipation and operating temperature. The impact of capacitance aging on power loss is mainly reflected in the I_{rms}, which can be incorporated into capacitor modeling; specific aging formulas are detailed in [7], [38]. Due to the direct impact of ESR on power loss, this article presents an ESR aging model.

The E-cap aging model can be expressed as [39]

$$\text{ESR}_{\text{E-cap}}(t) = \frac{\text{ESR}_{\text{E-cap}}(0)}{1 + D \cdot (T_{\text{E-cap}}(t) - T_{\text{amb}})} \cdot e^{\int_0^t C_{\text{E-cap}}(0) \cdot e^{-\frac{Ea}{k \cdot T_{\text{E-cap}}(t)}} dt}. \tag{2}$$

The aging model of F-cap is different from E-cap due to the presence of self-healing mechanisms, which can be expressed as [7]

$$\text{ESR}_{\text{F-cap}}(t) = \text{ESR}_{\text{F-cap}}(0) \cdot e^{t \cdot C_{\text{F-cap}}(0) \cdot 2^{\frac{T_{j,\text{F-cap}}(t)}{\alpha_{\text{F-cap}}}}}. \tag{3}$$

In the above (2) and (3), $\text{ESR}_x(0)$ is the initial value of ESR. $C_x(0)$ is the initial value of aging rate. E_a is activation energy. k is Boltzmann constant (1.38×10^{-23} J/K). $T_x(t)$ is hot spot temperature of capacitor. T_{amb} is ambient temperature. $\alpha_{\text{F-cap}}$ stands the temperature coefficient of F-cap. D is Constant. The subscript presents x = E-cap/F-cap. The method for obtaining all parameters is described in [32].

Lifetime models incorporating ESR aging effects correlate degradation with core temperature, thereby improving prediction accuracy [23]. A commonly used lifetime model for capacitors can be expressed as [8]

$$L_x = L_{N,x}\left(U/U_N\right)^{-n} 2^{\frac{T_N - T_{j,x}(t)}{\alpha_x}} (x = \text{E-cap/F-cap}) \tag{4}$$

where L_x is the actual working lifetime, $L_{N,x}$ is the lifetime under rated operating conditions, U is the actual working voltage, U_N is the voltage under rated operating conditions, $T_{\rm N}$ is the rated hotspot temperature, $T_{j,x}$ is the hotspot temperature, and n and α are the voltage and temperature coefficients obtained from accelerated aging tests.

Finally, the cumulative density function is obtained by fitting the life curve using the Weibull distribution, which represents the unreliability of HCBs.

The foregoing analysis shows that capacitor hotspot temperature is the critical influence on ESR aging and overall HCB reliability assessment. Therefore, accurate temperature estimation is essential for thermal modeling.

III. Thermal Analysis and Analytical Thermal Modeling Method Of HCBs

This section presents a method in which equivalent thermal capacitance is integrated into the steady-state state-space formulation, thereby enabling the proposed model to provide analytical capability for transient thermal characterization. A shape factor is introduced to quantify spatial relationships among geometrically heterogeneous capacitors. Furthermore, the PCB is explicitly incorporated into the case-ambient thermal resistance through a composite series thermal resistance representation.

A. Construction of the HCB Analytical Thermal Model

1) Analytical Thermal Network: Multiple heat sources are present in the capacitor banks and thermal coupling resistance between adjacent capacitors. A state-space model based on energy conservation and heat transmission between the capacitor case and the environment is an effective modeling approach [22]. The fundamental concept of this thermal network is based on the electrical-thermal analogy principle, where the internal losses, thermal resistance, thermal capacitance, and temperature of a capacitor are represented by a current source, resistor, capacitor, and voltage source, respectively. To enhance the model accuracy of HCBs, a thermal modeling method considering thermal transients and PCB mounting configurations is developed in this article. The proposed thermal model is illustrated using the commonly employed series arrangement of capacitor banks as an example.

Fig. 3(a) shows the in-line arrangement of the HCB, with serial numbers 1–9 being E-caps and serial numbers 10–13 being F-caps. Fig. 3(b) shows the corresponding thermal network model of the HCB with in-line arrangement.

The heat transmission process for each capacitor consists of three components: internal heat transfer $R_{h\text{-}c,i}$, heat transfer between case and environment $R_{i\text{-amb}}$, and heat transfer between adjacent capacitors $R_{i\text{-}j}$. In Fig. 3(b), $R_{h\text{-}c,i}$ represents the thermal resistance from hotspot to case. $R_{i\text{-amb}}$ represents the thermal resistance from the case to the ambient. $R_{i\text{-}j}$ represents the thermal resistance of the coupling between cases i and j. $T_{\rm amb}$ denotes the ambient temperature. $P_{\rm loss}^{\rm E-cap}$ is the power loss of the E-cap. $P_{\rm loss}^{\rm F-cap}$ is the power loss of the F-cap. $C_{c,i}$ is the equivalent thermal capacitance of the case. $C_{h,i}$ is the equivalent thermal capacitance of the hotspot.

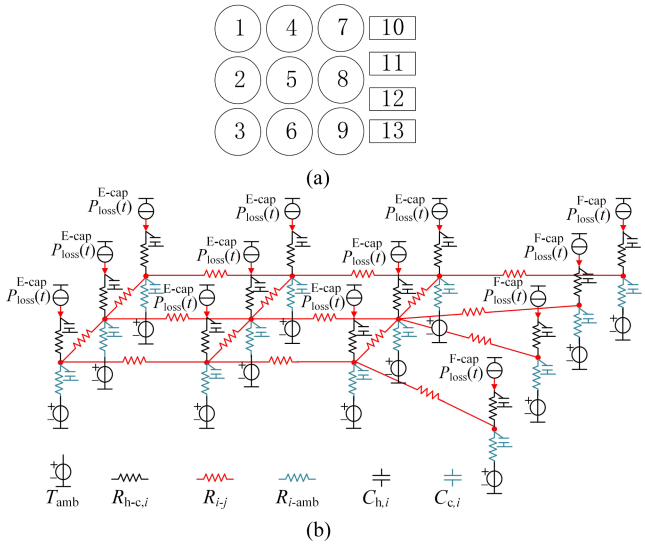


Fig. 3. Hybrid capacitor bank. (a) In-line arrangement. (b) Thermal network model for in-line arrangement.

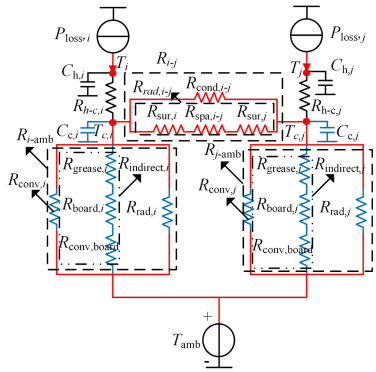


Fig. 4. Thermal network structure of two adjacent capacitors in HCB.

2) Transient State-Space Thermal Model: To enable the thermal model to describe thermal transients, the equivalent thermal capacitance is considered in the state-space formulation. Two adjacent capacitors in the thermal network are used as an example to illustrate the transient thermal equation, as shown in Fig. 4.

The hotspot temperature T_i can be obtained as follows:

$$T_i = T_{c,i} + P_{loss,i}\left(t\right) R_{h-c,i}\left(1 - {\rm e}^{-\frac{t}{R_{h-c,i}C_{h,i}}}\right) \tag{5}$$

where T_i represents the hotspot temperature. $R_{h\text{-}c,i}$ can be obtained from the capacitor datasheet. $C_{h,i}$ can be obtained by fitting a first-order Foster model through finite element simulation. $P_{{\rm loss},i}(t)$ can be obtained using (1)–(3).

The case temperature $T_{c,i}$ can be obtained using the transient state-space modeling

$$C_{{\rm c},i}^{x-{\rm cap}}\frac{{\rm d}T_{{\rm c},i}^{x-{\rm cap}}}{{\rm d}t} = P_{loss,i}\left(t\right) + \frac{T_{\rm amb} - T_{{\rm c},i}^{x-{\rm cap}}}{R_{i-{\rm amb}}} + \frac{T_{{\rm c},j}^{x-{\rm cap}} - T_{{\rm c},i}^{x-{\rm cap}}}{R_{i-j}}$$

$$(i, j = 1, \ldots, 13; j \neq i; x, y = \mathrm{E-cap/F-cap}) \quad (6)$$

where $T_{c,j}$ denotes the case temperature of capacitor j. $C_{c,i}$ can be obtained by fitting a first-order Foster model using finite element simulation. $R_{i\text{-}j}$ is related to factors such as relative position, geometry, and surface material properties. $R_{i\text{-amb}}$ accounts for both heat transfer through the circuit board and direct heat transfer between the capacitor case and the environment. Therefore, $R_{i\text{-}j}$ and $R_{i\text{-amb}}$ require further discussion, which is provided in Sections III-B and III-C.

For the HCB with $m+n$ order differential equations, the thermal dynamics of the case temperature is represented as follows:

$$\mathbf{C}_c \frac{d\mathbf{T}_c}{d\mathbf{t}} = \mathbf{AT} + \mathbf{BP}_{\mathrm{loss}}(\mathbf{t}) \quad (7)$$

where $\boldsymbol{C}_c$ is the equivalent thermal capacitance matrix of the cases and $\boldsymbol{T}_c$ is the case temperature matrix of the capacitors. $\boldsymbol{T}$ is the temperature matrix, which includes the case temperature of E-cap and F-cap as well as the ambient temperature. $\boldsymbol{A}$ denotes the thermal resistance matrix. $\boldsymbol{B}$ denotes the coefficient matrix. $\boldsymbol{P}_{\mathrm{loss}}(t)$ is the power loss matrix accounts for ESR aging effects, which can be obtained through iterative calculations using (1), (2), and (3). The specific expanded forms of each matrix are provided as (8) shown at the bottom of the next page.

B. Thermal Coupling Process Between Adjacent Capacitors

The coupling thermal resistance $R_{i\text{-}j}$ between adjacent capacitors is modeled as the parallel combination of radiation resistance $R_{\mathrm{rad},i\text{-}j}$ and conduction resistance $R_{\mathrm{cond},i\text{-}j}$.

1) Closed Radiative Heat Transfer Between Two Surfaces ($\mathrm{R}_{rad,\mathrm{i\text{-}j}}$): Each capacitor surface is assumed to behave as an opaque, diffuse, gray body. The two adjacent capacitor surfaces are treated as a closed system, with the net radiative heat transfer between them taken as the primary quantity of interest.

This heat transfer is primarily governed by three thermal resistances: $R_{\mathrm{sur},I}$; $R_{\mathrm{spa},i\text{-}j}$; and $R_{\mathrm{sur},j}$. Here, $R_{\mathrm{sur},i}$ and $R_{\mathrm{sur},j}$. represent the radiative thermal resistances of the two respective surfaces. These resistances depend on the radiative properties of the surface materials. $R_{\mathrm{spa},i\text{-}j}$ denotes the spatial radiative thermal resistance, which reflects the influence of geometric configuration between the two surfaces on radiative heat transfer. This resistance is primarily determined by the shape factor.

Therefore, the total radiative thermal resistance between the two surfaces can be expressed as [41]

$$\begin{aligned} R_{\mathrm{rad},i-j} &= R_{\mathrm{sur},i} + R_{\mathrm{spa},i-j} + R_{\mathrm{sur},j} \\ &= \frac{\frac{1-\varepsilon_i}{\sigma A_{\mathrm{side},i}\varepsilon_i} + \frac{1}{\sigma A_{\mathrm{side},i}X_{i-j}} + \frac{1-\varepsilon_j}{\sigma A_{\mathrm{side},j}\varepsilon_j}}{\left(T_{\mathrm{c},i} + T_{\mathrm{c},j}\right)\left(T_{\mathrm{c},i}^2 + T_{\mathrm{c},j}^2\right)} \end{aligned} \quad (9)$$

where $A_{\mathrm{side},i}$ and $A_{\mathrm{side},j}$ denote the areas of two adjacent capacitor side surfaces. ε_i and ε_j are the surface emissivities of materials on surface i and surface j, respectively, ($0 < \varepsilon_i < 1$, $0 < \varepsilon_j < 1$). σ denotes the Stephen–Boltzmann constant. $T_{c,i}$ and $T_{c,j}$ are the temperatures of surface i and surface j, respectively. $X_{i\text{-}j}$ is the shape factor, determined by the geometry and relative position of the two surfaces. There is a total of four adjacent relationships in the in-line arrangement layout of the HCB, as given in Table I. The corresponding expressions for the shape factors of these adjacent relationships are also given in Table I.

2) Conduction Heat Transfer ($\mathrm{R}_{cond,\mathrm{i\text{-}j}}$): The conduction heat transfer for the four adjacent relationships is given in Table I. According to Fourier's law, the conduction thermal resistance between adjacent capacitors, $R_{\mathrm{cond},i\text{-}j}$, can be expressed as

$$R_{\mathrm{cond},i-j} = \frac{\delta}{\lambda_{\mathrm{air}} A_{\mathrm{side},i} X_{i-j}} \quad (10)$$

where δ denotes the distance between the two surfaces. At atmospheric pressure (1 atm) and an ambient temperature of 25 °C, the thermal conductivity of air is $\lambda_{\mathrm{air}} = 0.02551$ W/m·K.

C. Heat Transfer Process Between the Capacitor Case and the Ambient

Heat transfer between the capacitor case surface and the ambient occurs through both convection and radiation [23]. In addition, an indirect case-ambient heat transfer process is introduced to account for the influence of the PCB.

1) Case-ambient Radiative Heat Transfer ($\mathrm{R}_{rad,\mathrm{i}}$): Taking F-caps as an example, the thermal radiation from the capacitor surface to the ambient environment is illustrated in Fig. 5. The radiative thermal resistance between the capacitor surface and the environment can be expressed as

$$R_{\mathrm{rad},i} = \frac{1}{\varepsilon_i \sigma \left(A_{\mathrm{side},i} - A_{\mathrm{side},i}X_{i-j} - A_{\mathrm{bottom},i}\right)\left(T_{c,i}+T_{\mathrm{amb}}\right)\left(T_{c,i}^2 + T_{\mathrm{amb}}^2\right)} \quad (11)$$

where $A_{\mathrm{side},i}$ denotes the surface area of the F-cap. $A_{\mathrm{bottom},i}$ denotes the bottom area of the F-cap.

2) Case-ambient Convection Heat Transfer ($\mathrm{R}_{conv,\mathrm{i}}$): Convection heat transfer between the capacitor and the environment occurs in two forms: natural convection and forced convection, as illustrated in Fig. 5.

The natural convection thermal resistance is shown as

$$R_{\mathrm{conv},i} = \frac{l}{\lambda_{\mathrm{air}} Nu_{\mathrm{natural}} \left(A_{\mathrm{side},i} - A_{\mathrm{side},i}X_{i-j} - A_{\mathrm{bottom},i}\right)} \quad (12)$$

where l denotes the characteristic length and Nu denotes the Nusselt number. It should be noted that F-cap and E-cap, owing to their different geometries, require distinct formulas for calculating the Nu number. Various methods have been proposed to determine the Nu number, and the formulas with higher accuracy are given in Table II.

The expression for thermal resistance under forced convection is the same as in (12), but the distinction from natural convection lies in the Nu number. Similarly, F-cap and E-cap, owing to their different geometries, require distinct formulas for calculating the Nu number. The formulas for calculating the Nu numbers of the two capacitor types under forced convection are given in Table III. It can be observed that the forced convection heat transfer coefficient depends not only on the fluid properties and surface geometry but also on the fluid flow rate.

3) Case-ambient Indirect Heat Transfer ($R_{\mathrm{indirect,i}}$): The capacitor is soldered to the bottom of the circuit board. The interface between the capacitor bottom and the board surface is not perfectly smooth at the microscopic level, resulting in significant contact voids. These voids introduce a contact thermal resistance that can significantly reduce heat transfer efficiency. To mitigate this, thermal paste is typically applied in the contact gap between the capacitor and the board to enhance heat transfer efficiency. Heat is dissipated through the board into the ambient, and the path can be modeled as a composite series thermal resistance consisting of three thermal resistances, as shown in Fig. 6.

Heat at the capacitor bottom is transferred by conduction through the thermally conductive paste, as shown in Fig. 6. The corresponding thermal resistance, $R_{\mathrm{grease},I}$, is defined as

$$R_{\mathrm{grease},i} = \frac{\delta_{\mathrm{grease}}}{\lambda_{\mathrm{grease}} A_{\mathrm{bottom},i}} \tag{13}$$

where $A_{\mathrm{bottom},i}$ denotes the bottom area of capacitor i. δ_{grease} represents the thickness of the thermal paste layer which is set to 0.05 m in this article. $\lambda_{\mathrm{grease}}$ denotes the thermal conductivity of the thermal paste, with $\lambda_{\mathrm{grease}} = 0.8$ W/m·K. Heat is then conducted through the circuit board, with the corresponding

$$A = \begin{bmatrix}
-\sum_{j=2}^{n}\frac{1}{R^{\mathrm{E-E}}_{1,j}} - \sum_{z=1}^{m}\frac{1}{R^{\mathrm{E-F}}_{1,z}} - \frac{1}{R^{\mathrm{E}}_{1,\mathrm{amb}}} & \frac{1}{R^{\mathrm{E-E}}_{1,2}} & \cdots & \frac{1}{R^{\mathrm{E-E}}_{1,n}} & \frac{1}{R^{\mathrm{E-F}}_{1,1}} \\
\frac{1}{R^{\mathrm{E-E}}_{2,1}} & -\sum_{j=1,j\neq 2}^{n}\frac{1}{R^{\mathrm{E-E}}_{2,j}} - \sum_{z=1}^{m}\frac{1}{R^{\mathrm{E-F}}_{2,z}} - \frac{1}{R^{\mathrm{E}}_{2,\mathrm{amb}}} & \cdots & \frac{1}{R^{\mathrm{E-E}}_{2-n}} & \frac{1}{R^{\mathrm{E-F}}_{2,1}} \\
\cdots & \cdots & \cdots & \cdots & \cdots \\
\frac{1}{R^{\mathrm{E-E}}_{n,1}} & \frac{1}{R^{\mathrm{E-E}}_{n,2}} & \cdots & -\sum_{j=1}^{n-1}\frac{1}{R^{\mathrm{E-E}}_{n,j}} - \sum_{z=1}^{m}\frac{1}{R^{\mathrm{E-F}}_{n,z}} - \frac{1}{R^{\mathrm{E}}_{n,\mathrm{amb}}} & \frac{1}{R^{\mathrm{E-F}}_{n,1}} \\
\frac{1}{R^{\mathrm{F-E}}_{1,1}} & \frac{1}{R^{\mathrm{F-E}}_{1,2}} & \cdots & \frac{1}{R^{\mathrm{F-E}}_{1,(n-1)}} & \frac{1}{R^{\mathrm{F-E}}_{1,n}} \\
\frac{1}{R^{\mathrm{F-E}}_{2,1}} & \frac{1}{R^{\mathrm{F-E}}_{2,2}} & \cdots & \frac{1}{R^{\mathrm{F-E}}_{2,(n-1)}} & \frac{1}{R^{\mathrm{F-E}}_{2,n}} \\
\cdots & \cdots & \cdots & \cdots & \cdots \\
\frac{1}{R^{\mathrm{F-E}}_{m,1}} & \frac{1}{R^{\mathrm{F-E}}_{m,2}} & \cdots & \frac{1}{R^{\mathrm{F-E}}_{m,(n-1)}} & \frac{1}{R^{\mathrm{F-E}}_{m,n}}
\end{bmatrix}$$

$$\begin{bmatrix}
\frac{1}{R^{\mathrm{E-F}}_{1,2}} & \frac{1}{R^{\mathrm{E-F}}_{1,3}} & \cdots & \frac{1}{R^{\mathrm{E-F}}_{1,m}} & \frac{1}{R^{\mathrm{E}}_{1,\mathrm{amb}}} \\
\frac{1}{R^{\mathrm{E-F}}_{2,2}} & \frac{1}{R^{\mathrm{E-F}}_{2,3}} & \cdots & \frac{1}{R^{\mathrm{E-F}}_{2,m}} & \frac{1}{R^{\mathrm{E}}_{2,\mathrm{amb}}} \\
\cdots & \cdots & \cdots & \cdots & \cdots \\
\frac{1}{R^{\mathrm{E-F}}_{n,2}} & \frac{1}{R^{\mathrm{E-F}}_{n,3}} & \cdots & \frac{1}{R^{\mathrm{E-F}}_{n,m}} & \frac{1}{R^{\mathrm{E}}_{n,\mathrm{amb}}} \\
-\sum_{j=1}^{n}\frac{1}{R^{\mathrm{F-E}}_{1,j}} - \sum_{z=2,z\neq 1}^{m}\frac{1}{R^{\mathrm{F-F}}_{1,z}} - \frac{1}{R^{\mathrm{F}}_{1,\mathrm{amb}}} & \frac{1}{R^{\mathrm{F-F}}_{1,2}} & \cdots & \frac{1}{R^{\mathrm{F-F}}_{1,m}} & \frac{1}{R^{\mathrm{F}}_{1,\mathrm{amb}}} \\
\frac{1}{R^{\mathrm{F-F}}_{2,1}} & -\sum_{j=1}^{n}\frac{1}{R^{\mathrm{F-E}}_{2,j}} - \sum_{z=1,z\neq 2}^{m}\frac{1}{R^{\mathrm{F-F}}_{2,z}} - \frac{1}{R^{\mathrm{F}}_{2,\mathrm{amb}}} & \cdots & \frac{1}{R^{\mathrm{F-F}}_{2,m}} & \frac{1}{R^{\mathrm{F}}_{2,\mathrm{amb}}} \\
\cdots & \cdots & \cdots & \cdots & \cdots \\
\frac{1}{R^{\mathrm{F-F}}_{m,1}} & \frac{1}{R^{\mathrm{F-F}}_{m,2}} & \cdots & -\sum_{j=1}^{n}\frac{1}{R^{\mathrm{F-E}}_{m,j}} - \sum_{z=1}^{m-1}\frac{1}{R^{\mathrm{F-F}}_{m,z}} - \frac{1}{R^{\mathrm{F}}_{m,\mathrm{amb}}} & \frac{1}{R^{\mathrm{F}}_{m,\mathrm{amb}}}
\end{bmatrix}.$$

$$T = \begin{bmatrix} T^{\mathrm{E-cap}}_{\mathrm{c},1} \\ T^{\mathrm{E-cap}}_{\mathrm{c},2} \\ \cdots \\ T^{\mathrm{E-cap}}_{\mathrm{c},n} \\ T^{\mathrm{F-cap}}_{\mathrm{c},1} \\ T^{\mathrm{F-cap}}_{\mathrm{c},2} \\ \cdots \\ T^{\mathrm{F-cap}}_{\mathrm{c},m} \\ T_{\mathrm{amb}} \end{bmatrix} \quad P_{\mathrm{loss}}(t) = \begin{bmatrix} P^{\mathrm{E-cap}}_{\mathrm{loss},1}(t) \\ \cdots \\ P^{\mathrm{E-cap}}_{\mathrm{loss},n}(t) \\ P^{\mathrm{F-cap}}_{\mathrm{loss},1}(t) \\ \cdots \\ P^{\mathrm{F-cap}}_{\mathrm{loss},m}(t) \end{bmatrix} \quad B = \begin{bmatrix} 1 & \cdots & 0 & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & 1 & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & 0 & 0 & \cdots & 1 \end{bmatrix}$$

$$C_{\mathrm{c}} = \begin{bmatrix} C^{\mathrm{E-cap}}_{\mathrm{c},1} & \cdots & 0 & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & C^{\mathrm{E-cap}}_{\mathrm{c},n} & 0 & \cdots & 0 \\ 0 & \cdots & 0 & C^{\mathrm{F-cap}}_{\mathrm{c},1} & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & 0 & 0 & \cdots & C^{\mathrm{F-cap}}_{\mathrm{c},n} \end{bmatrix}. \tag{8}$$

TABLE I
VIEW FACTOR [40]

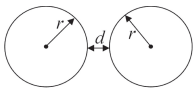
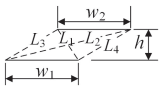
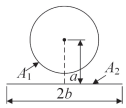
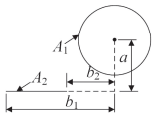
Geometry	Formula
	$M = 1 + d/2r$ $X_{1,2} = \frac{1}{\pi}\left(\sqrt{M^2-1} + \arcsin\frac{1}{M} - M\right)$
	$X_{1-2} = \sqrt{1+(h/w)^2} - (h/w)$
	$X_{1-2} = (L_1 + L_2 - L_3 - L_4)/2w_1$
	$X_{1-2} = (1/\pi)\bullet\tan^{-1}(b/a)$
	$X_{1-2} = (1/2\pi)\bullet\left(\tan^{-1}(b_1/a) - \tan^{-1}(b_2/a)\right)$

TABLE II
EMPIRICAL EXPRESSION FOR THE AVERAGE NUSSELT NUMBER FOR NATURAL CONVECTION OVER SURFACES [41]

Capacitor type	Characteristic length l	Range of Ra	Nu
E-cap (Vertical cylinder)	l	Entire range	$Nu = \left\{0.825 + 0.387Ra^{\frac{1}{6}} \Big/ \left[1+(0.492/\mathrm{Pr})^{\frac{9}{16}}\right]^{\frac{8}{27}}\right\}^2$
F-cap (Vertical plate)	l	10^4~10^9 10^9~10^{13}	$Nu = 0.59\mathrm{Ra}^{\frac{1}{4}}$ $Nu = 0.1\mathrm{Ra}^{\frac{1}{3}}$

Note: $Ra = g\beta(T_s - T_{amb})l^3\mathrm{Pr}/\nu^2$. l is the height. Gravitational acceleration g = 9.8 m/s^2. volume expansion coefficient $\beta = 1/T_{amb}$. Pr is the Prandtl number of air, Pr = 0.7296 at 1 atm pressure, 25°C. Kinematic viscosity $\nu = 1.562 \times 10^{-5}$ [42].

TABLE III
EMPIRICAL EXPRESSION FOR THE AVERAGE NUSSELT NUMBER FOR FORCED CONVECTION OVER CYLINDERS IN CROSS FLOW [41]

Capacitor type	Characteristic length l	Range of Ra	Nu
E-cap (Vertical cylinder)	l(the height of vertical cylinder)	Entire range	$Nu = 0.3 + \left[1+(\mathrm{Re}/282000)^{\frac{5}{8}}\right]^{\frac{4}{5}} \left\{0.6\,\mathrm{Re}^{\frac{1}{2}}\,\mathrm{Pr}^{\frac{1}{3}} \Big/ \left[1+(0.4/\mathrm{Pr})^{\frac{2}{3}}\right]^{\frac{1}{4}}\right\}$
F-cap (Vertical plate)	l(the height of vertical cylinder)	3900−79 000 32 000−1 600 000	$Nu = 0.094\,\mathrm{Re}^{0.675}\,\mathrm{Pr}^{\frac{1}{3}}$ $Nu = 0.0249\,\mathrm{Re}^{0.811}\,\mathrm{Pr}^{\frac{1}{3}}$

Note: $Re = ul/\nu$. u is the air velocity [41].

thermal resistance given by $R_{\mathrm{board},i}$

$$R_{\mathrm{board},i} = \frac{\delta_{\mathrm{board}}}{\lambda_{\mathrm{board}} A_{\mathrm{board}}} \tag{14}$$

where δ_{board} represents the thickness of the circuit board. λ_{board} denotes the thermal conductivity of the circuit board, with λ_{board} = 0.3 W/m·K. A_{board} denotes the surface area of the circuit board. Finally, convective heat transfer occurs between the bottom surface of the circuit board and the ambient environment

$$R_{\mathrm{conv,board}} = \frac{l}{h_{\mathrm{board}} A_{\mathrm{board}}} \tag{15}$$

where h_{board} denotes the convective heat transfer coefficient of the circuit board, which varies depending on the cooling conditions. Typical values of h_{board} are 10 W/(m^2·K) under natural cooling conditions and 14 W/(m^2·K) under forced cooling conditions [42], [43].

IV. MODEL VERIFICATION

To verify the effectiveness of the proposed thermal network model, an in-line arrangement of the HCB is used as the case study. The specifications of each individual capacitor are given in Table IV. In the parameters of E-cap, D denotes the diameter of the capacitor and L denotes the height. In the parameters of

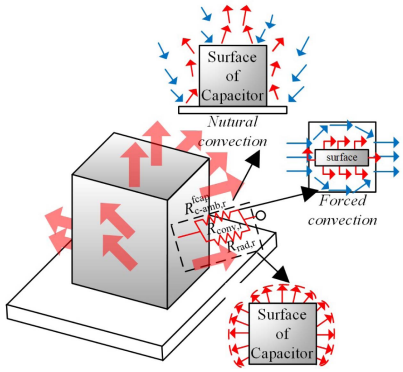


Fig. 5. Case-ambient heat transfer process.

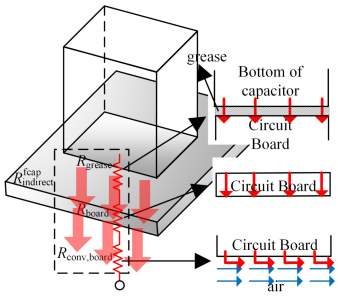


Fig. 6. Contact heat transfer process between capacitor- circuit board.

TABLE IV
SPECIFICATIONS OF E-CAP AND F-CAP

Parameters	E-cap	F-cap
DC voltage(V)	450	450
Capacitance(μF)	390	7.5
ESR(mΩ)	280	5
Dimension(mm)	$D \times L = 35 \times 35$	$w \times h \times l = 22.0 \times 36.5 \times 31.5$
$R_{h\text{-}c}$(°C/W)	3.63	2.2
C_h(J/°C)	140	140
C_c(J/°C)	77	71.1

F-cap, w is the width, h is the height, l is the length, C_h and C_c represent the equivalent core heat capacity and equivalent case heat capacity, respectively, with values derived from FEM fitting results.

A. Experimental Platform

The experimental platform is illustrated in Fig. 7. The ESR values of the E-cap and F-cap are measured using an LCR meter. The ripple current of the capacitor bank is provided by a programmable ac power source (Chroma 61609) at 100 Hz/9 A. After the temperature reaches steady state, the case temperature distribution of the capacitor bank is measured using a FIRT-420 handheld infrared thermal camera. The capacitor hotspot temperature is measured by a thermocouple embedded in advance, and the readings are displayed on a thermometer. A fan generating an air velocity of 0.5 m/s is employed to simulate a forced convection cooling. The experimental environment is assumed to be at standard atmospheric pressure (1 atm) and an ambient temperature of 25 °C. Under natural convection and forced air

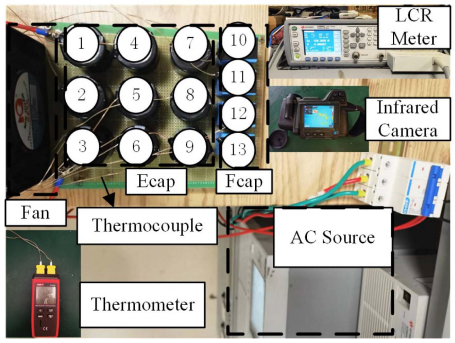


Fig. 7. Experimental platform.

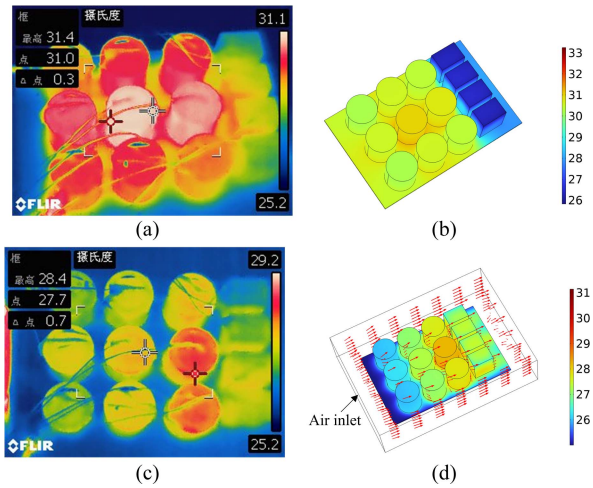


Fig. 8. Experimental results and FEM simulation results of in-line arrangement (Unit: °C). (a) Experimental results under natural cooling conditions. (b) FEM results under natural cooling conditions. (c)Experimental results under forced cooling. (d) FEM results under forced cooling.

cooling conditions, the convective heat transfer coefficients of the PCB are 10 W/(m^2·K) and 14 W/(m^2·K), respectively.

Experiment results are presented in Fig. 8(a)–(c), showing the thermal distribution images of the HCB captured with an infrared camera at an ambient temperature of 25 °C under different cooling conditions.

B. FEM Model

FEM simulation is employed to validate the proposed method by analyzing the temperature distribution in the HCB. A three-dimensional geometric model and heat transfer field are developed based on the actual HCB dimensions. Under forced convection, the width, height, and depth of the rectangular air duct opening are set to 250, 60, and 180 mm, respectively. The inlet airflow velocity is 0.5 m/s, with outlet normal stress equal to the outlet pressure. The fluid flow is assumed to be laminar. The capacitor bank is modeled for heat transfer in the solid domain. Since the windings of both E-cap and F-cap consist of complex multilayered structures with hundreds of turns, computational burden and time must be reduced. Thus, in the FEM, the internal windings are simplified as a thermally anisotropic solid instead

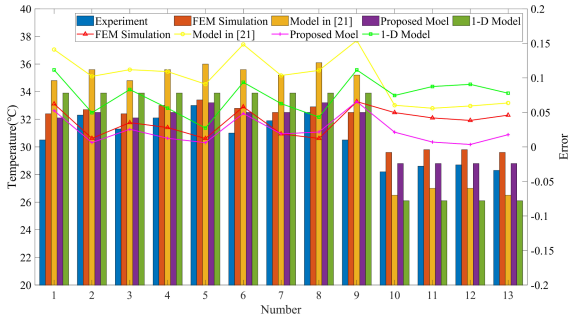


Fig. 9. Comparison of natural convection results.

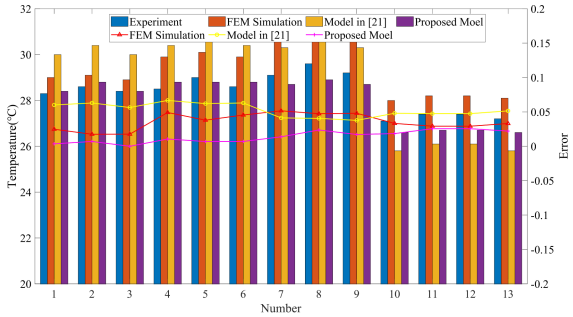


Fig. 10. Comparison of forced convection results.

of the actual multilayer structure. This simplification introduces an error of less than 3% [44]. Additionally, surface-to-surface radiation physics is considered, with all capacitor surfaces defined as diffuse reflectors.

The FEM temperature distributions under natural and forced convection are shown in Fig. 8(b) and (d). The FEM results differ from experiments by about 4%, while the temperature distributions are nearly identical.

C. Model Verification

To verify the steady-state temperature accuracy of the proposed thermal model, computational results from multiple thermal modeling methods are compared under different cooling conditions, as shown in Figs. 9 and 10. From the above hotspot temperature comparison, the proposed method yields results very similar to FEM, with an error within 5%. The runtime of the proposed model is less than 1 s, offering a clear speed advantage over FEM and greatly improving the efficiency of HCB temperature estimation.

To validate the accuracy of the proposed method for transient temperature prediction, the calculated case-to-ambient temperature rise is compared with measured results, as shown in Fig. 11. For most of the temperature rise process, the error remains below 0.05.

Because the ambient temperature changes dynamically, variations in capacitor hotspot temperature cannot be ignored. The performance of the proposed method is further verified under an abrupt ambient temperature variation from 25 °C to 35 °C to 25 °C, as shown in Fig. 12. During this dynamic process,

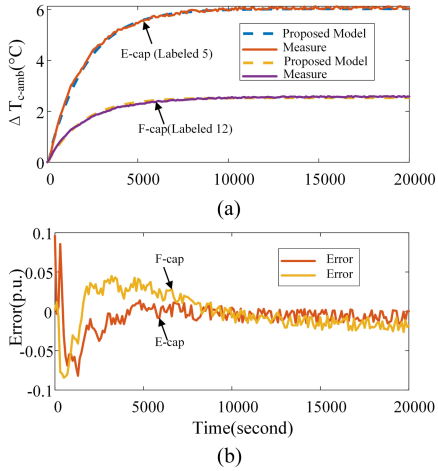


Fig. 11. Comparison of the measurement and proposed model. (a) Temperature rise from case to ambient. (b) Temperature rise error.

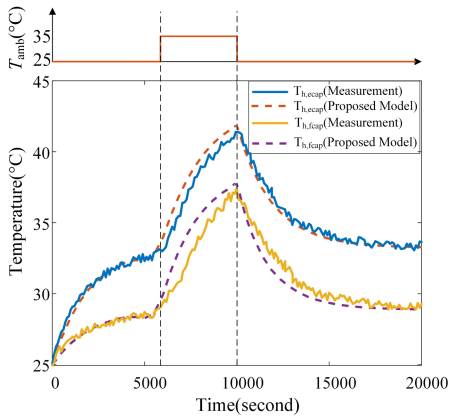


Fig. 12. Comparison of hot-spot temperature for measurement and proposed model under an abrupt ambient temperature variation.

the proposed thermal model shows good agreement with the measured results.

V. Optimized Design Method for HCB Arrangement

As shown in Fig. 9, a large temperature difference exists between the capacitor located at the center of the bank and the surrounding capacitors. During long-term operation, this temperature imbalance causes uneven capacitor aging, thereby reducing the lifetime of the entire bank. Staggered arrangement has been shown to provide better thermal performance [23]. In this section, an optimal staggered arrangement design method for HCBs is presented. The method achieves a more uniform temperature distribution without altering the number or size of devices, or the heat dissipation pattern.

A. Design Optimization of HCB Arrangement

The proposed design method consists of three steps: obtaining the optimal combination; optimizing the spacing between adjacent capacitors; and optimizing the staggering angle.

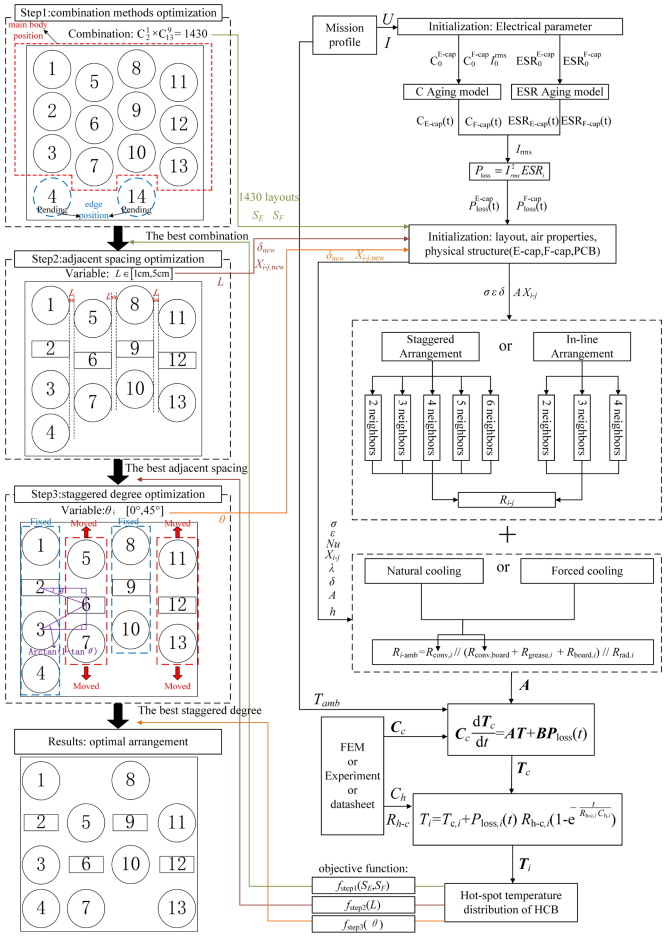


Fig. 13. Flowchart of the proposed optimization arrangement design method.

The flowchart of the proposed design method is shown in Fig. 13 (HCB:9 E-caps+4 F-caps).

Step 1: Obtaining the optimal combination. The geometric specifications of both PCB and capacitors are incorporated as boundary conditions. A staggered arrangement serves as the fundamental topological paradigm, exhaustively defining all possible positional permutations for HCBs on the PCB. All positions are classified into two categories: the main position and the edge position, as shown in Fig. 13. The total number of possible combinations is calculated as follows: If the total number of capacitors N (where $N = N_{\text{E-cap}} + N_{\text{F-cap}}$) is less than or equal to the number of main positions M_{main}, then the number of combinations is $N_{\text{combination}} = \mathrm{C}_{M_{main}}^{N_{E-\text{cap}}} \times \mathrm{C}_{M_{main}-N_{E-\text{cap}}}^{N_{F-\text{cap}}}$. If N exceeds M_{main}, the number of combinations is $N_{\text{combination}} = \mathrm{C}_{M_{edge}}^{M_{main}+M_{\text{edge}}-N} \times \mathrm{C}_{N}^{N_{E-\text{cap}}}$. For the 9E-cap + 4F-cap HCB, the combination number is $N_{\text{combination}} = \mathrm{C}_2^1 \times \mathrm{C}_{13}^9 = 1430$. Subsequently, all possible combinations are enumerated to generate the capacitor position set $P = \{1, \ldots, 14\}$.The proposed thermal model is then applied to perform a comprehensive temperature-field analysis for all topological configurations. The configuration that minimizes the steady-state peak temperature is selected as the optimal combination, aiming to reduce the maximum thermal stress difference within the capacitor bank.

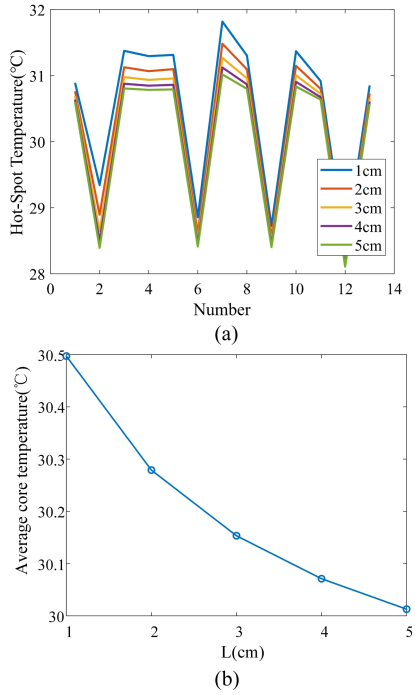


Fig. 14. Adjacent spacing optimization validation. (a) Hot-spot temperature distribution. (b) Average hot-spot temperature distribution.

Accordingly, the objective function can be expressed as follows:

$$f\left(S_E\right) = \min_{S_E \subset P} \left(\max_{i \in S_E} \left(T_{\text{core},i}\right) \right) \tag{16}$$

where S_E denotes the set of positions of the electrolytic capacitors. Finally, the optimal arrangement is S_E = [1,3,4,5,7,8,10,11,13], and the optimal arrangement of film capacitor is S_F = [2,6,9,12].

Step 2: Optimizing the adjacent capacitor spacing L. The geometric specifications of the PCB and capacitor elements are incorporated as boundary constraints, with L limited to the range of 1–5 cm. With L as the principal optimization variable, the HCB temperature distribution is calculated. The optimal spacing is determined by minimizing the average temperature, and the objective function along with its constraints is formulated as follows:

$$\begin{cases} f_{\text{step2}}\left(L\right) = \min\limits_{S_E, S_F \subset P} \left(\frac{1}{N} \sum_{i \in S_E, j \in S_F} \left(T_{\text{core},i}\left(L\right) \right.\right. \\ \qquad \left.\left. + T_{\text{core},j}\left(L\right)\right) \right) \\ L_{\min} \le L \le L_{\max} \\ L_{\max} = 0.05\text{m} \\ L_{\min} = 0.01\text{m} \end{cases} . \tag{17}$$

As shown in Fig. 14, the optimal spacing is 5 cm.

Step 3: Optimizing the staggering angle θ. The layout of one column in a pair of adjacent capacitor columns is fixed, while the other column is shifted as a whole, with the staggering angle treated as the optimization variable to determine the optimal layout. The optimal angle is determined by minimizing the average temperature, and the objective function together with

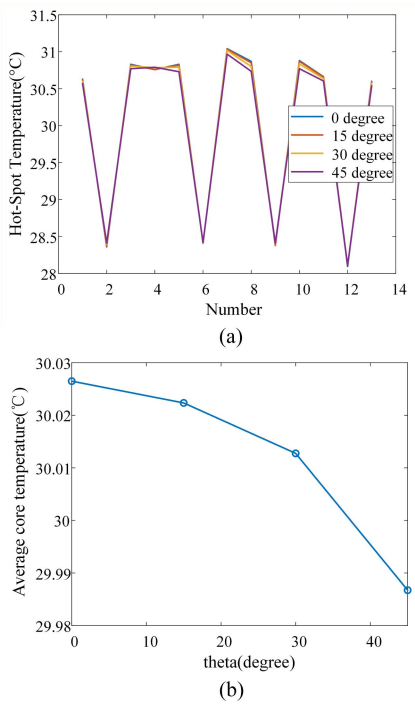


Fig. 15. Staggered degree validation. (a) Hot-spot temperature distribution. (b) Average hot-spot temperature distribution.

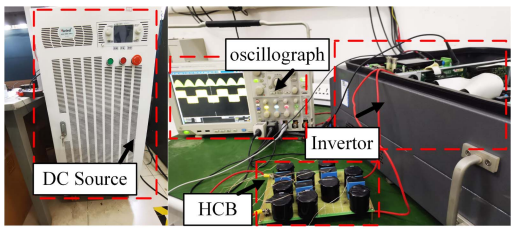


Fig. 16. Single-phase inverter platform.

its constraints is formulated as follows:

$$\begin{cases} f_{\text{step3}}(\theta) = \min\limits_{S_E, S_F \subset P} \left(\frac{1}{N} \sum_{i \in S_E, j \in S_F} \left(T_{\text{core},i}(\theta) + T_{\text{core},j}(\theta) \right) \right) \\ \theta_{\min} \le \theta \le \theta_{\max} \\ \theta_{\max} = 0^\circ \\ \theta_{\min} = 45^\circ \end{cases} . \quad (18)$$

As shown in Fig. 15, the optimal staggering angle is 45°.

B. Case Study

To validate the feasibility of the proposed thermal model and optimized arrangement in practical applications, a single-phase inverter is used as the experimental example, as shown in Fig. 16. The capacitor bank employs the optimized arrangement from the previous section, and the specific parameters of the experimental platform are given in Table V.

TABLE V
SPECIFICATIONS OF INVERTER

Parameters	Values
DC voltage(V)	400 V
Switching frequency	10 kHz
Grid frequency	50 Hz
Power of Inverter	5.3 kW
DC-Link capacitor	3540 uF

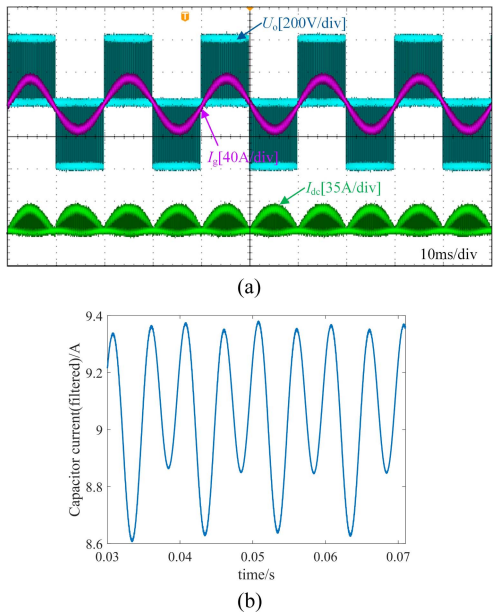


Fig. 17. Experimental waveforms. (a)Waveform of grid current, inverter output voltage, DC-side current. (b) Current of HCB.

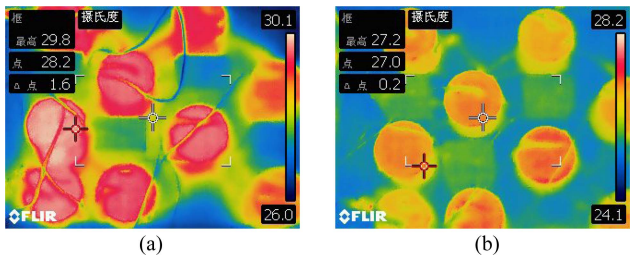


Fig. 18. Temperature distribution of the optimal arrangements under different cooling (Unit: °C). (a) Nature cooling. (b) Force cooling.

To prevent current sensor interference, the grid-side inductor current I_g and the dc-side current I_{dc} are used to synthesize the capacitor current I_c, as illustrated in Fig. 17.

The temperature distribution of the HCB is shown in Fig. 18. To verify the effectiveness of the proposed design method, thermal distribution results of the optimized arrangement are compared with those of the in-line arrangement under two cooling modes, as shown in Figs. 19 and 20. Under natural cooling, the average temperature of the E-cap in the hybrid staggered arrangement is reduced by 5.19% compared with that in the in-line arrangement. Under forced cooling, the average

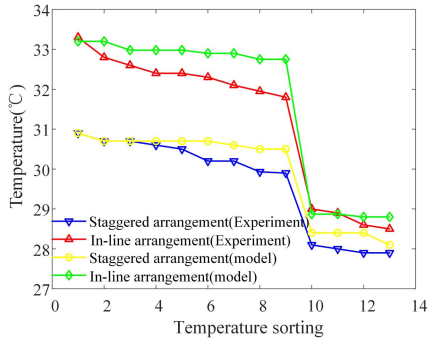


Fig. 19. Temperature distribution of two arrangements under natural convection.

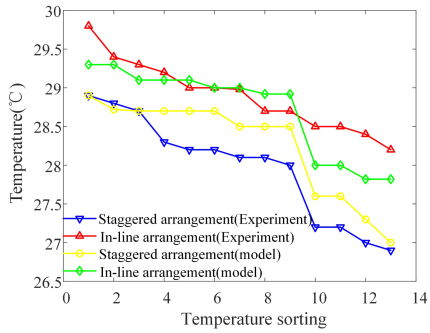


Fig. 20. Temperature distribution of two arrangements under forced convection.

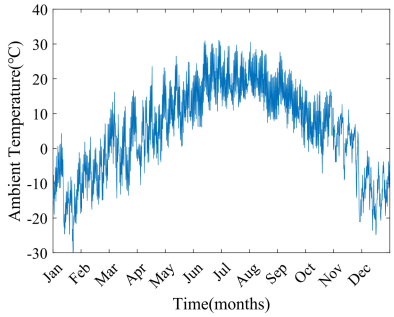


Fig. 21. Ambient temperature annual mission profiles.

temperature of the E-cap in the hybrid staggered arrangement is reduced by 3.22% compared with the in-line arrangement.

Validation of the proposed thermal model for inverter applications is shown in Figs. 19 and 20. The maximum steady-state thermal errors of the proposed model are 2.99%, 2.24% for in-line and staggered arrangements, respectively, under natural cooling. Under forced cooling, the maximum steady-state thermal errors are 2.04% and 2.8% for in-line and staggered arrangements, respectively.

To validate the impact of the proposed optimized arrangement on capacitor reliability, the mission profile-based reliability assessment methodology from [7] is applied. Fig. 21 presents the annual environmental temperature mission profile for Zhangjiakou, China.

To comprehensively account for the impact of model parameter variations on lifetime assessment, the parameters p_2, T_N, and L_0 in the lifetime model are assumed to vary within a range

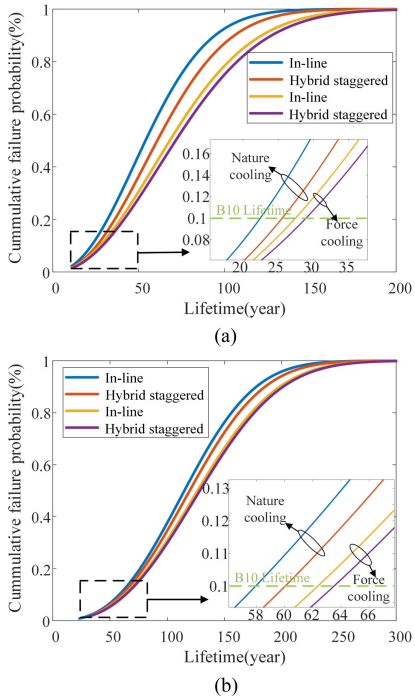


Fig. 22. Results of capacitance lifetime evaluation of hybrid capacitor bank with two arrangements and cooling methods. (a) Maximum temperature E-cap reliability assessment results. (b) Maximum temperature F-cap reliability evaluation results.

of 5% [13]. A Monte Carlo analysis with 10 000 samples is performed, followed by Weibull distribution fitting to construct the cumulative distribution function.

Fig. 22 shows the B10 life of E-cap and F-cap at the highest operating temperature, where B10 life represents the lifetime to a 10% failure rate.

For E-cap, under natural convection cooling, the lifetimes in the in-line and staggered arrangements are 22.3 and 25 years, respectively. Under forced cooling, the corresponding lifetimes for the E-cap in the in-line and staggered arrangements are 27.9 and 28.7 years. The staggered arrangement extends the E-cap lifetime by 12.1% under natural convection and by 2.8% under forced cooling.

For the F-cap, under natural convection cooling, the lifetimes in the in-line and staggered arrangements are 57.9 and 60 years, respectively. Under forced cooling, the corresponding lifetimes for the F-cap in the in-line and staggered arrangements are 62.3 and 63.5 years. The staggered arrangement extends the F-cap lifetime by 3.6% under natural convection and by 1.9% under forced cooling. These results show that the optimized arrangement of HCBs achieves a longer lifetime than the traditional in-line arrangement.

VI. Discussion

A. Analysis of Aging Effects

In studies of estimating capacitor lifespan, reliability methods that incorporate capacitor aging align most closely with observed failure characteristics under actual operating conditions [7]. Capacitor aging increases in ESR, which in turn leads to temperature rise. If these effects are not considered, lifespan

TABLE VI
COMPARISON OF DIFFERENT METHODS

	Comparative elements	Method in [22]	Method in [23]	Proposed
Thermal model	Objects	E-cap bank	F-cap bank	HCB
	Forced air cooling	/	Considered	Considered
	PCB thermal resistance	/	/	Considered
	Capacitor aging	/	Considered	Considered
	Thermal solution type	Steady state	Steady state	Steady/Transient state
Thermal even optimization	Arrangement	In-line	Staggered	Staggered
	Optimization method	thermal matching design	/	Proposed three steps method
	Optimization variable	rated parameters loading	/	Adjacent distance and angle
	Optimized results	Optimal capacitor type	Layout arrangement	Optimal layout arrangement

Note: The sign / represents not considering or not given out in refs.

estimates will be inaccurate. Therefore, ESR degradation must be incorporated into thermal modeling to simulate the stress conditions induced by long-term capacitor aging.

B. Analytical Thermal Models Comparison

Different analytical thermal models and thermal design methods for capacitor bank arrangements are compared in Table VI. In analytical thermal model, the approaches proposed in [22] and [23] are applicable only to steady-state thermal analysis of same type capacitor banks and do not account for PCB thermal resistance. Furthermore, Wang and H. Wang [22] neglect cooling conditions and aging effects, resulting in insufficient accuracy for lifetime estimation. In thermal optimization design, the staggered arrangement method proposed in [23] is derived only by shifting the relative positions of capacitors, and it does not provide a theoretical framework or specify array dimensions and variables. This method lacks a systematic design process, making it difficult to ensure an optimal temperature distribution. In [22], an in-line arrangement was designed to cool high-temperature zones by selecting capacitors with different ratings and loads. Compared with the methods in [22] and [23], the approach proposed for HCBs in this article enables precise transient thermal estimation and achieves optimal thermal layout design.

C. Discussion on System-Level Applications

From an application perspective, the integration of FEM and MOR is recognized for providing highly accurate and computationally efficient thermal analysis at the device level. However, at the system level, variations in operating conditions or circuit topologies necessitate regenerating the reduced-order matrices, resulting in considerable computational overhead [29]. Moreover, most FEM tools lack explicit circuit models, which restricts reliable electro–thermal co-simulation [30]. In contrast, analytical thermal network models can be seamlessly integrated with circuit simulators, providing rapid, nonintrusive, and parametrically flexible temperature estimation for system-level reliability evaluation [16]. In HCB layout optimization, this method rapidly evaluates different topologies to find the optimal temperature distribution, while the MOR–FEM approach needs to regenerate the reduced-order model whenever the topology is modified.

VII. CONCLUSION

This article investigates the thermal network modeling of HCB for the first time and proposes an analytical modeling and arrangement optimization method for transient-state thermal networks, considering thermal coupling and different heat dissipation modes. Theoretical analysis and comparative experimental results validate the effectiveness of the proposed approach, which offers the following advantages.

1) The proposed analytical thermal network model incorporates the influence of the PCB mounting method into the existing steady-state thermal model. By introducing equivalent heat capacity, the model is extended from the steady-state to the transient domain.
2) The proposed thermal network model achieves simulation times in the order of seconds while maintaining accuracy comparable to FEM simulations. Therefore, the proposed method provides significant performance improvements.
3) Based on the proposed thermal model, an optimized arrangement design method for HCBs is developed. This method enables thermal optimization and mitigates uneven thermal stress. Furthermore, reliability evaluation confirms that the optimized arrangement extends the service life of the capacitor bank.

APPENDIX

1) Derivation of the coupling thermal resistance $R_{i\text{-}j}$

$R_{i\text{-}j}$ consists of radiation thermal resistance $R_{\mathrm{rad},i\text{-}j}$ and conduction thermal resistance $R_{\mathrm{cond},i\text{-}j}$.

$$R_{i-j}=\frac{R_{\mathrm{cond},i-j}R_{\mathrm{rad},i-j}}{R_{\mathrm{cond},i-j}+R_{\mathrm{rad},i-j}}. \tag{A-1}$$

The derivation of $R_{\mathrm{rad},i\text{-}j}$ and $R_{\mathrm{cond},i\text{-}j}$ is detailed in (9)–(10).

1) Derivation of the case and ambient $R_{i\text{-amb}}$

$R_{i\text{-amb}}$ consists of radiation thermal resistance $R_{\mathrm{rad},i}$, convection thermal resistance $R_{\mathrm{conv},I}$, and composite thermal resistance $R_{\mathrm{indirect},i}$.

$$R_{i-\mathrm{amb}}=\frac{1}{\frac{1}{R_{\mathrm{rad},i}}+\frac{1}{R_{\mathrm{conv},i}}+\frac{1}{R_{\mathrm{indiret},i}}}. \tag{A-2}$$

The derivation of $R_{\mathrm{rad},i}$, $R_{\mathrm{conv},I}$, and $R_{\mathrm{indirect},i}$ is detailed in (11)–(15).

$R_{\mathrm{indirect},i}$ consists of the thermal conduction resistance of the thermal grease ($R_{\mathrm{grease},i}$), the thermal conduction resistance of the PCB ($R_{\mathrm{board},i}$), and the convective heat transfer resistance between the bottom surface of the PCB and the ambient environment ($R_{\mathrm{conv,board}}$)

$$R_{\mathrm{indirect},i}=\frac{1}{\frac{1}{R_{\mathrm{grease},i}}+\frac{1}{R_{\mathrm{board},i}}+\frac{1}{R_{\mathrm{conv,board}}}}. \tag{A-3}$$

The derivation of $R_{\mathrm{grease},i}$, $R_{\mathrm{board},I}$, and $R_{\mathrm{conv,board}}$ is detailed in (13)–(15).

1) Derivation of the thermal resistance Matrix $\boldsymbol{A}$

$$A = \begin{bmatrix}
-0.04 & 0.001 & 0 & 0.001 & 0 & 0 & 0 & 0 & 0 \\
0.001 & -0.0394 & 0.001 & 0 & 0.001 & 0 & 0 & 0 & 0 \\
0 & 0.001 & -0.04 & 0 & 0 & 0.001 & 0 & 0 & 0 \\
0.001 & 0 & 0 & -0.0394 & 0.001 & 0 & 0.001 & 0 & 0 \\
0 & 0.001 & 0 & 0.001 & -0.0389 & 0.001 & 0 & 0.001 & 0 \\
0 & 0 & 0.001 & 0 & 0.001 & -0.0394 & 0 & 0 & 0.001 \\
0 & 0 & 0 & 0.001 & 0 & 0 & -0.0392 & 0.001 & 0 \\
0 & 0 & 0 & 0 & 0.001 & 0 & 0.001 & -0.0383 & 0.001 \\
0 & 0 & 0 & 0 & 0 & 0.001 & 0 & 0.001 & -0..0392 \\
0 & 0 & 0 & 0 & 0 & 0 & 4.6431 \times 10^{-4} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 4.1821 \times 10^{-4} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 4.1821 \times 10^{-4} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 4.6431 \times 10^{-4}
\end{bmatrix}$$

$$\begin{bmatrix}
0 & 0 & 0 & 0 & 0.0379 \\
0 & 0 & 0 & 0 & 0.0363 \\
0 & 0 & 0 & 0 & 0.0379 \\
0 & 0 & 0 & 0 & 0.0363 \\
0 & 0 & 0 & 0 & 0.0347 \\
0 & 0 & 0 & 0 & 0.0363 \\
4.6431 \times 10^{-4} & 0 & 0 & 0 & 0.0367 \\
0 & 4.1821 \times 10^{-4} & 4.1821 \times 10^{-4} & 0 & 0.0343 \\
0 & 0 & 0 & 4.6431 \times 10^{-4} & 0.0367 \\
-0.0373 & 7.074 \times 10^{-4} & 0 & 0 & 0.0361 \\
7.074 \times 10^{-4} & -0.0369 & 7.0749 \times 10^{-4} & 0 & 0.0351 \\
0 & 7.0749 \times 10^{-4} & -0.0369 & 7.074 \times 10^{-4} & 0.0351 \\
0 & 0 & 7.074 \times 10^{-4} & -0.0373 & 0.0361
\end{bmatrix}. \quad \text{(A-4)}$$

After determining the thermal resistance, the thermal resistance matrix $\boldsymbol{A}$ is expressed using (8). For the in-line arrangement under natural convection, the specific form of $\boldsymbol{A}$ is given in equation (A-4) shown at the top of this page.

The equivalent heat capacity $\boldsymbol{C}_{\mathrm{c}}$ of the capacitor housing is obtained from FEM simulation. The transient temperature distribution is then calculated using (7).

Finally, the core temperature is derived from (5).

References

[1] S. M. Tayebi, H. Hu, and I. Batarseh, "Advanced DC-link voltage regulation and capacitor optimization for three-phase microinverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 307–317, Jan. 2019.

[2] M. Ghadrdan, S. Peyghami, H. Mokhtari, and F. Blaabjerg, "Condition monitoring of DC-link electrolytic capacitor in back-to-back converters based on dissipation factor," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9733–9744, Aug. 2022.

[3] H. Tong, W. Yao, C. Li, H. Luo, and W. Li, "Current sharing analysis and evaluation of parallel DC-link capacitors in vehicle motor drive," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 2188–2202, Apr. 2024.

[4] B. Yao, X. Ge, H. Wang, H. Wang, D. Zhou, and B. Gou, "Multitimescale reliability evaluation of DC-link capacitor banks in metro traction drive system," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 1, pp. 213–227, Mar. 2020.

[5] Z. Zhao, P. Davari, W. Lu, and F. Blaabjerg, "Online DC-link capacitance monitoring for digital-controlled boost PFC converters without additional sampling devices," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 907–920, Jan. 2023.

[6] P. Strajnikov, N. Amar, V. Yuhimenko, I. Aharon, and A. Kuperman, "Design constraints generalization for series-stacked buffer-based active DC links," *IEEE Trans. Ind. Electron.*, vol. 71, no. 2, pp. 2133–2136, Feb. 2024.

[7] C. Lv, J. Liu, Y. Zhang, W. Lei, R. Cao, and G. Lv, "Reliability modeling for metallized film capacitors based on time-varying stress mission profile and aging of ESR," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4311–4319, Aug. 2021.

[8] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[9] H. Wang, C. Li, G. Zhu, Y. Liu, and H. Wang, "Model-based design and optimization of hybrid DC-link capacitor banks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8910–8925, Sep. 2020.

[10] M. Chen, H. Wang, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "Reliability assessment of hybrid capacitor bank using electrolytic- and film-capacitors in three-level neutral-point-clamped inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2019, pp. 2826–2832.

[11] A. Yoshida, C. Kuji, T. Hasebe, and M. Ozawa, "A novel aluminum electrolytic capacitor suitable for high-frequency power converters," in *Proc. 20th Eur. Conf. Power Electron. Appl.*, Sep. 2018, pp. 1–10.

[12] X. Wang, M. Karami, and R. M. Tallam, "Test fixtures to apply variable DC bias and AC ripple current for reliability testing of electrolytic capacitors," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4073–4079, Jul./Aug. 2019.

[13] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of DC-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4064–4078, May 2019.

[14] M. Ghadrdan, B. Abdi, S. Peyghami, H. Mokhtari, and F. Blaabjerg, "Online condition monitoring system for DC-link capacitor of back-to-back converters using large-signal transients," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 1132–1142, Feb. 2023.

[15] M. A. Brubaker, D. E. Hage, T. A. Hosking, H. C. Kirbie, E. D. Sawyer, and P. Road, "Increasing the life of electrolytic capacitor banks using integrated high performance film capacitors," in *Proc. PCIM Eur. Conf.*, 2013.
[16] D. Zhou, Y. Song, Y. Liu, and F. Blaabjerg, "Mission profile based reliability evaluation of capacitor banks in wind power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4665–4677, May 2019.
[17] J. Wei, H. Feng, and L. Ran, "Integrated design for lifetime extension and ESR monitoring of hybrid DC link in solid-state transformer from the perspective of high-frequency ripple current," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15583–15593, Dec. 2022.
[18] A. Sangwongwanich et al., "Design for accelerated testing of DC-link capacitors in photovoltaic inverters based on mission profiles," *IEEE Trans. Ind. Appl.*, vol. 57, no. 1, pp. 741–753, Jan./Feb. 2021.
[19] Y. Wu and X. Du, "A VEN condition monitoring method of DC-link capacitors for power converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1296–1306, Feb. 2019.
[20] R. Yao, H. Li, W. Lai, A. S. Bahman, and F. Iannuzzo, "Lifetime analysis of metallized polypropylene capacitors in modular multilevel converter based on finite element method," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4248–4259, Aug. 2021.
[21] K. Kuang, X. Guo, Z. Zhou, C. Li, and X. Li, "Mission profile-based hotspot temperature and lifespan estimation of DC-link capacitors used in automotive traction inverters," *IEEE Trans. Device Mater. Rel.*, vol. 25, no. 1, pp. 134–143, Mar. 2025.
[22] H. Wang and H. Wang, "Analytical modeling and design of capacitor bank considering thermal coupling effect," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2629–2640, Mar. 2021.
[23] C. Lv, J. Liu, Y. Zhang, J. Yin, and X. Zhang, "A high-resolution analytical thermal modeling method of capacitor bank considering thermal coupling and different cooling modes," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7674–7684, Jun. 2023.
[24] C. Singhabahu, A. Ajiboye, R. Resalayyan, A. Singh, A. Hasnain, and A. Khaligh, "Modeling and optimal modulation of MAB converter using full-order impedance matrix," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 15231–15241, Nov. 2024.
[25] C. Xue, X. Wu, Y. Li, and Y. Li, "Virtual reduced-order model-based back EMF estimation and speed sensorless control for *LC*-filtered PMSM drives," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9749–9763, Jul. 2025.
[26] J. Yang, C. K. Tse, and D. Liu, "Nonlinear behavior and reduced-order models of islanded microgrid," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9212–9225, Aug. 2022.
[27] Y. Zhao, Z. Wang, D. Luo, C. Chen, B. Ji, and G. Li, "Multitimescale thermal network model of power devices based on POD algorithm," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 3906–3924, Apr. 2024, doi: 10.1109/TPEL.2023.3340675.
[28] R. Torchio et al., "Digital twins in power electronics: A comprehensive approach to enhance virtual thermal sensing," *IEEE Trans. Power Electron.*, vol. 40, no. 5, pp. 6977–6987, May 2025, doi: 10.1109/TPEL.2025.3531695.
[29] X. Dong, A. Griffo, and J. Wang, "Multiparameter model order reduction for thermal modeling of power electronics," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8550–8558, Aug. 2020, doi: 10.1109/TPEL.2020.2965248.
[30] Y. Jia, F. Xiao, Y. Duan, Y. Luo, B. Liu, and Y. Huang, "PSpice-COMSOL-based 3-D electrothermal–mechanical modeling of IGBT power module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4173–4185, Dec. 2020.
[31] J. He, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime evaluation of three-level inverters for 1500-V photovoltaic systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4285–4298, Aug. 2021.
[32] Y. Gupta, M. W. Ahmad, S. Narale, and S. Anand, "Health estimation of individual capacitors in a bank with reduced sensor requirements," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 7250–7259, Sep. 2019.
[33] Z. Lin, B. Yao, H. Sun, and H. Wang, "A robust capacitance control method for variable active capacitor," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11637–11649, Sep. 2024.
[34] M. Wang, W. Jiang, and K. Ma, "Circulating current controls for optimal thermal stress of capacitors in MMC systems," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 12435–12445, Oct. 2024.
[35] D. Shin, M. Poncino, and E. Macii, "Thermal management of batteries using supercapacitor hybrid architecture with idle period insertion strategy," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.*, vol. 26, no. 6, pp. 1159–1170, Jun. 2018.
[36] H. Wang and H. Wang, "Reliability evaluation and optimization of capacitor bank," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 7386–7390.
[37] Z. Zhao, D. Zhou, P. Davari, J. Fang, and F. Blaabjerg, "Reliability analysis of capacitors in voltage regulator modules with consecutive load transients," *IEEE Trans. Power Electron*, vol. 36, no. 3, pp. 2481–2487, Mar. 2021.
[38] Q. Gao et al., "Aging mechanism and life estimation of photovoltaic inverter DC-link capacitors in alternating humid and thermal environment," *Chin. J. Elect. Eng.*, vol. 10, no. 1, pp. 48–62, 2024.
[39] B. Sun, X. Fan, C. Qian, and G. Zhang, "PoF-simulation-assisted reliability prediction for electrolytic capacitor in LED drivers," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6726–6735, Nov. 2016.
[40] J. R. Howell and M. P. Mengüç, "Radiative transfer configuration factor catalog: A listing of relations for common geometries," *J. Quant. Spectrosc. Radiat. Transf.*, vol. 112, no. 5, pp. 910–912, Mar. 2011.
[41] Y. A. Cengel and A. J. Ghajar, *Heat and Mass Transfer: Fundamentals and Applications*, 4th ed., New York, NY, USA: McGraw Hill, 2011, pp. 90–833.
[42] G. Wan, K. Zhang, and K. Fu, "A 3-D finite difference method for obtaining the steady-state temperature field of a PCB circuit," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2032–2040, Feb. 2023.
[43] B. Kwon, T. Foulkes, T. Yang, N. Miljkovic, and W. P. King, "Air jet impingement cooling of electronic devices using additively manufactured nozzles," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 10, no. 2, pp. 220–229, Feb. 2020.
[44] K. Kuang, X. Guo, C. Li, and X. Li, "A novel lifetime estimation method and structural optimization design for film capacitors in EVs considering material aging and power losses," *IEEE Trans. Device Mater. Rel.*, vol. 24, no. 3, pp. 365–379, Sep. 2024.

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