Active Damping of *LC* Interphase Dynamics in Automotive 48-V Series-Capacitor Buck Converters

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***Abstract*—This article presents a 4:1 series-capacitor buck (SCB) converter designed for automotive 48 V-to-0.8 V applications, targeting improved transient response under rapid input voltage variations. The proposed design addresses the inherent interphase *LC* oscillations in hybrid dc–dc converters through a novel dynamic flying-capacitor voltage tracking technique. Unlike conventional methods, this approach employs dual flying-capacitor voltage regulators to dynamically adjust per-phase current commands, ensuring accurate current balancing and robust stability across a wide operating range. A comprehensive small-signal model is developed and analyzed to accurately capture and optimize the converter dynamics. Simulations indicate significant reductions in peak inductor currents during input transients. Experimental validation using a 62.5-A, 200-kHz prototype demonstrates a 4× reduction in flying-capacitor voltage settling time to 600 μs under fast input voltage transients. The proposed solution meets strict automotive reliability and performance requirements under rapid input-transient conditions, demonstrating improved overall transient response and enhanced system robustness.**

***Index Terms*—Active balancing, current-mode control, hybrid converter, input transient, interphase oscillation, series-capacitor buck, transient response.**

I. Introduction

THE shift from conventional 12-V or 24-V distribution networks to 48-V architectures in hybrid and electric vehicles (EVs) reduces current distribution losses and supports the development of compact, lightweight power delivery systems. Modern automotive processors operate at core voltages below 1 V, requiring higher voltage conversion ratios in power management units (PMUs). At power levels of 40 to 50 W [2], 48 V-to-core PMUs must deliver high efficiency and power density while ensuring tight output voltage regulation during fast transients [3], [4]. Original equipment manufacturers are still in the process of defining comprehensive 48-V PMU specifications, including input and output transient performance.

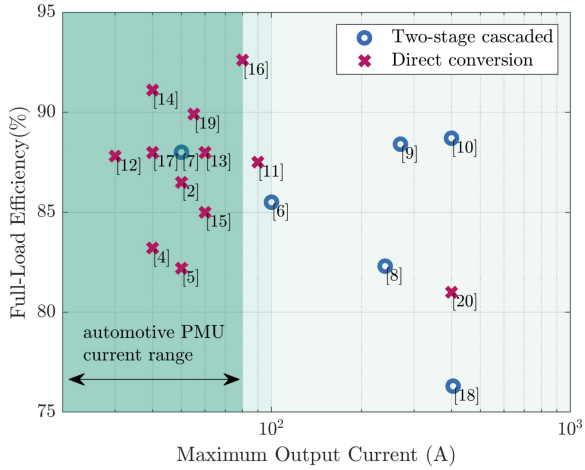

Fig. 1. Reported efficiency of 48 V-to-core converters operating at full load and an output voltage from 0.8 to 1.3 V [2], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20].

For the automotive PMU output current range shown in Fig. 1, the high step-down ratio is typically achieved using single-stage direct conversion to reduce power loss and minimize physical volume. In contrast, data-center applications with kilowatt-level output power often require two-stage architectures or heavily paralleled designs to meet much higher current and power density demands [3]. At the lower power levels considered in this work, such complex architectures offer limited advantage over optimized single-stage solutions. A survey of recent 48-V converter designs delivering output voltages from 0.8 V to 1.3 V supports this trend [2], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. Switched-capacitor converters are often used for high step-down-ratio direct conversion. To enhance current-handling capability while maintaining efficiency and compactness, hybrid topologies such as the series-capacitor buck (SCB) converter, as illustrated in Fig. 2, have emerged as a major focus of research in 48 V-to-core applications.

Strict output voltage regulation is essential for the reliable operation of advanced processors and electronic control units [4].

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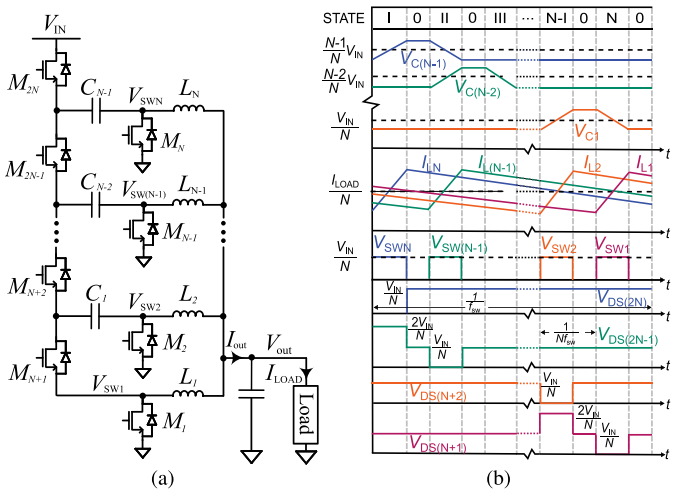

Fig. 2. (a) N:1 SCB converter. (b) Steady-state waveforms.

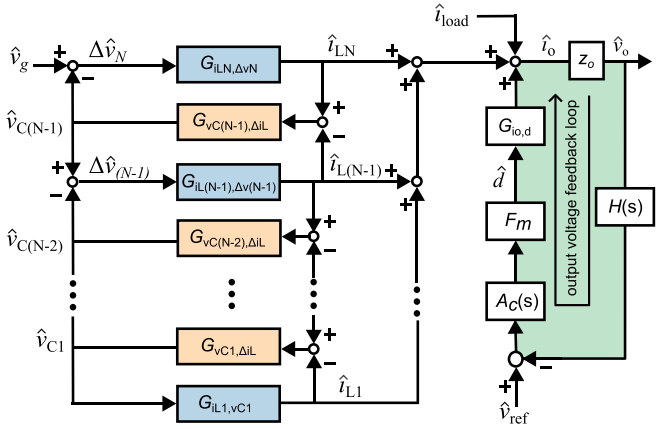

Fig. 3. Simplified small-signal block diagram of an N:1 SCB converter using PWM-based control, omitting $\hat{d}$-to-$\hat{i}_{\mathrm{Lj}}$, $\hat{d}$-to-$\hat{v}_{\mathrm{Cj}}$, and $\hat{v}_o$-to-$\hat{i}_{\mathrm{Lj}}$ dynamics.

In automotive electrical systems, load-dump transients represent a significant control challenge. A classical load dump occurs when the battery is suddenly disconnected while the alternator is charging, causing a high-voltage surge on the power bus, typically lasting from microseconds to milliseconds. The most severe conditions are defined in ISO 76372 for 12 and 24-V systems [21]. Although EVs do not employ traditional alternators, inductive subsystems such as electric power steering, pumps, and compressors connected in parallel on the 48-V bus can still generate similar overvoltage transients when their current paths are abruptly interrupted. These events are not classical load dumps but can exhibit comparable electrical stress and must be mitigated through appropriate transient suppression and control strategies. Without proper suppression, the bus voltage can exceed 200 V [22]. To limit overvoltage stress on the power delivery network, designers typically employ a 60-V transient voltage suppressor diode on the input bus [23]. Despite this, the bus voltage still rises quickly from 48 to 60 V, exciting oscillations in the LC network formed by the flying capacitors and power inductors of the SCB converter [24]. These oscillations increase the required saturation current of inductors and the maximum drain-source voltage ($V_{DS,\max}$) ratings of power devices, which raises converter cost and volume. This transient can also disturb the output voltage.

Prior SCB controller designs, primarily based on pulsewidth modulation (PWM), were developed to improve load-transient performance. Although PWM schemes provide steady-state current sharing [24], the voltage regulation loop is decoupled from cross-coupled LC interactions, as illustrated in Fig. 3. Thus, damping interphase LC oscillations depends on the parasitic resistances of the power stage [1]. Large capacitor banks near the battery help attenuate low-frequency ripple and slow voltage surges, but they cannot effectively suppress high-dV/dt transients at the point of load due to harness inductance and the equivalent series inductance (ESL) of the capacitors. For automotive PMUs, volume and cost are critical considerations, which limit the use of excessively large capacitance to suppress high dV/dt on the bus. Electrolytic capacitors offer high volumetric energy density, but suffer from high ESL, making them ineffective against fast transient events. Film capacitors provide improved high-frequency performance, but become bulky and costly at 48 V and above. Multilayer ceramic capacitors offer excellent volume efficiency for small capacitance values, but are limited by voltage derating, critical for 48-V applications. Moreover, sudden changes in flying-capacitor voltage or inductor current can still trigger interphase oscillations, which a higher input capacitance alone cannot suppress. As demonstrated in [25], using coupled inductors across all phases reduces resonance amplitude but increases settling time and design complexity due to the need for custom magnetic components.

Comparisons between the SCB converter and other topologies reveal key strategies for flying-capacitor voltage balancing and current sharing, which are critical for reducing interphase oscillations. For example, both the flying-capacitor multilevel (FCML) converter and the SCB converter use series-stacked inputs with flying capacitors. FCML converters, which use a single inductor, often require active balancing to maintain safe voltage limits but exhibit fewer cross-coupled LC interactions in comparison. The dual-inductor hybrid (DIH) converter with an auxiliary converter to improve transient response, proposed in [26], also introduces interphase LC oscillations due to abrupt flying-capacitor voltage steps; both voltage-sensed and sensorless current-balancing techniques have been applied to mitigate these oscillations. However, with only two power inductors, the DIH converter exhibits simpler LC dynamics, similar to those of the FCML architecture. Multiphase buck converters, similar to SCBs, provide parallel current paths to the output. The main distinction lies in the inductor voltage during transients: SCB phase inductors experience changing voltages due to flying-capacitor variations, whereas inductors in multiphase buck converters consistently see $V_{\mathrm{IN}} - V_{\mathrm{OUT}}$.

This work is an extension of [1], where an SCB converter control scheme that enables fast, active suppression of interphase LC oscillations during line transients while maintaining charge balancing in steady state was presented. The remainder of this article is organized as follows. Section II

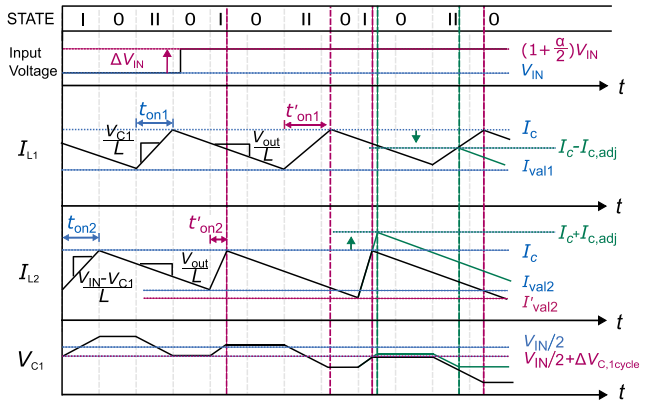

Fig. 4. Input step-up waveforms of a 2:1 SCB converter in PCM with a current command of I_c, showing a runaway capacitor voltage.

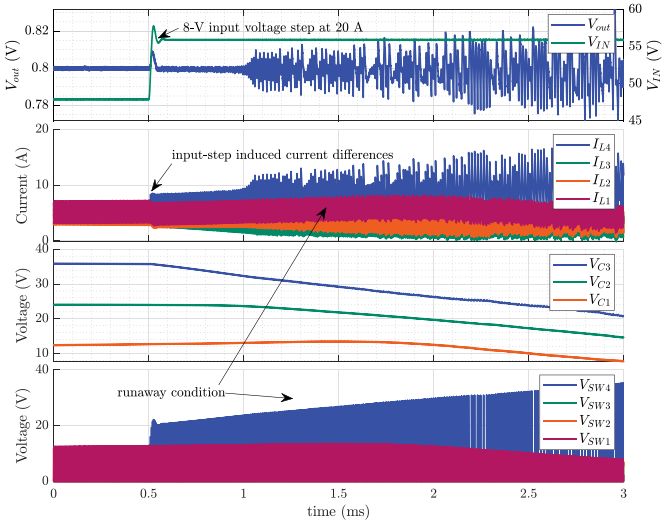

Fig. 5. Simulated 4:1 SCB using VCM control at $I_{\text{LOAD}} = 20\,\text{A}$ with the input stepped from 48 to 56 V at $1\,\text{V}/mu\text{s}$ without active balancing.

presents this control architecture with interphase oscillation suppression. Per-phase current commands are adjusted using the outputs of two neighboring flying-capacitor voltage-tracking regulators to achieve fast balancing after transient events. This article builds on [1] by introducing a small-signal model of the SCB converter that includes parasitic elements in Section III, enabling accurate modeling of interphase oscillations. In addition, the linearized valley-current-mode (VCM) controller with an integrated LC-oscillation suppressor is derived, with the system stability characteristics compared against those of a conventional PWM-based controller. Sections IV and V present the simulation and experimental results, respectively. Specifically, this work expands on [1] by including the experimental results for fast input-step and load-step transient response. Finally, Section VI concludes the article.

II. Current-Mode Controller With LC-Interphase Oscillation Suppression

Current-mode control (CMC) provides inherently fast rejection of input voltage variations. Direct regulation of output current by the inner loop enables the controller to respond to input changes before they affect the output voltage, while suppressing oscillations through cycle-by-cycle current comparison. However, conventional fixed-frequency peak-current-mode (PCM) or valley CMC introduces a positive feedback loop between the inductor current slew rate and the flying-capacitor voltages.

A 2:1 SCB converter, which exhibits simpler dynamics than higher level SCB converters, is analyzed using PCM control to examine the potential imbalance in response to an input voltage step-up. The timing diagram for this scenario is shown in Fig. 4, with the current command $I_c = I_{\text{L1,pk}} = I_{\text{L2,pk}}$. A step of size $\Delta V = \alpha(V_{\text{IN}} - V_{\text{C1}})$ is applied to the input of the converter. The duration in state I t_{on2} immediately after this input voltage step t'_{on2} is approximated as

$$t'_{\text{on2}} \approx \frac{(I_c - I_{\text{val2}})L}{V_{\text{IN}} - V_{\text{C1}} + \Delta V} = \frac{t_{\text{on2}}}{\alpha + 1} \tag{1}$$

where I_{val2} is the steady-state valley current before the transient. Given that $\Delta t_{\text{on2}} = t'_{\text{on2}} - t_{\text{on2}} < 0$, the valley current at the end of this switching cycle becomes

$$I'_{\text{val2}} = I_c - \frac{(T_{\text{SW}} - t'_{\text{on2}})V_{\text{out}}}{L_2} \tag{2}$$

which decreases with a shorter t'_{on2}. This negative feedback to t_{on2} helps balance the currents if I'_{val2} is significantly reduced. However, due to the significant difference in positive and negative inductor current slope in the 48V-to-core application, the impact of

$$\Delta I_{\text{val2}} = I'_{\text{val2}} - I_{\text{val2}} = \frac{\Delta t_{\text{on2}} V_{\text{out}}}{L_2} \tag{3}$$

remains insignificant compared to that of Δt_{on2}, allowing the approximation $\langle I'_{\text{L2}} \rangle_{T_{\text{SW}}} \approx \langle I_{\text{L2}} \rangle_{T_{\text{SW}}}$. Meanwhile, the change in on-time of M_4 reduces V_{C1} after a full switching period, where

$$\Delta V_{\text{C1,cycle}} = \frac{\langle I_{\text{L2}} \rangle_{T_{\text{SW}}} t'_{\text{on2}} - \langle I_{\text{L1}} \rangle_{T_{\text{SW}}} t_{\text{on1}}}{C_1}$$

$$= \frac{I_{\text{LOAD}} \Delta t_{\text{on2}}}{2C_1} \tag{4}$$

is negative and especially noticeable at higher output currents. With the goal of increasing V_{C1} to $(V_{\text{IN}} + \Delta V)/2$, the negative value of $\Delta V_{\text{C1,cycle}}$ drives the flying capacitor away from a balanced steady state. Furthermore, with

$$t'_{\text{on1}} \approx \frac{(I_c - I_{\text{val1}})L}{V_{\text{C1}} + \Delta V_{\text{C1,cycle}}} \tag{5}$$

the on-time of M_3 (state II duration) extends, further reducing V_{C1} when combined with the shortened t'_{on2} based on (1). The SCB converter requires nonoverlapping magnetization periods between inductors from consecutive phases, adding the constraint to the maximum high-side device turn-ON time to $t_{\text{on,max}} = T_{\text{SW}}/N$. Thus, t_{on1} eventually saturates at $T_{\text{SW}}/2$ as a result of the lowered V_{C1}. V_{C1} continues to drop, ultimately leading to voltage runaway. Fig. 5 presents the simulated results of a 4:1 SCB converter using a conventional fixed-frequency

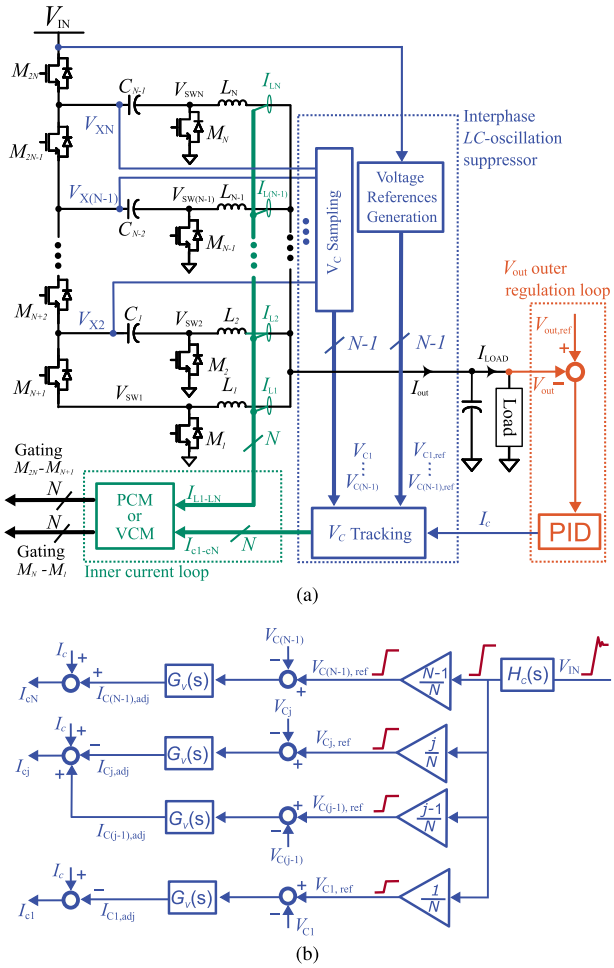

Fig. 6. (a) Proposed N:1 SCB converter control architecture using (b) the LC-oscillation suppressor with dynamic voltage-tracking.

VCM controller with slope compensation of $m_{\text{sc}} = 13.4\,\text{A}/\mu\text{s}$ to ensure the VCM stability, responding to a rapid input voltage step. The resulting runaway condition, initiated by the uppermost phase, leads to phase current imbalance and system instability. These results emphasize the need for active balancing when applying CMC to SCB converters.

A. Proposed Control

The proposed control architecture for an N:1 SCB converter is shown in Fig. 6(a), incorporating adjustment current commands $I_{\text{Cj,adj}}$ from the voltage-tracking regulators depicted in Fig. 6(b). This work considers both fixed-frequency PCM and VCM control schemes. Inductor currents I_{Lj} (for $j = 1, \ldots, N$) are equalized by maintaining uniform peak or valley values and identical current ripple amplitudes in steady state. The current ripple of inductor L_j on phase j, denoted ΔI_{Lj}, is given by

$$\Delta I_{\text{Lj}} = \frac{(V_{\text{Cj}} - V_{\text{C(j-1)}})t_{\text{on}}}{L_j} \tag{6}$$

with boundary conditions $V_{\text{CN}} = V_{\text{IN}}$ and $V_{\text{C0}} = 0$. For $N > 2$, inductor currents I_{Lj} for $j = 2, \ldots, N-1$ are influenced by two neighboring flying capacitors. To ensure uniform ΔV_{Cj}, the converter must satisfy $V_{\text{Cj}} - V_{\text{C(j-1)}} = V_{\text{IN}} - V_{\text{C(N-1)}} = V_{\text{C1}}$. Accordingly, the dynamic flying-capacitor voltage references are defined as $V_{\text{Cj,ref}} = jV_{\text{IN}}/N$ to maintain balanced phase currents.

The control scheme employs a feedforward path from the input voltage to adjust the current command generated by the outer voltage regulation loop, thereby suppressing interphase LC oscillations during line disturbances. Following a transient, each V_C tracking controller immediately detects a voltage error of

$$\Delta V_{\text{Cj,error}} = \frac{j\Delta V_{\text{IN}}}{N} \tag{7}$$

by comparing the input-voltage-based reference with the sensed flying-capacitor voltage. To regulate this error to zero, the controller generates adjustment current commands, denoted by $I_{\text{Cj,adj}}$. This mechanism prioritizes tracking for higher level flying capacitors, which is desirable since I_{LN} increases rapidly and M_N experiences the greatest voltage stress during a step-up transient. When the current commands for phase j, I_{cj}, are summed, the adjustment terms cancel, yielding

$$NI_c = \sum_{j=1}^{N} I_{\text{cj}} \tag{8}$$

which reduces the impact of line transients on I_{out}.

Fig. 4 illustrates how the proposed control achieves active balancing after a step change in input voltage. Upon detecting a decrease in flying-capacitor voltage, the control adjustment command extends t'_{on2} and reduces t'_{on1}, which increases $\langle I_{\text{L2}}\rangle_{T_{\text{SW}}}$ and decreases $\langle I_{\text{L1}}\rangle_{T_{\text{SW}}}$. These changes act to increase $\Delta V_{\text{C1,cycle}}$ in (4), eventually making it positive to restore the flying-capacitor voltage.

Although the series-input structure of an SCB converter reduces the magnetizing voltage across the inductors compared to a conventional step-down converter, the positive inductor current slope m_{mag} remains significantly greater than the negative slope at high conversion ratios. Under the nominal ratio of 48 V-to-0.8 V, m_{mag} is approximately $11\times$ larger. This makes accurate peak current sensing considerably more difficult than valley-current sensing. Consequently, VCM is the more practical control strategy for this topology and is adopted in the subsequent analysis. With a maximum on-time of $t_{\text{on,max}} = T_{\text{SW}}/N$, slope compensation with a minimum required slope of

$$m_{\text{sc}}^{\min} = \frac{m_{\text{mag}}}{2} = \frac{V_{\text{IN,max}} - NV_{\text{out}}}{2NL} \tag{9}$$

is necessary to prevent subharmonic oscillation under VCM-based control. Slope compensation can contribute to balancing by acting as a proportional controller with a low gain. However, the slope required to ensure current balancing, dependent on load current and switching frequency in addition to the parameters used to calculate $m_{sc}^{\min}$, is significantly greater than $m_{sc}^{\min}$ and is not suitable as a standalone method.

B. Flying-Capacitor Voltage Sensing

Accurate sensing of flying-capacitor voltages is essential for the proposed control scheme. To maintain charge balance, the

TABLE I
KEY SYSTEM PARAMETERS

Parameter	Value	Unit
Input voltage, V_{IN}	24 - 60	V
Nominal input voltage, $V_{\mathrm{IN,nom}}$	48	V
Output voltage, V_{OUT}	0.8	V
Switching frequency, f_{SW}	200	kHz
Rated load power, P_{RATED}	50	W
Line inductance, L_{line}	2.5	µH
Line resistance, R_{line}	300	mΩ
Output capacitor, C_{OUT}	800	µF
Input capacitor, C_{IN}	30	µF
High-side ON-resistance, $R_{\mathrm{ON,H}}$	6	mΩ
Low-side ON-resistance, $R_{\mathrm{ON,L}}$	0.8	mΩ
Inductors, $L_{4,3,2,1}$ or L_{main}	1	µH
Inductor DCR, R_L	1	mΩ
Flying capacitors, $C_{3,2,1}$	30	µF
Flying capacitors ESR, C_R	800	µΩ

most suitable method for estimating $V_{\mathrm{C1-3}}$ is to compute the average of the sensed peak and valley voltages over a complete switching cycle. At steady state, under the nominal 48 V-to-0.8 V condition, each flying capacitor remains at its peak voltage for approximately 18.3% of the cycle and at its valley for 68.3%. While this enables reliable capture of both peak and valley voltages at a switching frequency of 200 kHz, the timing margin is not guaranteed during fast transients. In worst-case events, such as load step-ups or line disturbances, a sharp reduction in I_{cj} can shorten the interval between adjacent nonzero switching states to nearly zero. Consequently, the available window for accurate peak voltage sensing is significantly reduced. In contrast, the valley voltage of each capacitor is maintained for at least 50% of the switching period, making valley-based sensing a more robust and practical approach.

Adopting valley-voltage sensing on the flying capacitors introduces a small inductor-current offset proportional to I_{OUT}. This offset is analytically predictable and remains negligible when the flying capacitors are properly sized. To correct this offset, the dynamically generated capacitor reference voltages can be adjusted based on the current command under varying loads. The midpoint voltage $V_{\mathrm{C1\text{-}3}}$ can also be estimated from the measured phase current and high-side switch on-times to compensate for the inductor current offset. Both correction techniques increase design complexity and are warranted only when precise inductor current offset control is required.

III. COMPARATIVE STABILITY ANALYSIS OF PWM AND PROPOSED CONTROL IN SCB CONVERTERS

A small-signal model of the converter is developed to analyze the dynamic behavior of the proposed control scheme. The analysis focuses on loop stability, accounting for the effects of slope compensation and the proposed flying-capacitor voltage feedback under VCM control. For the automotive 48 V-to-0.8 V application, a 4:1 SCB converter with parameters listed in Table I is used for the simulations.

TABLE II
DEFINITION OF VARIABLES FOR THE SMALL-SIGNAL MODEL

Symbol	Definition
R_{eq4}	$R_L + R_{\mathrm{ON,L}} + R_{\mathrm{ON,H}} D_4$
R_{eq3}	$R_L + R_{\mathrm{ON,L}} + (R_{\mathrm{ON,H}} + 2R_{\mathrm{ON,L}})\, D_3$
R_{eq2}	$R_L + R_{\mathrm{ON,L}} + (R_{\mathrm{ON,H}} + 2R_{\mathrm{ON,L}})\, D_2$
R_{eq1}	$R_L + R_{\mathrm{ON,L}} + (R_{\mathrm{ON,L}} + R_{\mathrm{ON,H}})\, D_1$
κ_4	$V_{\mathrm{IN}} - V_{\mathrm{C3}} - R_{\mathrm{ON,H}} I_{\mathrm{L4}}$
κ_3	$V_{\mathrm{C3}} - V_{\mathrm{C2}} - (R_{\mathrm{ON,H}} + 3R_{\mathrm{ON,L}})\, I_{\mathrm{L3}}$
κ_2	$V_{\mathrm{C2}} - V_{\mathrm{C1}} - (R_{\mathrm{ON,H}} + 3R_{\mathrm{ON,L}})\, I_{\mathrm{L2}}$
κ_1	$V_{\mathrm{C1}} - (R_{\mathrm{ON,H}} + 2R_{\mathrm{ON,L}})\, I_{\mathrm{L1}}$

A. Small-Signal Modeling

Key parasitic elements in the power stage, specifically the MOSFET on-resistances and the inductor DCR, must be included to accurately characterize interphase dynamics. A small-signal model is developed for the 4:1 SCB converter using the specifications listed in Table I. For clarity, selected expressions are simplified using the variable definitions provided in Table II.

The DC analysis reveals that $I_{\mathrm{L4}} = I_{\mathrm{L3}} = I_{\mathrm{L2}} = I_{\mathrm{L1}}$ and $D_4 = D_3 = D_2 = D_1$. Let $\beta_j = I_{\mathrm{Lj}}\hat{d}_j + D_j\hat{i}_{\mathrm{Lj}}$. The resulting system of equations for the converter is given as follows:

$$D_4\hat{v}_{\mathrm{IN}} - D_4\hat{v}_{\mathrm{C3}} - R_C\beta_4 + R_{\mathrm{ON,L}}\,(\beta_4 - \beta_3)$$

$$= L_4\frac{d\hat{i}_{\mathrm{L4}}}{dt} - \kappa_4\hat{d}_4 + R_{\mathrm{eq4}}\hat{i}_{\mathrm{L4}} + \hat{v}_{\mathrm{out}}$$

$$D_3\hat{v}_{\mathrm{C3}} - D_3\hat{v}_{\mathrm{C2}} - 2R_C\beta_3 + R_{\mathrm{ON,L}}\,(2\beta_3 - \beta_4 - \beta_2)$$

$$= L_3\frac{d\hat{i}_{\mathrm{L3}}}{dt} - \kappa_3\hat{d}_3 - R_{\mathrm{ON,L}}I_{\mathrm{L4}}\hat{d}_4 + R_{\mathrm{eq3}}\hat{i}_{\mathrm{L3}} + \hat{v}_{\mathrm{out}}$$

$$D_2\hat{v}_{\mathrm{C2}} - D_2\hat{v}_{\mathrm{C1}} - 2R_C\beta_2 + R_{\mathrm{ON,L}}\,(2\beta_2 - \beta_3 - \beta_1)$$

$$= L_2\frac{d\hat{i}_{\mathrm{L2}}}{dt} - \kappa_2\hat{d}_2 - R_{\mathrm{ON,L}}I_{\mathrm{L3}}\hat{d}_3 + R_{\mathrm{eq2}}\hat{i}_{\mathrm{L2}} + \hat{v}_{\mathrm{out}}$$

$$D_1\hat{v}_{\mathrm{C1}} - R_C\beta_1 + R_{\mathrm{ON,L}}\,(\beta_2 - \beta_1)$$

$$= L_1\frac{d\hat{i}_{\mathrm{L1}}}{dt} - \kappa_1\hat{d}_1 - R_{\mathrm{ON,L}}I_{\mathrm{L2}}\hat{d}_2 + R_{\mathrm{eq1}}\hat{i}_{\mathrm{L1}} + \hat{v}_{\mathrm{out}}$$

$$\beta_4 - \beta_3 = C_3\frac{d\hat{v}_{\mathrm{C3}}}{dt}$$

$$\beta_3 - \beta_2 = C_2\frac{d\hat{v}_{\mathrm{C2}}}{dt}$$

$$\beta_2 - \beta_1 = C_1\frac{d\hat{v}_{\mathrm{C1}}}{dt}.$$

For an N:1 SCB converter, the input-voltage-to-inductor-current transfer functions $G_{\mathrm{iLj,vg}}$ and the input-voltage-to-flying-capacitor-voltage transfer functions $G_{\mathrm{vCj,vg}}$ exhibit $N-1$ interphase resonant frequencies. The damping ratios of these resonances are strongly influenced by the converter's design parameters; in particular, highly efficient converters tend to exhibit lower damping.

The VCM controller and the LC-oscillation suppressor are linearized and incorporated into the model. The resulting

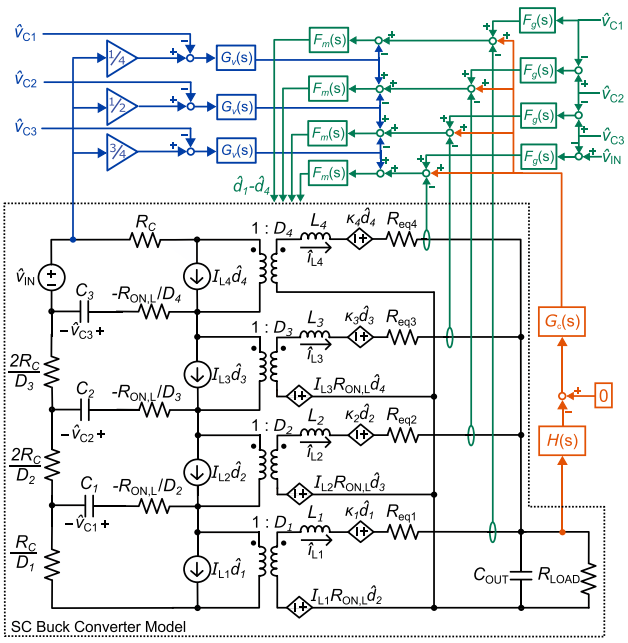

Fig. 7. Small-signal model of the proposed architecture.

system-level linearized model is shown in Fig. 7. In this model, $H(s)$ and $G_c(s)$ represent the output-voltage sensing block and the outer PID controller, respectively. $F_g(s)$ denotes the input-to-inductor-current transfer function for each phase, given by

$$F_g\,(\mathrm{s}) = \frac{D(1-D)}{2f_{\mathrm{SW}}L_{\mathrm{main}}}. \tag{10}$$

$F_m(s)$ models the conversion of the cycle-by-cycle current comparison into an effective duty cycle, incorporating the slope compensation term m_{sc}, defined as

$$\begin{aligned} F_m\,(\mathrm{s}) &= \frac{2f_{\mathrm{SW}}}{2m_{\mathrm{sc}} - m_1 + m_2} \\ &= \frac{L_{\mathrm{main}}f_{\mathrm{SW}}}{L_{\mathrm{main}}m_{\mathrm{sc}} + V_{\mathrm{out}} - V_{\mathrm{IN}}/8} \end{aligned} \tag{11}$$

where m_1 and m_2 are the magnetizing and demagnetizing slopes of the inductors $L_{4,3,2,1}$, respectively.

The linear model is validated in Fig. 8 by comparing its response to a small input step with that of the full converter switching circuit. The "Filtered Average" waveform is obtained from the switching circuit simulation result: the output voltage and inductor currents are processed using a third-order Butterworth filter, while the flying-capacitor voltages are calculated by averaging their peak and valley values within each switching cycle. The results show strong agreement in both output and interphase dynamic behavior, confirming the model's suitability for controller design and system-level stability analysis.

B. Stability Analysis

The derived linear model of the proposed controller is used to compare stability and interphase dynamic response against a

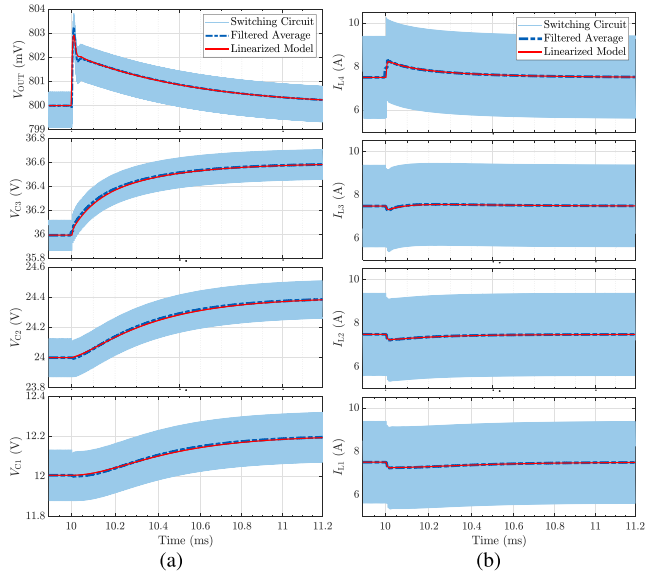

Fig. 8. Dynamic response of key (a) voltages and (b) currents of the 4:1 SCB converter using the proposed controller under a small input transient of 1 V at 0.1 V/ns, simulated using the full switching model and the linearized model.

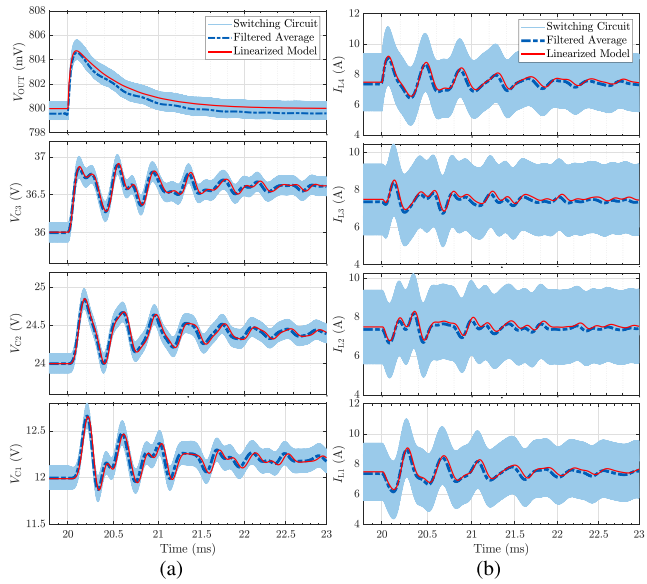

Fig. 9. Dynamic response of key (a) voltages and (b) currents of the SCB converter using a conventional PWM controller under a small input transient of 1 V at 0.1 V/ns, simulated using both the full switching model and the linearized model.

conventional PWM-based controller. Both controllers are tuned to have a phase margin of approximately 40° at 50% load and the nominal conversion ratio. The linear model of the PWM controller is validated in Fig. 9, showing a near-perfect match in LC interphase dynamics with the switching model, despite the underlying complexity of interphase interactions.

For automotive applications, the wide range of operating conditions, including variations in load current, presents a significant challenge for controller design. To ensure the proposed controller maintains stability across the full operating range, loop gain is evaluated from 5 A (light-load condition) to 62.5 A

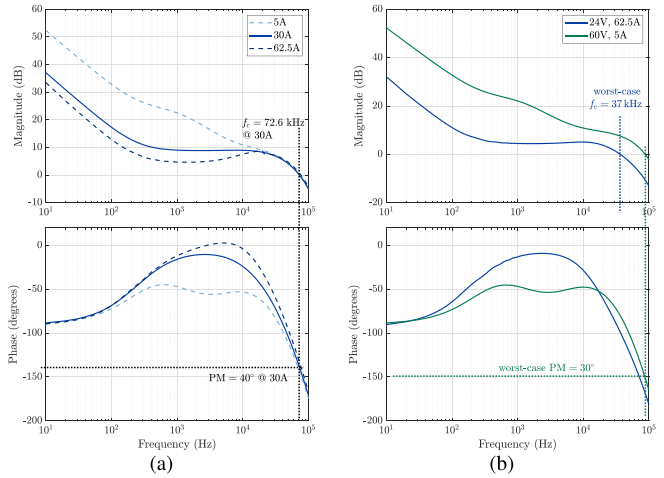

Fig. 10. Loop gain of the converter using proposed controller (a) with a 48-V bus at various load conditions and (b) at operating corners with the worst-case crossover frequency f_c and phase margin.

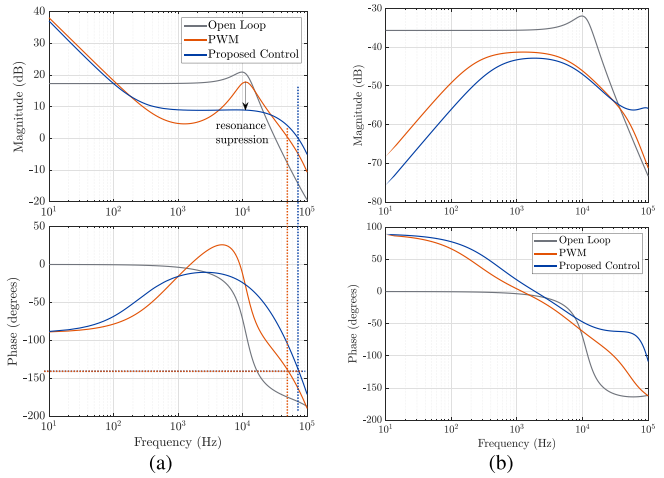

Fig. 11. Comparison between PWM-based control and the proposed VCM-based control of (a) control-to-output and (b) closed-loop $\hat{v}_{\text{IN}}$-to-$\hat{v}_{\text{out}}$ transfer function at 48 V-to-0.8 V conversion ratio and 30-A load condition.

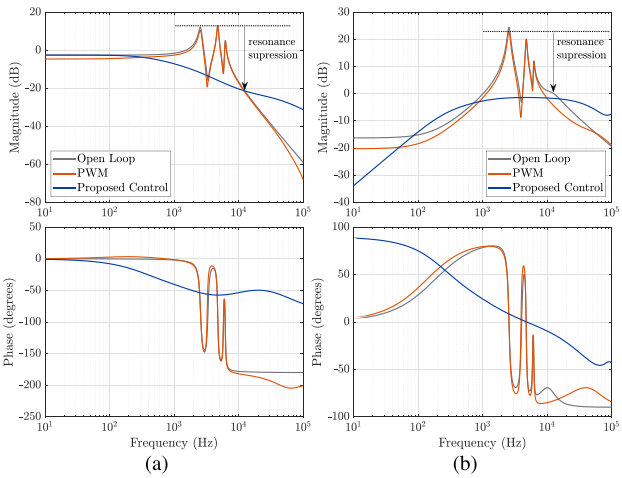

Fig. 12. Transfer characteristic comparison between the PWM-based and the proposed control from $\hat{v}_{\text{IN}}$ (a) to $\hat{v}_{\text{C3}}$ and (b) to $\hat{i}_{\text{L4}}$, respectively.

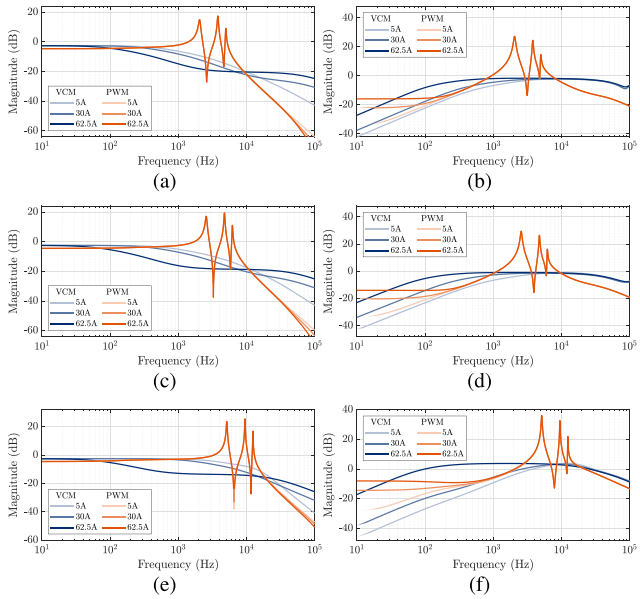

Fig. 13. Gain response comparison across load conditions, specifically (a) $\hat{v}_{\text{IN}}$-to-$\hat{v}_{\text{C3}}$ and (b) $\hat{v}_{\text{IN}}$-to-$\hat{i}_{\text{L4}}$ for $\hat{v}_{\text{IN}} = 60$ V, (c) $\hat{v}_{\text{IN}}$-to-$\hat{v}_{\text{C3}}$ and (d) $\hat{v}_{\text{IN}}$-to-$\hat{i}_{\text{L4}}$ for $\hat{v}_{\text{IN}} = 48$ V, and (e) $\hat{v}_{\text{IN}}$-to-$\hat{v}_{\text{C3}}$ and (f) $\hat{v}_{\text{IN}}$-to-$\hat{i}_{\text{L4}}$ for $\hat{v}_{\text{IN}} = 24$ V.

(full-load condition), and at both the minimum and maximum V_{IN} values listed in Table I. The simulation result, as shown in Fig. 10, confirm robust performance under all required conditions. The primary tuning objective is to achieve high control bandwidth at full load while maintaining sufficient phase margin at light load. In addition, the phase margin must remain adequate at the highest conversion ratio, which represents the worst-case stability condition, as shown in Fig. 10(b). Loop-gain simulation results show a minimum phase margin of 30° at $V_{\text{IN}} = 60$ V and $I_{\text{OUT}} = 5$ A, and a minimum crossover frequency of 37 kHz at $V_{\text{IN}} = 24$ V and $I_{\text{OUT}} = 62.5$ A.

The proposed controller demonstrates an improvement of approximately 22 kHz in crossover frequency f_c, compared to the benchmark PWM-based design when both are tuned to a similar phase margin, as shown in Fig. 11(a). Unless otherwise specified, all stability analyses are performed with the models biased at $I_{\text{OUT}} = 30$ A and the nominal conversion ratio. As shown in Fig. 11(b), the $\hat{v}_{\text{IN}}$-to-$\hat{v}_{\text{out}}$ transfer function shows greater improvement at lower frequencies, while the two controllers exhibit minimal difference at higher frequencies. This is primarily due to the effectiveness of the derivative term in the PWM-based PID controller and the output filter in attenuating the resonance observed in Fig. 11(a). However, the attenuation effect of the output filter is reduced under light-load conditions for the PWM-controlled converter.

In contrast, the improvement in interphase dynamics achieved by the proposed controller is clearly demonstrated in Fig. 12. The absence of resonance in $\hat{v}_{\text{C3}}$ and $\hat{i}_{\text{L4}}$ highlights the effectiveness of its resonance-suppression mechanism. The PWM-based controller provides virtually no attenuation of interphase LC resonances compared to the open-loop response, exhibiting peak gains of 12.9 dB in $\hat{v}_{\text{C3}}$ and 23.2 dB in $\hat{i}_{\text{L4}}$, as shown in Fig. 12. By contrast, the proposed controller achieves a maximum gain

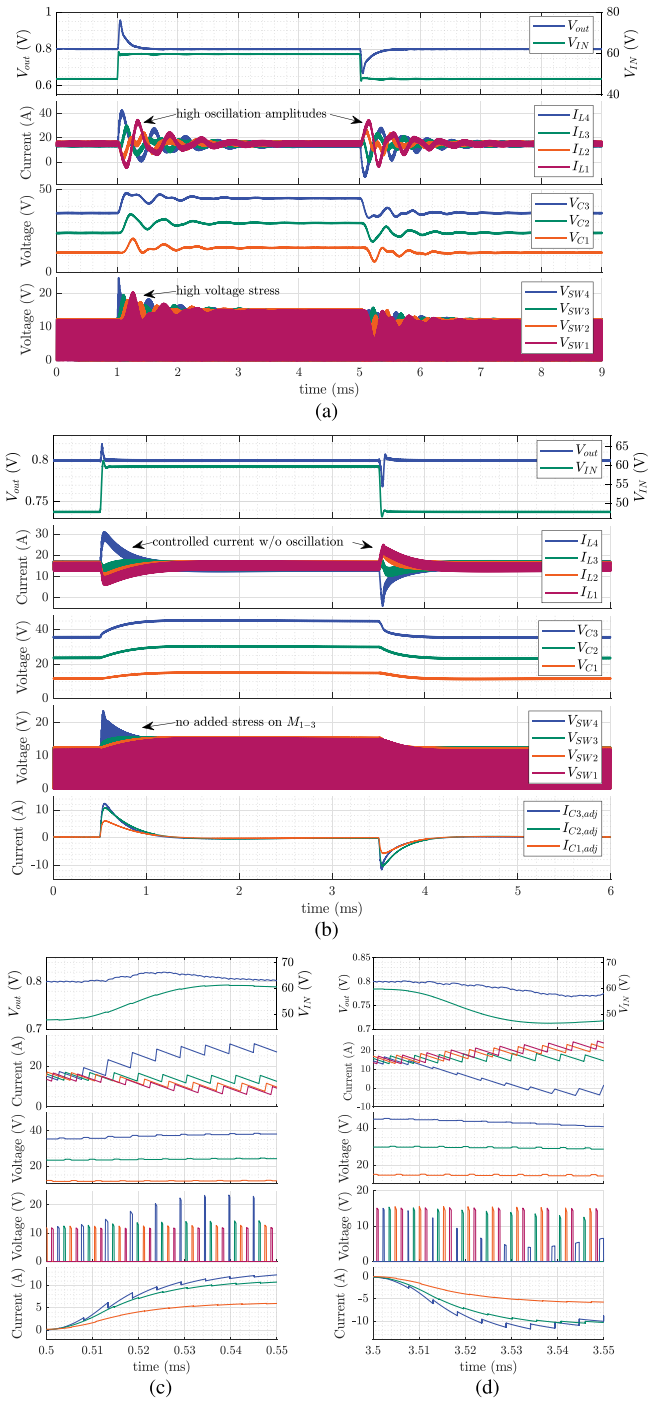

Fig. 14. Simulated response of a 4:1 SCB converter to a line step from 48 to 60 V with a 1-V/μs slew rate at $I_{\mathrm{LOAD}} = 60$ A using (a) PWM control and (b) VCM control, zoomed in to the (c) step-up and (d) step-down transient timestamp when using the proposed control.

reduction of approximately 28 dB in the $\hat{v}_{\mathrm{IN}}$-to-$\hat{v}_{\mathrm{C3}}$ path and 24 dB in the $\hat{v}_{\mathrm{IN}}$-to-$\hat{i}_{\mathrm{L4}}$ path relative to the PWM-based design. Automotive applications present additional challenges due to the wide operating range, including significant input voltage variation and large load-current swings. As shown in Fig. 13, the proposed approach achieves substantial and consistent suppression of interphase oscillations across the full range. These

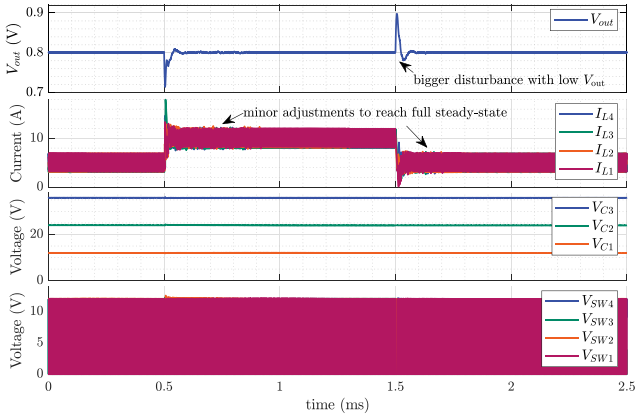

Fig. 15. Simulated response of a load-step from 20 to 40 A at 1 A/ns using VCM control with V_C-tracking.

results demonstrate that the proposed controller not only maintains robust stability across a wide operating range, but also delivers superior interphase dynamic performance and effective resonance suppression.

IV. Transient Simulation Results

Fig. 14 shows the dynamic response of a 4:1 SCB converter at $I_{\mathrm{LOAD}} = 60$ A. The converter is subjected to input voltage steps between 48 and 60 V with a slew rate of 1 V/μs. The input-bus parasitic elements, L_{line} and R_{line}, listed in Table I, are estimated based on a 1-m, 1-AWG wire (approximately 7.35 mm in diameter).

Significant LC oscillations are observed under conventional PWM-based control, as shown in Fig. 14(a). In comparison, with a current-reference saturation of 32 A, $I_{\mathrm{L,peak}}$ is reduced by over 10 A during transients when using the proposed VCM control, which incorporates both LC-interphase oscillation suppression and slope compensation, as shown in Fig. 14(b). As indicated in (8), the current adjustment terms I_{cj} from the oscillation suppressor cancel at the output. Minor deviations in V_{out} are attributed to the slope compensation, which introduces small deviations in the averaged inductor currents during transients due to shifts in switching instances. The inductor current settling time improves from 2 ms to 500 μs, accompanied by a significantly smaller output voltage disturbance. During the line transient, voltage stress on all low-side devices except M_4 remains within their maximum steady-state V_{DS} ratings.

To demonstrate full system stability, a 20-A load step from $I_{\mathrm{OUT}} = 20$ A is applied to the SCB converter operating under the proposed control scheme, with the simulated response shown in Fig. 15. The results confirm stable load regulation; however, a relatively large output voltage deviation is observed. The critical output specification for an automotive PMU is $\pm 5\%$ of the nominal output voltage during a 50% load step [2]. Output voltage regulation is primarily limited by the converter's switching frequency and the linear nature of the controller. To minimize voltage deviation during large load transients without significantly increasing the output filter volume, a high-frequency auxiliary converter, as proposed in [17], can

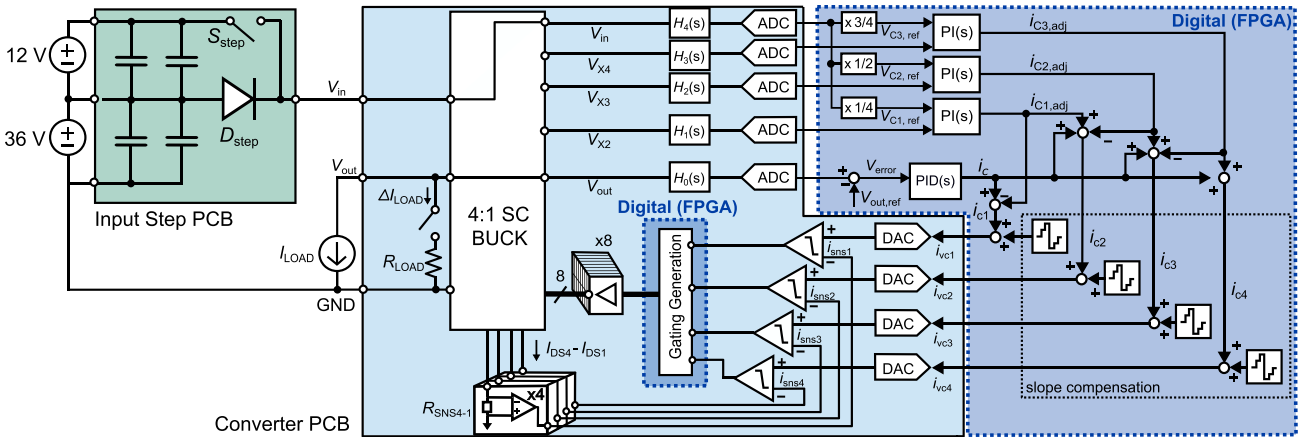

Fig. 16. System hardware implementation.

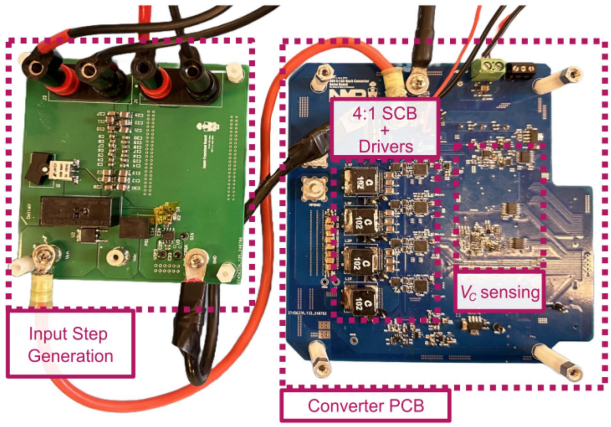

Fig. 17. DC–DC converter experimental prototype.

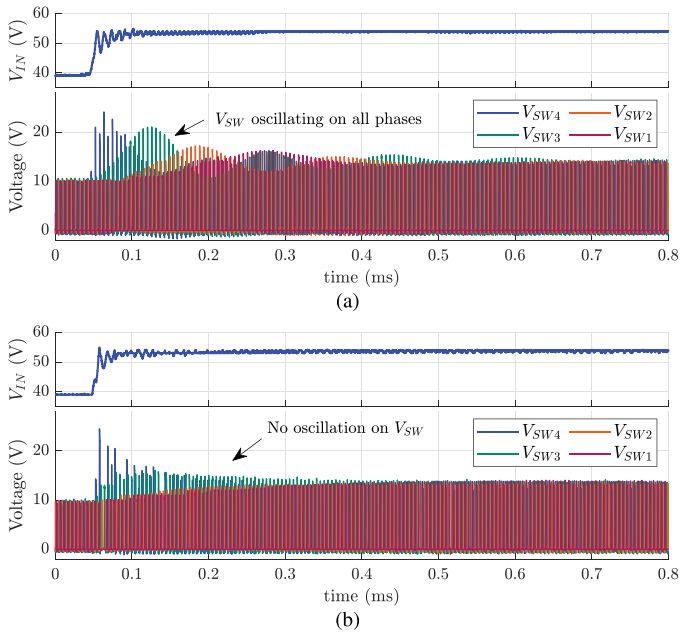

Fig. 18. Measured V_{SW} of the 4:1 SCB converter subjected to an input voltage step up from 40 to 54 V in 10 μs at $I_{LOAD} = 20$ A using (a) PWM control and (b) VCM control with oscillation suppression.

complement the primary control scheme. A 48 V-to-1 V system can achieve as up to 6.75× reduction in output capacitance using a low-voltage, high-frequency auxiliary converter. While adding such a parallel auxiliary converter enables compliance with stringent automotive PMU requirements without sacrificing efficiency and improves the capacitance-per-ampere metric, the implementation lies beyond the scope of this work, which focuses on input-transient LC-oscillation suppression rather than output-transient optimization.

V. Experimental Results

The 4:1 SCB converter in Fig. 16 was implemented using 60-V, 5-mΩ IAUZ40N06S5 and 40-V, 0.55-mΩ IAUC120N04S6 devices for switches M_{5-8} and M_{1-4}, respectively, as shown in Fig. 17. An input-step PCB was developed to achieve a high input-voltage slew rate, which is not attainable with standard bench-top supplies. Similarly, a 50-mΩ R_{LOAD} was added into the converter PCB to realize a high load-step slew rate. A VCM-based control with V_C tracking was implemented using an FPGA-based digital controller. 2-mΩ current-sense resistors were connected to the sources of M_{1-4} and placed on the reverse side of the converter PCB. The front side contains the power stage with passive component values matching those in Table I, except for an increased $C_{out} = 1.2$ mF to reduce output voltage deviation during load steps and bring the response closer to typical automotive PMU requirements. The inductor current was not measured to avoid noise injection into the sensing circuits; instead, capacitor or switch-node voltages were monitored to detect potential interphase oscillations.

A comparison of the interphase response of the converter using PWM-based and VCM-based control to an input step between 40 and 54 V, with a step-up slew rate of 1.2 V/μs at $I_{out} = 20$ A, is shown in Fig. 18. The plotted switch-node voltage measurements were processed using a 2-ns moving-average filter to suppress hard-switching ringing and enhance the visibility of interphase oscillations. Comparing V_{SW} in Fig. 18(a)

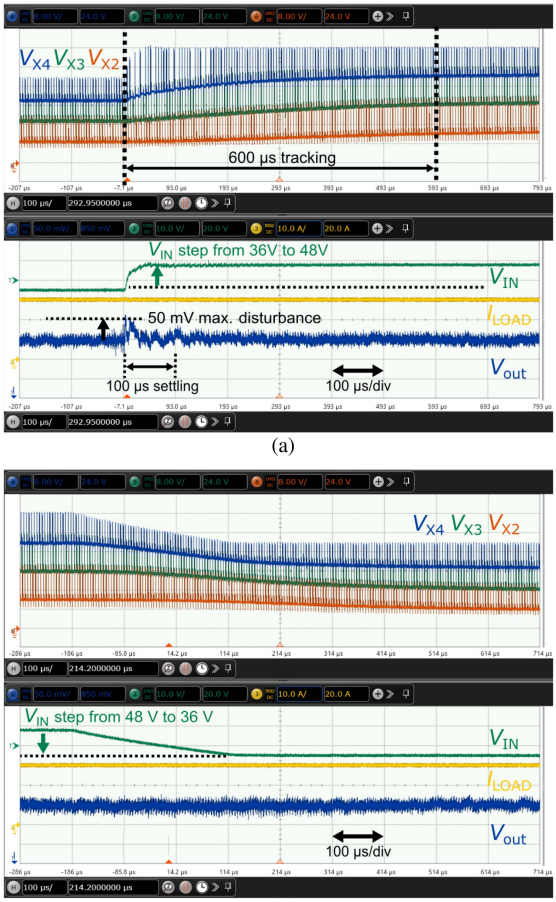

Fig. 19. Experimentally measured converter dynamics using the proposed controller subjected to an input-voltage step at $I_{\mathrm{LOAD}} = 30\,\mathrm{A}$ (a) from 36 to 48 V at $1\,\mathrm{V}/\mu\mathrm{s}$, (b) from 48 to 36 V at a slower rate.

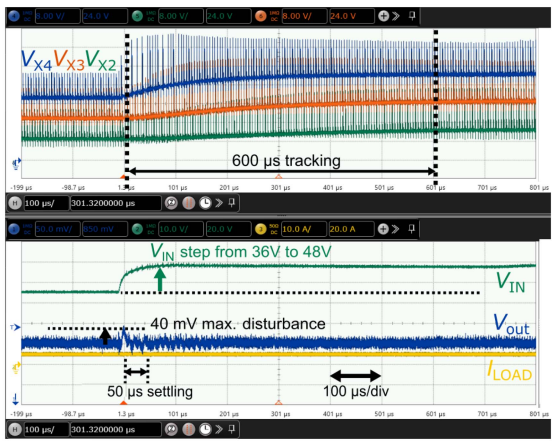

Fig. 20. Experimentally measured converter dynamics with the proposed control subjected to a V_{IN} step at $I_{\mathrm{LOAD}} = 5\,\mathrm{A}$ from 36 to 48 V at $1\,\mathrm{V}/\mu\mathrm{s}$.

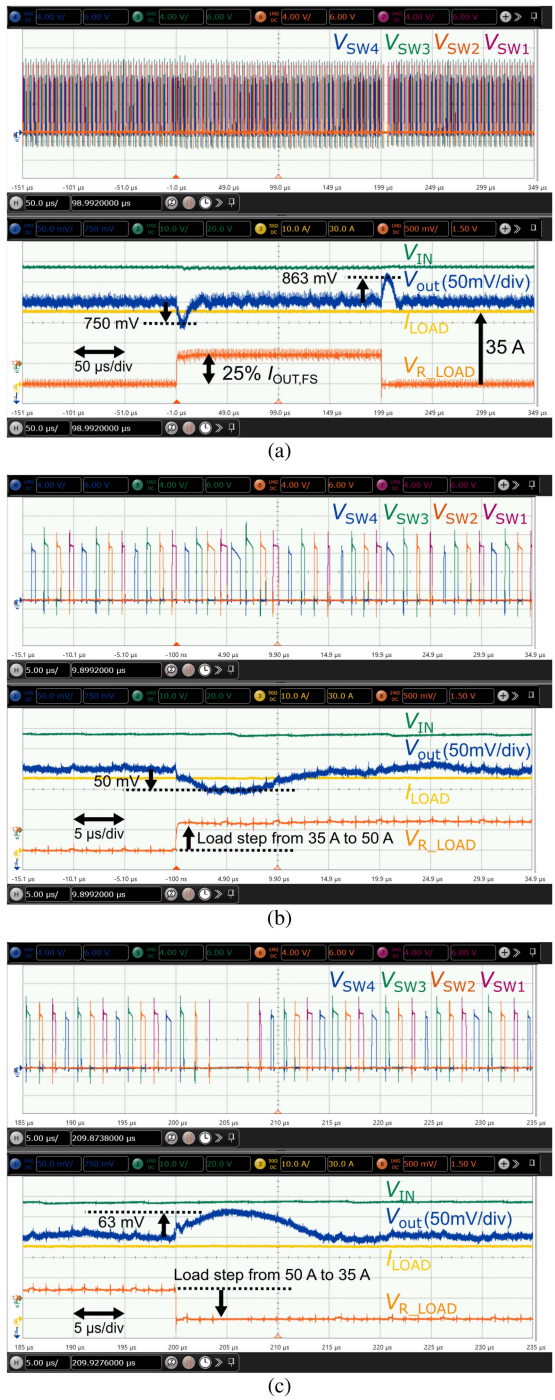

Fig. 21. (a) Experimentally measured converter dynamics using the proposed controller subjected to a 25% load step with $V_{\mathrm{IN}} = 48\,\mathrm{V}$ input (b) from 35 to 50 A at $100\,\mathrm{A}/\mu\mathrm{s}$ and (c) from 50 to 35 A at $500\,\mathrm{A}/\mu\mathrm{s}$.

and (b), the VCM controller effectively reduces interphase LC oscillations and lowers voltage stress on switches M_{1-3}.

The input step response of the converter, stepped from 36 to 48 V at $1\,\mathrm{V}/\mu\mathrm{s}$ and back, is shown in Fig. 19. As indicated in Fig. 2(b), the valley of V_{X2-4} reflects the voltage behavior of C_{1-3}. The flying-capacitor voltages are regulated to their dynamically generated references without any oscillatory behavior within 600 μs, similar to the simulated response. The maximum output voltage deviation was 50 mV, settling within 100 μs—a significant improvement over the PWM-based converter input transient response reported in [1]. As a fast input-capacitor discharge mechanism was not implemented, the input voltage

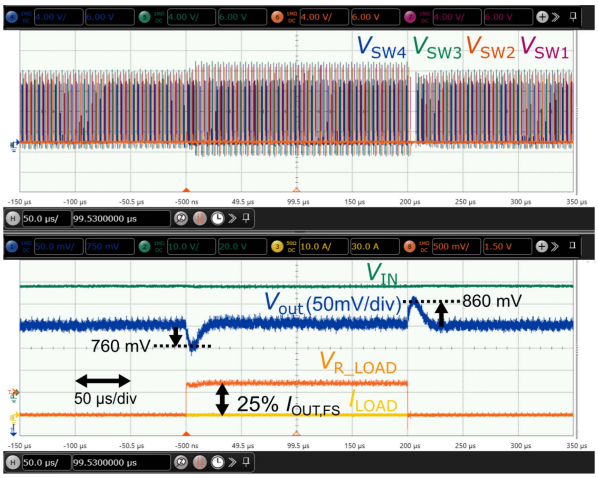

Fig. 22. Experimentally measured converter dynamics using the proposed controller subjected to a 25% load step with $V_{\mathrm{IN}} = 48\,\mathrm{V}$ input from 0 to 15 A at $100\,\mathrm{A}/\mu\mathrm{s}$.

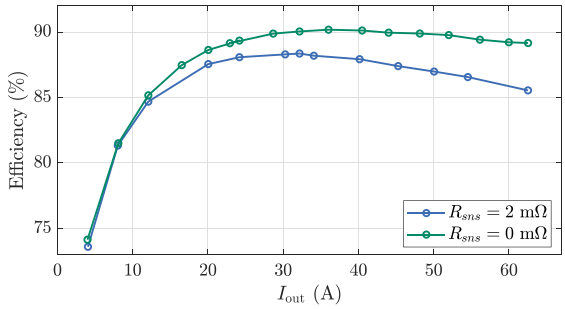

Fig. 23. Measured power-stage efficiency.

slew rate of $40\,\mathrm{V}/\mathrm{ms}$ was dependent on the load of the converter. In this case, the flying-capacitor voltage decreased in a controlled manner, closely following the input step down without disturbance on V_{out}, as shown in Fig. 19(b). Fig. 20 demonstrates light-load input-step stability, with the output voltage settling time reduced to $50\,\mu\mathrm{s}$ and a maximum output-voltage deviation of $40\,\mathrm{mV}$.

The load-step stability of the converter was validated using a fast 25% full-load ($I_{\mathrm{OUT,FS}}$) step from 35 A, with a slew rate of approximately $100\,\mathrm{A}/\mu\mathrm{s}$, based on the slope of $V_{\mathrm{R\_LOAD}}$, as shown in Fig. 21. The sum of I_{LOAD} and $V_{\mathrm{R\_LOAD}}/R_{\mathrm{LOAD}}$ represents the total output current of the converter. The output voltage deviation remains within $50\,\mathrm{mV}$ during the load step-up, demonstrating effective regulation. The load step-down produces a larger voltage deviation, attributed to the low nominal steady-state duty cycle and the low inductor demagnetizing slew rate due to the low output voltage level. Nevertheless, converter stability is maintained, as shown in Fig. 21(c). Light-load stability is shown in Fig. 22, with fast 25% $I_{\mathrm{OUT,FS}}$ load steps from and to 0-A output current.

At the nominal conversion ratio of 48 V-to-0.8 V, the peak efficiency of 88.4% was measured at 32 A, with a rated-load efficiency of 85.6% at 62.5 A. The converter losses include the contribution from the 2-$\mathrm{m}\Omega$ current-sense resistors, R_{sns}, placed on each phase. The cumulative sensing loss from all phases is calculated as $P_{\mathrm{sense}} = R_{\mathrm{sns}} I_{\mathrm{out}}^2/4$, which becomes significant at $I_{\mathrm{out}} > 20\,\mathrm{A}$, as shown in Fig. 23.

To emulate lossless current sensing, the sense resistors were removed from the prototype power stage. This resulted in a measured peak efficiency of 90.2% and rated-load efficiency of 89.2%. In the intended automotive application of this scheme, such lossless current sensing could be implemented using integrated sense FETs [27], enabling an efficiency improvement without increasing system complexity. These results demonstrate that with appropriate current-sensing techniques, the converter can achieve efficiency levels on par with other high-performance 48-V converters [7], [12], [13].

The proposed control method introduces additional sensing elements in the experimental setup, resulting in area overhead, as shown in Fig. 17. However, compactness and efficiency are critical for reliable system-level integration, as reflected in ongoing design trends in automotive PMUs. To overcome the design volume penalty, current sensing, voltage sensing, and control circuitry can be integrated into a power management IC, as demonstrated in [28]. The IC in [28] was derived from a discrete two-stage power delivery prototype presented in [29] for automotive processors. Such integration eliminates the need for discrete sensing components, reduces parasitic effects, and improves overall power density.

VI. Conclusion

This article presented a novel CMC strategy incorporating dynamic flying-capacitor voltage regulation for N:1 SCB converters, aimed at improving the dynamic response in automotive 48-V applications. By dynamically regulating the flying-capacitor voltages, the control scheme mitigates interphase LC oscillations, which are distinctive of hybrid dc–dc converters in which the magnetizing voltages across the phase inductors may vary significantly during input transients. Building on current-mode control, the current command of each inductor is adjusted using the voltage regulation of two neighboring flying capacitors. The proposed method was validated using a 62.5-A prototype. Stability analysis confirmed robust performance in accordance with stringent automotive reliability requirements. Experimental results demonstrated effective suppression of interphase oscillations during input transients and stable regulation during load transients. Compared to a conventionally adopted PWM-based controller, the proposed scheme reduced inductor current settling time from approximately $2\,\mathrm{ms}$ to $600\,\mu\mathrm{s}$, while maintaining output voltage deviations within $50\,\mathrm{mV}$ under severe line disturbances. This facilitates reductions in input capacitance and inductor saturation current requirements, thereby enhancing power density and transient performance in automotive power management applications.

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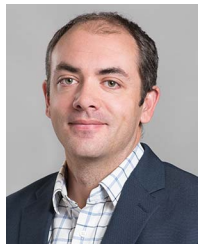

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