A Simplified Cost-Effective DuC-UPQC With Multiobjective Optimization Design

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***Abstract*—A simplified cost-effective dual-capacitor unified power quality conditioner (DuC-UPQC) is proposed. It could maintain sinusoidal standard load voltage and in-phase grid current, obtain reduced dc-link voltage, improve modulation indexes, achieve active power balance between inside dynamic voltage restorers and active power filters. Compared to existing methods, DuC-UPQC is cost-effective as less bipolar capacitors are required and external bidirectional dc power source could be removed. Besides, it exhibits robustness against grid voltage harmonics pollution and enables independent control for internal submodules. Next, two-dimensional multiobjective optimization strategy is developed through load voltage phase angle adjustment, so that multiple control objectives could be managed in buffer-capacitor-based topologies. Subsequently, phasor analysis is employed to derive the constraints and analytical solutions. Then associated control strategy can be designed. Finally, theoretical analysis was validated through simulation and laboratory experiments, with detailed results presented and discussed.**

***Index Terms*—Cost-effective, dual-capacitor unified power quality conditioner (DuC-UPQC), multiple objectives, power balance, reduced dc-link voltage, superior modulation indexes.**

I. INTRODUCTION

WITH the rapid proliferation of distributed generation (e.g., rooftop solar PV) and nonlinear loads (e.g., LED lighting, household electronics, and EV chargers), modern power distribution networks face escalating power quality (PQ) challenges [1]. Voltage-related PQ issues (e.g., grid sags/swells and distortions) could disrupt sensitive equipment, degrade grid reliability, and incur significant economic losses for industries [2], [3]. Current-related PQ issues (e.g., nonunity power factors, current distortions) induce reactive power circulation, increase transmission losses, and intensify the distortion of grid voltage [4], [5].

Traditional dynamic voltage restorers (DVRs) and active power filters (APFs) have established their efficacy in voltage-related and current-related mitigation scenarios, respectively. While in industrial applications, PQ disturbances often occur simultaneously while standalone DVRs or APFs cannot provide comprehensive compensation. Emerging as a new alternative, unified power quality conditioners (UPQCs) adopted in [6], [7], [8], and [9] integrates DVRs and APFs to address both voltage and current-related PQ issues, which results in compact design and high comprehensive performance. However, these methods requires external bidirectional dc power supply (ExBD-PS) providing active power, which leads to high cost. To address this limitation, improved methods in [10] and [11] design power balance strategy so that the internal DVR could obtain the required active power from the APF, thereby eliminating ExBD-PS and featuring plug-and-play capability.

However, the inherent differences between APFs and DVRs introduce critical challenges in global optimization. As per IEEE 1453-2022 guidelines, standard grid voltage variations are generally maintained below 10% of the nominal voltage level [12]. Generally, the internal APF interfaces with the ac power source while the DVR addresses grid fluctuations. Due to common dc bus, the entire UPQC design must meet the requirements of the APF [13]. As a result, the DVR suffers from unfitted high dc-link voltage, leading to severe issues: 1) excessive voltage stress on devices; 2) higher switching losses; 3) amplified harmonics pollution; and 4) severe electromagnetic interference.

On the other hand, owing to excessive dc-link voltage, DVR operates at low modulation indexes. The achievable PWM pulse width approaches the minimum controllable duration, which is limited by gate driver dead time and DSP resolution. This truncates fine voltage adjustments, quantizes the output into larger discrete steps and reduces control precision. While narrow pulses caused by low modulation indexes amplify the relative impact of switching transients (e.g., rise/fall times and dead time) and timing errors, causing nonlinear distortions that override intended control signals.

To address the aforementioned dual challenges, the schemes based on line-frequency transformers (LFTs) is proposed in [14], [15], and [16]. By configuring the turns ratio of LFT, the ac voltage regulated by DVR could be amplified to approach the ac source voltage interfacing with APF, achieving optimized

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TABLE I
COMPARISON OF FOUR MAJOR CATEGORIES IN UPQCS

	ExBD-PS based UPQCs	LFT-based UPQCs	HFT-based UPQCs	Non-Isolated UPQCs
References	[6], [7], etc.	[14], [15], etc.	[19], [20] etc.	[24], [25]
Power rating	Medium	High	Medium	Low
Complexity	Medium	Low	High	Medium
Reliability	Medium	High	Low	Medium
Volume	High	High	Medium	Low
Weight	High	High	Medium	Low
Cost	High	High	Medium	Low

TABLE II
THREE EXISTING NONISOLATED TWO-LEG UPQCS

	GHLF UPQC	GFLH UPQC	DT-UPQC
References	[26], [27] etc.	[30]	[31]
Grid-side converter	Half bridge	Full bridge	Full bridge
load-side converter	Full bridge	Half bridge	Full bridge
Dc-link voltage during swell	Highest	High	High
Shared Bridge arms	Two split capacitors	Two split capacitors	Two switches
Hardware Decoupling	No	No	Yes

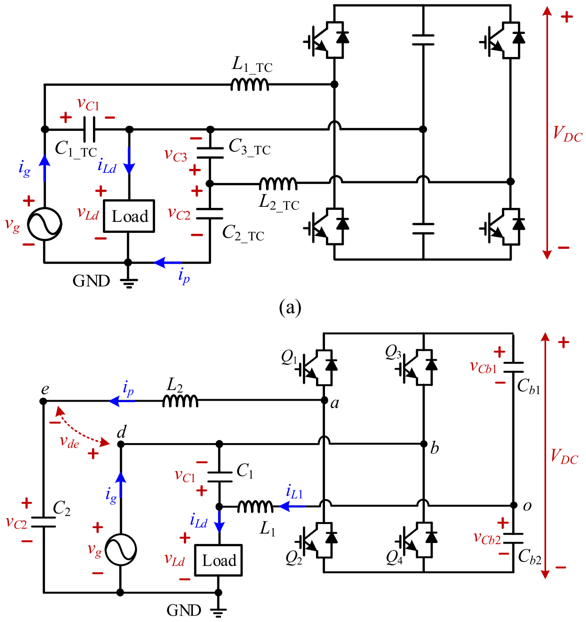
modulation indexes despite maintaining an elevated dc-link voltage. Thus, improved scheme is proposed in [17] and [18]. By placing another LFT in APF, the dual challenges are addressed simultaneously. The limitation is that LFTs suffer from large volume, excessive weight and high manufacturing costs due to their inherent low-frequency operation principles.

As an alternative to LFT, high-frequency transformer (HFT) is employed in [19] and [20]. Through two fitted dc-link voltages and dual active bridges, both the DVR and APF could obtain optimal modulation indexes. The drawback is that the APF and its adjacent devices still bear high voltage stress. On this basis, multilevel converter schemes is applied [21], [22], [23], which could reduce switching harmonics and losses. Nonetheless, these schemes requires a large number of semiconductors, which increases cost and complexity, degrades efficiency, and reduces overall reliability.

Cost efficiency represents another pivotal design criterion for UPQCs. Schemes employing ExBD-PS, LFTs, and HFTs face significant economic challenges. Taking this into account, cost savings could be achieved through active capacitors. Therefore, a single-phase nonisolated UPQC is presented in [24], which contains two H-bridge converters. Besides, an improved three-leg UPQC is developed in [25]. Applying shared bridge arms, less semiconductors are demanded. The comparison of four major categories are depicted in Table I. Apparently, in low-power applications, nonisolated UPQCs offer benefits in terms of volume, weight, and cost. Consequently, subsequent research will focus on nonisolated UPQCs.

To further save cost, nonisolated two-leg UPQCs emerge as a considerable research interest. With split-capacitors replacing shared legs, the number of semiconductor devices is reduced and leakage current is suppressed. There are three typical nonisolated topologies, e.g., GHLF UPQC [26], [27], [28], [29], GFLH UPQC [30], and decoupled two-leg (DT-) UPQC [31]. Comparison of these schemes are shown in Table II. As DT-UPQC exhibits optimal performance due to its decoupling ability and dual full bridge structure, it will be the representative of two-leg UPQCs in the following analysis.

Based on buffer capacitor enduring redundant voltage, three-capacitor UPQC (TC-UPQC) is proposed in [32], as showed in Fig. 1(a). With buffer capacitor bearing the excessive voltage, the controllable active capacitor magnitude in APF is decreased so that reduced dc-link voltage is obtained. In addition, two added bipolar capacitors elevate the filter in APF to a second-order *LC* type, which is beneficial for suppressing switching harmonics. However, the differential operator induced by buffer capacitor will distort grid current due to the harmonic components in grid voltage.



(a)

(b)

Fig. 1. Buffer-capacitor-based UPQC. (a) Existing TC-UPQC. (b) Proposed DuC-UPQC.

DT-UPQC is a cost-effective option, which avoids expensive devices (e.g., ExBD-PS, LFTs) but suffers from unfitted dc-link voltage. TC-UPQC exhibits low dc-link voltage while shows low immunity to harmonics. Integrating the schemes above, a simplified DuC-UPQC is proposed, as showed in Fig. 1(b), which retains their merits and corrects defects. Table III provides a comparison among three-leg, DT-, TC-, and DuC-UPQC. Green background areas mean the advantages in DuC-UPQC, e.g., reduced dc-link voltage, improved modulation indexes, second-order *LC* filter, low voltage stress, power loss, decoupling ability, and harmonics immunity.

As for control strategies in UPQCs based on buffer capacitor, there are limited in-depth researches, owing to the complexities

TABLE III
COMPARISON OF NONISOLATED UPQCS

	Three-leg UPQC	DT-UPQC	TC-UPQC	DuC-UPQC
References	[25]	[31]	[32]	Proposed
The Number of bipolar capacitor	1	1	3	2
The Number of switches	6	4	4	4
Power rating	High	Medium	Low	Low
Controller complexity	Low	Low	High	Medium
Cost	High	Low	High	Medium
Reliability	High	Medium	Low	Medium
Operating range	Wide	Wide	Narrow	Medium
Dc-link voltage	High	High	Low	Low
Modulation indexes differences	Large	Large	Small	Small
APF Filter	First-order	First-order	Second-order	Second-order
Voltage stress	High	High	Low	Low
Switching Losses	High	High	Low	Low
Hardware Decoupling	Yes	Yes	No	Yes
Harmonics immunity	High	High	Low	High

Note: Green background means the advantages while grey background means the disadvantages.

of managing multiple control objectives. In general, UPQC need to mitigate the disturbances caused by both grid voltage and load current, and ensure active power balance between its DVR and APF units. The insertion of buffer capacitor further complicates the constraint equations. In [32], multiobjective optimization algorithm is applied in *dq*-frame, which imposes significant computational burden on the controller. Moreover, this algorithm mandates that load voltage and grid voltage remain in phase. Thus, its multiobjective optimization is one-dimensional (1-D), which restricts the operating range.

This article investigates deeper study for the control strategy in buffer-capacitor-integrated UPQCs. Phase angle adjustment is introduced to the load voltage, which elevates multiobjective constraints to 2-D. Next, multiple solutions could be obtained via fundamental phasor analysis, which enables the pursuit of optimal solution.

In brief, the main contributions of this research encompass as follows.

1) A simplified cost-effective buffer-capacitor-based DuC-UPQC is proposed. It only requires two bipolar capacitors and one H-bridge, which reduces hardware complexity.
2) DuC-UPQC integrates multiple merits, e.g., reduced dc-link voltage, improved modulation indexes, second-order *LC* filter in APF, low voltage stress, low power loss, decoupling ability, and harmonics immunity.
3) The 2-D multiobjective optimization analysis is carried out by introducing load voltage phase angle adjustment. Thus, DuC-UPQC achieves multiple objectives concurrently, including ensuring standard sinusoidal load voltage, in-phase sinusoidal grid current, DVR/APF power balance, reduced dc-link voltage, and superior modulation indexes.
4) Applying fundamental phasor analysis, the constraints and analytical solutions for achieving these objectives is deduced. Following this, the corresponding control strategy is designed.

II. TOPOLOGY AND OPERATING PRINCIPLE

The proposed DuC-UPQC, as shown in Fig. 1(b), mainly consists of DVR and APF. The dc–ac conversion is composed by three legs, i.e., dc-link split capacitors (C_{b1} and C_{b2}), bridge arm I (switches Q_1 and Q_2), bridge arm II (Q_3 and Q_4).The DVR is made up by bridge arm II, dc-link split capacitors, filter inductor L_1 and active capacitor C_1. Whereas APF is composed of bridge arm I and II, filter inductor L_2 and buffer capacitor C_2. Node *e* is the midpoint of L_2 and C_2. Let v_g, i_g, v_{Ld}, i_{Ld}, v_{C1}, i_p, v_{C2}, and V_{dc} denote grid voltage, grid current, load voltage, load current, active capacitor voltage, compensation current, buffer capacitor voltage, and dc-link voltage, respectively. Whereas v_{de} denotes the voltage across nodes *d* and *e*, which is named node voltage.

A. Multiple Control Objectives for DuC-UPQC

For conciseness, the fundamental and harmonic components of one signal is denoted as subscripts "*_f*" and "*_h*" in text narrative. In addition, lowercase the first letter to represent ac signal in time-domain while capitalize the first letter to denote the magnitude of fundamental component.

Grid voltage v_g is set as phase reference, which is denoted as

$$v_g(t) = V_g \sin \omega t + \sum_{n=3,5,\ldots} V_{gn} \sin(n\omega t - \psi_n) \tag{1}$$

where V_g and ω are the magnitude and angular frequency of v_{g_f}.

Integer *n* represents harmonic order. And V_{gn}, $n\omega$, and ψ_n are magnitude, angular frequency, and phase of odd harmonics v_{g_h}, respectively.

Applying a pure sinusoidal voltage excitation signal to linear and nonlinear loads, the response load current i_{Ld} is written as

$$i_{Ld}(t) = I_{Ld} \sin(\omega t - \varphi) + \sum_{n=3,5,\ldots} I_{Ldn} \sin(n\omega t - \varphi_n) \tag{2}$$

where φ is the phase of i_{Ld_f}. Symbols I_{Ldn}, $n\omega$, and φ_n are the magnitude, angular frequency, and phase of harmonics i_{Ld_h}, respectively. Phase φ is mainly caused by linear loads while harmonics i_{Ld_h} are produced by nonlinear loads.

Load voltage v_{Ld} and grid current i_g could be expressed as

$$\begin{cases} v_{Ld}(t) = V_{Ld} \cdot \sin(\omega t - \delta) + v_{Ld\_h} \\ i_g(t) = I_g \cdot \sin(\omega t - \varphi_g) + i_{g\_h} \end{cases} \tag{3}$$

where δ and φ_g are the lagging phase of v_{Ld_f} and i_{g_f}.

Active capacitor voltage v_{C1} and current i_p are defined as

$$\begin{cases} v_{C1}(t) = V_{C1} \sin(\omega t + \alpha) + v_{C1\_h} \\ i_p(t) = I_p \sin(\omega t + \beta) + i_{p\_h} \end{cases} \tag{4}$$

where α and β are the phase of v_{C1_f} and i_{p_f}.

There are four control objectives for DuC-UPQC.

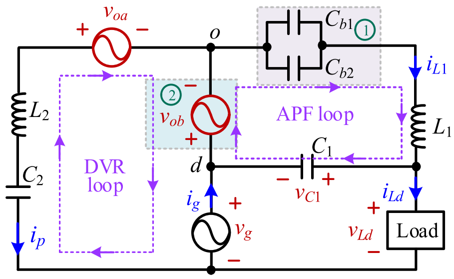


Fig. 2. AC equivalent circuit of DuC-UPQC.

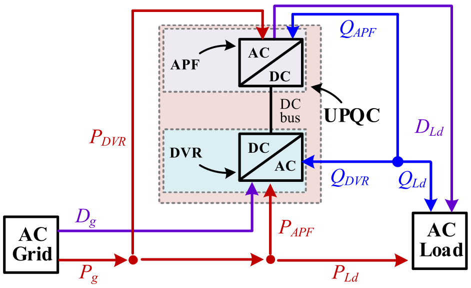


Fig. 3. Power flow in DuC-UPQC.

Objective 1: Load voltage v_{Ld} keeps sinusoidal with constant standard magnitude V_{Ld}^*, i.e., $V_{Ld} = V_{Ld}^*$ and $v_{Ld\_h} = 0$. Applying Kirchhoff voltage law, the appropriate v_{C1_f} and v_{C1_h} can be calculated as

$$\begin{cases} v_{C1\_f} = V_g \sin \omega t - V_{Ld}^* \sin(\omega t - \delta) \\ v_{C1\_h} = v_{g\_h}. \end{cases} \tag{5}$$

The injected v_{C1_f} could maintain the magnitude of load voltage at constant value V_{Ld}^* during grid fluctuation. While the harmonic component v_{C1_h} is the undesired grid harmonics v_{g_h}, ensuring sinusoidal load voltage v_{Ld}.

Objective 2: Grid current i_g is shaped sinusoidal with zero phase shift relative to grid voltage v_g, i.e., $\varphi_g = 0$ and $i_{g\_h} = 0$. Applying Kirchhoff current law, the fitted i_{p_f} and i_{p_h} can be computed as

$$\begin{cases} i_{p\_f} = I_g \sin \omega t - I_{Ld} \sin(\omega t - \varphi) \\ i_{p\_h} = -i_{Ld\_h}. \end{cases} \tag{6}$$

With i_{p_f} injected into inductance L_2, the phase difference between grid voltage and grid current could be eliminated. For sinusoidal grid current, the injected i_{p_h} need offset the annoying harmonics i_{Ld_h}.

Objective 3: Achieve active power balance between DVR and APF so that ExDB-PS could be removed. With active power injecting into DVR, the regulation range for voltage compensating can be expanded.

Objective 4: Reduce dc-link voltage and obtain superior modulation indexes. With buffer capacitor bearing excessive grid voltage, the magnitude of ac voltage v_{de} decreases and the magnitude difference between v_{de} and v_{C1} is narrowed.

The DVR accomplishes *Objective 1*, whereas the APF fulfills the remaining three objectives.

B. Hardware Decoupling Analysis

Generally, nonisolated two-leg UPQCs (e.g., [26], [31]) are classified as multiple-input multiple-output (MIMO) system due to multiple control objectives and shared state variables. While in DuC-UPQC, MIMO system can be decoupled into multiple single-input single-output systems by altering the position of state variables. Fig. 2 shows the ac equivalent circuit of DuC-UPQC. Bridge arm output voltage v_{ob} locates at the shared loop of DVR and APF, replacing the state variables (i.e., $C_{b1}//C_{b2}$). Since the mutual interference caused by state variables is removed, the modeling could be simplified and software decoupling strategy is unnecessary.

TABLE IV
COMPARISON OF DT-UPQC AND DUC-UPQC

DT-UPQC	$V_{DC} > 2\max\left\{V_{C1}, V_g, \max\left[v_g(t) - v_{C1}(t)\right]\right\}$	(7)
	$m_1 = \dfrac{V_{C1}}{V_{DC}} << \dfrac{V_g}{V_{DC}} = m_2 < 1$	(8)
DuC-UPQC	$V_{DC} > 2\max\left\{V_{C1}, V_{de}, \max\left[v_{de}(t) - v_{C1}(t)\right]\right\}$	(9)
	$m_1 = \dfrac{V_{C1}}{V_{DC}} \approx \dfrac{V_{de}}{V_{DC}} = m_2 < 1$	(10)

C. Power Flow Analysis

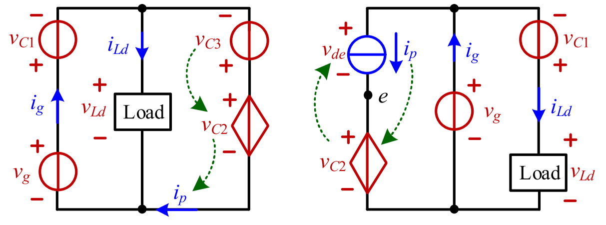
The power flow in DuC-UPQC is depicted in Fig. 3. Let P_g, Q_g, and D_g denote the generated active power, reactive power, and distortion power in power grid, respectively, with P_{Ld}, Q_{Ld}, D_{Ld} being the mapped power absorbed by residential loads. Define P_{DVR} and P_{APF} as the absorbed active power in DVR and APF, with Q_{DVR} and Q_{APF} being the mapped absorbed reactive power. Let P_{loss} denote converter losses.

Since grid voltage v_g and grid current i_g are required to be in phase, grid reactive power should be eliminated, i.e., $Q_g = 0$. Thus, reactive power exchanges between DVR, APF, and load, which satisfies $Q_{\text{APF}} + Q_{\text{DVR}} + Q_{Ld} = 0$.

Distortion power D_g results from grid voltage harmonics and D_{Ld} is produced by load current harmonics. To prevent their cross-coupling, D_g is absorbed by DVR while D_{Ld} is supplied by APF. Based on active power flow, there are following formulas, $P_{\text{DVR}} + P_{\text{APF}} = P_{\text{loss}}$, and $P_g = P_{Ld} + P_{\text{loss}}$.

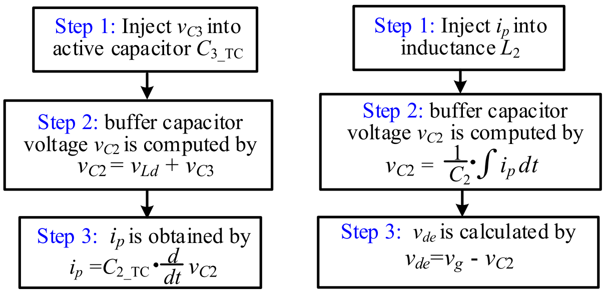
D. Comparison With DT-UPQC

Due to the boost effect in nonisolated active PWM dc–ac conversion and shared dc bus, dc-link voltage should exceed the maximum peak value of interacted ac voltages (e.g., v_g, v_{C1}, v_{de}) to obtain controllable inductor current. Define m_1 and m_2 as the modulation indexes for DVR and APF. Table IV shows the characteristics of dc-link voltage and modulation indexes in DT-UPQC and DuC-UPQC.



(a) (b)

Fig. 4. Buffer capacitor characteristics. (a) TC-UPQC. (b) DuC-UPQC.



(a) (b)

Fig. 5. Flowcharts. (a) TC-UPQC. (b) DuC -UPQC.

In DT-UPQC, high dc-link voltage is caused by grid voltage v_g, which depends on external circumstances. Since magnitude V_{C1} is much smaller than V_g, DVR operates with annoying low modulation degree, leading to higher proportion of switching harmonics and unnecessary switching losses. Besides, valid modulation range (i.e., $0.1 < m < 0.9$) ensures stable PWM resolution, while excessively low modulation indexes ($m < 0.1$) degrades precision.

In DuC-UPQC, these deficiencies above can be overcome by applying buffer capacitor. Decompose grid voltage v_g into node voltage v_{de} and buffer capacitor voltage v_{C2}. Then, controllable v_{de} and v_{C1} emerge as the interacted ac voltages. Thus, dc-link voltage can be reduced by setting suitable ac magnitude V_{de} and V_{C1}. In addition, the magnitude gap between V_{de} and V_{C1} can be narrowed so that modulation indexes can be improved.

E. Comparison With TC-UPQC

Utilizing buffer capacitor, TC-UPQC can also achieve both dc-link voltage reduction and modulation indexes refinement. The drawback is that its buffer capacitor introduces derivative element, resulting in undesirable grid harmonic currents. This deficiency is resolved by the proposed DuC-UPQC.

The buffer capacitor characteristics of TC-UPQC and DuC-UPQC are depicted in Fig. 4, with their flowcharts presented in Fig. 5. The APF is required to generate fitted compensating current i_p and magnitude-controlled ac voltage (i.e., v_{C3} in TC-UPQC and v_{de} in DuC-UPQC).

In TC-UPQC, the conversion chain occurs as: $v_{C3} \rightarrow v_{C2} \rightarrow i_p$. Since i_p is the response of buffer capacitor voltage v_{C2}, the derivative operation magnifies voltage harmonics, leading to grid current pollution.

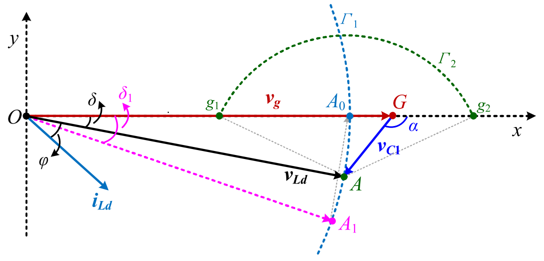


Fig. 6 Phasor diagram for the DVR.

While in DuC-UPQC, the signal flows through successive transformations: $i_p \rightarrow v_{C2} \rightarrow v_{de}$. Since compensating current i_p is initially generated, it avoids harmonic pollution caused by other conversion stages.

III. MULTIOBJECTIVE OPTIMIZATION DESIGN

To fulfill multiple control objectives, the analysis for 2-D multiobjective optimization is carried out here. As the THD of PCC voltage shall not exceed 8% [33], the primary influence is exerted by fundamental components. Harmonics could be neglected here to streamline subsequent analysis and derivations. For brief expression, the fundamental sinusoid is converted from time domain to phasor domain. Phasors are denoted as boldface quantities, e.g., $\boldsymbol{v_g}$ denotes $v_{g\cdot f}$. Define $V_C{}^*$ as the maximum magnitudes of both $\boldsymbol{v_{C1}}$ and $\boldsymbol{v_{de}}$. The constraints and solutions for DuC-UPQC achieving four objectives are detailed here.

A. Active Capacitor Voltage Regulation

Load voltage with stable standard magnitude $V_{Ld}{}^*$ could be obtained by regulating phasor $\boldsymbol{v_{C1}}$, as shown in Fig. 6. Construct rectangular coordinate system and set phasor $\boldsymbol{v_g}$ as referenced phasor with target point G, which is oriented along x-axis. Arc Γ_1 centered at origin O with radius $V_{Ld}{}^*$ is the collection for the common target points (e.g., A_0, A, and A_1) of phasors $\boldsymbol{v_{C1}}$ and $\boldsymbol{v_{Ld}}$. Point A_0 lies on x-axis as well. Each target point on arc Γ_1 maps to related phase angle δ.

Connect chord A_0A_1 with length V_C^*. The associated phase angle δ_1 could be computed as

$$\delta_1 = \arccos\left(1 - \frac{V_C^{*\,2}}{2V_{Ld}^{*\,2}}\right). \tag{11}$$

Owing to the maximum magnitude limits V_C^*, phase angle δ should satisfy the constraints $0 < |\delta| < \delta_1$ to ensure its operation during grid swell. Select any phase angle δ and mapped target point A from the constraints. Centered at point A, plot Γ_2 with radius V_C^*. Chord g_1g_2 is the intercepts of x-axis and arc Γ_2, which is partitioned into segments A_0g_1 for grid sag and A_0g_2 for grid sag. Generally, the fluctuating range for sag exceeds that for swell, with equality holding only at target point A_0.

Define λ as grid fluctuation ratio. Grid voltage magnitude V_g equals to $\lambda V_{Ld}{}^*$. Thus, $\lambda > 1$ denotes swell while $\lambda < 1$ for sag. Then V_{C1}, i.e., the magnitude of $\boldsymbol{v_{C1}}$, could be calculated as

$$V_{C1} = V_{Ld}^* \cdot \sqrt{1 + \lambda^2 - 2\lambda \cdot \cos\delta}. \tag{12}$$

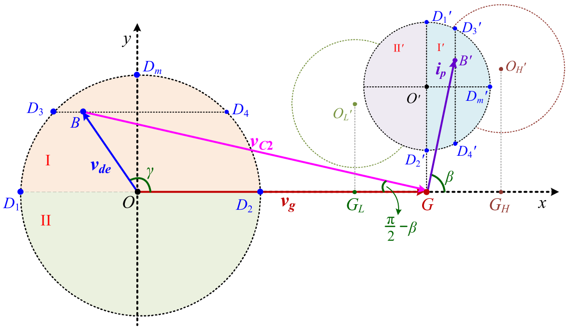


Fig. 7. Phasor diagram for buffer capacitor voltage regulation.

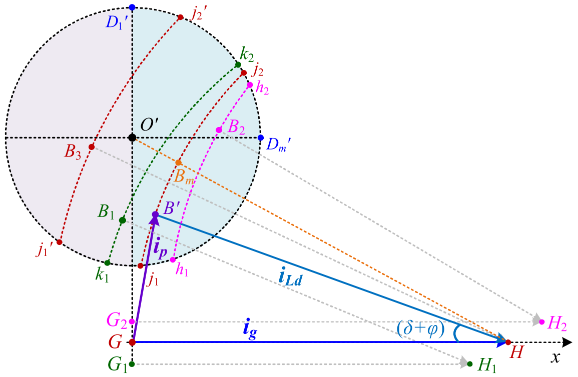


Fig. 8. Phasor diagram for compensating current regulation.

Thus, it can be concluded that V_{C1} increases with δ. The range of λ could be expressed as

$$\cos\delta - \sqrt{\frac{{V_C^*}^2}{{V_{Ld}^*}^2} - \sin^2\delta} < \lambda < \cos\delta + \sqrt{\frac{{V_C^*}^2}{{V_{Ld}^*}^2} - \sin^2\delta}. \tag{13}$$

Linear load is assumed to be connected, with load current $\boldsymbol{i}_{Ld}$ characterized by magnitude I_{Ld} and phase lag φ to load voltage $\boldsymbol{v}_{Ld}$. Then, the active power absorbed by DVR is computed as

$$P_{\mathrm{DVR}} = \frac{V_{Ld}^* I_{Ld}}{2} \cdot [\lambda\cos(\delta+\varphi) - \cos\varphi]. \tag{14}$$

B. Buffer Capacitor Voltage Regulation

The magnitude constraint for ac voltage $\boldsymbol{v}_{de}$ is achieved by regulating buffer capacitor voltage $\boldsymbol{v}_{C2}$, as depicted in Fig. 7. Let θ and γ denote the phase angles for $\boldsymbol{i}_p$ and $\boldsymbol{v}_{de}$.

Based on the characteristics of capacitor, the injected current $\boldsymbol{i}_p$ is perpendicular to buffer capacitor voltage $\boldsymbol{v}_{C2}$. Besides, the magnitudes of $\boldsymbol{i}_p$ and $\boldsymbol{v}_{C2}$ satisfy the following formula:

$$I_p = \omega C_2 \cdot V_{C2}. \tag{15}$$

The absorbed active power in APF could be depicted as

$$P_{\mathrm{APF}} = \frac{1}{2} \cdot \lambda V_{Ld}^* \cdot I_p \cdot \cos\beta. \tag{16}$$

Grid voltage $\boldsymbol{v}_g$ is decomposed into buffer capacitor voltage $\boldsymbol{v}_{C2}$ and ac voltage $\boldsymbol{v}_{de}$. Applying Law of Sines, V_{de} and V_{C2} satisfy the following formula:

$$\frac{V_{C2}}{\sin\gamma} = \frac{V_{de}}{\sin\left(\frac{\pi}{2}-\beta\right)}. \tag{17}$$

Thus, P_{APF} can be rewritten in another form

$$P_{\mathrm{APF}} = \frac{1}{2} \cdot \omega C_2 \cdot \lambda V_{Ld}^* \cdot V_{de} \cdot \sin\gamma. \tag{18}$$

Based on trigonometric principles, P_{APF} is proportional to the area of triangle *GOB* (i.e., $S_{\triangle GOB}$). Plot circle O centered at origin O with radius V_{C}^*. Thus, all target points for $\boldsymbol{v}_{de}$ should locate inside circle O to guarantee its magnitude below V_C^*. Let x-axis intersects circle O at points D_1 and D_2. Diameter D_1D_2 divide circle O into semicircle I where APF releases active power and semicircle II where APF absorbs. Draw chord D_3D_4 parallel to x-axis through vertex B. It could be deduced that the active power P_{APF} will not change no matter how point B moves along chord D_3D_4. Let y-axis intersects circle O at point D_m. At vertex D_m, the APF will obtain the maximum P_{APF}.

Since phasor $\boldsymbol{v}_{C2}$ is the response of the excitation $\boldsymbol{i}_p$, for any target point B inside circle O, there exists mapped target point B'. Let point G act as the point of reflection. In the realm of geometry, the collection of the mapped point B' forms another circle O' with radius $\omega C_2 V_{\mathrm{C}}^*$. Points D_1, D_2, D_3, D_4, D_m are mapped to points D_1', D_2', D_3', D_4', D_m'. Provided that the target point of $\boldsymbol{i}_p$ lies inside circle O', the magnitude of $\boldsymbol{v}_{de}$ will be limited below V_C^*, which is the key constrains for reducing dc-link voltage and improve modulation indexes.

Let point G coincide with A_0. Then, grid voltage with target point G carries standard magnitude V_{Ld}^*. The y-coordinate of center O' is $\omega C_2 \lambda V_{Ld}^*$. Circle O' retains constant radius while its center undergoes displacement confronting grid fluctuations. Under swell, its center shifts to point O_H'. Whereas for sag, it relocates to point O_L'.

C. Compensating Current Regulation

For the APF, there are three objectives, including regulating $V_{de} < V_C^*$, ensuring DVR/APF power balance and obtaining in-phase grid current. Given that the target point B' lies within circle O', *objective 4* will be achieved.

As for the power balance between the APF and DVR, it can be achieved by regulating the magnitude of grid current $\boldsymbol{i}_g$. Under steady operation, the grid-side input power P_g equals to the sum of the load-side power consumption P_{Ld} and converter losses P_{loss}. The required magnitude I_g can be computed as

$$I_g = \frac{2}{\lambda V_{Ld}^* \cos\varphi_g} \cdot \left(\frac{1}{2} V_{Ld}^* I_{Ld}\cos\varphi + P_{\mathrm{loss}}\right). \tag{19}$$

Provided grid current magnitude satisfies this formula, active power P_{DVR} could be offset by the P_{APF} by the law of energy conservation.

To achieve unity power factor, phasor $\boldsymbol{i}_g$ should align with x-axis, as depicted in Fig. 8. The phase angle of phasor $\boldsymbol{i}_{Ld}$ is ($\delta + \varphi$). Under standard grid voltage (i.e., $V_g = V_{Ld}^*$) and resistive load (i.e., $\varphi = 0$), the response grid current $\boldsymbol{i}_g$ emits from point G and terminates at point H with length I_g^* while load current $\boldsymbol{i}_{Ld}$ is in phase with load voltage $\boldsymbol{v}_{Ld}$. Neglecting the losses P_{loss}, load current $\boldsymbol{i_{Ld}}$ shares equal magnitude $I_g{}^*$ with $\boldsymbol{i_g}$ according to power balance. Centered at point H with radius $I_g{}^*$, plot arc j_1j_2, intersecting circle O' at point j_1 and j_2. While arc j_1j_2 is the collection of the desired point B' for achieving three objectives of the APF simultaneously.

To address the y-axis displacement of center O' caused by grid fluctuations, relocate the initial and terminal points of grid current $\boldsymbol{i_g}$. Points G, G_1, and G_2 lie on line $O'G$. The length of $O'G_1$ and $O'G_2$ equal to the y-coordinates of $O_H{}'$ and $O_L{}'$, respectively. During swell, points G_1 and H_1 are selected as the initial and terminals point of $\boldsymbol{i_g}$ with magnitude $I_g{}^*/\lambda$. Centered at point H_1, plot arc k_1k_2 with radius $I_g{}^*$, which is the desired trajectory. Similarly, arc h_1h_2 for sag could be derived.

Under standard grid voltage and linear load (i.e., $\varphi \neq 0$), the magnitude of load current $\boldsymbol{i_{Ld}}$ is computed as $I_g{}^*/\cos\varphi$ to obtain equivalent grid current magnitude $I_g{}^*$. Centered at point H, plot arc $j_1{}'j_2{}'$ with radius $I_g{}^*/\cos\varphi$. While arc $j_1{}'j_2{}'$ is the trajectory for linear load.

D. AC Voltage Magnitudes Optimization

Since multiple solutions exist achieving three objectives of the APF, the subsequent optimization is obtain the solution with minimum ac voltage magnitude. Draw a line passing through center O' and the target point (e.g., H, H_1, and H_2) of grid current $\boldsymbol{i_g}$ and let this line intersects the matched trajectory at point B_m, as shown in the example (point H and arc j_1j_2 of Fig. 8). Since segment $O'B_m$ is the minimum distance from center O' to the related trajectory, target point B_m for $\boldsymbol{i_p}$ will obtain the minimum magnitude V_{de}.

Corresponding to target point B_m, the phase angle of load voltage $\boldsymbol{v_{Ld}}$ is δ_m, it could be calculated as

$$\delta_m = -\varphi + \arctan\frac{\lambda^2\omega C_2 V_{Ld}^*}{I_g^*}. \tag{20}$$

With the line serving as the axis of symmetry for related trajectory, let δ_n denote the bisected half-angle (e.g., $\angle j_2HG$), which is derived as

$$\begin{cases} \delta_n = \arccos\frac{\cos^2\varphi+\lambda^2\cos^2(\delta_m+\varphi)-\chi^2}{2\lambda\cos(\delta_m+\varphi)\cos\varphi} \\ \chi = \frac{V_C^*}{\lambda V_{Ld}^*}\sin\left(\delta_m+\varphi\right)\cos\varphi. \end{cases} \tag{21}$$

Let $\delta_{\max}$ and $\delta_{\min}$ denote the maximum and minimum phase angle for the desired trajectory. Thus, $\delta_{\max} = \delta_m + \delta_n$, $\delta_{\min} = \delta_m - \delta_n$. Besides, the expression for V_{de} as a function of δ is given by

$$\begin{cases} V_{de} = \frac{\lambda V_{Ld}^*}{\sin(\delta_m+\varphi)} \cdot \sqrt{1+\xi^2-2\xi\cos(\delta_m+\varphi-\delta)} \\ \xi = \frac{\lambda\cdot\cos(\delta_m+\varphi)}{\cos\varphi}. \end{cases} \tag{22}$$

At $\delta = \delta_m + \varphi$, where points B' and B_m coincide, V_{de} reaches its minimum value.

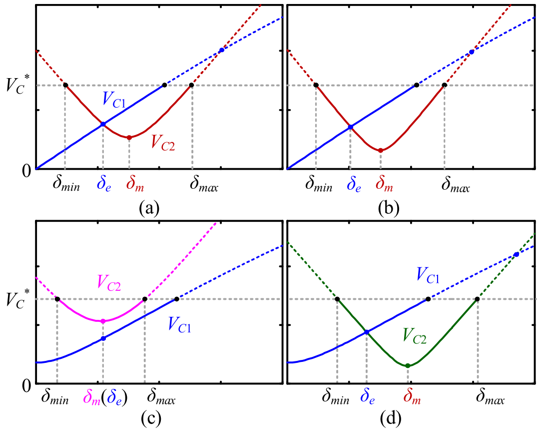


Fig. 9. AC voltage magnitude optimization. (a) $\lambda = 1$ and $\varphi = 0$. (b) $\lambda = 1$ and $\varphi \neq 0$. (c) $\lambda < 1$ and $\varphi = 0$. (d) $\lambda > 1$ and $\varphi = 0$.

Considering the expressions of V_{C1} and V_{C2}, they are both affected by phase angle δ. Fig. 9 compares the curves of V_{C1} and V_{C2} under four conditions: 1) standard grid with resistance load (arc j_1j_2); 2) standard grid with linear load (arc $j_1{}'j_2{}'$); 3) swell with resistance load (arc k_1k_2); 4) sag with resistance load (arc h_1h_2). Magnitude V_{C2} exhibits a U-shaped curve that initially decreases until its vertex at $\delta = \delta_m$ and then rises. While Magnitude V_{C1} increases with the phase angle δ. Define δ_e as the phase angle that minimizes the value of min (V_{C1}, V_{de}).

Two distinct scenarios characterize the relationship between V_{C1} and V_{C2}. For intersecting curves depicted in Fig. 9(a), (b) and (d), δ_e corresponds to the phase angle at the left intersection point, which obtains the minimum magnitudes. While for nonintersecting curves shown in Fig. 9(c), δ_e equals to δ_m.

IV. DESIGN OF KEY PARAMETERS

A. Design of Passive Components in DVR

The design of filter inductor L_1 is typically governed by the permitted maximum inductor current ripple, which is denoted as ΔI_{L1}. Let $V_{\mathrm{dc}}{}^*$, f_{sw} denote the preset dc-link voltage and switching frequency. Then, the value of L_1 is calculated as

$$L_1 = \frac{V_{\mathrm{dc}}^*}{2f_{sw}\cdot\Delta I_{L1}}. \tag{23}$$

The cutoff frequency (i.e., f_{r1}) in DVR filter is expressed as

$$f_{r1} = \frac{1}{2\pi\sqrt{L_1C_1}}. \tag{24}$$

Fitted f_{r2} should be high enough to pass the fundamental and adjacent low-frequency harmonics, while being low enough to attenuate high-frequency switching harmonics. Let f_0 denote the fundamental frequency. Based on general rule in engineering, $10f_0 < f_{r1} < 0.1f_{sw}$.

Thus, the value of C_1 is calculated as

$$C_1 = \frac{f_{sw}\cdot\Delta I_{L1}}{2\pi^2 f_{r1}{}^2 V_{\mathrm{dc}}^*}. \tag{25}$$

B. Design of Passive Components in APF

Let Z_n denote the impedance of APF filter, which is given by

$$\begin{cases} Z_n = R_{tot} + jX_{LCn} \\ X_{LCn} = n\omega L_2 - \frac{1}{n\omega C_2} \end{cases} \tag{26}$$

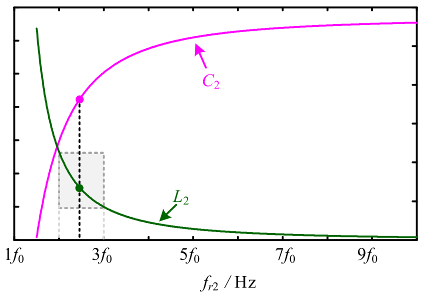


Fig. 10. Curves of L_2 and C_2 versus cutoff frequency f_{r2}.

where R_{tot} is the total resistance of APF series branch and X_{LCn} is the reactance. The fundamental reactance should be capacitive, i.e., X_{LC1} <0. With the increase of harmonic order *n*, there exists X_{LCn} >0, which is inductive reactance.

The design of buffer capacitor C_2 is based on fundamental reactive power consumption. With capacitive reactive current injected into capacitive reactance, in-phase buffer voltage component can be generated to counteract large-magnitude grid voltage $v_{g\cdot f}$. Let $Q_{Ld}{}^*$ denote the preset load-side reactive power, which is derived by long-term recorded data from residential loads. Thus, the fundamental reactance satisfies

$$X_{LC1} = \omega L_2 - \frac{1}{\omega C_2} = -\frac{{V^*_{Ld}}^2}{2Q^*_{Ld}}. \tag{27}$$

The cutoff frequency (i.e., f_{r2}) in APF can be expressed as

$$f_{r2} = \frac{1}{2\pi\sqrt{L_2 C_2}}. \tag{28}$$

Then, C_2 and L_2 are calculated as

$$\begin{cases} C_2 = \frac{2Q^*_{Ld}}{\omega {V^*_{Ld}}^2} \cdot \left(1 - \frac{\omega^2}{4\pi^2 {f_{r2}}^2}\right) \\ L_2 = \frac{\omega {V^*_{Ld}}^2}{2Q^*_{Ld}} \cdot \frac{1}{4\pi^2 {f_{r2}}^2 - \omega^2}. \end{cases} \tag{29}$$

Thus, the curves of L_2 and C_2 versus crossover frequency f_{r2} can be plotted, as shown in Fig. 10. With the increasing of f_{r2}, C_2 increases while L_2 decreases. The closer f_{r2} is to the fundamental f_0, the more rapidly the values of L_2 and C_2 change. The selection of L_2 is critical. An excessively large L_2 increases size, weight, and cost. While an overly small L_2 fails to provide sufficient attenuation for switching harmonics. The optimal compromise dictates f_{r2} in the range of $2f_0 < f_{r2} < 3\,f_0$.

C. Comparison With Passive Components in TC-UPQC

As for DVR, TC- and DuC-UPQC have identical structure so that they can share same *LC* parameter design.

For the APF design in TC-UPQC, let $L_{2\cdot TC} = L_2$. Under same power $Q_{Ld}{}^*$, capacitors $C_{2\cdot\mathrm{TC}}$ and $C_{3\cdot\mathrm{TC}}$ satisfy

$$\frac{1}{1 - \omega^2 L_2 C_{3\_\mathrm{TC}}} \cdot \omega L_2 - \frac{1}{\omega C_{2\_\mathrm{TC}}} = -\frac{{V^*_{Ld}}^2}{2Q^*_{Ld}}. \tag{30}$$

The discussion can be divided into two cases.

If $\omega^2 L_2 C_{3\cdot\mathrm{TC}} > 1$, then $C_{2\cdot\mathrm{TC}} > \mathrm{C}_{2\cdot\mathrm{DuC}}$, so that the total APF capacitance ($C_{2\cdot\mathrm{TC}} + C_{3\cdot\mathrm{TC}}$) in TC-UPQC is greater.

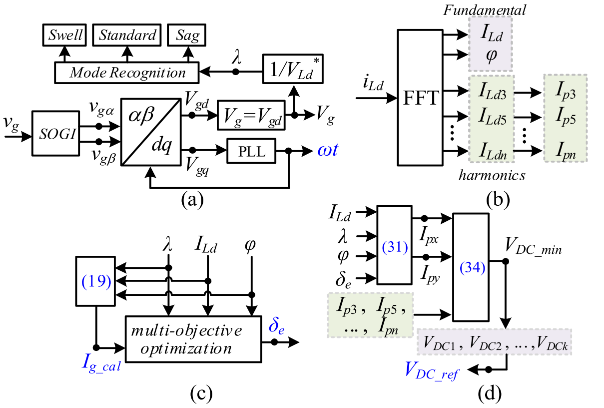


Fig. 11. Parameter identification. (a) Grid voltage. (b) Load current. (c) Multiobjective optimization. (d) Reference of DC-link voltage.

If $\omega^2 L_2 C_{3\cdot\mathrm{TC}} < 1$, then the *LCC* structure in TC-UPQC can be transformed into equivalent *LC* structure with parameters (i.e., $L_2{}'$ and $C_{2\cdot\mathrm{TC}}$). Here, $L_2{}' = \omega/(1\text{-}\omega^2 L_2 C_{3\cdot\mathrm{TC}})$. Thus, for any given parameters in TC-UPQC, there exists equivalent DuC-UPQC so that the redundant filter capacitor $C_{3\cdot\mathrm{TC}}$ is no longer needed.

From the analysis of two cases above, DuC-UPQC requires lower total capacitance than TC-UPQC.

D. Design of Minimum DC-Link Voltage

Decompose APF current i_p into orthogonal components (i.e., i_{px} and i_{py}). Here, i_{px} is in phase with v_g while i_{py} is in quadrature with it. Their magnitudes can be calculated as

$$\begin{cases} I_{px} = \frac{I_{Ld}}{\lambda} \cdot [\lambda \cos(\delta_e + \varphi) - \cos\varphi] \\ I_{py} = I_{Ld} \sin(\delta_e + \varphi). \end{cases} \tag{31}$$

The magnitude of fundamental voltage $v_{ao\cdot f}$ in APF bridge arm can be calculated as

$$V_{ao\_f} = \sqrt{(I_{px} \cdot X_{LC1})^2 + (I_{py} \cdot X_{LC1} - V_g)^2}. \tag{32}$$

Let I_{pn} denote the magnitude of the mapped APF harmonic current i_{ph}. The magnitude of total harmonic voltage $v_{ao\cdot h}$ is

$$V_{ao\_h} = \sqrt{\sum\nolimits_{n=3,5,\ldots} (I_{pn} \cdot X_{LCn})^2}. \tag{33}$$

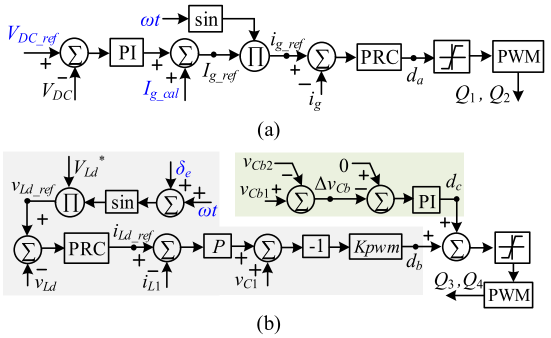
Thus, the minimum dc-link voltage is expressed as

$$V_{\mathrm{dc\_min}} = \sqrt{(I_{px} \cdot X_{LC1})^2 + (I_{py} \cdot X_{LC1} - V_g)^2 + \sum_{n=3,5,\ldots} (I_{pn} \cdot X_{LCn})^2}. \tag{34}$$

V. CONTROL SYSTEM FOR DUC-UPQC

A. External Parameter Identification

The implementation of parameter identification is depicted in Fig. 11. First, utilize SOGI-PLL to detect magnitude V_g and phase angle ωt from grid voltage v_g. Apply FFT algorithm to obtain the fundamental (i.e., I_{Ld} and φ) and harmonics (i.e., I_{Ld3},



(a)

(b)

Fig. 12. Control implementation of DuC-UPQC. (a) APF. (b) DVR.

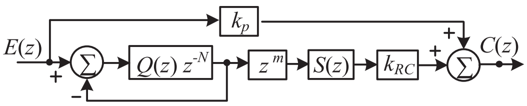


Fig. 13. Block diagram of PRC.

$I_{Ld5}, \ldots, I_{Ldn}$). Next, multiobjective optimization in previous phasor analysis can be employed to obtain optimal load voltage phase angle δ_e. Then, theoretical minimum dc-link voltage is calculated. To ensure robustness against variations in external environment, sufficient voltage margin should be reserved in $V_{\mathrm{dc}\cdot\mathrm{ref}}$. Besides, $V_{\mathrm{dc}\cdot\mathrm{ref}}$ can be set to multiple predefined levels ($V_{\mathrm{dc}1}, V_{\mathrm{dc}2}, \ldots, V_{\mathrm{dc}n}$) to achieve optimal performance.

B. Implementation of Control System

With the key parameters (e.g., ωt, δ_e, $V_{\mathrm{dc}\cdot ref}$, $I_{g\cdot cal}$) secured, the overall control diagram of DuC-UPQC is obtained, which is depicted in Fig. 12. Since the mutual interference caused by state variables is eliminated, the control systems of APF and DVR can be designed separately.

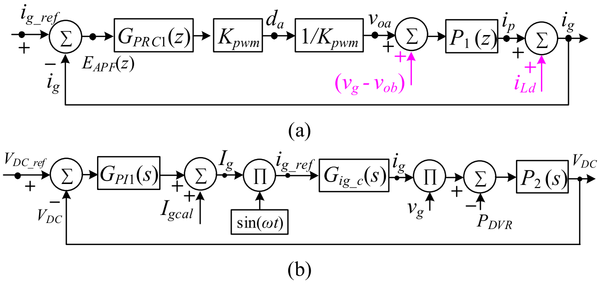
For APF, dc-link voltage outer loop is embedded for power balance control. While $I_{g\cdot cal}$ is utilized as a feedforward term to enhance dynamic response and minimize overshoot. Next, grid current inner loop uses proportional repetitive controller (PRC) to track ac signal and mitigate harmonics. The block diagram of PRC is shown in Fig. 13 and its transfer function in z-domain can be written as

$$G_{\mathrm{PRC}}(z) = k_p + k_{\mathrm{RC}} \cdot \frac{Q(z)z^{-N}}{1 - Q(z)z^{-N}} \cdot z^m \cdot S(z) \qquad (35)$$

where k_p and k_{RC} are the gain of controllers P and RC; N is the number of samples in one fundamental period. $Q(z)$ is low-pass filter or a constant less than 1. $S(z)$ is Butterworth low-pass filter and z^m is phase lead compensator.

As for DVR, standard sinusoidal load voltage is managed by modulation signal d_b. Here, proportional (P) controller is used in inner current loop and PRC controller is employed in outer voltage loop. Besides, active capacitor voltage feedforward is incorporated to enhance dynamic performance.

On the other hand, neutral point voltage imbalance between split capacitors is regulated by signal d_c and PI controller is applied for processing error signal.



(a)

(b)

Fig. 14. Whole control diagram of APF. (a) Inner loop. (b) Outer loop.

C. Stability Analysis

Fig. 14(a) shows the current inner loop in APF, the plant $P_1(s) = (R_{tot} + sL_2 + 1/sC_2)^{-1}$. $P_1(z)$ is the z-domain expression for $P_1(s)$. Since $(v_g - v_{ob})$ and i_{Ld} vary at certain range, they can be regarded as disturbance. The tracking error $E_{\mathrm{APF}}(z)$ is

$$E_{\mathrm{APF}}(z) = \frac{1}{1 + G_{\mathrm{PRC1}}(z)P_1(z)} \cdot i_{g\_ref}(z) \qquad (36)$$

where $i_{g\cdot ref}(z)$ is reference of grid current $i_g(z)$. G_{PRC1} is the PRC controller in APF. k_{p1} and k_{RC1} are the mapped gains.

Then, the characteristic polynomial is expanded as

$$\begin{aligned} &1 + G_{\mathrm{PRC1}}(z)P_1(z) \\ &= [1 + k_{p1}P_1(z)] \cdot \left[1 + k_{\mathrm{RC1}}\frac{Q(z)z^{-N}}{1 - Q(z)z^{-N}} \cdot z^m \cdot \frac{S(z)P_1(z)}{1 + k_{p1}P_1(z)}\right]. \end{aligned} \qquad (37)$$

Let $P_1{}'(z) = P_1(z) / (1+k_{p1} P_1(z))$. The stability of current inner loop in APF depends on following conditions.

The roots of $1 + k_{p1}P_1(z) = 0$ are inside the unit circle.

$$\left|1 + k_{\mathrm{RC1}}\frac{Q(z)z^{-N}}{1 - Q(z)z^{-N}} \cdot z^m \cdot S(z)P_1'(z)\right| \neq 0. \qquad (38)$$

A sufficient condition for (38) is that

$$\begin{aligned} &\left|Q(z)z^{-N} \cdot [1 - k_{\mathrm{RC1}} \cdot z^m \cdot S(z)P_1'(z)]\right| \\ &< 1 \quad \forall z = e^{j\omega}, \quad 0 < \omega < \frac{\pi}{T_s} \end{aligned} \qquad (39)$$

where T_s is the sampling period.

Since the reference and disturbances are at integer multiples of the fundamental $|z^{-N}| = 1$. Let $P_1{}'(j\omega) = N_p(\omega)\exp(j\theta_p(\omega))$, $S(j\omega) = N_s(\omega)\exp(j\theta_s(\omega))$. Then, (39) can be written as

$$\left|1 - k_{RC1} \cdot N_S(\omega)N_P(\omega)e^{j[\theta_S(\omega)+\theta_P(\omega)+m\omega]}\right| < 1. \qquad (40)$$

Since k_{RC1}>0, $N_s(\omega)$ >0, $N_p(\omega)$ >0, then (40) transforms to

$$\begin{cases} |\theta_S(\omega) + \theta_P(\omega) + m\omega| < \pi/2 \\ 0 < k_{RC1} < \frac{2\cos[\theta_S(\omega)+\theta_P(\omega)+m\omega]}{N_S(\omega)N_P(\omega)}. \end{cases} \qquad (41)$$

Fig. 14(b) shows the voltage outer loop in APF. Let $G_{i_g\cdot c}(s)$ denote the close-loop transfer function of current inner loop. To maintain system stability, the bandwidth of current inner loop is designed to be much greater than that of voltage outer loop. With current inner loop achieving zero steady-state tracking error, it

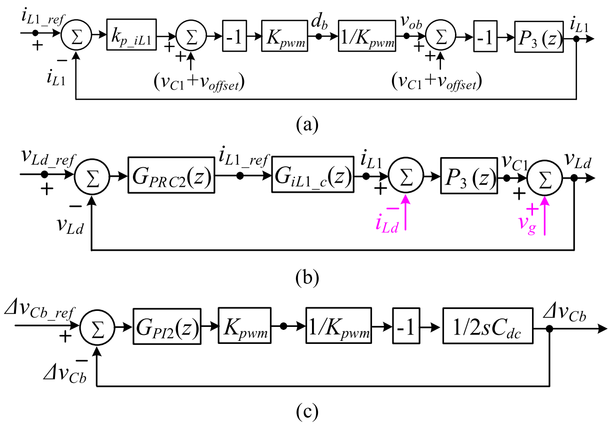


Fig. 15. Whole control diagram of DVR. (a) AC inner loop. (b) AC outer loop. (c) DC-bias loop.

TABLE V
MAIN PARAMETERS OF THE SYSTEM

Parameters	Value
Nominal load voltage (V_L^*)	100V
Nominal grid frequency (f_0)	50Hz
Switching frequency (f)	10kHz
Linear load	10Ω + 26mH
Nonlinear load	6mH + diode rectifier + 4mF + 20Ω

can be regarded as ideal element, i.e., $G_{ig\cdot c}(s) = 1$. The plant $P_2(s)$ in voltage outer loop is integral element, i.e., $P_2(s) = K_{\mathrm{dc}}/s$. Let C_{dc} denote the capacitance of C_{b1} and C_{b1}. Thus, $K_{\mathrm{dc}} = V_g/(C_{dc}V_{\mathrm{dc}\cdot ref})$. Controller $G_{PI1}(s) = k_{p1\cdot PI1} + k_{i1\cdot PI1}/s$. Simplifying the control diagram, $G_{\mathrm{VDC}}(s)$, the open-loop transfer function of the voltage outer loop, is indicated as

$$G_{\mathrm{VDC}}(s) = \frac{V_g}{C_{\mathrm{dc}}V_{\mathrm{dc}\_ref}} \cdot \left(k_{p1\_PI1} + \frac{k_{i1\_PI1}}{s}\right) \cdot \frac{1}{s}. \tag{42}$$

Clearly, this is a typical Type II system. Thus, conventional PI design methodology and stability analysis in [34] could be applied here.

As for load voltage regulating in DVR, the whole control diagram for inner current loop and outer voltage loop are shown in Fig. 15(a) and (b). While the whole control diagram for neutral point voltage imbalance is presented in Fig. 15(c). The corresponding transfer function can be obtained. Since the design of controllers (e.g., PRC and PI) and stability analysis in DVR are similar to that in APF, which will not be discussed in detail here.

VI. SIMULATION VERIFICATION

Validation of the preceding theoretical analysis is conducted through MATLAB/Simulink. The implementation parameters are specified in Tables V and VI, with ac quantities measured by peak value and dc quantities by root-mean-square (rms) value.

TABLE VI
FILTER COMPONENTS OF NONISOLATED UPQCS

UPQC type	APF			DVR	
	Filter inductor	Buffer capacitor	Filter capacitor	Filter inductor	Filter capacitor
DT-	6mH	/		1.5mH	50μF
TC-	6mH	250μF	50μF		
DuC-	6mH	300μF	/		

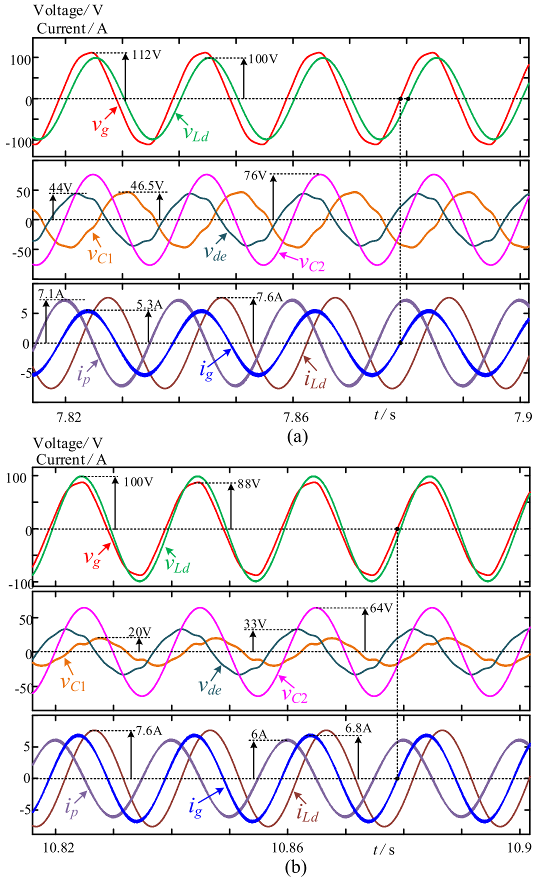


Fig. 16. Simulation results for DuC-UPQC with linear load. (a) During swell. (b) During sag.

A. Simulation Results for DuC-UPQC With Linear Load

The steady-state simulation results of DuC-UPQC operating under nonideal grid with linear loads are presented in Fig. 16. The reconstructed grid voltage v_g (sampled from real-world data and modeled in MATLAB) exhibits 2.56% THD with visible waveform distortion. Peak grid voltages are 112 V (i.e., grid swell) and 88 V (i.e., grid sag), as shown in Fig. 16(a) and (b), respectively.

To maintain sinusoidal load voltage v_{Ld} and grid current i_g, harmonics are redirected to v_{C1} and v_{de}. During swell, v_{C1} carries 6.23% THD and v_{de} exhibits 6.59% THD. Under sag, these values shift to 12.2% THD for v_{C1} and 6.99% THD for v_{de}. This harmonic confinement limits distortion to only v_g, v_{C1},

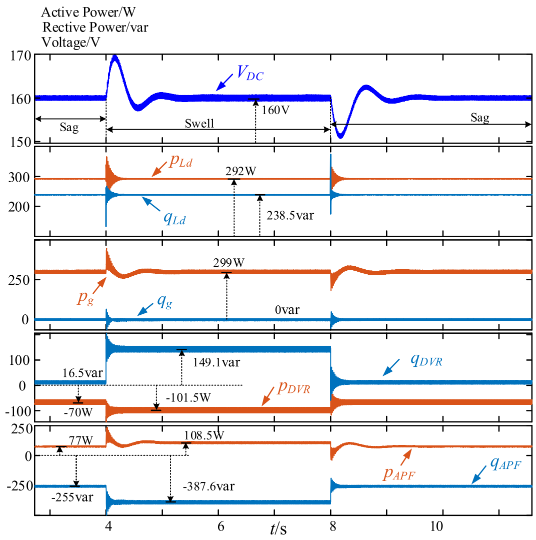


Fig. 17. Power flow in DuC-UPQC during grid fluctuations.

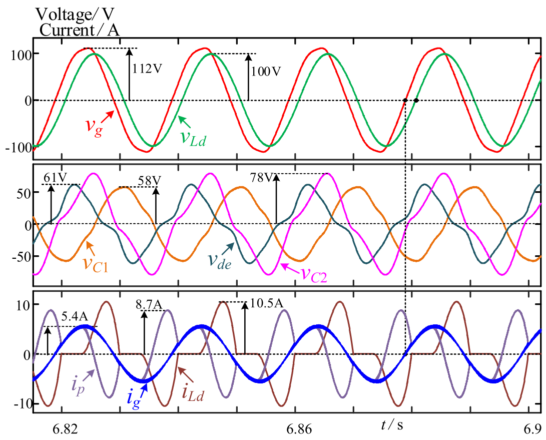


Fig. 18. Simulation results for DuC-UPQC with nonlinear load.

and v_{de}, preserving clean sinusoids elsewhere. Furthermore, the DuC-UPQC demonstrates robust voltage regulation capability by maintaining the load voltage v_{Ld} at the nominal 100 V standard regardless of swell or sag, which ensures a standard sinusoidal voltage to critical load.

Due to the inherent characters of linear load (i.e., 10 Ω + 26 mH), the resulting load current i_{Ld} measures 7.6 A in magnitude with a 39.2°(i.e., 4.36 ms) phase lag relative to v_{Ld}. To prevent load-side phase lag from propagating to grid-side unity power factor, precise compensation current i_p is generated by APF. During swell, i_p measures 7.1 A with a 4.0 ms phase lead while it measures 6 A with a 4.0 ms lead during sag. This active compensation ensures phase-synchronized grid current i_g with magnitudes at 5.3 A during swell and 6.8 A during sag.

Peak voltage reduction for v_{de} is achieved through controlled phase angle δ. During grid swell, $\delta = 25°$ and the peak value of v_{de} and v_{C1} are limited to 44 V and 46.5 V, representing 60.7% and 58.5% reductions compared to the 112 V (peak excessive grid voltage v_g). This voltage redistribution is facilitated by v_{C2} with peak voltage 76 V. During grid sag, δ is set as 10° that peak v_{de} and v_{C1} are maintained at 33 V (62.5% reduction) and 20 V (77.3% reduction) relative to 88 V (peak insufficient grid voltage v_g), with peak v_{C2} stabilizing at 64 V.

Considering the half-bridge structures in DuC-UPQC, the reference of dc-link voltage is set to 160 V to ensure sufficient modulation margin. Under grid swell, the modulation indexes of DVR and APF reach 0.55 and 0.58, respectively, while during sag they adjust to 0.41 and 0.25, demonstrating acceptably small intermodule discrepancies.

The power flow of DuC-UPQC during grid fluctuations is depicted in Fig. 17. Grid voltage changes from sag to swell at $t = 4$ s while turns back to sag at $t = 8$ s. DC-link voltage accurately tracks its reference (160 V), achieving power balance between DVR and APF. Besides, instantaneous power theory [35] is employed to measure the instantaneous active and reactive power at four ac ports. Let $p_g, p_{Ld}, p_{\mathrm{DVR}}, p_{\mathrm{APF}}$ denote the instantaneous active power in grid, load, DVR and APF, with q_g, q_{Ld}, q_{DVR}, q_{APF} being the mapped instantaneous reactive power. It could be calculated that total converter losses here is 14 W. The simulation results satisfy the previous power flow analysis.

B. Simulation Results for DuC-UPQC With Nonlinear Load

Under the aforementioned distorted grid swell (i.e., 112 V peak), simulation for nonlinear loads is performed. Nonlinear load consists of ac-side 6 mH inductor, uncontrolled rectifier followed by dc-link 4 mF capacitor and 20 Ω resistive load. The steady results are depicted in Fig. 18. Owing to DVR compensation, load voltage is regulated to a standard sinusoidal waveform with 31° phase lag relative to grid voltage.

Due to nonlinear loads, distorted load current occurs with 10.5 A peak current and 49.77% THD. To prevent harmonic currents from polluting the grid current, the APF absorbs the current harmonics while injecting fitted fundamental current. The APF's compensating current i_p shows 8.7 A peak current and 53.36% THD. Thus, grid current is adjusted to be sinusoidal grid-synchronized with 5.4 A peak value.

Buffer capacitor voltage v_{C2}, generated through integration of i_p, exhibits 78 V peak value with 17.35% THD. Therefore, the regulated ac voltages v_{de} and v_{C1} demonstrate peak values of 61 V and 58 V, corresponding to significant attenuations of 45.5% and 48.2% relative to the peak grid voltage v_g (112 V). Besides, the intermediate ac voltages v_{de} and v_{C1} absorb harmonics originated from distorted grid and nonlinear loads, as evidenced by their respective THD of 21.21% and 5.05% . As the peak values of v_{de} and v_{C1} in nonlinear load are higher than linear load, dc-link voltage is elevated to 170 V to enhance modulation margin. The DVR and APF achieve modulation indexes of 0.68 and 0.71, indicating permissible minimal difference between two units.

Fig. 19 shows the response of dc-link voltage during load transitions. At the beginning, dc-link voltage follows its 170 V reference successfully. With nonlinear load switched to linear

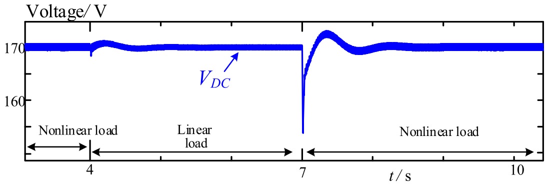


Fig. 19. Simulation results for DuC-UPQC during load switch.

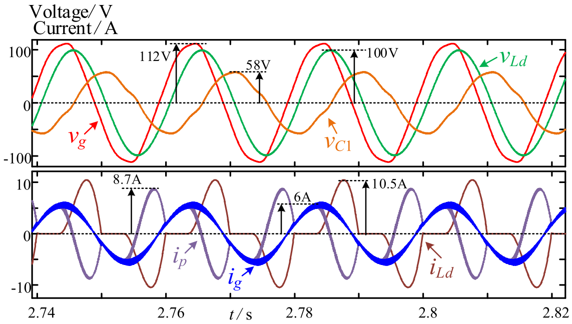


Fig. 20. Simulation results of DT-UPQC with nonlinear load.

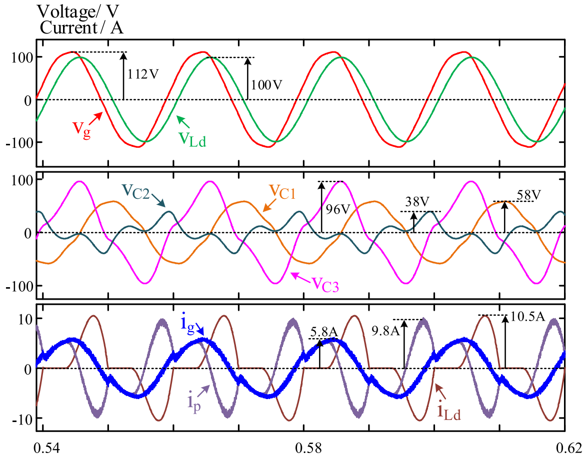


Fig. 21. Simulation results for TC-UPQC with nonlinear load.

load (i.e., 10 Ω + 26 mH) at $t = 4$ s, dc bus voltage shows negligible disturbance. During the reverse transition (linear → nonlinear load) at $t = 7$ s, an instantaneous voltage dip occurs due to dc-side 4 mF capacitor with initial zero voltage. Promptly, the closed-loop control restores the dc bus voltage to its reference, validating the strong robustness of DuC-UPQC.

C. Comparative Simulation Results

Based on the parameters of Table V and VI, comparative simulations (i.e., DT- and TC-UPQC with nonlinear load during grid swell) are conducted, with waveforms depicted in Figs. 20 and 21. Besides, Table VII shows the comparison of key performance data. It can be obtained that the APF modulation index m_1 in three UPQCs are nearly equal, while DuC- and TC-UPQC bear lower dc-link voltage (i.e., 170 V) due to buffer capacitor. As a result, the THD of load voltage v_{Ld} in DuC- and TC-UPQC can be decrease due to lower switching harmonics. As for the THD of grid current i_g, DuC-UPQC achieves superior performance. In contrast, grid current in TC-UPQC is polluted since its buffer capacitor amplifies annoying voltage noise. Finally, DuC-UPQC exhibits optimal modulation indexes since the difference between m_1 and m_2 is minimal.

TABLE VII
SIMULATION RESULTS FOR THREE UPQCS DURING NONLINEAR LOAD

UPQC type	m_1 of APF	m_2 of DVR	THD of i_g	THD of v_{Ld}	V_{dc} /V
DT-	0.67	0.38	5.88%	0.89%	300
TC-	0.68	0.44	11.77%	0.79%	170
DuC-	0.68	0.71	2.74%	0.79%	170

TABLE VIII
SIMULATION RESULTS FOR SEMICONDUCTOR LOSS

UPQC type	Test Conditions			APF switches losses/W	DVR switches losses/W
	Grid	Load	V_{dc} /V		
DT-	Sag	Linear	280	63.47	64.65
	Swell	Linear	280	64.23	65.01
	Swell	Nonlinear	300	70.64	70.36
TC-	Sag	Linear	160	30.85	31.11
	Swell	Linear	160	32.23	31.42
	Swell	Nonlinear	170	34.39	33.78
DuC-	Sag	Linear	160	31.23	32.15
	Swell	Linear	160	31.89	32.42
	Swell	Nonlinear	170	34.36	34.13

D. Simulation for Semiconductor Loss

The previous simulations relied on ideal IGBT modules in Simulink. To obtain a more accurate power loss analysis for DT-, TC- and DuC-UPQC, the datasheet lookup-table method from [36] was adopted here. First, power loss model based on FF100R12RT4 is established in Simulink. Using digital tools, plot critical curves from its datasheets. Next, translate these static curves into dynamic real-time loss calculation blocks. Then power losses are computed from the real-time inputs of duty cycle, collector current, and dc-link voltage to determine the instantaneous IGBT power loss, which is then processed via a moving average filter. Finally, IGBT power losses for non-isolated UPQCs are obtained, which are shown in Table VIII. A comparative of simulation results reveals that DuC-UPQC achieves lowest semiconductor losses.

VII. EXPERIMENTAL VERIFICATION

The experimental platform of DuC-UPQC is developed to further examine the performances, as depicted in Fig. 22. The experimental tests implement the same parameters previously specified in Tables V and VI. The IGBT module type is FF100R12RT4. Autotransformer serves as a variable grid voltage conditioner by adjusting the voltage magnitude through

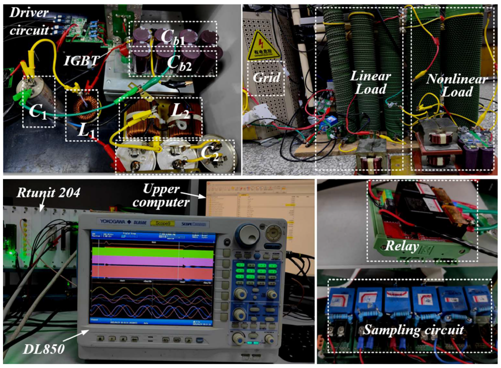


Fig. 22. Experimental platform of DuC-UPQC.

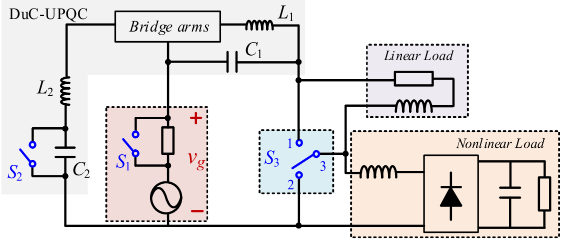


Fig. 23. Structure of test scheme.

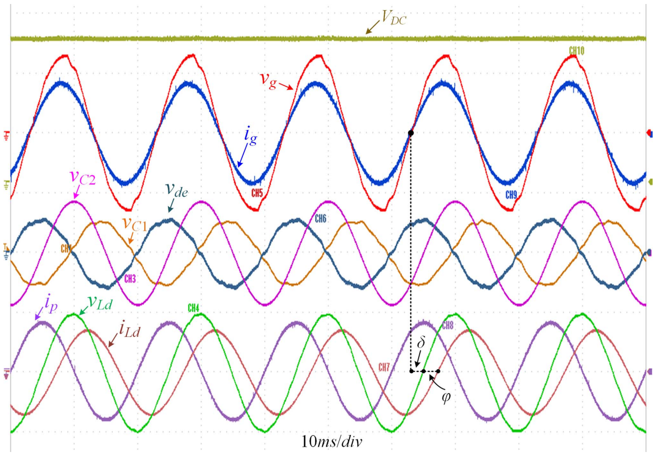


Fig. 24. Experimental results for DuC-UPQC with linear load during swell. ($V_{\rm dc}$, 70 V/*div*; v_g, 80 V/*div*; i_g, 9 A/*div*; v_{C1}, 100 V/*div*; v_{C2}, 100 V/*div*; v_{de}, 100 V/*div*; i_p, 10 A/*div*; v_L, 100 V/*div*; i_{Ld}, 10 A/*div*.).

its tap-changing mechanism. DL850 is applied for recording experimental waveforms and RTUNIT 204 is employed for processing digital signals. Relays (e.g., S_1, S_2, and S_3) are used for transient performance tests, as shown in Fig. 23.

A. Test Results for DuC-UPQC During Linear Load

Fig. 24 shows experimental results of DuC-UPQC operating with linear loads. Grid voltage demonstrates visible harmonics distortion with 105.4 V peak. With grid harmonics filtering into ac voltages v_{C1} and v_{de}, load voltage v_{Ld}, and buffer capacitor voltage exhibit sinusoidal waveforms with peak values of 100 V and 87.85 V, respectively. While v_{C1} and v_{de} are polluted with peak values of 55.35 V and 59.85 V, representing 43.2% and 47.5% reductions compared to peak grid voltage. With respect to dc-link voltage $V_{\rm dc}$, it maintains stable 160 V, indicating active power balance between DVR, APF, and losses. Next, the modulation indexes of DVR and APF could be calculated as 0.69 and 0.75, exhibiting superior modulation indexes.

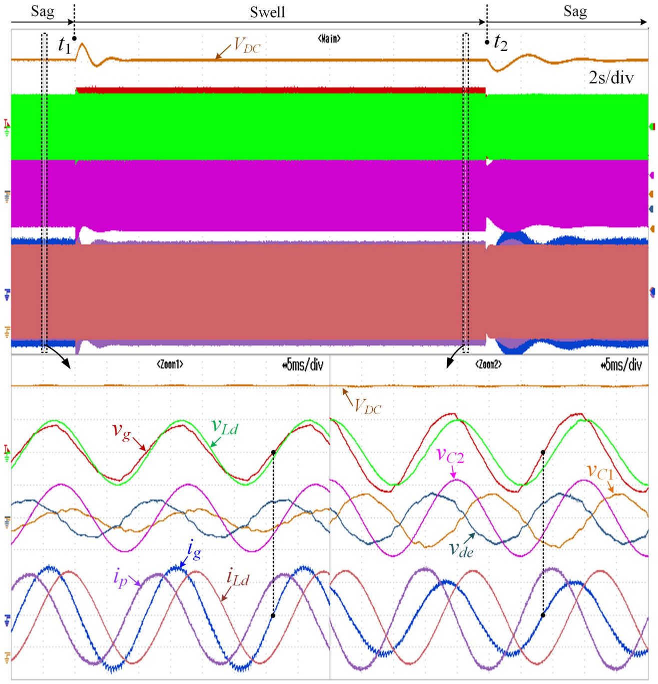


Fig. 25. Transient response during rapid voltage fluctuations. ($V_{\rm dc}$, 20 V/*div*; v_g, 100 V/*div*; v_{Ld}, 100 V/*div*; v_{C1}, 75 V/*div*; v_{C2}, 75 V/*div*; v_{de}, 75 V/*div*; i_p, 6 A/*div*; i_g, 6 A/*div*; i_{Ld}, 6 A/*div*.).

Load voltage v_{Ld} lags grid voltage v_g by 30° (i.e., 1.67 ms). Load current i_{Ld} measuring 7.24 A peak lags load voltage v_{Ld} by 39.2° (i.e., 2.18 ms) due to linear load (i.e., 10 Ω + 26 mH). For grid-side unity power factor, compensating current i_p leading grid voltage v_g by 3.1 ms is produced so that phase-synchronized sinusoidal grid current i_g is regulated. The peak values of i_p and i_g are 8.6 A and 7.4 A, which is higher than the simulation results due to losses.

Under distorted grid with linear loads, grid swell/sag is produced by switching relay S_1 (parallel to a resistor) ON/OFF, as shown in Fig. 23. The transient response of DuC-UPQC during grid fluctuations are depicted in Fig. 25. Grid voltage transitions from swell to sag at t_1, then returns to swell at t_2. Obviously, dc-link voltage $V_{\rm dc}$ is well regulated at 160 V reference. Zoom 1 and Zoom 2 of Fig. 25 are the magnified waveforms detailing the swell and sag condition. The magnitude of sinusoidal load voltage v_{Ld} maintains constant 100 V peak.

During the sag-to-swell transition at t_1, the energy surplus causes a transient overshoot that is stabilized via active damping control. Conversely, the swell-to-sag transition at t_2 produces an initial undershoot with subsequent compensatory overshoot before converging to the reference through closed-loop regulation.

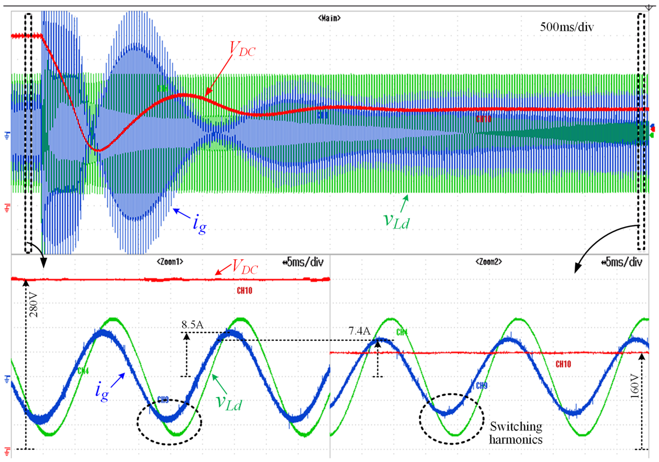


Fig. 26. Performance under different DC-link voltage. ($V_{\rm dc}$, 40 V/*div*; v_{Ld}, 45 V/*div*; i_g; 5 A/*div*.).

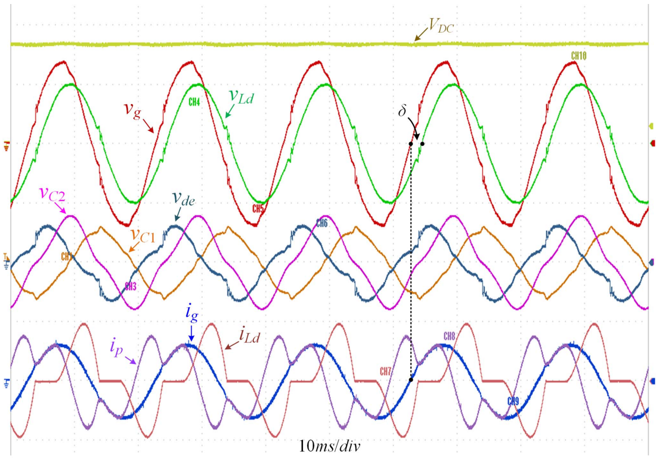


Fig. 27. Experimental results for nonlinear load. ($V_{\rm dc}$, 100 V/*div*; v_g, 80 V/*div*; v_{Ld}, 100 V/*div*; v_{C1}, 100 V/*div*; v_{C2}, 100 V/*div*; v_{de}, 100 V/*div*; i_p, 10 A/*div*; i_g, 10 A/*div*; i_{Ld}, 10 A/*div*.).

B. Comparison With Existing Method

As shown in Fig. 23, relay S_2 (parallel to buffer capacitor) ON/OFF corresponding to the existing DT-UPQC and the proposed DuC-UPQC. Under distorted grid with 105.4 V peak and linear loads (i.e., 10 Ω + 26 mH), experimental test for two methods are carried out and Fig. 26 depicts the results. In the beginning, S_2 is ON and the system operates as DT-UPQC. As magnified in Zoom 1 of Fig. 26, dc-link voltage $V_{\rm dc}$ stabilizes at 280 V rms while load voltage v_{Ld} and grid current i_g exhibit sinusoidal profiles with peak values of 100 V and 8.5 A. With S_2 turning OFF exactly at zero point of compensating current i_p, the system transitions from DT-UPQC to DuC-UPQC and the reference value of dc-link voltage varies from 280 V to 160 V. After undergoing oscillatory transient regulation, the system reaches the steady state, as shown in Zoom 2 of Fig. 26. DC-link voltage tracks its new referenced value at 170 V rms while maintaining sinusoidal v_{Ld} (100 V peak) and i_g (7.4 A peak). With input grid current decreased (8.5 A→7.4 A), the efficiency of DuC-UPQC is improved comparing to DT-UPQC. Besides, it could be observed from magnified parts that the switching harmonics on load voltage v_{Ld} and grid current i_g of DuC-UPQC is mitigated due to reduced dc-link voltage.

C. Test Results for DuC-UPQC During Nonlinear Load

Experimental results in Fig. 27 illustrate the performance of DuC-UPQC operating with nonlinear load. The grid power supply exhibits harmonic distortion with measured 112 V peak. Through DVR intervention, load voltage v_{Ld} is corrected to standard sinusoidal waveform with 100 V peak and 31° phase lag. Nonlinear load generate distorted load current reaching 9.7 A peak. By absorbing current harmonics and injecting fundamental current, precisely calibrated compensating current i_p is produced with 8 A peak, which enables grid current i_g to achieve sinusoidal synchronization at 6.75 A peak. Owing to the current harmonics, the waveform of buffer capacitor voltage v_{C2} are distorted with 79.8 V peak. Subsequent voltage regulation yields ac voltages v_{de} (65.35 V peak) and v_{C1} (61.65 V peak), representing attenuations of 41.7% and 45.0% compared to the 112 V grid voltage peak. With dc-link voltage tracking its 170 V reference value, modulation indexes for APF and DVR are 0.77 and 0.73, demonstrating allowable differences.

TABLE IX
CONDITIONS FOR EXPERIMENTAL EFFICIENCY TEST

$V_{Ld}{}^*$/V		100	120	140	160	180	200
V_g/V		112	134	157	180	202	224
$V_{\rm dc}$ /V	DT-UPQC	300	360	420	480	540	600
	TC-UPQC	170	204	238	272	306	340
	DuC-UPQC	170	187	187	204	221	255
Load		Nonlinear load (6mH + diode rectifier + 4 mF + 20 Ω)					

Relay S_3 operates as a single-pole double-throw switching device, where its common terminal toggles between two contact positions to select load operational modes. When engaged with contact 1, nonlinear load is activated. While connected to contact 2, linear load is energized. The dynamic performance of DuC-UPQC during load variations is presented in Fig. 28. Initially, linear load is engaged and dc-link voltage stabilizes at 170 V reference. With common terminal toggles to position 2 (nonlinear to linear), dc-link voltage exhibits small voltage fluctuation. While the reverse transition (linear to nonlinear), triggers a momentary voltage sag, which is consistent with simulation results.

D. Experimental Efficiency Tests

Comprehensive experimental tests were conducted on three nonisolated UPQCs. The test conditions are shown in Table IX and input grid current i_g is maintained at a unity power factor. Same hardware components (capacitors, inductors and IGBTs)

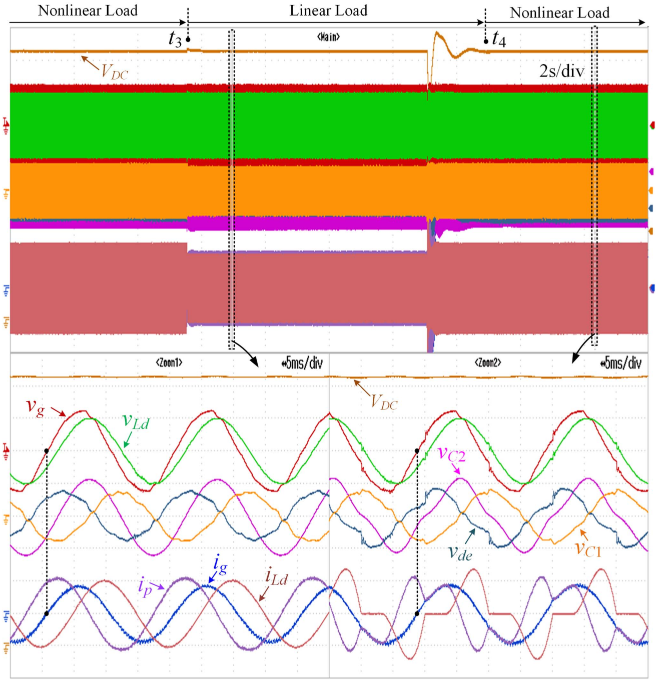


Fig. 28. Transient response during load switch. (V_{dc}, 20 V/*div*; v_g, 100 V/*div*; v_{Ld}, 100 V/*div*; v_{C1}, 75 V/*div*; v_{C2}, 75 V/*div*; v_{de}, 75 V/*div*; i_p, 7.5 A/*div*; i_g, 7.5 A/*div*; i_{Ld}, 7.5 A/*div*.).

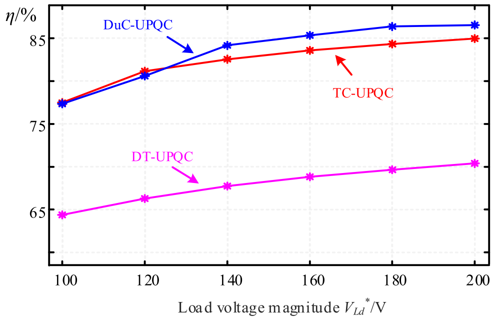


Fig. 29. Experimental efficiency curves for three UPQCs with nonlinear load.

are employed in these UPQCs. Input and output active power are recorded with power analyzer (i.e., WT1806E).

The experimental test efficiency (i.e., η) curves are depicted in Fig. 29. Obviously, three curves shows an upward trend with the increase of load voltage level. DuC- and TC-UPQC exhibit higher efficiency than DT-UPQC. Besides, the efficiency of DuC-UPQC is slightly higher than TC-UPQC.

VIII. CONCLUSION

This article proposes a novel buffer-capacitor-based DuC-UPQC, which exhibits multiple advantages, e.g., reduced dc-link voltage, improved modulation indexes, second-order *LC* filter in APF, low voltage stress, and low power loss.

Compare with existing TC-UPQC, it possesses simplified cost-effective structure due to less bipolar capacitor. Second, it can eliminate coupling between inside DVR and APF so that independent control can be applied. Third, it features robustness against grid voltage harmonics.

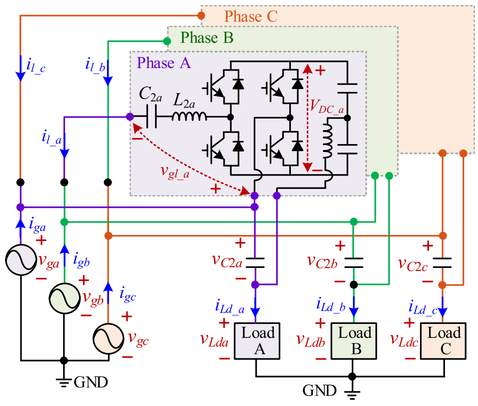


Fig. 30. Derivative three-phase DuC-UPQC.

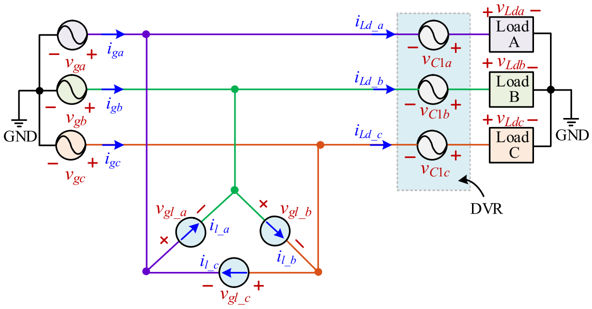


Fig. 31. Equivalent circuit of three-phase DuC-UPQC.

To accomplish multiple objectives, 2-D multiobjective optimization strategy is designed by introducing load voltage phase angle adjustment. Thus, buffer-capacitor-based structure can manage voltage and current-related power quality issues, achieve inside power balance between DVR and APF, obtain reduced dc-link voltage concurrently. Next, phasor analysis is applied to deduce the constraints and their analytical solutions. Then, associated control strategy is designed.

Finally, simulation and experimental results confirm the superior performance of the proposed DuC-UPQC.

APPENDIX I

With regard to unbalance and harmonics issues in three-phase system, the derivative three-phase DuC-UPQC topology is proposed, as depicted in Fig. 30. Its equivalent circuit is shown in Fig. 31. Delta-connected configuration is employed in APF. There are three separate dc buses (e.g., $V_{\mathrm{dc}'a}$, $V_{\mathrm{dc}'b}$, $V_{\mathrm{dc}'c}$). The control strategy of DVRs are same as previous single-phase DuC-UPQC, which will not be discussed in detail here. While the control strategy of APFs, separate decoupling of positive, negative and zero sequence currents is adopted to address the load imbalance currents and harmonics issues. The control diagrams are shown in Figs. 32 and 33.

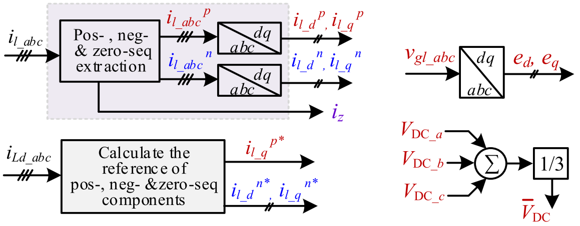


Fig. 32. Parameters transformation.

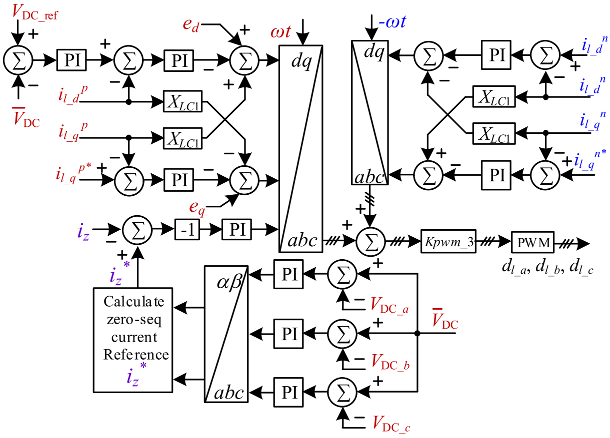


Fig. 33. APF control strategy in three-phase DuC-UPQC.

REFERENCES

[1] S. Behera, V. R. N. N., A. K. Panda, S. K. Behera, and N. Tiwary, “An enhanced grid-tied off-board electric vehicle charger with improved power quality using unified control approach,” *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9775–9785, Jul. 2025.

[2] S. M. Mortazavi and R. Beiranvand, “A direct AC-AC switched-capacitor converter with input-series output-parallel and in-phase/out-of-phase capabilities,” *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12221–12235, Oct. 2023.

[3] H. F. Ahmed, M. S. E. Moursi, B. Zahawi, K. A. Hosani, and A. A. Khan, “Switching-cell buck-boost AC-AC converter with common-ground and noninverting/inverting operations,” *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13944–13957, Dec. 2021.

[4] S. Hou, J. Han, Y. Chu, C. Zhou, and J. Fei, “Practical terminal sliding mode control of active power filters by self-organizing hermite fuzzy neural network,” *IEEE Trans. Power Electron.*, vol. 41, no. 1, pp. 626–639, Jan. 2026.

[5] Z. Zhang, H. Yi, Y. Li, X. Jiang, Z. Wang, and F. Zhuo, “A novel decentralized droop control scheme for multiparalleled APFs with grid current detected,” *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 5922–5938, Apr. 2025.

[6] C. D. Sanjenbam and B. Singh, “Modified adaptive filter based UPQC for battery supported hydro driven PMSG system,” *IEEE Trans. Ind. Inform.*, vol. 19, no. 7, pp. 8018–8028, Jul. 2023.

[7] V. Monteiro et al., “A novel three-phase multiobjective unified power quality conditioner,” *IEEE Trans. Ind Electron.*, vol. 71, no. 1, pp. 59–70, Jan. 2024.

[8] P. Ray, P. K. Ray, P. S. Puhan, and M. L. T. K. Liyanage, “Performance improvement of microgrid with strategic control of distributed energy resources integrated UPQC,” *IEEE Trans. Ind. Appl.*, vol. 61, no. 3, pp. 4695–4705, May/Jun. 2025.

[9] C. D. Sanjenbam and B. Singh, “Power quality enhancement of synchronous reluctance generator based standalone distributed system utilizing universal active filter,” *IEEE Trans. Ind. Appl.*, vol. 61, no. 3, pp. 4971–4981, May/Jun. 2025.

[10] Y. Peng, X. Huang, S. Xie, and F. Zhong, “Advanced single-phase to three-phase power conversion systems for medium and low voltage single-phase AC systems in remote areas,” *IEEE Trans. Ind Electron.*, vol. 72, no. 6, pp. 5857–5866, Jun. 2025.

[11] Z. Li, R. Yang, Y. Zhou, C. Wang, and Z. Wang, “A unified framework for adaptive and flexible phase angle regulation in single-phase UPQC,” *IEEE Trans. Power Electron.*, vol. 40, no. 9, pp. 12779–12793, Sep. 2025.

[12] *IEEE Standard for Measurement and Limits of Voltage Fluctuations and Associated Light Flicker On AC Power Systems*, IEEE Std 1453-2022, 2022.

[13] A. M. Aboutaleb, J. Desmet, and J. Knockaert, “A novel active power filter for supraharmonic emissions of single phase grid-connected inverters,” *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 8109–8124, Jun. 2025.

[14] G. Wang, Y. Jiang, Z. Liu, Y. Ma, and J. Wang, “Predictive direct control of nine-switch converter unified power quality conditioner based on time-sharing cooperative control,” *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 5895–5906, Apr. 2025.

[15] X. Zhao, H. Dang, M. Li, X. Wang, H. Ding, and X. Guo, “Performance enhancement for unified power quality conditioner using passivity fractional-order sliding mode control,” *IEEE Trans. Consum. Electron.*, vol. 71, no. 2, pp. 2675–2688, May 2025.

[16] P. Ray, P. K. Ray, B. P. Behera, and N. Singh, “An ANF cascaded normalized-CF-SOHO based control approach and analysis of PV-UPQC under highly non-ideal grid and load conditions,” *IEEE Trans. Ind. Appl.*, vol. 60, no. 5, pp. 7757–7770, Sep./Oct. 2024.

[17] W. Jia, Q. Guo, C. Tu, F. Jiang, L. Wang, and Y. Hou, “Improved single-phase UPQC with integrating auxiliary capacitor for power rating reduction,” *IEEE Trans. Ind Electron.*, vol. 70, no. 9, pp. 9091–9102, Sep. 2023.

[18] H. Nourmohamadi, G. Gohil, and P. T. Balsara, “Intelligent multi-functional fault current limiter,” *IEEE Trans. Smart Grid*, vol. 15, no. 3, pp. 2434–2446, May 2024.

[19] J. T. Cardoso, C. B. Jacobina, P. L. S. Rodrigues, and A. M. N. Lima, “Single-phase AC-DC-AC multilevel five-leg converter based on a high-frequency transformer,” *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6288–6299, Sep./Oct. 2023.

[20] M. Lu, M. Qin, W. Mu, J. Fang, and S. M. Goetz, “A hybrid gallium-nitride–silicon direct-injection universal power flow and quality control circuit with reduced magnetics,” *IEEE Trans. Ind Electron.*, vol. 71, no. 11, pp. 14161–14174, Nov. 2024.

[21] R. P. de Lacerda, C. B. Jacobina, E. L. L. Fabricio, A. S. Felinto, and J. T. Cardoso, “Single-phase AC-DC-AC multilevel five-leg converter with high-frequency link,” *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 3504–3519, May/Jun. 2023.

[22] J. T. Cardoso, C. B. Jacobina, A. S. Felinto, and M. Beltrão de Rossiter Corrêa, “Three-phase four-wire transformerless unified power quality conditioner based on AC-DC-AC nine-leg converter and shunt converter,” *IEEE Trans. Ind. Appl.*, vol. 61, no. 1, pp. 395–405, Jan./Feb. 2025.

[23] C. Jiang, C. Yuan, F. Wang, and S. Zhang, “Coordinated direct power strategy based active disturbance rejection control for MMC-UPQC,” *IEEE Trans. Ind Electron.*, vol. 72, no. 11, pp. 11778–11790, Nov. 2025.

[24] W. R. N. Santos, E. de Moura Fernandes, E. R. C. da Silva, C. B. Jacobina, A. C. Oliveira, and P. M. Santos, “Transformerless single-phase universal active filter with UPS features and reduced number of electronic power switches,” *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4111–4120, Jun. 2016.

[25] Y. Lu, G. Xiao, X. Wang, F. Blaabjerg, and D. Lu, “Control strategy for single-phase transformerless three-leg unified power quality conditioner based on space vector modulation,” *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2840–2849, Apr. 2016.

[26] R. M. Abdalaal, C. N. M. Ho, C. K. Leung, and H. S.-H. Chung, “A remotely central dimming system for a large-scale LED lighting network providing high quality voltage and current,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5455–5465, Sep./Oct. 2019.

[27] R. M. Abdalaal and C. N. M. Ho, “Analysis and validations of modularized distributed TL-UPQC systems with supervisory remote management system,” *IEEE Trans. Smart Grid*, vol. 12, no. 3, pp. 2638–2651, May 2021.

[28] R. M. Abdalaal and C. N. M. Ho, “System modeling and stability analysis of single-phase transformerless UPQC integrated input grid voltage regulation,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 670–682, Jul. 2022.

[29] W. Xu, W. Zhu, and Z. Shu, “Suppression of DC voltage ripple impact on non-isolated single-phase half-bridge unified power quality conditioner,” *IEEE Trans. Ind Electron.*, vol. 71, no. 9, pp. 10523–10532, Sep. 2024.

[30] V. S.-P. Cheung, R. S.-C. Yeung, H. S.-H. Chung, A. W.-L. Lo, and W. Wu, “A transformer-less unified power quality conditioner with fast dynamic control,” *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3926–3937, May 2018.

[31] S. Wang, C. Tang, J. Nie, L. Meng, and Z. Shu, "4-vector SVPWM for single-phase transformerless UPQC with two-leg and low DC voltage," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 98–104, Jan. 2025.

[32] W. Fu, Q. Wang, W. Hua, M. Cheng, and G. Buja, "A novel single-phase transformerless TC-UPQC with reduced DC-link voltage," *IEEE Trans. Power Electron.*, vol. 40, no. 5, pp. 7200–7214, May 2025.

[33] *IEEE Standard for Harmonic Control in Electric Power Systems*, IEEE Std 519-2022, 2022.

[34] Y. Yuan and Z. Zhang, "A single-phase vienna rectifier with wide output voltage range," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 3, pp. 3884–3895, Sep. 2022.

[35] J. Wang, H. Zhao, P. Wang, and Y. Gui, "Characterization of impedance and stability for doubly-fed induction generator based on voltage-modulated direct power control," *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 15529–15544, Oct. 2025.

[36] S. K. Yadav, A. Patel, and H. D. Mathur, "Study on comparison of power losses between UPQC and UPQC-DG," *IEEE Trans. Ind. Appl.*, vol. 58, no. 6, pp. 7384–7395, Nov./Dec. 2022.

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