A Novel Push–Pull Class-E Inverter With Low-Harmonic Constant Current Output

Xiao Zheng, Chenwen Cheng, Meng Song, *Senior Member, IEEE*, Fei Teng, and Wei Hua, *Senior Member, IEEE*

***Abstract*—This article presents a novel push–pull Class-E inverter that can achieve zero voltage switching (ZVS) and deliver a low-harmonic ac constant-current (CC) output. Building upon the single-switch CC Class-E inverter, a new push–pull topology configuration is introduced in this research. With the proposed push–pull structure, the inverter's output current exhibits low harmonics. As a result, no additional filter is required at the output terminal, which effectively mitigates the issues of output current distortion and excessive losses. To verify the theoretical analysis, a 3.33-MHz circuit prototype was developed. Experimental results confirm that load-independent ZVS is consistently achieved for both power switches. The output current deviation remains below 3% under varying load conditions with low distortion. The inverter outputs a maximum output power of 121.1 W with an input dc voltage of 48 V, whereas a peak efficiency of 94.7% occurs at an output power of 64.1 W.**

***Index Terms*—Constant current (CC), high-frequency converter, load-independent, push–pull Class-E inverter, zero voltage switching (ZVS).**

I. Introduction

HIGH-FREQUENCY MHz power converters are extensively studied for their advantages in high power density, particularly in medium and low-power applications where device size is crucial [1], [2], [3]. Class-E inverters are widely used in high-frequency applications due to their ability to implement soft switching, which reduces switching losses and electromagnetic interference (EMI) [4], [5], [6]. While traditional Class-E inverters can achieve zero voltage switching (ZVS) and zero voltage derivative switching, they are less suitable for applications with varying loads [7]. Load-independent Class-E inverters, which can maintain ZVS across a wide load range and provide a constant voltage (CV) output, are more appropriate for load-varying scenarios [8], [9]. In Class-E inverters, the output waveform is customarily modeled as a pure fundamental component that is completely free of harmonics. This assumption is usually achieved by employing an output filter [10]. However, the harmonics cannot be eliminated by the output due to the filtering bandwidth. If harmonics are present in the output branch, they will not only cause additional losses but also affect the waveform of the switch voltage [11]. Therefore, the design of the output filter is significant for the inverters, especially in applications that require low-harmonic output [12], [13].

To reduce the total harmonic distortion (THD) of the output and simplify the filter design, Class-E inverters can be configured in a push–pull structure [13]. This configuration offers advantages for enhancing efficiency and reducing EMI. Moreover, the dual-switch configuration enables push–pull inverters to handle higher power levels. A complementary Class-E power amplifier was proposed in [14] based on the traditional Class-E power amplifier, effectively reducing the THD of the output signal. A push–pull Class-E power amplifier with a simplified output circuit design was put forward in [15]. It did not use a filtering network at the output end, yet the third harmonic is relatively large. It was proposed in [16] that adding a differential capacitor on the output side can improve the efficiency of the push–pull Class-E inverter. In [17], parallel push–pull Class-E inverters were used to achieve 3 kW and 3.39 MHz power transfer in a wireless power transfer (WPT) system. In [18], multiple inverter cells were employed to further enhance the power level of the high-frequency WPT system, realizing 9 kW and 3.47 MHz power transfer, which is applicable to industrial applications in the multi-kW range. The CV output push–pull Class-E inverter was studied in [19]. With the magnetic coupling design of the two input inductors, the input current ripple was reduced. Subsequently, the magnetic design of the input inductors was further optimized in [20].

In addition to Class-E inverters, various single-switch inverters with different characteristics have been widely developed [21], [22], [23], [24]. The push–pull structure can also be applied to other single-switch topologies. The push–pull Class-E/F_3 power amplifier was investigated in [25]. The push–pull structure and the harmonic suppression circuit were jointly used to achieve harmonic suppression. The push–pull Class-E_M power amplifier was explored in [26], where the push–pull structure was utilized to reduce the output harmonics and increase the output power. The push–pull class-Φ_2 topology was studied in [27]. The circulating current was reduced through a T network,

Received 9 July 2025; revised 14 October 2025 and 8 November 2025; accepted 16 November 2025. Date of publication 21 November 2025; date of current version 25 February 2026. This work was supported by the National Key R∓D Program of China under Grant 2024YFE0209900. Recommended for publication by Associate Editor J. Lam. *(Corresponding author: Chenwen Cheng.)*

Xiao Zheng, Chenwen Cheng, Meng Song, and Wei Hua are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: chenwen_cheng@seu.edu.cn).

Fei Teng is with the Department of Electrical and Electronic Engineering, Imperial College London, SW7 2AZ London, U.K. (e-mail: f.teng@imperial.ac.uk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3635469.

Digital Object Identifier 10.1109/TPEL.2025.3635469

TABLE I
DIFFERENT TYPES OF HIGH-FREQUENCY PUSH–PULL TOPOLOGIES

Research	Topology	Output	Frequency (MHz)	Maximum power (W)	Maximum efficiency (%)
[16]	Class-E	-	1	355	93.7
[19]	Class-E	CV	3	350	95.2
[25]	Class-E/F_3	-	10.5	15.3	91.3
[26]	Class-E_M	-	1	24.4	94.1
[27]	Class-Φ_2	CV	6.78	300	96
This work	Class-E	CC	3.33	121.1	94.7

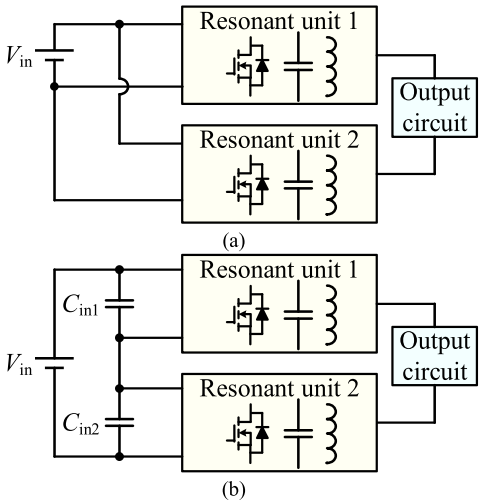

Fig. 1. Structure of high-frequency push–pull inverter. (a) Standard configuration. (b) Series-stacked configuration.

and the switching voltage stress was lowered by using a series-stacked structure. Later, this topology was applied to a WPT system in [28]. A summary of various topologies is presented in Table I.

Existing studies on push–pull topologies have employed the configuration shown in Fig. 1. Two resonant units are combined with a switching phase difference of π, effectively eliminating even-order harmonics from the output voltage and ultimately achieving a low-harmonic output. Specifically, Fig. 1(a) shows the commonly used structure, whereas Fig. 1(b) shows a series-stacked structure. The series-stacked structure can reduce the switch voltage stress, making it suitable for high-input-voltage scenarios. The existing push–pull inverters exhibit relatively low output harmonics. However, in scenarios where extremely low harmonics are required, filters are still necessary. Moreover, as shown in Table I, in the current research on push–pull topologies, there is no type with a constant-current (CC) output. In specific applications, CC output is required [29]. While a passive network can convert a CV output to a CC output, it necessitates additional passive components, resulting in increased volume and power losses [30]. Although a CC Class-E inverter based on a parallel resonant network was proposed in [31], this topology is not applicable to the existing push–pull structure.

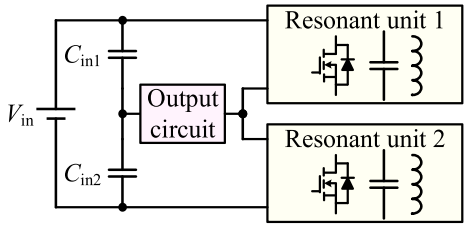

Fig. 2. Proposed push–pull Class-E inverter structure.

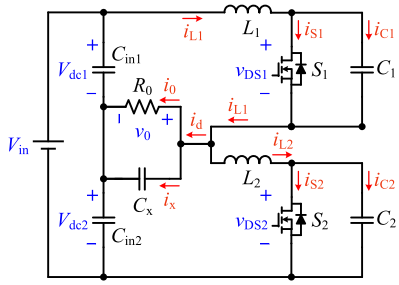

Fig. 3. Topology of the proposed push–pull CC Class-E inverter.

This article proposes a novel push–pull topology, as shown in Fig. 2. Based on the series-stacked push–pull Class-E inverter, the output circuit is redesigned to filter the current of the resonant inductor, thereby achieving a CC output. Compared with previous push–pull topologies, the proposed topology in this article has two notable features. First, it can provide a CC output, which is well-suited for applications requiring a CC source. Second, it offers an output with lower harmonics. Within a reasonable parameter design range, the harmonic content of the inverter's output current is so small that a low-THD output can be achieved without the need for a filtering network at the output end. This reduces the number of passive components and additional circulating current losses. Moreover, due to the adoption of the push–pull and series-stacked structures, this topology is more suitable for applications with higher input voltages and larger output powers than a single Class-E inverter. The proposed inverter shows promise for applications in high-frequency WPT systems, high-frequency induction heating, ultrasonic transducer drivers, and power amplifiers, among other areas.

This article begins with an analysis of the circuit description and modeling of the proposed topology. Then the circuit characteristics are analyzed, including the switch stress, output THD analysis, and load characteristic analysis. Finally, the circuit parameter design procedure is outlined, and a 3.33-MHz, 121.1-W prototype was fabricated for validation and analysis.

II. CIRCUIT DESCRIPTION AND MODELING

A. Topology and Equivalent Circuit

The topology of the proposed push–pull Class-E inverter is shown in Fig. 3. The inverter comprises a dc input voltage source V_{in}, two Class-E resonant units, two dc capacitors C_{in1} and

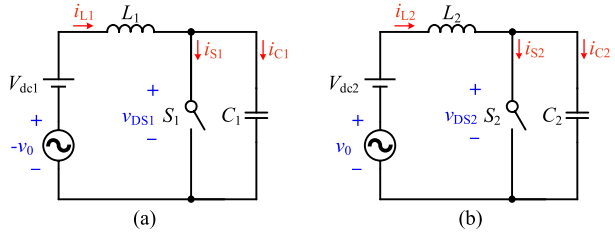

Fig. 4. Equivalent circuit for two resonant units. (a) Unit 1. (b) Unit 2.

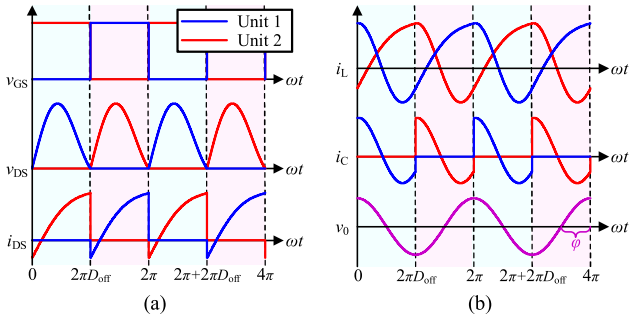

Fig. 5. Operation waveforms. (a) Waveforms of the driving voltage v_{GS}, the switch voltage v_{DS}, and the switch current i_{DS}. (b) Waveforms of the inductor current i_L, the capacitor current i_C, and the output voltage v_0.

C_{in2}, a compensating capacitor C_x, and an output resistor R_0. The passive parameters of the two resonant units are identical, specifically $L_1 = L_2$ and $C_1 = C_2$. C_{in1} and C_{in2} can be equivalently treated as dc voltage sources V_{dc1} and V_{dc2}. The switching frequencies and duty cycles of S_1 and S_2 are identical, with their driving signals having a phase difference of π. The output circuit can be modeled as a sine voltage source since the current through R_0 is a constant fundamental wave with low harmonic distortions, which will be explained later. Assuming all components are ideal, the equivalent circuit diagram of each resonant unit is shown in Fig. 4.

The duty cycle of the switch-off time is denoted by D_{off}, the switch frequency is represented by f, and the angular frequency is $\omega = 2\pi f$. S_1 is ON when $0 \le \omega t < 2\pi D_{off}$, and OFF when $2\pi D_{off} \le \omega t \le 2\pi$, whereas S_2 is ON when $\pi \le \omega t < 2\pi D_{off}+\pi$, and OFF when $2\pi D_{off}+\pi \le \omega t \le 3\pi$. The key waveforms under ideal operating conditions are shown in Fig. 5, where v_{GS} represents the driving signal of the switch. The switch turns on when v_{GS} is at a high level, and vice versa. v_{DS} denotes the voltage across the switch, while i_L indicates the current flowing through the inductor. The blue and red curves correspond to the waveforms in resonant Unit 1 and Unit 2, respectively. The signal waveforms in both resonant units are identical but exhibit a phase difference of π. The expression for the output voltage v_0 is

$$v_0 = V_0 \sin(\omega t + \varphi) \tag{1}$$

where φ is the phase of v_0.

As shown in Fig. 4, the equivalent circuit structures of the two resonant units are the same. Therefore, it is only necessary to analyze the working principle of one of them. Taking resonant Unit 1 as an example, in Fig. 5, it can be observed that it has two

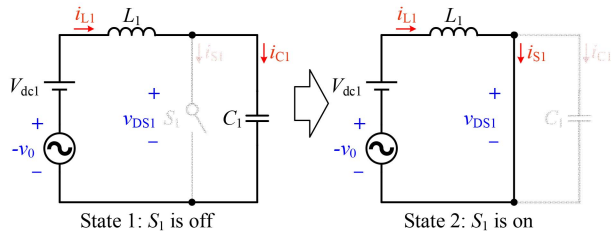

Fig. 6. State transition diagram of Unit 1.

states: S_1 is in the ON and OFF states. Based on Figs. 4 and 5, its switching modes are shown in Fig. 6.

B. Modeling of the Class-E Resonant Unit

In the following, the resonant Unit 1 will be analyzed in detail. The analysis of the Class-E resonant unit can be divided into two steps. First, the circuit response expressions are obtained by analyzing the switching modes. Second, based on the derived expressions and combined with Fourier analysis, the solutions that meet the load-independent conditions are found. A comprehensive analysis of a single Class-E resonant unit has been previously documented, such as in [7] and [31]. Hence, some conclusions from these references will be adopted here.

By analyzing the circuit modes during the turn-ON and turn-OFF states of S_1, the circuit equations can be formulated. Subsequently, the expressions for v_{DS1} and i_{L1} can be obtained as follows [7]:

$$v_{DS1}(\omega t) = \begin{cases} V_{dc1} + A\cos(q\omega t) + B\sin(q\omega t) \\ +\frac{q^2}{1-q^2}V_0\sin(\omega t+\varphi), & 0 \le \omega t \le 2\pi D_{off} \\ 0, & 2\pi D_{off} < \omega t \le 2\pi \end{cases} \tag{2}$$

$$i_{L1}(\omega t) = \begin{cases} \omega C_1 \frac{dv_{DS1}(\omega t)}{d\omega t}, & 0 \le \omega t \le 2\pi D_{off} \\ i_{L1}(2\pi D_{off}) + \\ \frac{1}{\omega L_1}\begin{bmatrix} V_{dc1}\omega t + V_0\cos(\omega t+\varphi) \\ -V_0\cos\varphi \end{bmatrix}, & 2\pi D_{off} < \omega t \le 2\pi \end{cases} \tag{3}$$

where

$$A = \frac{q^2}{q^2-1}V_0\sin\varphi - V_{dc1} \tag{4}$$

$$B = -\frac{\csc^2(\pi D_{off} q)}{2(q^2-1)}\begin{bmatrix} \sin(2\pi D_{off} q)\begin{pmatrix} V_{dc1} - q^2 V_{dc1} \\ +q^2 V_0\sin\varphi \end{pmatrix} \\ -2q^3 V_0\sin(\pi D_{off})\sin(\pi D_{off}+\varphi) \\ -2\pi(1-D_{off})\,q\,(q^2-1)\,V_{dc1} \end{bmatrix} \tag{5}$$

$$q = \frac{1}{\omega\sqrt{L_1 C_1}} = \frac{1}{\omega\sqrt{L_2 C_2}}. \tag{6}$$

The Class-E resonant unit should satisfy load-independent ZVS and CC output conditions. The load-independent ZVS

condition is as follows:

$$v_{\mathrm{DS1}}\left(2\pi D_{\mathrm{off}}\right)=0. \tag{7}$$

A CC output can be obtained by filtering the inductor current i_{L1}. The fundamental component of i_{L1} is not load-independent, but it can be decomposed into a load-independent quantity and a load-dependent quantity. The load-independent quantity can be designed to be extracted as the CC output. For the load-dependent part, a compensation capacitor needs to be designed to ensure that this current does not flow through the output resistor. The fundamental component $i_{\mathrm{L1\_1}}$ of the current i_{L1} can be expanded based on the phase angle φ as follows:

$$\begin{aligned} i_{\mathrm{L1\_1}}\left(\omega t\right) &= i_1\left(\omega t\right)+i_{1\mathrm{x}}\left(\omega t\right) \\ &= I_1\sin\left(\omega t+\varphi\right)+I_{1\mathrm{x}}\cos\left(\omega t+\varphi\right) \end{aligned} \tag{8}$$

where i_1 is the fundamental sine component of i_{L1}, and $i_{1\mathrm{x}}$ is the fundamental cosine component of i_{L1}. i_1 can be designed to be a CC output, and $i_{1\mathrm{x}}$ flows through the compensation capacitor.

I_1 and $I_{1\mathrm{x}}$ can be calculated by the following two equations:

$$I_1=\frac{1}{\pi}\int_0^{2\pi} i_{\mathrm{L1}}\left(\omega t\right)\sin\left(\omega t+\varphi\right)d\omega t \tag{9}$$

$$I_{1\mathrm{x}}=\frac{1}{\pi}\int_0^{2\pi} i_{\mathrm{L1}}\left(\omega t\right)\cos\left(\omega t+\varphi\right)d\omega t. \tag{10}$$

V_0 is related to the load. Taking V_0 as the load parameter, the load-independent CC condition is as follows:

$$\frac{\partial I_1}{\partial V_0}=0. \tag{11}$$

From (7) and (11), the solutions that satisfy the load-independent conditions are obtained as follows:

$$\tan\left[\pi\left(D_{\mathrm{off}}-1\right)q\right]=\pi D_{\mathrm{off}}q \tag{12}$$

$$\varphi=\left(1-D_{\mathrm{off}}\right)\pi. \tag{13}$$

Equation (12) is an equation involving q and D_{off}. By utilizing (12), q can be determined.

Then, $i_{\mathrm{L1\_1}}$ can be derived as

$$\begin{aligned} i_{\mathrm{L1\_1}}\left(\omega t\right) &= \tfrac{g\left(D_{\mathrm{off}}\right)}{\omega L_1}V_{\mathrm{dc1}}\sin\left(\omega t+\varphi\right) \\ &+\tfrac{h\left(D_{\mathrm{off}}\right)+1}{\omega L_1}V_0\cos\left(\omega t+\varphi\right) \end{aligned} \tag{14}$$

where

$$g\left(D_{\mathrm{off}}\right)=\frac{2}{\pi\left(q^2-1\right)}\begin{bmatrix} q^2\sin\left(\pi D_{\mathrm{off}}\right) \\ -\pi\left(D_{\mathrm{off}}-1\right)q^2\cos\left(\pi D_{\mathrm{off}}\right)\end{bmatrix} \tag{15}$$

$$\begin{aligned} h\left(D_{\mathrm{off}}\right) &= \tfrac{q^2}{2\pi\left(q^2-1\right)^2} \\ &\cdot\begin{bmatrix} -2\pi D_{\mathrm{off}}\left(q^2-1\right) \\ +\left(q^2+1\right)\sin\left(2\pi D_{\mathrm{off}}\right) \\ -4q\sin^2\left(\pi D_{\mathrm{off}}\right)\cot\left(\pi D_{\mathrm{off}}q\right)\end{bmatrix}. \end{aligned} \tag{16}$$

Through the above analysis, the solutions for Unit 1 that satisfy the load-independent conditions are obtained.

C. Modeling of the CC Output Push–Pull Class-E Inverter

In the previous subsection, the working principle of a single Class-E resonant unit was analyzed. For the equivalent circuit shown in Fig. 4(b), the solving process is the same as above. Then, the working principle of a push–pull operation mode formed by two Class-E resonant units through a series-stacking structure is explained as follows.

Based on the principle of power conservation, Unit 1 and Unit 2 satisfy the following equations, respectively,

$$\frac{V_0 I_1}{2}=V_{\mathrm{dc1}}I_{\mathrm{L1\_0}} \tag{17}$$

$$\frac{V_0 I_2}{2}=V_{\mathrm{dc2}}I_{\mathrm{L2\_0}} \tag{18}$$

where I_2 represents the sine component amplitude of i_{L2}, and $I_{\mathrm{L1\_0}}$ and $I_{\mathrm{L2\_0}}$ are the dc components of i_{L1} and i_{L2}, respectively.

When V_{dc1} and V_{dc2} are stable, the following condition holds:

$$I_{\mathrm{L1\_0}}=I_{\mathrm{L2\_0}}. \tag{19}$$

From (17)–(19), (20) can be obtained

$$V_{\mathrm{dc1}}=V_{\mathrm{dc2}}=\frac{1}{2}V_{\mathrm{in}}. \tag{20}$$

Then, i_{L2} can be expressed as

$$i_{\mathrm{L2}}\left(\omega t\right)=i_{\mathrm{L1}}\left(\omega t+\pi\right). \tag{21}$$

Since i_{d} is a differential signal between Unit 1 and Unit 2, the fundamental component of i_{d} is the sum of the fundamental components of i_{L1} and i_{L2}.

$$\begin{aligned} i_{\mathrm{d\_1}}\left(\omega t\right) &= i_{\mathrm{L1\_1}}\left(\omega t\right)+i_{\mathrm{L2\_1}}\left(\omega t\right) \\ &= \frac{g\left(D_{\mathrm{off}}\right)}{\omega L_1}V_{\mathrm{in}}\sin\left(\omega t+\varphi\right) \\ &+\frac{2\left[h\left(D_{\mathrm{off}}\right)+1\right]}{\omega L_1}V_0\cos\left(\omega t+\varphi\right). \end{aligned} \tag{22}$$

It can be seen from (22) that the sine component of i_{d} is independent of the load, which is the constant current i_0.

$$I_0=\frac{g\left(D_{\mathrm{off}}\right)}{\omega L_1}V_{\mathrm{in}}. \tag{23}$$

The cosine component is compensated by the design of the compensating capacitor C_{x}, so C_{x} can be calculated as

$$C_{\mathrm{x}}=\frac{2\left[h\left(D_{\mathrm{off}}\right)+1\right]}{\omega L_1}. \tag{24}$$

Usually, the power metal–oxide–semiconductor field-effect transistors (MOSFETs) are used as switches S_1 and S_2. They typically can only withstand unidirectional voltage, which imposes a requirement to limit the maximum output power [10]. The maximum output power $P_{0\max}$ is

$$P_{0\,\max}=\frac{\pi q^2\left(D_{\mathrm{off}}-1\right)^2{V_{\mathrm{in}}}^2}{2\omega L_1}. \tag{25}$$

In the above, a detailed analysis of the modeling and working principle of the proposed inverter is conducted, which lays a foundation for the subsequent analysis of the circuit characteristics.

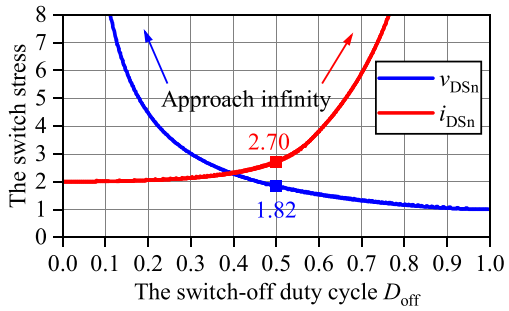

Fig. 7. Variations of the normalized switch voltage stress and current stress with D_{off}.

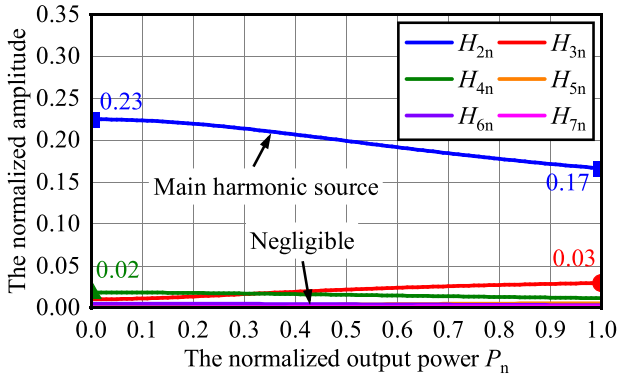

Fig. 8. Normalized amplitude of the mth harmonic H_{mn} versus the normalized power P_n at $D_{off} = 0.5$.

III. Circuit Characteristics

A. Voltage and Current Stresses

The normalized voltage stress v_{DSn} and current stress i_{DSn} of the circuit are defined by the following two equations, respectively:

$$v_{DSn} = \frac{v_{DS1max}}{V_{in}} \tag{26}$$

$$i_{DSn} = \frac{i_{DS1max}}{I_{L1\_0}} \tag{27}$$

where v_{DS1max} represents the maximum value of v_{DS1}, and i_{DS1max} represents the maximum value of i_{DS1}.

Based on (2)–(6), (26), and (27), the values of v_{DSn} and i_{DSn} can be computationally determined. Calculations confirm that both v_{DSn} and i_{DSn} depend on D_{off}. The variations of v_{DSn} and i_{DSn} with D_{off} are shown in Fig. 7.

As shown in Fig. 7, the switch voltage stress decreases with an increasing D_{off}, whereas the current stress exhibits an opposite varying trend. The proposed topology effectively halves the voltage stress across each switch compared to conventional single-switch topologies, owing to its series-stacked configuration. Specifically, when $D_{off} = 0.5$, the voltage stress is 1.82 and the current stress is 2.70.

The power-output capability c_p of the switch takes into account both the voltage stress and the current stress, which reflects the utilization rate of the switch. The push–pull topology exhibits identical power-output capacity to single-switch configurations, demonstrating equivalent switch utilization efficiency between the two architectures. For the Class-E inverter, the maximum power-output capacity of 0.102 occurs when $D_{off} = 0.49$. Thus, during circuit design, D_{off} should be set near 0.5 [7].

B. Harmonic Analysis and Comparison

In the analysis above, it was assumed that the distortion in i_0 is small enough. The following analysis focuses on the THD of i_d to validate this assumption. Additionally, a comparison is made between the THD of i_d and the output waveform of other Class-E inverters before filtering.

The amplitude of the mth harmonic in i_{L1} is defined as

$$H_m = \frac{1}{\pi}\sqrt{\left[\int_0^{2\pi} i_d(\omega t)\sin(m\omega t)\,d\omega t\right]^2 + \left[\int_0^{2\pi} i_d(\omega t)\cos(m\omega t)\,d\omega t\right]^2}. \tag{28}$$

Based on (28), the harmonic components of each order of i_{L1} can be calculated. The normalized amplitude of the mth harmonic is defined as

$$H_{mn} = \frac{H_m}{H_1}. \tag{29}$$

The normalized power of the circuit is defined as

$$P_n = \frac{P_0}{P_{0\,max}}. \tag{30}$$

The output harmonics of the Class-E inverter beyond the seventh are small enough and can be neglected [12]. Through calculation and simplification using (28)–(30), harmonic variations versus normalized power at $D_{off} = 0.5$ are shown in Fig. 8.

It can be seen from Fig. 8 that H_{2n} is significantly larger than the others, and H_{5n}, H_{6n}, and H_{7n} are negligible. H_{2n} decreases as P_n increases, with a maximum value of 0.23 and a minimum value of 0.17. H_{3n} increases as P_n increases, reaching a maximum of 0.03. H_{4n} decreases as P_n increases, with a maximum value of 0.02. The analysis shows that the second-order harmonic accounts for the vast majority of the harmonics in i_{L1}, which should be removed to reduce the THD of the load current. The proposed push–pull structure constructs a differential current branch, which ensures that the current i_d is free of even-order harmonics. Since there are no even-order harmonics in i_d, the THD of i_d can be calculated as

$$\mathrm{THD} = \sqrt{{H_{3n}}^2 + {H_{5n}}^2 + {H_{7n}}^2} \times 100\%. \tag{31}$$

Calculated by (31), the variation trends of the THD of i_d with the turn-OFF duty cycle D_{off} under different load conditions are shown in Fig. 9(a). Similarly, the THDs of the output waveforms of other Class-E inverters are also influenced by their normalized power and duty cycle, as shown in Fig. 9.

Fig. 9(a) shows how the THD of i_d varies with D_{off} under low, medium, and full load conditions. From Fig. 9(a), it is evident that the THD of the CC push–pull Class-E inverter remains below 3% across the most load range when D_{off} is greater than 0.5. Considering both c_p and THD, a D_{off} value between 0.5 and 0.6 is preferable.

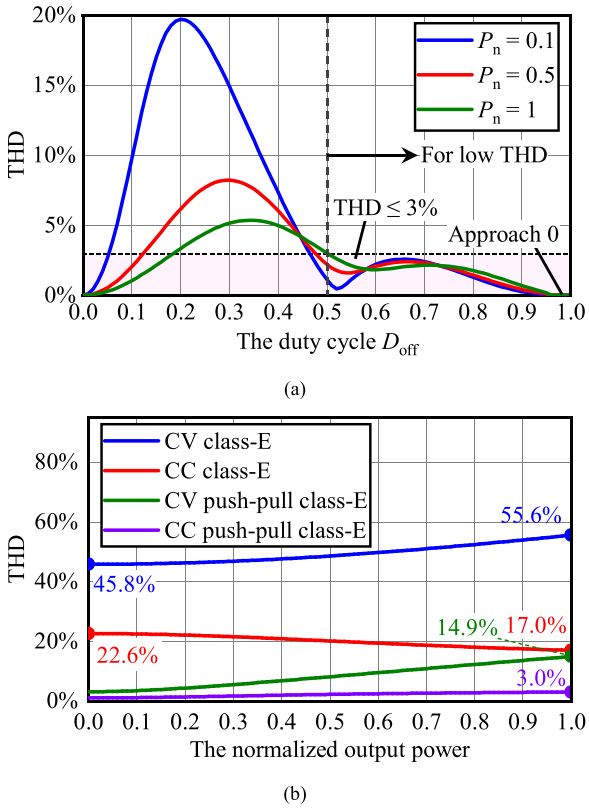

Fig. 9. Theoretical THDs of the output waveform of Class-E inverters vary with the normalized power and duty cycle before filtering. (a) THD versus D_{off} when the CC push–pull Class-E under different loads. (b) THD versus normalized power when the Class-E inverters at $D_{off} = 0.5$.

Fig. 9(b) shows the variation of THD with normalized power for different Class-E inverters in [8], [31], and [19] at $D_{off} = 0.5$. It can be observed that the THD of other Class-E inverters is significantly higher than that of the CC push–pull Class-E inverter, indicating that the other inverters require output filter design. In contrast, the CC push–pull Class-E inverter demonstrates excellent low harmonic performance. Additionally, the capacitor C_x has a filtering effect, further reducing harmonics in i_0. Therefore, when D_{off} exceeds 0.5, i_0 can be approximated as distortion-free, eliminating the need for additional filtering at the output.

C. Load Characteristic

Based on theoretical analysis, the inverter operates under ideal conditions only when driving a purely resistive load. Deviation from resistive load characteristics disrupts optimal operation. The impact of load characteristics on inverter performance is analyzed below to guide the circuit design.

When the load is nonresistive, the phase angle φ of the equivalent voltage source v_0 in Fig. 4 no longer satisfies (13). Consequently, the circuit no longer satisfies the load-independent ZVS and CC output conditions. For inductive loads, φ increases, while for capacitive loads, φ decreases. Assuming that all circuit parameters except φ remain constant, (7) is solved by varying φ to analyze whether the circuit can achieve ZVS. When φ increases, (7) has no solution, meaning that the circuit fails to meet ZVS. When φ decreases, a value of D_{off} that satisfies (7) can be obtained. Nevertheless, the obtained D_{off} no longer meets (12) but is smaller than the value in (12). In this situation, v_{DS} drops to zero before the switch turns on, and then the body diode of the MOSFET conducts. Combined with simulations for analysis, Fig. 10 can be obtained.

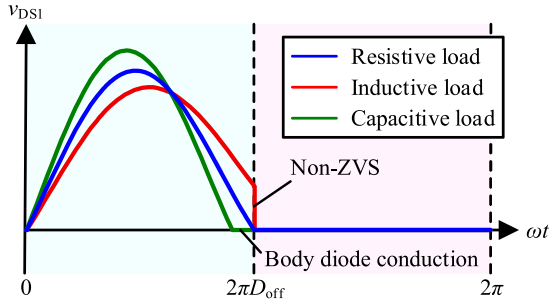

Fig. 10. Switch voltage waveforms under different load characteristics.

As can be seen from Fig. 10, there are three states of the switch voltage v_{DS} depending on the phase of v_0. When φ satisfies (13), it corresponds to a purely resistive load on the inverter, and v_{DS} drops to zero exactly at the moment the switch is turned ON. When φ is greater than the reference value in (13), it corresponds to an inductive load on the inverter. In this case, v_{DS} cannot drop to zero when the switch is turned ON, and the switch no longer meets the ZVS condition. When φ is less than the reference value in (13), it corresponds to a capacitive load on the inverter. v_{DS} drops to 0 before the switch is turned ON, and then the body diode of the switch starts to conduct, allowing the switch to still achieve ZVS.

Based on the above analysis, an inductive load will cause the inverter to lose its ZVS characteristic. Therefore, the output load of the inverter should be resistive or weakly capacitive to achieve ZVS.

IV. Experimental Validation

A. Parameter Design

In this subsection, the circuit design process is summarized, and specific numerical examples are provided for building the experimental circuits. The design flowchart is shown in Fig. 11.

1) The input voltage is chosen as $V_{in} = 48$ V. The inverter switching frequency is $f = 3.33$ MHz, and the maximum circuit transmission power is $P_{max} = 135$ W.
2) Considering the power-output capability of the switch and the output THD, $D_{off} = 0.49$ is selected. At this time, the power-output capability of the switch is maximized, and the maximum THD of i_d is about 3%.
3) Substitute $D_{off} = 0.49$ into (12) and solve for $q = 1.3094$. Based on (15) and (16), $g(D_{off})$ and $h(D_{off})$ are obtained as 1.6038 and 0.2486, respectively.
4) Calculate the resonant inductors L_1 and L_2 using (25) as 0.57 μH. Calculate the resonant capacitors C_1 and C_2 using (6) as 2.33 nF. Calculate the compensating capacitor C_x using (24) as 9.98 nF.

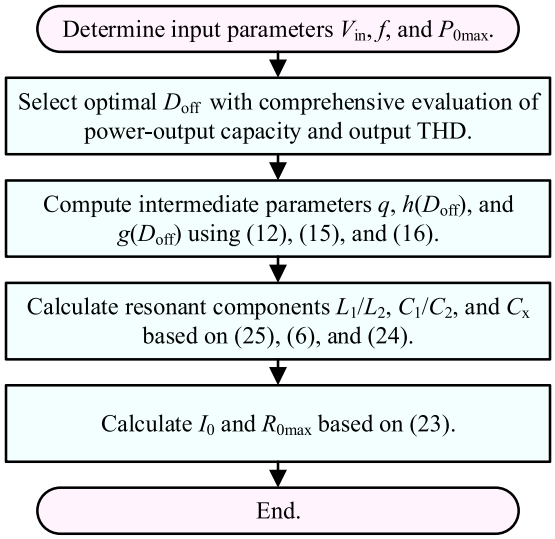

Fig. 11. Design flowchart of the proposed inverter.

TABLE II
CIRCUIT PARAMETERS AND THEIR THEORETICAL DESIGN VALUES

Parameters	Values	Parameters	Values
V_{in}	48 V	R_{0max}	6.5 Ω
f	3.33 MHz	L_1/L_2	0.57 μH
P_{0max}	135 W	C_1/C_2	2.33 nF
I_0	6.44 A	C_x	9.98 nF

5) Calculate the output current I_0 using (23) as 6.44 A. Calculate the maximum output resistance $R_{0\max}$ as follows:

$$R_{0\max} = \frac{2P_{0\max}}{I_0^2} = 6.5\Omega. \tag{32}$$

Then, all parameters in the circuit have been calculated. The parameters are listed in Table II.

B. Experimental Setup

A circuit prototype was constructed in accordance with the parameters listed in Table II for experimental verification. Fig. 12(a) shows the experimental system setup, whereas Fig. 12(b) shows the implemented inverter prototype along with its dimensional specifications.

The resonant inductors L_1 and L_2 are fabricated using ZnNi high-frequency magnetic cores with EEQ structure, wound with 2.5 mm copper wire. Inductances are precisely adjusted through turn-count optimization and air-gap tuning. All circuit capacitors employ multilayer ceramic capacitors, selected for their superior high-frequency performance. The parasitic capacitances of switches S_1 and S_2 are absorbed into parallel capacitors C_1 and C_2. Silicon MOSFETs (Infineon IPB339N20NM6) serve as power switches, driven by isolated gate signals generated from an external controller board with dedicated power supplies.

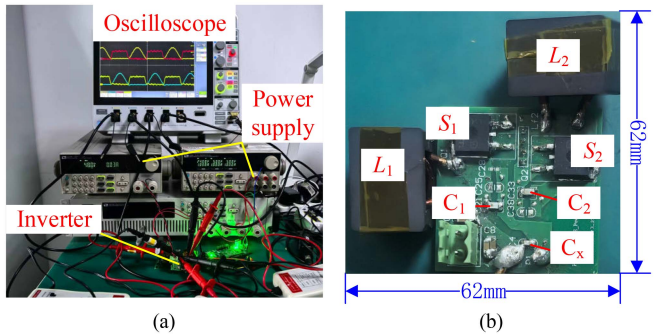

Fig. 12. Experimental platform. (a) Experimental setup. (b) Circuit prototype and its dimensions.

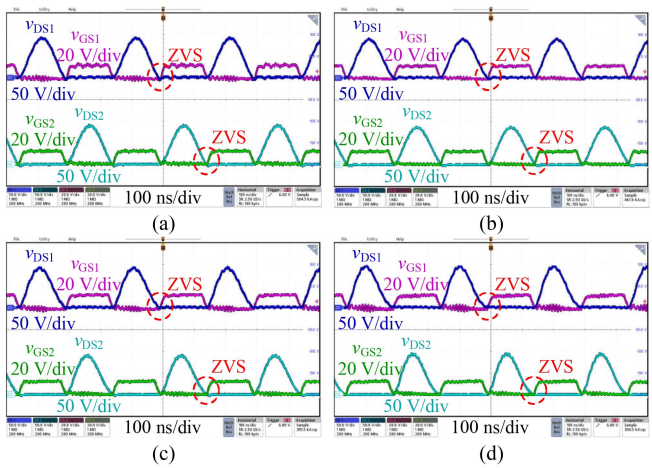

Fig. 13. Switch voltage and corresponding gate-drive signal waveforms under different load conditions. (a) No load ($P_0 = 0$). (b) Light load ($P_0 = 22.3$ W). (c) Medium load ($P_0 = 64.1$ W). (d) Heavy load ($P_0 = 102.8$ W).

C. Experimental Results

Fig. 13 shows the operational waveforms of the inverter under different load conditions. Each figure displays the drain-source voltage waveforms v_{DS1} and v_{DS2} and corresponding gate-drive signals v_{GS1} and v_{GS2} of both switches. The results confirm that ZVS can be achieved across the entire load range, as evidenced by the voltage collapse to zero before the switch turn-ON. Thus, the load-independent soft-switching capability of the proposed inverter is validated.

The output current waveforms under varying load conditions are shown in Fig. 14. Experimental current profiles were acquired using a Rogowski coil and systematically consolidated into unified graphical representations. As shown in Fig. 14, the output current traces over three cycles reveal a small amplitude difference as the output power varies from 22.3 to 121.1W, indicating that the CC output has been achieved.

The output current characteristics are evaluated through FFT analysis, with the fundamental amplitude and THD results shown in Fig. 15. The fundamental current amplitude decreases with increasing load, ranging from a maximum of 6.53 A to a minimum of 6.25 A, showing a maximum deviation of 2.9%. This small variation confirms effective CC output.

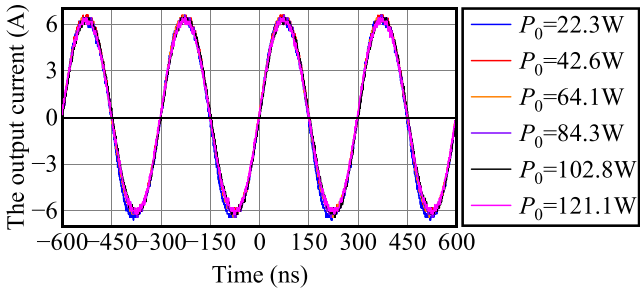

Fig. 14. Output current waveforms under different output powers.

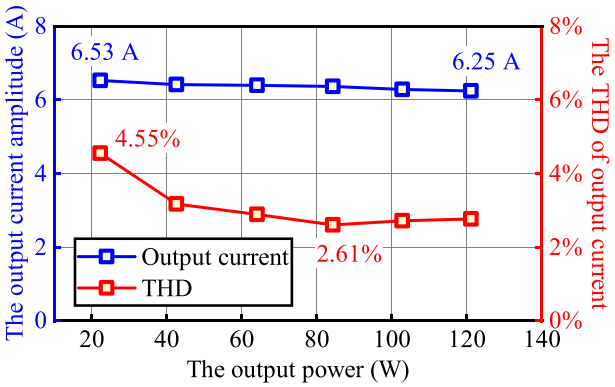

Fig. 15. FFT analysis results for the output current at different output power levels.

The THD inversely correlates with load power, achieving a minimum value of 2.61% at the output power of 84.3 W, demonstrating low harmonic distortion without additional filtering. Experimental observations revealed that stray inductance in the load resistance branch forms a parallel resonant circuit with compensation capacitor C_x, amplifying harmonic currents. This resonance effect results in elevated harmonic content in the output current, especially under low-resistance conditions.

Fig. 16 shows the low-frequency observed waveforms of the switch voltages v_{DS1} and v_{DS2}, as well as the output current i_0, along with their zoom-in waveforms. From Fig. 16, it can be observed that the operating state of the inverter is stable, with the switch voltages and output current remaining constant.

D. Efficiency and Loss Characterization Analysis

The output power and efficiency of the inverter were experimentally evaluated under varying load conditions, as shown in Fig. 17. The efficiency curve exhibits a nonmonotonic relationship with output power, initially increasing to a peak value of 94.7% at 64.1 W output power before gradually decreasing at higher power levels. Total system losses demonstrate a progressive upward trend with increasing output power, reaching a maximum value of 8.5 W under heavy-load operation.

The losses in the inverter can be categorized into four components: the loss of the resonant inductors, the loss of the resonant capacitors, the loss of the switches, and other losses. The detailed loss calculation process is outlined below [32].

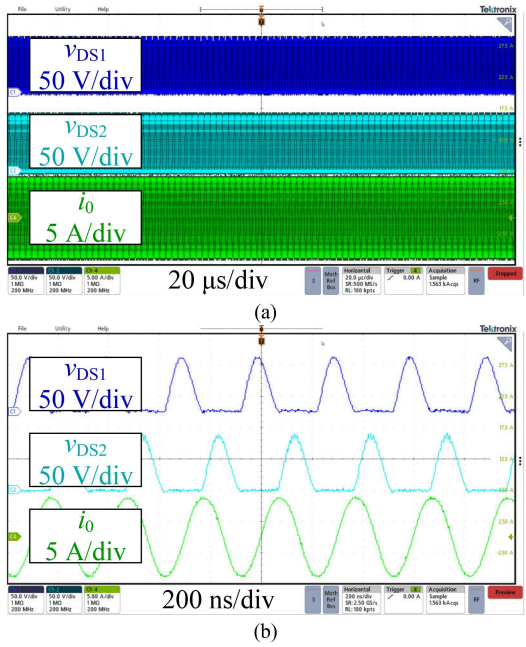

Fig. 16. Low-frequency observed waveforms of the switch voltages v_{DS1} and v_{DS2}, as well as the output current i_0, along with their zoom-in waveforms. (a) Low-frequency observed waveforms. (b) Zoom-in waveforms.

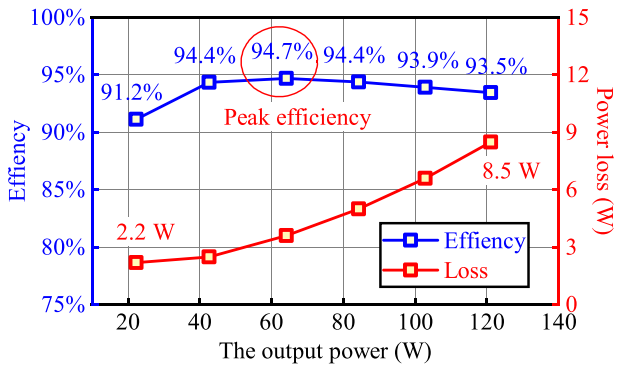

Fig. 17. Inverter efficiency and losses at different output power levels.

The inductor loss is calculated using the average power calculation method, as represented by

$$P_L = \frac{1}{N}\sum_{n=0}^{N-1} v_L[n]\, i_L[n] \tag{33}$$

where P_L represents the loss of the inductor, N is the total number of sampling points within one cycle, $v_L[n]$ is the inductor voltage at the nth sampling point, and $i_L[n]$ is the inductor current at the nth sampling point.

The capacitor loss is calculated as follows:

$$P_C = I_{C\_\mathrm{RMS}}^2 R_{C\_\mathrm{ESR}} \tag{34}$$

where P_C is the loss of the capacitor, I_{C_RMS} is the root mean square value of the capacitor current, and R_{C_ESR} is the parasitic resistance of the capacitor.

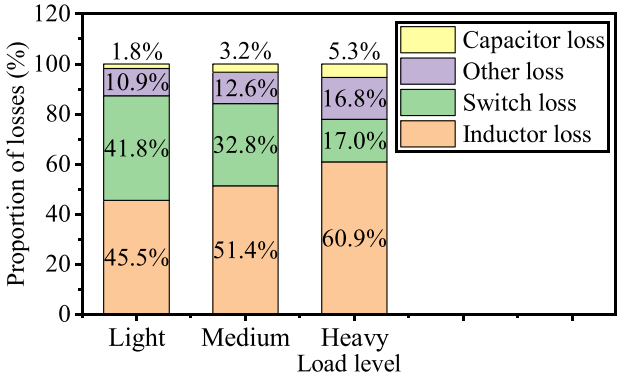

Fig. 18. Loss distribution under light load (22.3 W), medium load (64.1 W), and heavy load (121.1 W) conditions.

The switch loss is calculated as follows:

$$P_{\mathrm{SW}}=\frac{1}{N}\sum_{n=0}^{N-1} v_{\mathrm{SW}}[n]\, i_{\mathrm{SW}}[n] \tag{35}$$

where P_{SW} represents the loss of the switch, $v_{\mathrm{SW}}[n]$ is the switch voltage at the nth sampling point, and $i_{\mathrm{SW}}[n]$ is the switch current at the nth sampling point.

The total loss, minus the above components, accounts for the other losses, which include wire losses, PCB losses, and more.

Based on a comprehensive analysis of experimental and simulation results, the loss distribution of the inverter under light-load, medium-load, and heavy-load conditions was examined, as shown in Fig. 18. As the load increases, the proportion of losses in capacitors grows significantly. This occurs because C_{x} carries the cosine component of the differential current i_{d}, which is load-dependent and increases with higher loads, leading to elevated losses. The loss proportion of the switches decreases as the output power increases. Resonant inductors account for the majority of total losses, maintaining approximately 40%-60% contribution. The high-frequency harmonic content in the inductor current causes substantial losses, representing the primary limiting factor for further efficiency improvement in the inverter.

V. Conclusion

This article proposes a novel CC push–pull Class-E inverter topology. The operational principles and design methodology of the circuit are analyzed in detail. The main contributions are summarized as follows.

1) With appropriate parameter design, the proposed circuit achieves load-independent CC output and ZVS across varying loads.
2) The output current's THD was analyzed, demonstrating that low-harmonic output can be attained without the need for output filters within a specific duty cycle range, specifically when D_{off} is greater than 0.5.
3) A 3.33-MHz prototype was designed and tested, achieving a peak efficiency of 94.7%. The circuit's load-independent ZVS operation and low-THD CC characteristics are also experimentally validated.

The proposed inverter topology features soft switching, CC output, and low-harmonic output characteristics, which endows it with broad application prospects in scenarios such as high-frequency operations, CC output requirements, and low-harmonic environments.

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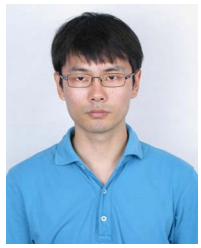
Xiao Zheng received the B.S. degree in electrical engineering from Taiyuan University of Technology, Taiyuan, China, in 2021, and the M.S. degree in electrical engineering from Southeast University, Nanjing, China, in 2025. He is currently working toward the Ph.D. degree with the School of Electrical Engineering, Southeast University, Nanjing, China.

His research interests include resonant power converters.



Chenwen Cheng received the B.S. and Ph.D. degrees from Zhejiang University, Hangzhou, China, in 2012 and 2017, respectively, both in electrical engineering.

From 2018 to 2021, he was a postdoctoral researcher with San Diego State University, San Diego, CA, USA. He is currently with Southeast University, Nanjing, China. His research interests include high-frequency resonant converters, wireless power transfer, renewable power generation, and motor control.

Meng Song (Senior Member, IEEE) received the B.S. degree in electrical engineering from Southeast University, Nanjing, China, in 2012, the M.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2014, and the Ph.D. degree in electrical engineering from Southeast University, in 2018.

From 2018 to 2020, she was a Postdoctoral Fellow with the University of Central Florida. She is currently an Associate Professor with the School of Electrical Engineering, Southeast University. Her research interests include demand response, load modeling and control, transactive energy, and power system resilience.

Fei Teng received the B.Eng. degree in electrical engineering from Beihang University, Beijing, China, in 2009, and the M.Sc. and Ph.D. degrees in electrical engineering from Imperial College London, London, U.K., in 2010 and 2015, respectively.

He is currently a Reader in Intelligent Energy Systems with the Department of Electrical and Electronic Engineering, Imperial College. His research interests include power system operation with a high penetration of inverter-based resources and the cyber-resilient and privacy-preserving cyber-physical power grid.

Wei Hua (Senior Member, IEEE) received the B.Sc. and Ph.D. degrees in electrical engineering from Southeast University, Nanjing, China, in 2001 and 2007, respectively.

From 2004 to 2005, he was with the Department of Electronics and Electrical Engineering, The University of Sheffield, Sheffield, U.K., as a joint-supervised Ph.D. student. His research interests include design, analysis, and control of electrical machines, especially for permanent magnetic (PM) brushless machines and switching reluctance machines.