A High-Efficiency TPCM/DCM Mixed Conduction Mode for Five-Level Inverter

Baojian Ji, Chao Li, and Feng Hong

***Abstract*—Discontinuous conduction mode (DCM) leverages its ZCS characteristics to significantly improve inverter efficiency. However, its inherent drawback of higher peak-to-average ratio (PAR) in inverter-side inductor current leads to increased current stress and device losses, thereby limiting practical applications. To address this issue, this article takes the T-type hybrid bridge five-level topology as an example and proposes a fixed-frequency mixed conduction mode modulation strategy for five-level inverters. By introducing a half-level implementation to achieve trapezoidal conduction mode, the inductor current is divided into three stages within one switching period, effectively reducing PAR and minimizing losses. When the instantaneous power is insufficient to maintain trapezoidal conduction mode, the inverter operates in five-level DCM, where the introduced half-level not only reduces PAR, but also improves duty cycle utilization in DCM. This article systematically analyzes the operational characteristics of the inverter under the proposed hybrid conduction mode modulation strategy. Mathematical derivations are provided for switch duty cycle calculations in each operating mode, along with a unified decision logic for mode selection based on real-time circuit conditions, enabling seamless mode transitions. Furthermore, an inductance selection methodology is developed to minimize both losses and current stress in the inverter-side inductor. A 500 W experimental prototype was constructed to validate the theoretical analysis, and the efficiency was significantly improve.**

***Index Terms*—Discontinuous conduction mode (DCM), five-level inverter, trapezium conduction mode (TPCM), zero current switching (ZCS), zero voltage switching (ZVS).**

I. INTRODUCTION

PHOTOVOLTAIC (PV) generation being a crucial manifestation and the most rapidly growing sector of renewable energy, has been vigorously advanced across nations [1], [2], [3]. As the mainstream power rating of PV modules increases from 300–400 W to 500–600 W, microinverters must correspondingly boost their single-channel power capacity. The industry has enhanced microinverters' competitiveness against string inverters by increasing individual unit power and power density, while spreading system costs like components and installation. "4 in 1" and "2 in 1" configurations have become mainstream products [4]. As power levels rise, improving thermal performance while controlling cooling costs becomes critical. The most compelling approach is to reduce losses. As such, alongside essential requirements for reliability, compactness, and cost-effectiveness, efficiency constitutes a critical performance indicator [5], [6], [7]. Inverters operating in continuous conduction mode (CCM) can reduce switching losses by incorporating soft-switching auxiliary circuits [8], [9], [10], [11], [12] and further enhance power density by increasing switching frequency. However, complex soft-switching circuits and control methods compromise reliability. Consequently, mainstream CCM inverter products typically employ hard switching. In comparison, boundary conduction mode (BCM) [13], [14], [15], [16] and DCM [21] inverters employ smaller inductance values and achieve zero current switching (ZCS) without auxiliary circuits. However, their inverter-side inductor currents demonstrate larger PAR, resulting in increased conduction losses. Such operation sacrifices partial conduction loss to obtain ZCS, suitable for low-to-medium power applications. As power levels increase, the overall losses of the switch gradually exceed those of CCM.

The BCM can achieve zero voltage switching (ZVS) or valley switch through resonance. Zhang et al. [17], Amirahmadi et al. [18], and Biela et al. [19] modifying the reset value of BCM to a minor negative value enables bidirectional inductor current flow within each switching cycle to ensure the realization of ZVS, this control method is also known as the triangular conduction mode (TCM). Compared with DCM, BCM achieves a lower current PAR. However, its switching frequency cannot maintain fixed values during line frequency periods, resulting in implementation challenges for digital control systems and stringent requirements for current-sensing circuitry. Zhang et al. [20] employed a T-type hybrid bridge five-level topology to realize five-level BCM, which narrowed the switching frequency variation range but failed to achieve fixed-frequency operation. DCM maintains fixed switching frequency and no special current sampling circuit is required, thereby facilitating digital control implementation. But the PAR of inductor current is higher. To address this problem, DCM operating with fixed off-time control [21] or off-time discrete control [32] can effectively reducing the PAR however at the expense of sacrificing the fixed switching frequency feature.

Zhang et al. [25] proposed the trapezium conduction mode (TPCM), which can be understood as a special BCM. By integrating unipolar modulation and bipolar modulation within a

Received 10 March 2025; revised 19 June 2025, 26 August 2025, and 30 October 2025; accepted 5 December 2025. Date of publication 15 December 2025; date of current version 25 February 2026. This work was supported by National Defense Basic Scientific Research Program of China under Grant JCKY2021606B014. Recommended for publication by Associate Editor N. Zargari. *(Corresponding author: Feng Hong.)*

Baojian Ji and Chao Li are with the Nanjing University of Sci-ence and Technology, Nanjing 210091, China (e-mail: jibaojian@njust.edu.cn; Lic@njust.edu.cn).

Feng Hong is with the Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: hongfeng@nuaa.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3644398.

Digital Object Identifier 10.1109/TPEL.2025.3644398

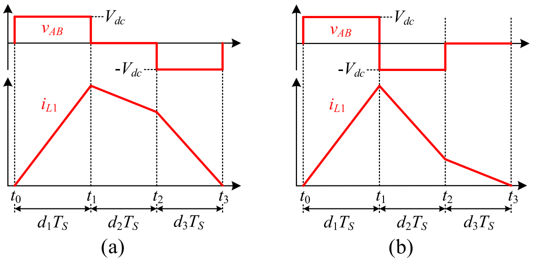


Fig. 1. Schematic of HP-TPCM operation. (a) Unipolar-bipolar modulation; (b) Bipolar-unipolar modulation.

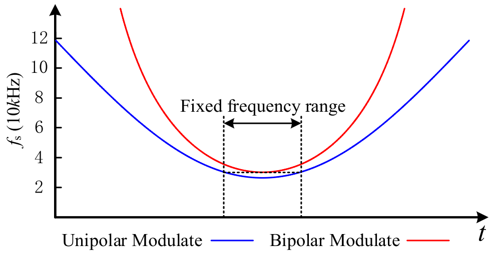


Fig. 2. Schematic of fixed-frequency range of HP-TPCM.

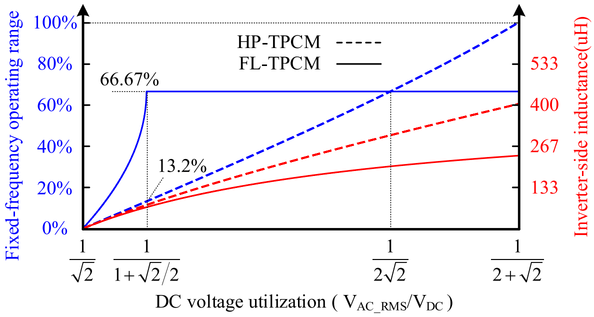


Fig. 3. Relationship between DC voltage utilization and both fixed-frequency operating range and inverter-side inductance.

single switching cycle, this method divides the inductor current falling edge into two segments, as shown in Fig. 1. Unipolar modulation makes the inductor current fall with a smaller slope, and bipolar modulation obtains a fall with a larger slope, adjusting the proportional duration of these two polarities generates an equivalent intermediate voltage level, enabling fixed-frequency operation at any value between unipolar BCM and bipolar BCM frequencies. This achieves fixed-frequency BCM within a certain range but with lower dc-bus voltage utilization. For ease of differentiation, it is referred to here as hybrid polarity TPCM (HP-TPCM). Zhang et al. [26] compared HP-TPCM with DCM and demonstrated its superiority. Zhang et al. [27] applied TPCM to five-level topologies, but did not implement fixed-frequency control.

The mixed conduction mode (MCM) can integrate the advantages of multiple modes while mutually compensating for their limitations. In [29], CCM and segmented fixed-frequency DCM are combined for application in power factor (PF) correction rectifiers. In [22], CCM and DCM are combined during the inverter's line-frequency cycle to reduce the filter inductance without worsening the grid current THD, where the inverter operates in CCM when instantaneous power exceeds the threshold and in DCM when it falls below. Christidis et al. [23] and Lodh et al. [24] adopted a similar approach by integrating DCM with BCM in flyback inverters, though limited to low-power applications. Son et al. [30] employs a MCM of BCM/ TCM/DCM, where TCM operates near the output voltage zero-crossing to reduce leakage current, while DCM serves as the transition between BCM and TCM to improve light-load efficiency. In [31], a T-type five-level topology is employed to implement a MCM combining BCM/TPCM/CCM, with transition modes specifically designed but requiring complex control logic, where the BCM/TPCM switching frequency are determined by ZVS required reverse current with fixed dead-time, and the CCM frequency is obtained through a fitting function. Yin et al. [15] and Huang et al. [32] adopted HP-TPCM/BCM hybrid conduction mode, in [15], HP-TPCM operates near the output voltage zero-crossing to mitigate BCM's zero-crossing distortion while simultaneously enabling reactive power generation, In [32], HP-TPCM operates when $v_o < V_{\mathrm{dc}}/2$ to achieve full-range ZVS, but with high current PAR remaining. Zhao et al. [28] combines HP-TPCM with DCM within the line frequency period to realize MCM that operates at fixed-frequency while reducing the PAR. The operating range of the TPCM is shown in Fig. 2 ($V_{\mathrm{dc}} = 200$ V, $V_o = 110$ V, $L_1 = 101$ μH, $P_o = 500$ W), which shows that it has a narrower operating range, and if its fixed-frequency operating range is expanded it is necessary to reduce the dc-voltage utilization. For the sake of distinction, this mode is referred to as HP-MCM.

In summary, both DCM and BCM suffer from power limitations due to their nonnegligible conduction losses. While introducing CCM via MCM can mitigate this limitation, the presence of inductance prevents fixed-frequency operation, makes identical duty cycle calculation logic inapplicable, and requires designed transition modes. HP-TPCM can likewise mitigate conduction loss limitations, but exhibits strong mutual exclusion (see Fig. 3) between its fixed-frequency operating range and dc voltage utilization, resulting in limited optimization under commonly adopted voltage utilization ratios. Therefore, retaining natural soft-switching capability while reducing conduction losses persists as the key research challenge.

In this article, half level is introduced using the five-level inverter topology, combining five-level BCM [20] and three-level unipolar modulated BCM within a single switching cycle to realize five-level TPCM (FL-TPCM), enabling the coexistence of high voltage utilization ($>1/\sqrt{3}$) and a wide fixed-frequency operating range (66.67%),while the remaining portions utilize five-level DCM as supplementation, where bipolar five-level DCM provides reactive power support. By substantially reducing the PAR of inductor current, achieving soft-switching with less conduction loss sacrificed, effectively alleviating power limitations.

In Section II, the operating characteristics and principles of the proposed modulation strategy are introduced, and a unified judgment logic is constructed to select the operating modes according to the operating state of the circuit, and the duty cycle calculation method for each operating mode is derived to realize the ZVS or valley switching by fixing the dead time reserved for resonance.

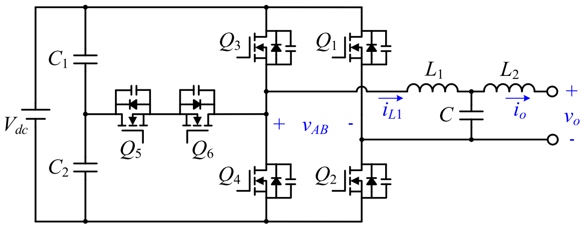


Fig. 4. T-type hybrid bridge five-level inverter topology.

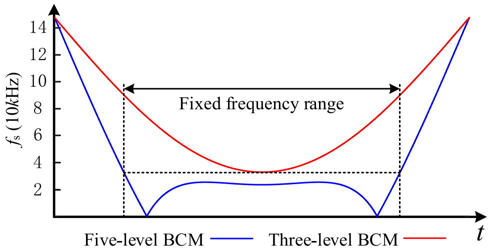
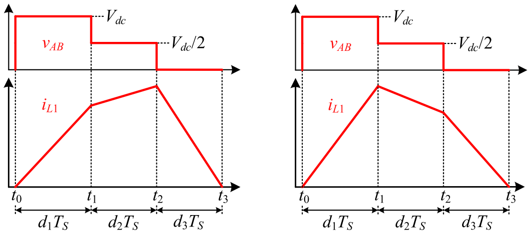


Fig. 5. Schematic of fixed-frequency range of FL-TPCM.



(a) (b)

Fig. 6. Schematic of FL-TPCM operation. (a) $v_0 < V_{dc}/2$. (b) $v_0 > V_{dc}/2$.

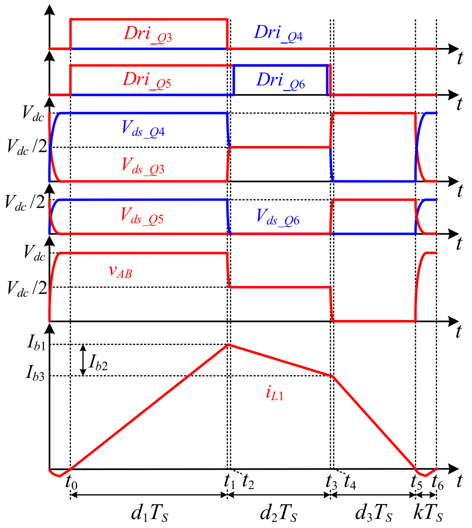


Fig. 7. Key waveforms of the inverter operating in FL-TPCM.

In Section III, loss analysis and comparison with conventional DCM and HP-MCM are carried out to propose a method of calculating the inductor inductance value of the inverter-side that minimizes the loss and at the same time minimizes the current stress, and finally, a 500 W experimental prototype is constructed for validation, and the experimental results prove the superiority of the control method proposed in this article.

II. CHARACTERISTICS OF THE PROPOSED MODULATION STRATEGY

The T-type hybrid bridge five-level inverter topology is shown in Fig. 4, in which the T-type three-level bridge arm operates at high frequency for modulating sinusoidal waveforms, and it can output three levels: V_{dc}; $V_{\mathrm{dc}}/2$; and 0; and the two-level bridge arm changes the power supply polarity. The two bridge arms work together to output five levels, respectively, V_{dc}, $V_{\mathrm{dc}}/2$, 0, $-V_{\mathrm{dc}}/2$, $-V_{\mathrm{dc}}$.

The five-level BCM and the three-level unipolar modulation BCM are combined within a single switching cycle to achieve FL-TPCM, which can significantly expand the operating range of the fixed-frequency of the TPCM with guaranteed voltage utilization, as shown in Fig. 5 ($V_{\mathrm{dc}} = 200$ V, $V_o = 110$ V, $L_1 = 77$ μH, and $P_o = 500$ W). Depending on the relationship between the output voltage and the half-level, it is decided that the half-level acts on the rising or falling edge, as shown in Fig. 6. When the instantaneous power cannot be maintained by FL-TPCM the five-level DCM is used as a supplement to fix the switching frequency, which is the FL-TPCM/DCM MCM modulation strategy. This significantly reduces PAR of the inductor current while decreasing conduction losses and current stress.

The following detailed analysis of its operating characteristics, Due to its symmetrical operation, the output voltage is analyzed as an example of positive half-cycle. Since the switching frequency is much higher than the line frequency, the output voltage can be considered constant within a single switching cycle.

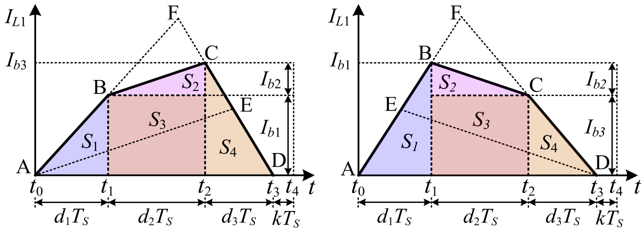
A. Five-Level TPCM

Fig. 7 shows the waveforms of the on-time sequence of the switch, the drain-source voltage, the output level of the inverter bridge arm, and the inductor current at the inverter-side when the inverter operates in FL-TPCM. The switch Q_1, Q_4 remains in the turn-OFF, the switch Q_2 remains in the turn-ON, and the switch Q_3, Q_5, and Q_6 operate at high frequency to modulate the waveforms.

Interval 1 [t_0-t_1]: Q_3 turns ON at t_0 under the ZCS, Q_5 turns ON but the body diode of Q_6 is reverse cutoff, the output level of the inverter bridge arm is V_{dc}, i_{L1} rises linearly from zero with a large slope $s_1(n)$, and rises to the peak I_{b1} at t_1

$$s_1(n) = \frac{V_{\mathrm{dc}} - v_o(n)}{L_1}. \tag{1}$$

Interval 2 [t_1-t_2]: Q_3 turns OFF at t_1, i_{L1} charges and discharges the junction capacitor of $Q_3 \sim Q_6$, an extremely brief interval that can be viewed as i_{L1} being constant, V_{ds_Q3} charges from zero to $V_{\mathrm{dc}}/2$ and V_{ds_Q4} discharges from V_{dc} to $V_{\mathrm{dc}}/2$ at t_2.



(a) (b)

Fig. 8. Calculation of FL-TPCM unit switching cycle. (a) $v_0 < V_{dc}/2$. (b) $v_0 > V_{dc}/2$.

Interval 3 [t_2-t_3]: The body diode of Q_6 loses cutoff voltage, Q_5 turns ON at t_2 under the ZVS, the output level of the inverter bridge arm is $V_{\rm dc}/2$. The slope of i_{L1} can be expressed by (2), when $v_o(n)<V_{\rm dc}/2$, $i_{\rm L1}$ continues to increase linearly with a smaller slope; when $v_o(n)>V_{\rm dc}/2$, $s_2(n)$ is negative and $i_{\rm L1}$ decreases linearly with a smaller slope; when $v_{\rm o}(n) = V_{\rm dc}/2$, the slope of i_{L1} is zero

$$s_2(n) = \frac{V_{\rm dc}/2 - v_o(n)}{L_1}. \tag{2}$$

After a dead time, Q_6 turns ON under the ZVS and the $i_{\rm L1}$ state is unchanged. One dead time before t_3, Q_6 turns OFF under the ZVS, i_{L1} through the body diode of Q_6 renewed current. i_{L1} changes to I_{b3} at t_3, the amount of change in this interval is I_{b2}.

Interval 4 [t_3-t_4]: Q_5 turns OFF at t_3, i_{L1} charges and discharges the junction capacitor of Q_3~Q_6, V_{ds_Q3} charges from $V_{\rm dc}/2$ to $V_{\rm dc}$ and V_{ds_Q4} discharges from $V_{\rm dc}/2$ to zero at t_4.

Interval 5 [t_4-t_5]: i_{L1} is renewed by the body diode of Q_4, and the output level of the inverter bridge arm is 0. i_{L1} decreases linearly with a large slope $s_3(n)$ from the peak I_{b3} and decreases to 0 at t_5

$$s_3(n) = \frac{-v_o(n)}{L_1}. \tag{3}$$

Interval 6 [t_5-t_6]: Dead time, the T-type bridge arm of the switch all OFF, junction capacitor of Q_3~Q_6 and inverter-side inductor L_1 resonance occurs, the use of resonance to achieve ZVS or valley switch, resonance process in the specific analysis of the latter.

After that this switching cycle ends and the next cycle starts.

The FL-TPCM significantly extends the fixed-frequency operating range over the HP-TPCM, but still does not cover the entire line frequency cycle, and the remaining range is supplemented by a five-level DCM. The FL-TPCM is referred to as operating mode 1. Since the circuit resonates during current interruptions, the output voltage of the inverter bridge arm fluctuates sinusoidally with a center value of $v_o(n)$, and the average voltage during a switching cycle is clamped to $v_o(n)$, average current control is used. Controls the current command value $I_{\rm com}(n)$ to a sinusoidal reference value.

The calculation of i_{L1} in unit switching period is schematically shown in Fig. 8. Its average current $i_{\rm avg}(n)$ is

$$i_{\rm avg}(n) = I_{\rm com}(n) = \frac{S_1 + S_2 + S_3 + S_4}{T_s} \tag{4}$$

where T_s is the switching period and S_1~S_4 are the areas of triangles or rectangles in Fig. 8 which can be expressed as

$$S_1 = \frac{1}{2} I_{b1} d_1 T_s \tag{5}$$

$$S_2 = \frac{1}{2} I_{b2} d_2 T_s \tag{6}$$

$$S_3 = I_{b1} d_2 T_s \tag{7}$$

$$S_4 = \frac{1}{2} I_{b3} d_3 T_s. \tag{8}$$

The expressions for I_{b1}~I_{b3} are as follows:

$$I_{b1} = s_1(n) d_1(n) T_s \tag{9}$$

$$I_{b2} = s_2(n) d_2(n) T_s \tag{10}$$

$$I_{b3} = s_3(n) d_3(n) T_s \tag{11}$$

$$I_{b1} = I_{b2} + I_{b3} \tag{12}$$

where d_1~d_3 are the duty cycles of different levels of the inverter bridge arm outputs and k denotes the relationship between dead time and switching period

$$(d_1 + d_2 + d_3) T_s = (1 - k) T_s. \tag{13}$$

By calculating S_1~S_4 by substituting into (4) in parallel with (9)–(13), the duty cycle calculation formula for each interval can be derived as shown in (14)–(16) shown at the bottom of the next page.

B. Five-Level DCM

Operating Mode 2: When v_o and i_o are in the same direction and $v_o(n)<V_{\rm dc}/2$, the inverter operates in mode 2 if the instantaneous power is small enough not to maintain FL-TPCM, the output level of the inverter bridge arm is $V_{\rm dc}/2$ at the rising edge, and 0 at the falling edge, as shown in Fig. 9, after i_{L1} falls to 0, L_1 and the junction capacitance of Q_3~Q_6 enter the resonant state. The duty cycle derivation process is similar to that of the FL-TPCM and is calculated as

$$d_2 = \sqrt{\frac{2 i_{\rm avg}(n) L_1 f_s v_o(n)}{(V_{\rm dc}/2 - v_o(n)) V_{\rm dc}/2}} \tag{17}$$

$$d_3 = \sqrt{\frac{2 i_{\rm avg}(n) L_1 f_s (V_{\rm dc}/2 - v_o(n))}{v_o(n) V_{\rm dc}/2}}. \tag{18}$$

Operating Mode 3: When v_o and i_o are in the same direction and $v_o(n)>V_{\rm dc}/2$, the inverter operates in mode 3 if the instantaneous power is small enough not to maintain FL-TPCM, switch Q_1 remains in the turn-OFF while switch Q_2 maintains turn-ON, the output level of the inverter bridge arm is $V_{\rm dc}$ at the rising edge, and $V_{\rm dc}/2$ at the falling edge, as shown in Fig. 10, after i_{L1} falls to 0, L_1 and the junction capacitance of Q_3~Q_6 enter the resonant state. The duty cycle is calculated as

$$d_1 = \sqrt{\frac{2 i_{\rm avg}(n) L_1 f_s (V_{\rm dc} - v_o(n))}{(v_o(n) - V_{\rm dc}/2) V_{\rm dc}/2}} \tag{19}$$

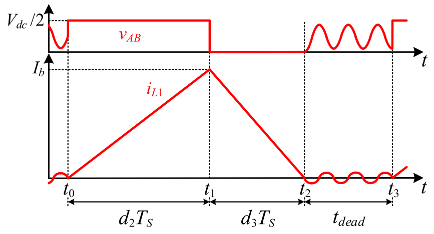


Fig. 9. Schematic of inductor current and inverter bridge arm output voltage in mode 2.

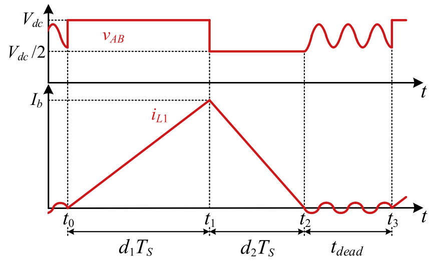


Fig. 10. Schematic of inductor current and inverter bridge arm output voltage in Mode 3.

$$d_2 = \sqrt{\frac{2i_{\text{avg}}(n)\,L_1 f_s\,(v_o(n) - V_{\text{dc}}/2)}{(V_{\text{dc}} - v_o(n))\,V_{\text{dc}}/2}}. \tag{20}$$

Operating Mode 4: When the inverter operates on a nonpure resistive load, near the point where the v_o crosses zero, v_o and i_o are in opposite directions and the inverter operates in mode 4. The T-type bridge arm outputs half-level voltage, while the two-level bridge arm generates negative polarity during falling edges and positive polarity during rising edges, as shown in Fig. 10, after i_{L1} rises to 0, L_1 and the junction capacitance of $Q_1 \sim Q_6$ enter the resonant state. The duty cycle is calculated as

$$d_1 = \sqrt{\frac{-2i_{\text{avg}}(n)\,L_1 f_s\,(V_{\text{dc}}/2 - v_o(n))}{(V_{\text{dc}}/2 + v_o(n))\,V_{\text{dc}}}} \tag{21}$$

$$d_2 = \sqrt{\frac{-2i_{\text{avg}}(n)\,L_1 f_s\,(V_{\text{dc}}/2 + v_o(n))}{(V_{\text{dc}}/2 - v_o(n))\,V_{\text{dc}}}}. \tag{22}$$

Near another zero-crossing point with the same output voltage polarity, mode 1 or mode 2 may fail to deliver sufficient power due to the limitation of falling edge slope, and the inverter operates in mode 4$*$ as shown in Fig. 11(b), with the duty cycle is calculated as (23), (24). The operating principle of mode 4$*$ is completely consistent with that of Mode 4 with negative half cycle output voltage, which will be collectively referred to as mode 4 in the following text

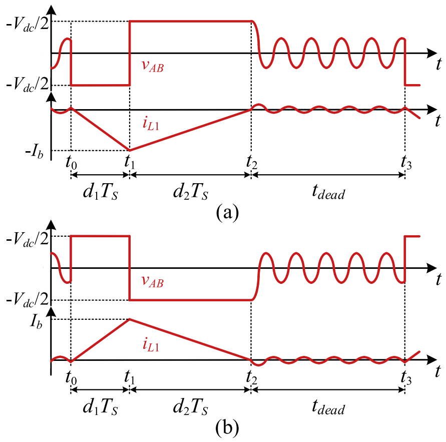


Fig. 11. Schematic of inductor current and inverter bridge arm output voltage in Mode 4. (a) Mode 4. (b) Mode4*.

$$d_1 = \sqrt{\frac{2i_{\text{avg}}(n)\,L_1 f_s\,(V_{\text{dc}}/2 + v_o(n))}{(V_{\text{dc}}/2 - v_o(n))\,V_{\text{dc}}}} \tag{23}$$

$$d_2 = \sqrt{\frac{2i_{\text{avg}}(n)\,L_1 f_s\,(V_{\text{dc}}/2 - v_o(n))}{(V_{\text{dc}}/2 + v_o(n))\,V_{\text{dc}}}}. \tag{24}$$

The above mode 4 can provide reactive power output with a minimum PF of 0.766. If an even lower PF is required, simply upgrade the half level to the full level to achieve reactive power output of any PF value.

C. Modulation Strategy

As mentioned above FL-TPCM is a special BCM that can adjust the area of rectangle *ABCD*, which is the average current output from the inverter bridge arm per unit switching cycle, by adjusting the duty cycle d_2, thus changing the instantaneous output power. As shown in Fig. 8, increasing d_2 decreases $i_{\text{avg}}(n)$; decreasing d_2 increases $i_{\text{avg}}(n)$. The rectangle *ABCD* changes to the triangle AED when d_2 is increased to the limit, which is the minimum average current threshold that the FL-TPCM can

---

$$d_1 = \frac{v_o(n)\,(1-k) - \sqrt{(1-k)^2\,(V_{\text{dc}} - v_o(n))\,v_o(n) - 2i_{\text{avg}}(n)\,L_1 f_s V_{\text{dc}}}}{V_{\text{dc}}} \tag{14}$$

$$d_2 = \frac{2\sqrt{(1-k)^2\,(V_{\text{dc}} - v_o(n))\,v_o(n) - 2i_{\text{avg}}(n)\,L_1 f_s V_{\text{dc}}}}{V_{\text{dc}}} \tag{15}$$

$$d_3 = \frac{(V_{dc} - v_o(n))\,(1-k) - \sqrt{(1-k)^2\,(V_{\text{dc}} - v_o(n))\,v_o(n) - 2i_{\text{avg}}(n)\,L_1 f_s V_{\text{dc}}}}{V_{\text{dc}}}. \tag{16}$$

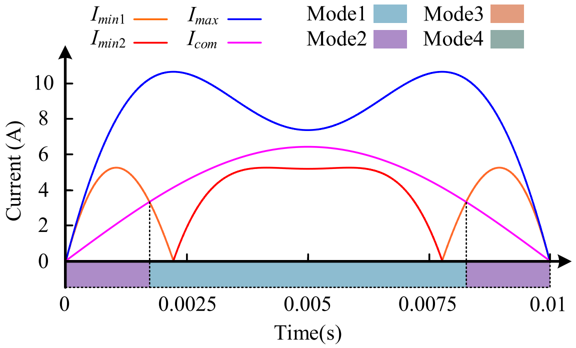


Fig. 12. Schematic of current threshold and current command values of FL-TPCM under the rated load.

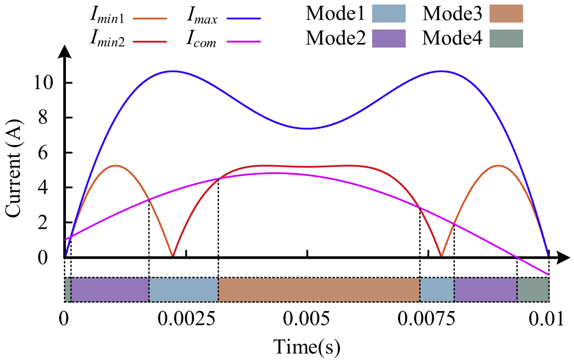


Fig. 13. Schematic of the current threshold and current command values of FL-TPCM when output current exceeds $\pi/15$ under 3/4 rated load.

output per unit switching cycle. When $v_o(n)<V_{\mathrm{dc}}/2$

$$d_1 = 0 \tag{25}$$

$$d_3 = 1 - k - d_2 \tag{26}$$

the expression for the minimum average current threshold 1 I_{min1} is obtained by derivation as

$$I_{\mathrm{min1}} = \frac{(1-k)^2 \left(V_{\mathrm{dc}}/2 - v_o(n)\right) v_o(n)}{L_1 f_s V_{\mathrm{dc}}}. \tag{27}$$

When $v_o(n)>V_{\mathrm{dc}}/2$

$$d_3 = 0 \tag{28}$$

$$d_1 = 1 - k - d_2 \tag{29}$$

the minimum average current threshold 2 I_{min2} is

$$I_{\mathrm{min2}} = \frac{(1-k)^2 \left(V_{\mathrm{dc}} - v_o(n)\right) \left(v_o(n) - V_{\mathrm{dc}}/2\right)}{L_1 f_s V_{\mathrm{dc}}}. \tag{30}$$

The rectangle *ABCD* changes to the triangle AFD when d_2 is decreased to the limit, which is the maximum average current threshold that the FL-TPCM can output per unit switching cycle

$$d_2 = 0 \tag{31}$$

$$d_3 = 1 - k - d_1 \tag{32}$$

$$I_{\max} = \frac{(1-k)^2 \left(V_{\mathrm{dc}} - v_o(n)\right) v_o(n)}{2 L_1 f_s V_{\mathrm{dc}}}. \tag{33}$$

The schematic of the current threshold and current command values $I_{\mathrm{com}}(n)$ of the FL-TPCM over a half-line cycle under the rated load of the inverter is shown in Fig. 12. However, the inverter does not always operate under a purely resistive load. Fig. 13 shows the schematic for a typical operating condition with output current exceeding $\pi/15$ under 3/4 rated load. The current threshold varies with v_{o}. In order to maintain fixed switching frequency, the FL-TPCM cannot operate in the full operating range, and the five-level DCM is used as a supplement.

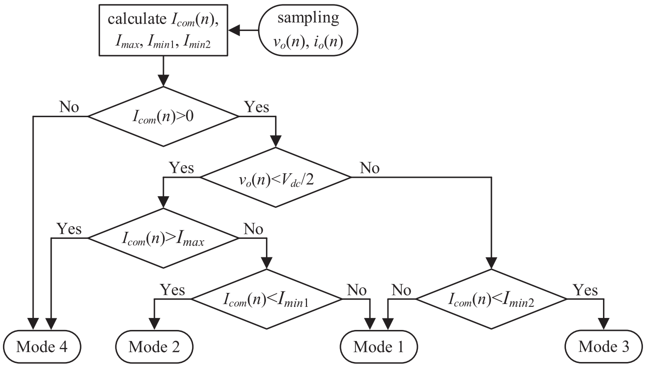


Fig. 14. Schematic of FL-TPCM/DCM mode judgment logic.

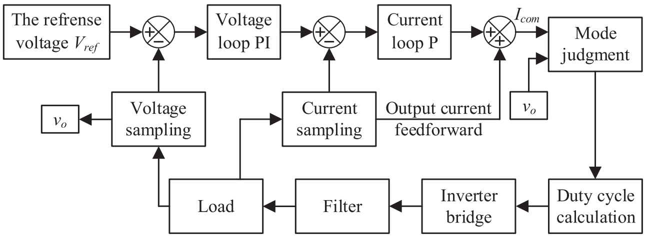


Fig. 15. Control block diagram of the proposed inverter.

The mode judgment logic is shown in Fig. 14, still taking the positive half cycle of output voltage as an example. First, judge the polarity of the current command value $I_{\mathrm{com}}(n)$, when $I_{\mathrm{com}}(n)$ is negative, the inverter operates in mode 4; when $I_{\mathrm{com}}(n)$ is positive, determine whether $v_o(n)<V_{\mathrm{dc}}/2$. When $v_o(n)<V_{\mathrm{dc}}/2$, then compare $I_{\mathrm{com}}(n)$ with $I_{\max}$, and if $I_{\mathrm{com}}(n)>I_{\max}$, the inverter operates in mode 4. After that, compare $I_{\mathrm{com}}(n)$ with I_{min1}, if $I_{\mathrm{com}}(n)<I_{\mathrm{min1}}$ select mode 2, otherwise select mode 1. When $v_o(n)>V_{\mathrm{dc}}/2$, compare $I_{\mathrm{com}}(n)$ with I_{min2}, if $I_{\mathrm{com}}(n)<I_{\mathrm{min2}}$ select mode 3, otherwise select mode 1.

Fig. 15 shows the control block diagram of the proposed inverter. According to the proposed modulation strategy, mode 3 may be entered when the inverter is lightly loaded or when the load is not purely resistive, and mode 4 only occurs when the load is not purely resistive. The judgment logic for mode selection is unified and fully considers the unexpected situation, and the different modes can be switched smoothly. In addition, Fig. 16 shows the control block diagram of the inverter in grid connected mode.

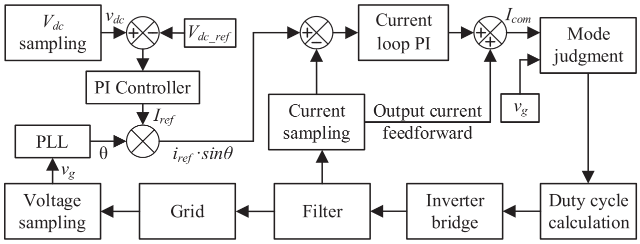


Fig. 16. Control Block Diagram of the Proposed Inverter in Grid Connected Mode.

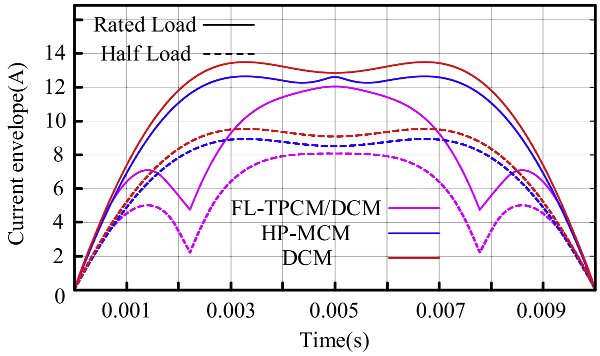


Fig. 17. Inverter-side inductor current envelope comparison.

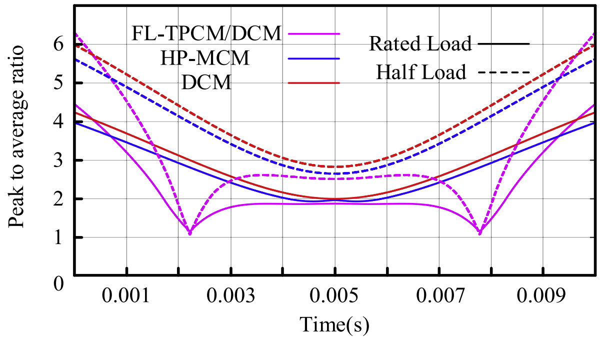


Fig. 18. Inverter-side inductor current PAR comparison.

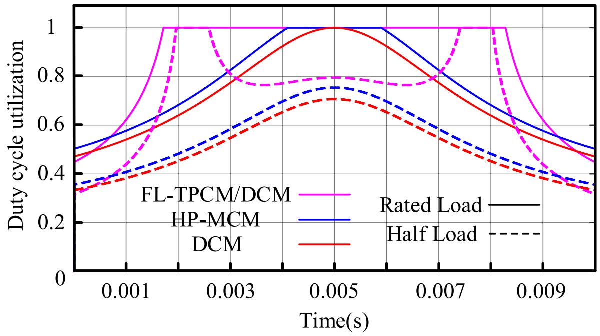
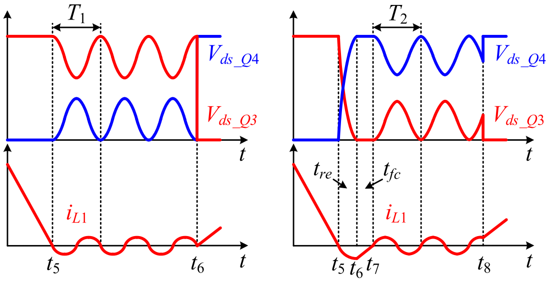


Fig. 19. Duty cycle utilization comparison.



(a) (b)

Fig. 20. Schematic of resonant types. (a) $v_0 < V_{dc}/2$. (b) $v_0 > V_{dc}/2$.

The inverter-side inductor current envelope comparison of the proposed FL-TPCM/DCM modulation strategy with HP-MCM and conventional DCM is shown in Fig. 17. The inductor current PAR comparison is shown in Fig. 18. The duty cycle utilization comparison is shown in Fig. 19. The instantaneous power maximum point of HP-MCM operates in HP-TPCM, therefore the inverter-side inductance is taken to be slightly larger than that of the conventional DCM, so the inverter-side inductance current amplitude is reduced in the whole operating range, the PAR is optimized, and the duty cycle utilization is improved. However, due to the narrower operating range of HP-TPCM, the PAR is optimized less. FL-TPCM/DCM significantly expands the fixed-frequency operating range of TPCM while ensuring the voltage utilization, further reduces the inverter-side inductor current amplitude, optimizes the PAR, and improves the duty cycle utilization, which helps to reduce the current stress as well as the device loss, improves the efficiency. Moreover, the inverter-side inductance of the FL-TPCM/DCM takes a smaller value, which is favorable to the power density.

D. ZVS Analysis

During dead-time in FL-TPCM or current discontinuity periods in DCM, the junction capacitance of Q_3~Q_6 and the inverter-side inductor L_1 enter into resonant state. The resonance action can be divided into two types as shown in Fig. 20(b). The period of the first type of resonance is T_1 and the period of the second type is T_2. t_{dead} can be expressed as

$$t_{\text{dead}} = T_1 + nT_2. \tag{34}$$

In the first resonant cycle, V_{ds_Q3} resonates to zero or valley voltage, and the expressions of V_{ds_Q3} and i_{L1} are as

$$v_{ds\_Q3}\left(t\right) = V_{\text{dc}} + v_o\left(n\right)\left(\cos\left(\omega_r\left(t - t_5\right)\right) - 1\right) \tag{35}$$

$$i_{L1}\left(t\right) = \frac{-\sqrt{5/2}v_o\left(n\right)\sin\left(\omega_r\left(t - t_5\right)\right)}{\sqrt{L_1/C_{\text{oss}}}} \tag{36}$$

where

$$\omega_r = 1\Big/\sqrt{5L_1C_{\text{oss}}/2} \tag{37}$$

where C_{oss} is the equivalent output junction capacitance of the mosfet, assuming that the parasitic parameters of different switch are the same. the valley voltage of V_{ds_Q3} can be obtained by substituting cos(ω_r(t-t_5)) = -1 into (33), as shown in (38):

$$v_{ds\_Q3\_\min} = V_{\text{dc}} - 2v_o\left(n\right). \tag{38}$$

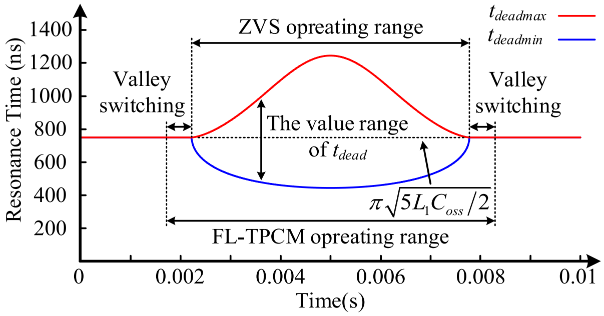


Fig. 21. Value range for fixed dead time.

Thus, ZVS can be realized when $v_o(n)>V_{\mathrm{dc}}/2$, and only valley switch can be realized when $v_o(n)<V_{\mathrm{dc}}/2$. t_{re} is the time required for V_{ds_Q3} to discharge from V_{dc} to 0, which can be obtained by solving for $v_{ds\_Q3}(t)=0$

$$t_{\mathrm{re}}=\frac{1}{\omega_r}\arccos\left(\frac{v_o\left(n\right)-V_{\mathrm{dc}}}{v_o\left(n\right)}\right). \tag{39}$$

The negative voltage will be cut off by the body diode after V_{ds_Q3} drops to 0, and the inverter bridge arm output level is clamped at V_{dc} because the inductor current i_{L1} flowing in the reverse direction is still present, and the amplitude of i_{L1} decreases with a fixed slope from t_6 to t_7, which can be expressed as

$$i_{L1}\left(t\right)=\frac{V_{\mathrm{dc}}-v_o\left(n\right)}{L_1}\left(t-t_6\right)-\frac{\sqrt{5/2}v_o\left(n\right)}{\sqrt{L_1/C_{\mathrm{oss}}}}\sin\left(\omega_r t_{\mathrm{re}}\right) \tag{40}$$

t_{fc} is the duration of body diode freewheeling and V_{ds_Q3} is maintained at 0

$$t_{fc}=\frac{L_1}{V_{\mathrm{dc}}-v_o\left(n\right)}\frac{\sqrt{5/2}v_o\left(n\right)}{\sqrt{L_1/C_{\mathrm{oss}}}}\sin\left(\omega_r t_{\mathrm{re}}\right). \tag{41}$$

When i_{L1} returns to 0, the body diode loses its clamping ability and the circuit enters the second type of resonance, V_{ds_Q3} resonates from 0, and the resonance period and V_{ds_Q3} can be expressed as (42), (43). It is important to note here that V_{ds_Q3} does not resonate to 0 when $v_o(n)<V_{\mathrm{dc}}/2$, so it is always the first type of resonance, as shown in Fig. 20(a)

$$T_2=\frac{2\pi}{\omega_r} \tag{42}$$

$$v_{ds\_Q3}\left(t\right)=\left(V_{\mathrm{dc}}-v_o\left(n\right)\right)\left(1-\cos\left(\omega_r\left(t-t_7\right)\right)\right). \tag{43}$$

Based on the above analysis, the dead time is left to resonate V_{ds_Q3} to 0 after i_{L1} drops to 0, and the ZVS of Q_3 can be realized by starting the next cycle during the duration when V_{ds_Q3} is maintained at 0. The lower limit of the dead time is $t_{\mathrm{deadmin}}=t_{\mathrm{re}}$, and the upper limit of the dead time is $t_{\mathrm{deadmax}}=t_{\mathrm{re}}+t_{fc}$, the range of the values in half line cycle is shown in Fig. 21.

From Fig. 21, it can be seen that the ZVS can be realized in the vast majority of the time in the operating range of the FL-TPCM under rated load, and the value range of fixed dead time has some space, which is generally chosen to be half of the resonance period in order to maximize the range of the ZVS as shown in (44). However, it needs to be fine-tuned according to the experimental phenomena due to the differences in the parasitic parameters of the switch

$$t_{\mathrm{dead}}\approx\pi\sqrt{5L_1C_{\mathrm{oss}}/2}. \tag{44}$$

III. Discussion of Inverter-Side Inductor Parameter Design and Loss Analysis

A. Loss Analysis

The loss of the inverter mainly includes the switching loss and conduction loss of the switch, and the conduction loss and reverse recovery loss of the body diode, as well as the iron loss in the core and copper loss in the winding of the filter inductor.

Switch Q_1 Q_2 of the low frequency bridge arm operate in the line frequency state, only conduction losses are considered. Due to the special modulation method, the high-frequency T-type bridge arm can realize ZCS, by reserving a fixed dead time for resonance, FL-TPCM can realize ZVS or valley switch, so the T-type bridge arm only considers the turn-OFF loss $P_{Q\mathrm{sw}}$ for level switching during the switching cycle and the conduction loss $P_{Q\mathrm{con}}$.

The conduction loss P_{Qcon} is calculated as

$$P_{Q\mathrm{con}}=f\sum_{n=1}^{f_s/f}\int_0^{T_s}i_d^2(n)(t)R_{ds(\mathrm{on})}dt \tag{45}$$

where $i_d(n)(t)$ is the drain current, $R_{ds(\mathrm{on})}$ is the drain-source ON-state resistance, f is the line frequency, f_s is the switching frequency and T_s is the switching period.

Note here that when the T-type bridge arm outputs half-level, the current flows through two switches, and $R_{ds(\mathrm{on})}$ should be doubled; when outputs zero level, the current flows through the body diode of the freewheeling switch.

The switching loss $P_{Q\mathrm{sw}}$ is calculated as

$$P_{Q\mathrm{sw}}=f\sum_{n=1}^{f_s/f}\left[\frac{1}{2}V_{\mathrm{dc}}i_p\left(n\right)\left(t_{d(\mathrm{off})}+t_f\right)\right]. \tag{46}$$

Conventional DCM level-switches once in one switching cycle, and TPCM level-switches twice in one operating cycle, but the amount of change in the drain-source voltage of the switch before and after level-switching of HP-TPCM and DCM is V_{dc}, while FL-TPCM is $V_{\mathrm{dc}}/2$, and the current amplitude has been reduced, therefore, although the number of level-switches of the FL-TPCM increased compared with that of the DCM, the switching loss experiences a slight reduction.

The conduction loss of the body diode can be obtained by integrating the voltage drop and drain current

$$P_{D\mathrm{con}}=f\sum_{n=1}^{f_s/f}\int_0^{T_s}V_F i_d(n)(t)dt. \tag{47}$$

The reverse recovery loss of the body diode is

$$P_{D\mathrm{sw}}=\frac{1}{2}V_F I_{rp}t_f f_s=V_F Q_{rr}f_s. \tag{48}$$

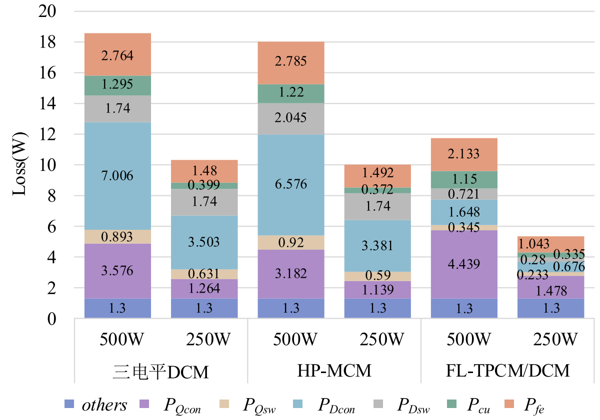


Fig. 22. Comparison of loss distribution.

Iron loss is calculated using the formulas provided in the datasheet by magnetics. The iron loss $P_{\rm fe}$ and copper loss $P_{\rm cu}$ are respectively,

$$P_{\rm fe} = 44.3{B_m}^{1.988} f_s^{1.541} V_{\rm e} \tag{49}$$

$$P_{\rm cu} = f\sum_{n=1}^{f_s/f}\int_0^{T_s} i_L^2(n)(t)R_{L1}dt + f\int_0^{1/f} i_o^2(t)R_{L2}dt. \tag{50}$$

Fig. 22 shows the comparison of loss distribution. It can be seen that because HP-MCM operates near the highest instantaneous power point in HP-TPCM, the current PAR of the inductor is reduced. This results in a slightly larger inductor value on the inverter side compared to conventional DCM. Therefore, the peak current is reduced across the entire operating range, especially in the HP-TPCM operating range. However, since HP-MCM has a narrow operating range and operates in conventional DCM modulation for the rest of the time, the loss in each part of the HP-MCM are slightly lower than those in conventional three-level DCM, though the improvement is limited. The FL-TPCM/DCM significantly expands the TPCM operating range by introducing half-levels, with improved duty cycle utilization, and with the output half-level current flows through two switches, resulting in a slight increase in switch conduction loss, this also leads to both reduced body diode freewheeling duration and current amplitude during zero-level output, resulting in significantly decreased body diode conduction losses. Although the number of FL-TPCM level switches increases, the change in V_{ds} before and after the switching operation is one half and the current amplitude decreases, so the switching loss of the switch is reduced. Thanks to the reduction in PAR and the reduction in inductance value, the inductance loss is reduced accordingly. The overall efficiency has improved significantly.

B. Inverter-Side Inductor Parameters Design

The selection of the inverter-side inductance value directly affects the feasibility of the operational modes analyzed in the previous sections. The waveforms of the maximum average current threshold $I_{\max}$ and minimum average current threshold $I_{\min1}$, $I_{\min2}$ of the FL-TPCM and the current command value $I_{\rm com}(n)$ at rated power are shown in Fig. 12. $I_{\rm com}(n)$ must be less than $I_{\max}$ or the inverter will enter CCM

$$I_{\rm com}(n) \le I_{\max}. \tag{51}$$

The highest instantaneous power point bridge arm needs to output the most energy, if the equal sign holds at this point the fixed-frequency operating range of the FL-TPCM can be maximized

$$\frac{P_o}{V_o}\sqrt{2}\sin(\omega t+\phi) \le \frac{(1-k)^2(V_{\rm dc}-v_o)v_o}{2L_1 f_s V_{\rm dc}} \tag{52}$$

where $v_o = \sqrt{2}\,V_o\sin(\omega t)$, ϕ is the phase difference between the output voltage and current.

The left side of the inequality obtains a maximum at $(\omega t+\phi) = \pi/2$ and the right side obtains a regional minimum at $\omega t = \pi/2$. Let $\omega t = \pi/2$, $\phi = 0$ to obtain:

$$L_1 \le 85.626\ \mu\text{H}. \tag{53}$$

When $I_{\rm com}(n)$ is less than $I_{\min2}$, the inverter needs to be switched to a five-level DCM in order to operate at a fixed-frequency. To minimize the switching of operating modes, the DCM is made to appear only near the output voltage crossing point as much as possible at rated load as

$$I_{\rm com}(n) \ge I_{\min2}. \tag{54}$$

Let $\phi = 0$ and derive both sides of (55) shown at the bottom of the next page; the equality sign holds when the derivatives are equal

$$\omega t = \arcsin\left(\left(\frac{3\sqrt{2}V_{\rm dc}V_o}{2} - \frac{\sqrt{2}P_oL_1f_sV_{\rm dc}}{V_o(1-k)^2}\right)\Big/ 4V_o^2\right). \tag{56}$$

Substituting (56) into (55) with constant iteration yields $\omega t = 0.36319\,\pi$

$$L_1 \ge 66.122\ \mu\text{H}. \tag{57}$$

To summarize, the value range of the inverter-side inductance L_1 is

$$66.122\ \mu\text{H} \le L_1 \le 85.626\ \mu\text{H}. \tag{58}$$

The relationship between the inverter-side inductance value and the fixed-frequency operating range of the FL-TPCM at rated load is shown in Fig. 23. Also, the inductance value affects the duty cycle of the different levels, leading to changes in the current envelope as well as the losses of the various parts. The peak current envelope is approximately linear in the line frequency period, and the relationship between them is obtained by choosing $\omega t = \pi/2$ as the reference point as (59) shown at the bottom of the next page. The relationship between the inverter-side inductance and the maximum current stress and overall loss at rated load is shown in Fig. 24.

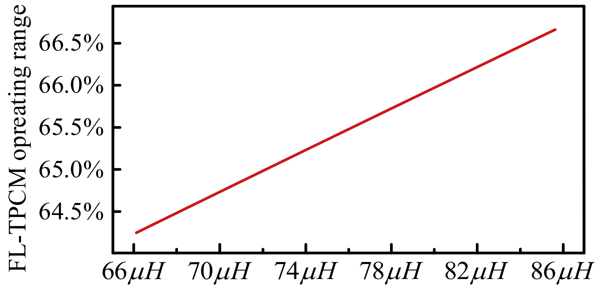


Fig. 23. Relationship between the inverter-side inductance value and the fixed-frequency operating range of the FL-TPCM at rated load.

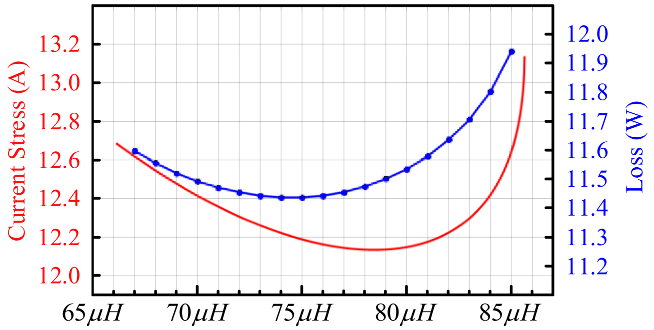


Fig. 24. Relationship between the inverter-side inductance and the maximum current stress and overall loss at rated load.

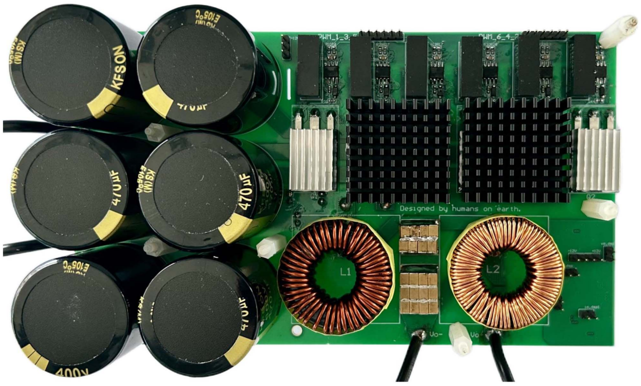


Fig. 25. T-type hybrid-bridge five-level inverter prototype.

TABLE I
MAIN PARAMETERS OF THE PROTOTYPE

Item	Symbol	Value
Input voltage	V_{dc}	200 VDC
Output voltage	V_o	110 VAC
Rated power	P_o	500 W
FL-TPCM/DCM Inverter-side inductor	L_1	77 μH
HP-MCM Inverter-side inductor	L_1	101 μH
DCM Inverter-side inductor	L_1	89 μH
Filter capacitor	C	3.2 μF
Output-side inductor	L_2	410 μH
Switching frequency	f_s	30 kHz
MOSFET output capacitor	C_{oss}	300 pF

In order to minimize the losses as much as possible and at the same time minimize the current stress, the value of inverter-side inductance is selected as

$$L_1 = 77\ \mu\text{H}. \tag{60}$$

IV. EXPERIMENTAL RESULTS

An experimental prototype of a T-type hybrid-bridge five-level inverter, digitally controlled by a DSP TMS320F28335 with a rated power of 500 W, has been constructed as shown in Fig. 25. Use GC3M0065090D for the switch. To verify the superiority of the proposed FL-TPCM/DCM, as well as to make the comparison more reasonable, and HP-MCM, conventional DCM are run on the same prototype, all the parameter settings are identical, the only distinction is the inverter-side inductance value, as for HP-MCM, it aims to maximize the operating range of HP-TPCM, while for DCM, it is to prevent entering CCM at the maximum power point, thus attaining optimal performance. HP-MCM and DCM are realized by disabling switches Q_5 and Q_6. The main parameters of the prototype are given in Table I.

The proposed FL-TPCM/DCM output voltage v_{o} and current i_o waveforms under rated load are shown in Fig. 26. The inverter-side inductor current i_{L1} waveforms and inverter bridge arm output voltage v_{AB} waveforms are shown in Fig. 27, it can be seen that the fixed-frequency operating range of the FL-TPCM is greatly expanded compared with that of the HP-TPCM. The details of mode 2 switching to mode 1 are shown in Fig. 29(a), details of the typical operating point $v_o = V_{\text{dc}}/2 = 100$ V are shown in Fig. 29(b), details of the typical operating point $v_o = \sqrt{2}\, V_o = 155.6$ V are shown in Fig. 29(c).

Fig. 28 shows the inverter-side inductor current i_{L1} and the inverter bridge arm output voltage v_{AB} waveforms when the output current exceeds $\pi/15$ under 3/4 rated load for a typical condition that can demonstrate the four modes at the same time. The details of mode 1 switching to mode 3 are shown

$$\frac{P_o}{V_o}\sqrt{2}\sin(\omega t + \phi) \geq \frac{(V_{\text{dc}} - v_o(\omega t))(v_o(\omega t) - V_{\text{dc}}/2)(1-k)^2}{L_1 f_s V_{\text{dc}}}. \tag{55}$$

$$i_{\text{peak}}(L_1) = \frac{V_{\text{dc}} - v_o}{L_1}\frac{v_o(1-k) - \sqrt{(1-k)^2(V_{\text{dc}} - v_o)v_o - 2\left(\sqrt{2}P_o/V_o\right)L_1 f_s V_{\text{dc}}}}{V_{\text{dc}}}T_s. \tag{59}$$

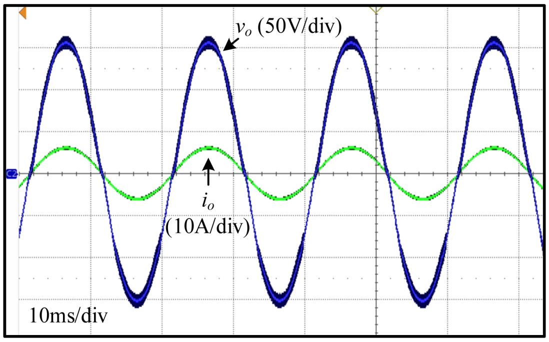


Fig. 26. Output voltage and current waveforms of FL-TPCM/DCM under rated load.

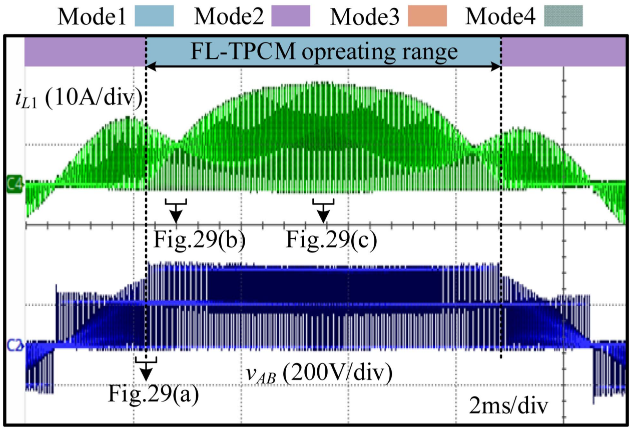


Fig. 27. Inverter-side inductor current and inverter bridge arm output voltage waveforms of FL-TPCM/DCM under rated load.

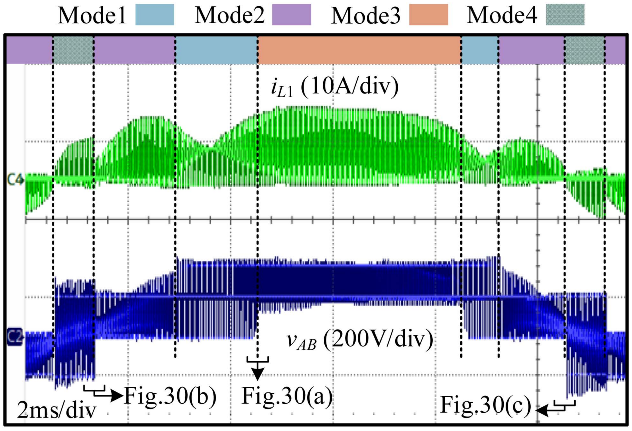


Fig. 28. Inverter-side inductor current and inverter bridge arm output voltage waveforms of FL-TPCM/DCM when output current exceeds $\pi/15$ under 3/4 rated load.

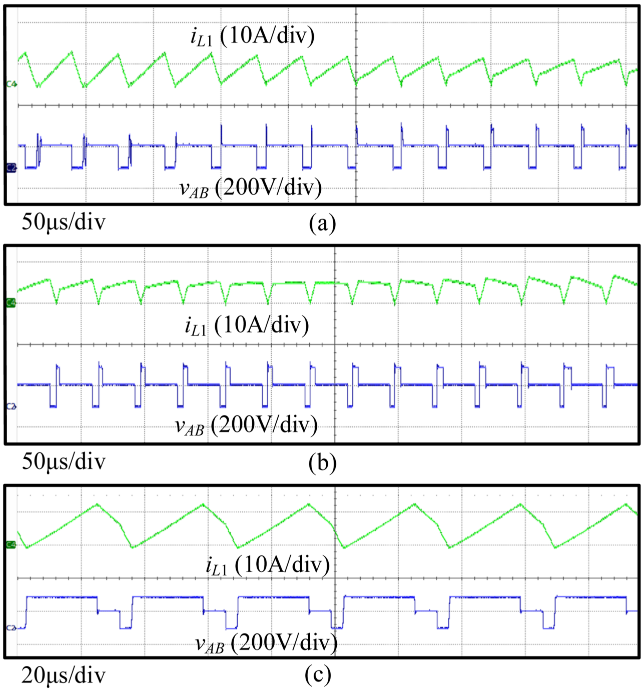


Fig. 29. Typical operating point details at rated load. (a) Mode 2 to Mode 1 Switching. (b) Mode 1 (vo = Vdc/2 = 100V). (c) Mode 1 (vo = √("2")Vo = 155.6V).

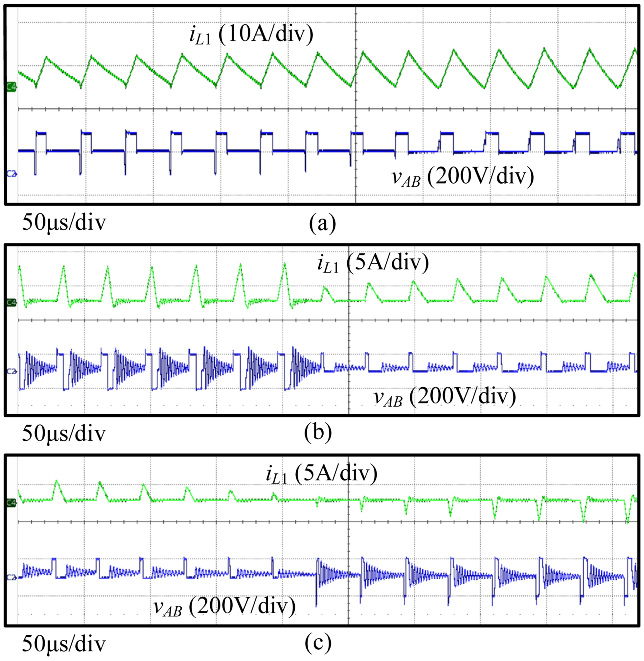


Fig. 30. Typical operating point detail at 3/4 rated load with output current exceeding "π"/15. (a) Mode 1 to Mode 3 Switching. (b) Mode 4 to Mode 2 Switching. (c) Mode 2 to Mode 4 Switching.

in Fig. 30(a), with the details of mode 4 switching to mode 2 are shown in Fig. 30(b), with the details of mode 2 switching to mode 4 are shown in Fig. 30(c). It can be seen that the modulation strategy designed in this article can be smoothly switched between different modes according to the working conditions, and it can also operate safely and reliably under nonpure resistive loads.

The waveform details of the inverter-side inductor current and the main switch drain-source voltage for each mode are shown in Fig. 31, where Fig. 31(a) shows mode 1 ($v_o = V_{\rm dc}/2 = 100$ V)

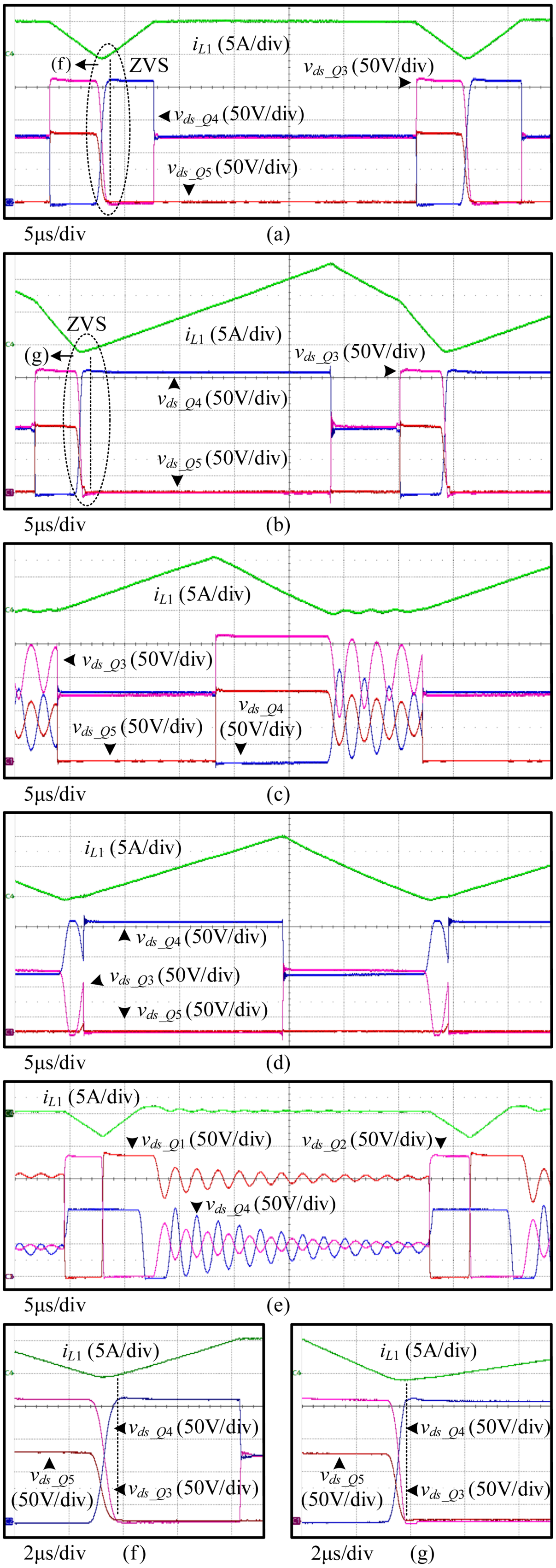


Fig. 31. Waveform details of the inverter-side inductor current and the main switch drain-source voltage for each mode. (a) Mode 1 (vo = Vdc/2 = 100V) at rated load. (b) Mode 1 (vo = √("2")Vo = 155.6V) at rated load. (c) Mode 2 (vo = 65V) at rated load. (d) Mode 3 (vo = √("2")Vo = 155.6V) at 3/4 load. (e) Mode 4 at 3/4 rated load with output current exceeding "π"/15. (f) ZVS details

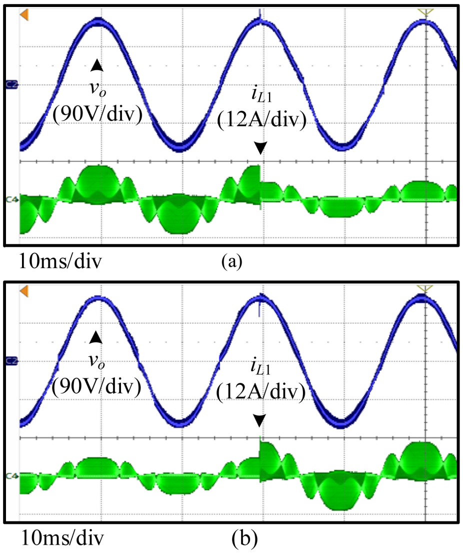


Fig. 32. Dynamic response between full-load and quarter-load. (a) Transition from rated load to quarterload. (b) Transition from quarter-load to rated load.

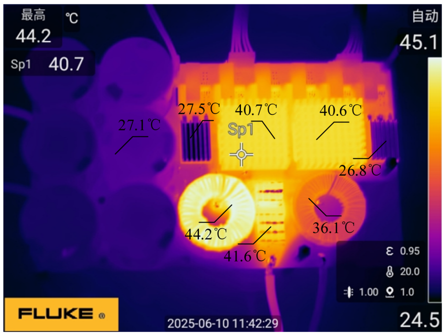


Fig. 33. Infrared thermographic picture of proposed inverter at rated power with heat sink.

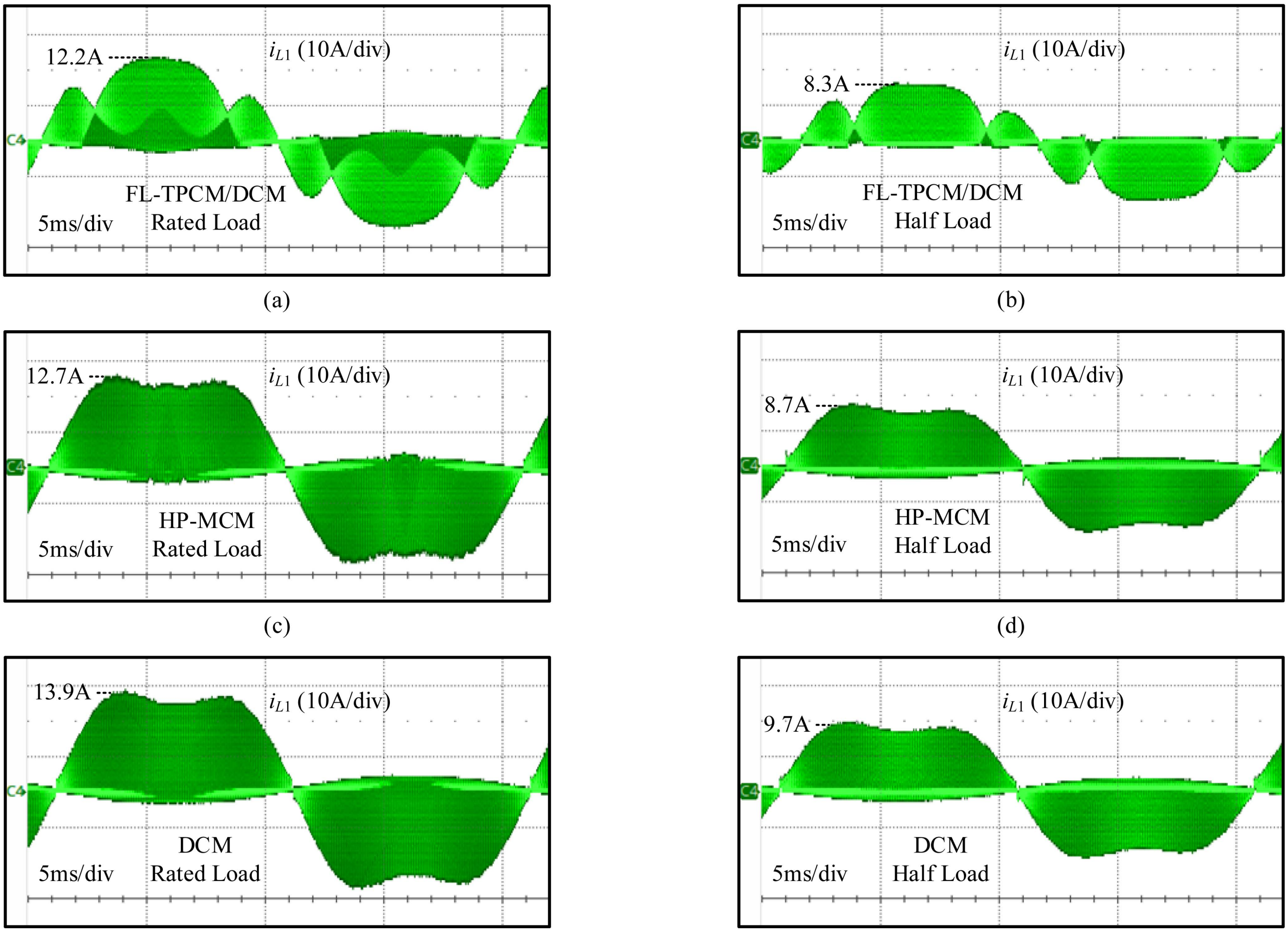
at rated load, Fig. 31(b) shows mode 1 ($v_o = \sqrt{2}\ V_o = 155.6$ V) at rated load, Fig. 31(c) shows mode 2 ($v_o = 65$ V) at rated load, Fig 31(d) shows mode 3 ($v_o = \sqrt{2}\ V_o = 155.6$ V) at 3/4 load, Fig. 31(e) shows mode 4 at 3/4 rated load with output current exceeding $\pi/15$. The waveform details can be seen to be consistent with the previous analysis.

As shown in Fig. 31 that ZCS can be realized in all modes, and ZVS can be realized in mode 1 (FL-TPCM) through reserved fixed dead time for resonant action, details are shown in Fig. 31(f) and (g).

The dynamic response experimental results are shown in Fig. 32. It can be seen that the output voltage of the circuit remains basically stable when transitioning from rated load to quarter-load and from quarter load to rated load demonstrating good dynamic response performance.

Fig. 33 shows the infrared thermographic picture of the inverter during steady-state operation at rated load. The peak temperature of the high-frequency switch is about 40.7 °C, the peak temperature of the inverter side inductor is about 44.2 °C, and the temperature of the filter capacitor is about 41.6 °C, indicating the stability of the prototype's operation.

Fig. 34 shows the inverter-side inductor current waveforms of the proposed FL-TPCM/DCM, HP-MCM, and conventional



(a) (b)

(c) (d)

(e) (f)

Fig. 34. Comparison of inverterside inductor current waveforms of FL-TPCM/DCM, HP-MCM, and conventional DCM. (a) FL-TPCM/DCM under rated load. (b) FL-TPCM/DCM under half load. (c) HP-MCM under rated load. (d) HP-MCM under half load. (e) DCM under rated load. (f) DCM under half load.

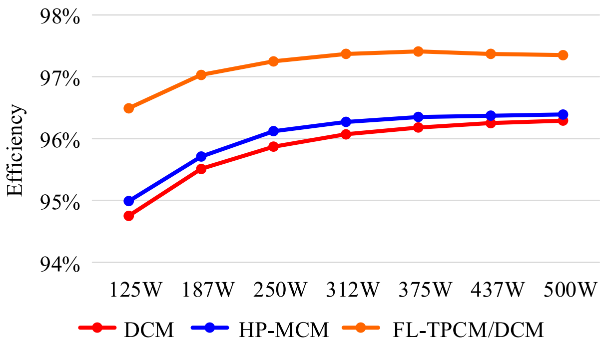


Fig. 35. Comparison of the efficiency curves of the inverter operating in the proposed FL-TPCM/DCM, HP-MCM, and conventional DCM.

reveals that the envelope of the HP-MCM is slightly reduced compared to the conventional DCM, while FL-TPCM/DCM achieves further optimization, leading to reduced current stress and lower switching and inductor losses. A comparison of the efficiency curves of the inverter operating in the proposed FL-TPCM/DCM, HP-MCM, and conventional DCM is shown in Fig. 35. It can be seen that the efficiency of the HP-MCM is slightly improved over the conventional DCM, while the FL-TPCM/DCM is further improved with a peak efficiency of 97.4%. This verifies the effectiveness of reducing the PAR of the inverter-side inductor current through the expansion of the TPCM operating range, consequently lowering switch and inductor losses.

The output voltage harmonic content of the inverter operating at FL-TPCM/DCM, HP-MCM, and conventional DCM is shown in Fig. 36. It can be seen that the THD of FL-TPCM/DCM is lower than that of conventional DCM, but higher than HP-MCM. Since FL-TPCM/DCM improves the duty cycle utilization and reduces the high frequency harmonics generated by resonance during current interruptions, a lower cutoff frequency can be selected when designing the filter thus obtaining higher high frequency harmonic attenuation. However, FL-TPCM/DCM has higher 9th, 11th, and 13th order harmonics. Although HP-MCM introduces a pronounced fifth-order harmonic resulting from the HP-TPCM distribution, its other harmonic orders maintain levels similar to conventional DCM. The comparison between the FL-TPCM/DCM mixed conduction inverter and other MCM

TABLE II
COMPARISON OF FL-TPCM/DCM MIXED CONDUCTION MODE INVERTER WITH OTHER MIXED CONDUCTION MODE INVERTERS

	Operation modes	Topology	Switching frequency	Mode selection criterion	Output power	Output voltage	Efficiency (rated-load)	Output current THD	Inverter-side current PAR
[21]	CCM/DCM	H-bridge	Constant	Duty cycle	1 kW	200 V	97.2%	2.9%	1.41
[22]	BCM/DCM	Flyback inverter	Variable in BCM Constant in DCM	Phase and function of the input power	200 W	230 V	89.1%	3.69%	2
[29]	BCM/TCM/DCM	H-bridge	Variable in BCM/DCM Constant in TCM	Phase and load	2.4 kW	220 V	98.1%	2.75%	2
[30]	FL-TPCM/BCM/CCM	T-type hybrid bridge	Variable	Optimal efficiency	1 kW	220 V	98.4%	2.02%	1
[31]	HP-TPCM/BCM	H-bridge	Variable	ZVS and optimal efficiency	400 W	200 V	96.7%	——	2.87
[27]	HP-TPCM/DCM	H-bridge	Constant	Minimum current stress	800 W	110 V	96.5%	1.29%	2
Proposed	FL-TPCM/DCM	T-type hybrid bridge	Constant	Minimum current stress	500 W	110 V	97.4%	1.63%	1.89

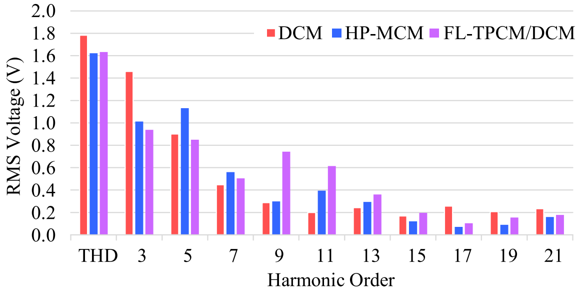


Fig. 36. Comparison of the output voltage harmonic content of FL-TPCM/DCM, HP-MCM, and conventional DCM.

inverters is given in Table II. It can be seen that the proposed FL-TPCM/DCM inverter achieves the highest efficiency under constant switching frequency, simplifies control, and outperforming other MCM inverters in current stress optimization.

V. CONCLUSION

A high-efficiency FL-TPCM/DCM MCM modulation strategy for five-level inverter topology is proposed, FL-TPCM to reduce conduction losses and current stress, applied for medium-to-high loads; FL- DCM as a supplement for fixed switching frequency, suitable for light-to-medium loads; bipolar FL-DCM to provide reactive power and expand application scenarios. It significantly expands the TPCM's fixed-frequency operating range by introducing a half-level, reduces the PAR of inverter-side inductor currents, lowers conduction losses for improved efficiency, and achieves high dc voltage utilization. A 500 W inverter prototype was built. Experimental results show that the proposed FL-TPCM/DCM significantly improves efficiency, achieving a peak efficiency of 97.4%.

APPENDIX

The loss analysis parameters are given in Table III.

The magnetic flux density B_m is calculated as

$$B_m = \left(\frac{a + bH + cH^2}{1 + dH + eH^2}\right)^x. \quad (61)$$

TABLE III
LOSS ANALYSIS PARAMETERS

$R_{\text{ds(on)}}$	65 mΩ
$t_{\text{d(off)}}$	20 ns
t_{f}	8 ns
V_{F}	4.4 V
Q_{rr}	145 nC
R_{L1}	21.5 mΩ
R_{L2}	27.7 mΩ

TABLE IV
INVERTER-SIDE INDUCTOR PARAMETERS

Core	Magnetics 0077550A7
V_{e}	5340 mm^3
L_{e}	81.4 mm
$N_{\text{FL-TPCM/DCM}}$	51
$N_{\text{HP-MCM}}$	55
N_{DCM}	59
a	3.763×10^{-2}
b	1.1712×10^{-2}
c	5.155×10^{-4}
d	9.19×10^{-2}
e	4.909×10^{-4}
x	1.812

where $H = N(i_{\text{peak}}/L_e)$, the inverter-side inductor core parameters are given in Table IV.

REFERENCES

[1] K. Alluhaybi, I. Batarseh, and H. Hu, "Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1310–1329, Jun. 2020.

[2] D. Meneses, F. Blaabjerg, O. Garcia, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic AC module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[4] C. Xiao et al., “A novel single-phase nonisolated dual-input microinverter with active power decoupling,” *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 4437–4448, Mar. 2025.

[5] Y. Chen and D. Xu, “Review of soft-switching topologies for single-phase photovoltaic inverters,” *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1926–1944, Feb. 2022.

[6] X. Guo et al., “Overview of recent advanced topologies for transformerless dual-grounded inverters,” *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12679–12704, Oct. 2022.

[7] W. J. Cha, Y. W. Cho, J. M. Kwon, and B. M. Kwon, “Highly efficient microinverter with soft-switching step-up converter and single-switch-modulation inverter,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3516–3523, Jun. 2015.

[8] R. Samani, D. S. Beyragh, and M. Pahlevani, “A new grid-connected DC/AC inverter with soft switching and low current ripple,” *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4480–4496, May 2019.

[9] H. Zhang, Q. Wang, E. Chu, X. Liu, and L. Hou, “Analysis and implementation of a passive lossless soft-switching snubber for PWM inverters,” *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 411–426, Feb. 2011.

[10] H. Li, K. Wang, J. Fang, and Y. Tang, “Pulse density modulated ZVS full-bridge converters for wireless power transfer systems,” *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 369–377, Jan. 2019.

[11] R. Li, Z. Ma, and D. Xu, “A ZVS grid-connected three-phase inverter,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3595–3604, Aug. 2012.

[12] Y. Xia and R. Ayyanar, “Naturally adaptive, low-loss zero-voltagetransition circuit for high-frequency full-bridge inverters with hybrid PWM,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4916–4933, Jun. 2018.

[13] M. Gao, M. Chen, C. Zhang, and Z. Qian, “Analysis and implementation of an improved flyback inverter for photovoltaic AC module applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3428–3444, Jul. 2014.

[14] S. M. Tayebi, C. Jourdan, and I. Batarseh, “Dynamic dead-time optimization and phase skipping control techniques for three-phase microinverter applications,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7523–7532, Dec. 2016.

[15] H. Yin, T. Lang, X. Li, S. Du, and H. Hu, “A hybrid boundary conduction modulation for a single-phase H-bridge inverter to alleviate zero-crossing distortion and enable reactive power capability,” *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8311–8323, Aug. 2020.

[16] A. Amirahmadi, L. Chen, U. Somani, H. Hu, N. Kutkut, and I. Bartarseh, “High efficiency dual-mode current modulation method for low-power DC/AC inverters,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2638–2642, Jun. 2014.

[17] Q. Zhang, H. Hu, D. Zhang, X. Fang, Z. J. Shen, and I. Bartarseh, “A controlled-type ZVS technique without auxiliary components for the low power DC/AC inverter,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3287–3296, Jul. 2013.

[18] A. Amirahmadi, H. Hu, A. Grishina, F. Chen, J. Shen, and I. Batarseh, “Hybrid control of BCM soft-switching three phase micro-inverter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 4690–4695.

[19] J. Biela, D. Hassler, J. Miniböck, and J. W. Kolar, “Optimal design of a 5kW/dm^3/98.3% efficient TCM resonant transition single-phase PFC rectifier,” in *Proc. Int. Power Electron. Conf.*, 2010, pp. 1709–1716.

[20] Z. Zhang, J. Zhang, and X. K. Wu, “A single phase T-type inverter operating in boundary conduction mode,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.

[21] Z. Zhang, J. Zhang, S. Shao, X. Wu, and K. Sheng, “A novel fixed off-time control method for single-phase micro-inverter without sensing inductor current,” in *Proc. IEEE 3rd Int. Future Energy Electron. Conf. ECCE Asia*, 2017, pp. 1886–1891.

[22] H. N. Le and J. Itoh, “Inductance-Independent nonlinearity compensation for single-phase grid-tied inverter operating in both continuous and discontinuous current mode,” *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4904–4919, May 2019.

[23] G. C. Christidis, A. C. Nanakos, and E. C. Tatakis, “Hybrid discontinuous/boundary conduction mode of flyback microinverter for AC–PV modules,” *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4195–4205, Jun. 2016.

[24] T. Lodh, N. Pragallapati, and V. Agarwal, “An improved control scheme for interleaved flyback converter based micro-inverter to achieve high efficiency,” in *Proc. IEEE 1st Int. Conf. Power Electron., Intell. Control Energy Syst.*, 2016, pp. 1–6.

[25] J. Zhang, R. A. Barrera-Cardenas, T. Isobe, and H. Tadano, “Trapezium current mode (TPCM) boundary operation for single phase grid-tied inverter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1745–1752.

[26] J. Zhang, R. A. Barrera-Cardenas, T. Isobe, and T. Hiroshi, “Evaluation of trapezium current mode in comparison to the discontinuous current mode for single phase Grid-tied inverter,” in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 1125–1132.

[27] Z. Zhang, J. Zhang, and S. Shao, “A novel trapezoidal wave control method for a single-phase grid-tied T-Type inverter,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4711–4722, Apr. 2021.

[28] P. Zhao, Y. Zhang, Q. Guan, and J. M. Guerrero, “Direct charge control for mixed conduction mode grid-connected inverter,” *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 316–331, Jan. 2023.

[29] R. Fernandes and O. Trescases, “A multimode 1-MHz PFC front end with digital peak current modulation,” *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5694–5708, Aug. 2016.

[30] G. Son, Z. Huang, Q. Li, and F. C. Lee, “Analysis and control of critical conduction mode high-frequency single-phase transformerless PV inverter,” *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13188–13199, Nov. 2021.

[31] L. Lin and J. Zhang, “High-efficiency single-phase T-type LCL-filtered inverter with multimode control and smooth mode transition,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 13, no. 1, pp. 954–965, Feb. 2025.

[32] C. Huang, T. Mannen, and T. Isobe, “Current ripple reduction and ZVS realization with optimized DCM modulation based on off-time discrete control for grid-tied inverters,” *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 15835–15851, Oct. 2025.