A Generic SVPWM Method of Suppressing Common-Mode Voltages for Multilevel Converters

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***Abstract*—Multilevel converters are widely used in various industrial applications. One of the critical challenges in these systems is the suppression of common-mode voltage (CMV). Due to the intuitive nature of the space vector diagram, space vector pulsewidth modulation (SVPWM) can effectively regulate CMV. However, as the number of voltage levels in multilevel converters increases, the complexity of the SVPWM method also grows. Existing simplified SVPWM techniques, which are helpful, have not been fully successful in suppressing the CMV. To address the above issues, this article proposes a generic SVPWM (GSVPWM) method. Unlike conventional approaches, the GSVPWM is based on the natural *abc* coordinate system, eliminating the need for coordinate transformations. In addition to effectively suppressing both the magnitude and frequency of the CMV, the GSVPWM further reduces the *dv/dt* values of the CMV by subdividing the equilateral triangular sectors into obtuse triangular sectors. The proposed method operates in real-time, without requiring look-up tables or complex calculations. It is easy to implement across different multilevel converters. Simulations and experiments are conducted in a five-level converter to verify the effectiveness of the proposed GSVPWM.**

***Index Terms*—Common-mode voltage (CMV), multilevel topologies, space vector pulsewidth modulation (SVPWM).**

I. Introduction

In RECENT years, multilevel converters have gained significant attention and have been widely deployed in various medium- and high-voltage industrial applications, such as renewable energy systems, motor drives, and high-voltage direct current transmission [1], [2], [3]. The growing interest in multilevel converters is attributed to their advantageous features, such as lower voltage stress on power switches, higher output voltage capability, and improved output waveform quality [4], [5].

Pulsewidth modulation (PWM) technology is the foundation for the normal operation of multilevel converters. Among various PWM techniques, Sinusoidal PWM (SPWM) is one of the most widely used due to its simplicity and ease of implementation. However, in three-phase systems, SPWM cannot directly achieve full utilization of the dc bus voltage and lacks independent control flexibility for each phase [6]. In contrast, as another widely adopted modulation technique, space vector PWM (SVPWM) can overcome the above limitations in three-phase systems, and it provides more flexibility in selecting redundant switching states, dividing various subsectors, and calculating duty ratios [7].

Common-mode voltage (CMV) is harmful to the system and may cause issues such as electromagnetic interference, bearing currents, and insulation stress [8]. CMV is directly related to the vectors involved in synthesizing the reference voltage vector ($\boldsymbol{V}_{\mathbf{ref}}$). Therefore, by selecting appropriate vectors, it is possible to suppress or even eliminate CMV without introducing additional hardware. Benefiting from the intuitive structure of the space vector diagram, SVPWM enables the precise selection of appropriate vectors, thereby facilitating convenient regulation of the CMV. However, the implementation of SVPWM becomes more complex in multilevel topologies with higher voltage levels [9]. An n-level converter contains $3n^2$-$3n$+1 vectors and $6n^2$-$12n$+6 small sectors. As the number of voltage levels increases, the number of candidate vectors and sectors grows significantly, resulting in a substantial increase in the amount of data that must be prestored in look-up tables [10]. Numerous available vectors have to be processed in real time, making online implementation time-consuming [11].

To address this issue, many studies have proposed simplified SVPWM strategies [12], [13], [14], [15], [16]. In these methods, the identification of sectors or switching states is achieved through online calculations rather than relying on look-up tables. However, these approaches still involve certain coordinate transformations or require complex mathematical operations, such as square root and trigonometric function evaluations. In [17] and [18], simplified SVPWM techniques are proposed that eliminate coordinate transformations by utilizing specific logic-based computations. Nevertheless, none of the methods in [12], [13], [14], [15], [16], [17], [18] consider the CMV suppression. A number of simplified SVPWM strategies have been proposed to

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simultaneously eliminate CMV and reduce the implementation complexity of conventional SVPWM (CSVPWM) in multilevel converters. In [19], [20], [21], different methods are proposed based on various optimal coordinate systems, which eliminate the need for look-up tables in multilevel converters. In all cases, only zero-CMV (ZCMV) vectors are employed to synthesize the $\mathbf{V_{ref}}$, thereby achieving an elimination of CMV. Nevertheless, using only ZCMV vectors inherently limits the maximum dc bus voltage utilization to 86.6% [22]. In addition, unavoidable double commutations within each switching period result in higher switching losses [23].

Employing vectors with low CMV values can avoid the aforementioned issues while suppressing CMV effectively [24]. Several simplified SVPWM methods share this idea. In [25], an additional judgment is added to select reduced-CMV (RCMV) vectors from redundant state combinations based on a *gh*-coordinate system. In [26], an improved 3D SVPWM technique selects offset vectors that are closest to the ZCMV plane, effectively reducing CMV. In [27], an optimized SVPWM based on a 45° coordinate system is proposed to identify the vectors with minimum CMV values. These approaches effectively suppress the CMV without the need for look-up tables, and they are extendable to different multilevel converters. However, these methods primarily focus on magnitude suppression of the CMV while overlooking the *dv*/*dt* values of the CMV. High *dv*/*dt* values of the CMV can cause other serious problems, such as serious leakage currents in motor drive systems or transformless photovoltaic topologies [28].

To the best of our knowledge, limited research has focused on simplifying SVPWM while simultaneously suppressing both the magnitude and *dv*/*dt* values of CMV in multilevel converters. In this article, a novel generic SVPWM (GSVPWM) strategy based on natural *abc*-coordinate system is proposed to address the above issues. Based on the reference signal obtained from the current loop, the proposed GSVPWM applies a unified modulation logic to determine the candidate switching states and their corresponding duty ratios for synthesizing the $\mathbf{V_{ref}}$ within a given multilevel converter.

The proposed method is validated on a five-level active-neutral-point-clamped (5L-ANPC) converter. The key contributions of this work are summarized as follows.

1) The GSVPWM does not involve complex calculations such as square roots and trigonometric functions. It is designed based on a three-phase natural coordinate system, eliminating the need for coordinate transformations.
2) In GSVPWM, the state combinations and coordinate values of the vectors are both calculated online, thus, no look-up tables are needed. The duty ratio is derived based on geometric algebraic analysis, and it is easy to implement.
3) GSVPWM can suppress both the magnitude and *dv*/*dt* values of the CMV. GSVPWM can be applied to different multilevel topologies, and the computational burden is constant according to the theoretical analysis.

The rest of this article is organized as follows. The 5L-ANPC converter is introduced in Section II. The proposed GSVPWM method is presented in detail in Section III. Simulations and experiments are given in Section IV. Finally, Section V concludes the article.

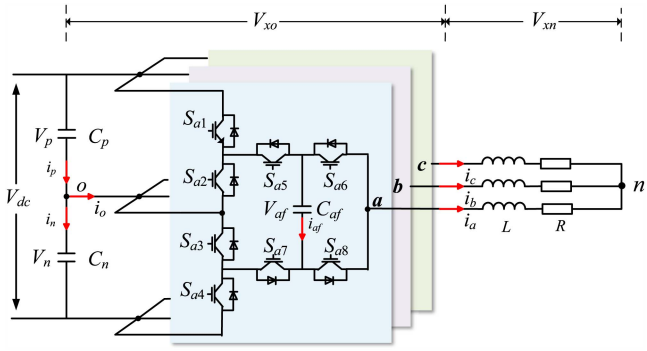


Fig. 1. Topology of the 5L-ANPC converter.

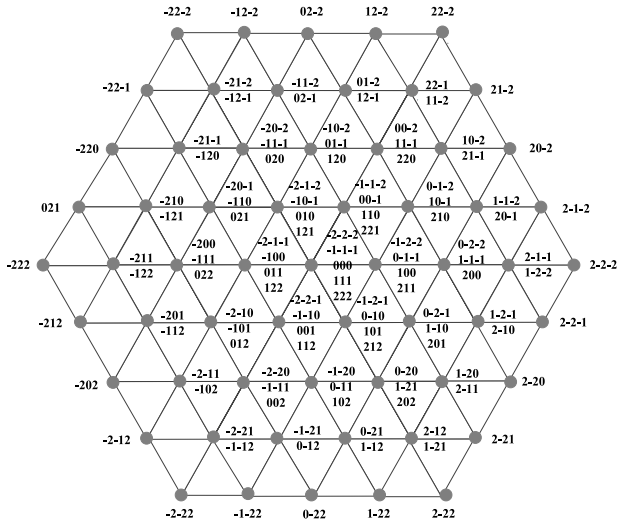


Fig. 2. 125 vectors in the 5L-ANPC converter.

II. Introduction of 5L-ANPC

The topology of the 5L-ANPC converter is shown in Fig. 1. The dc-link voltage is $V_{\rm dc}$. The upper and lower capacitors on dc-link are C_p and C_n, and their voltages are donated as V_p and V_n, respectively. The neutral-point (NP) on dc link is o. i_o is the current flowing out of o. L and R represent the filter and the load, respectively. C_{xf} are the flying capacitors (FC), and the current flows through them are i_{xf}; the voltages of C_{xf} are defined as V_{xf}; the three-phase output currents are i_x; the voltages between the output point x and o as well as between the output point x and the three-phase common point n are defined as V_{xo} and V_{xn} ($x = a, b, c$).

The five output voltages are -1/4$V_{\rm dc}$, -1/2$V_{\rm dc}$, 0, 1/4$V_{\rm dc}$, and 1/2$V_{\rm dc}$, and they can be written as the switching state -2, -1, 0, 1, and 2, respectively. Therefore, the 5L-ANPC converter has 125 (5^3) vectors as shown in Fig. 2.

In the open-loop condition, the three-phase modulation waveforms u_{rx} ($x = a, b, c$) can be expressed as

$$\begin{cases} u_{ra} = \frac{\sqrt{3}m}{3}\sin\theta \\ u_{rb} = \frac{\sqrt{3}m}{3}\sin(\theta - \frac{2\pi}{3}) \\ u_{rc} = \frac{\sqrt{3}m}{3}\sin(\theta + \frac{2\pi}{3}) \end{cases} \tag{1}$$

where m is the modulation index and θ is the initial phase angle.

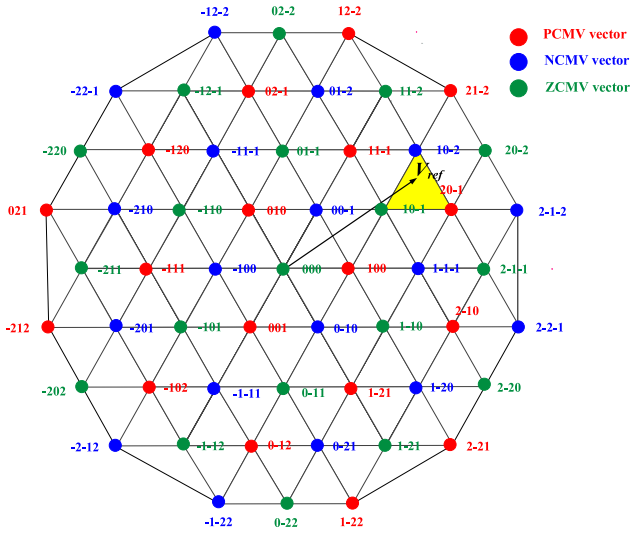


Fig. 3. 55 vectors with low CMV values.

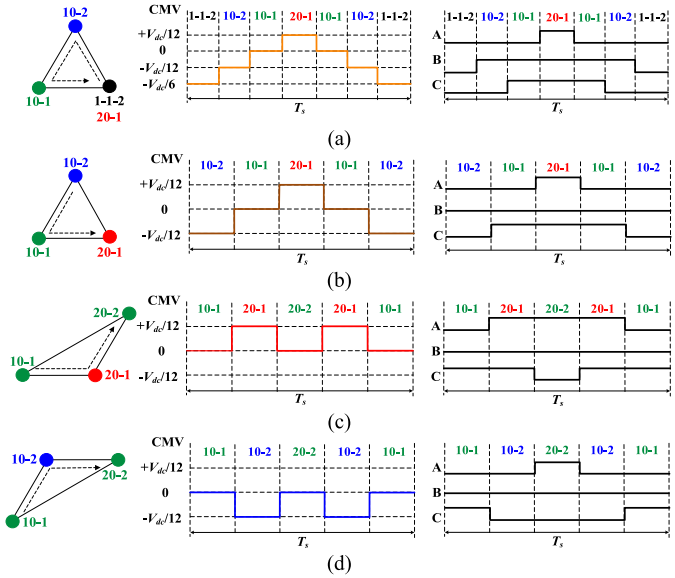


Fig. 4. Sequences and CMV. (a) CSVPWM. (b) Reduced CMV SVPWM. (c) Using ZCMV and PCMV. (d) Using ZCMV and NCMV.

III. GSVPWM Strategy

A. Mechanism of Suppressing CMV

The CMV is defined as

$$\mathrm{CMV} = \frac{1}{3}\sum_{x=a,b,c} V_{xo}. \tag{2}$$

According to (2), there are a total of 13 different CMV values in the 5L-ANPC converter: -1/2V_{dc}, -5/12V_{dc}, -1/3V_{dc}, -1/4V_{dc}, -1/6V_{dc}, -1/12V_{dc}, 0, 1/12V_{dc}, 1/6V_{dc}, 1/4V_{dc}, 1/3V_{dc}, 5/12V_{dc}, and 1/2V_{dc}. In order to suppress the magnitude of the CMV, the vectors with small CMV values should first be selected. Therefore, the CMV values with +1/12V_{dc}, -1/12V_{dc}, and 0 are selected, and they are defined as positive CMV (PCMV), negative CMV (NCMV), and zero CMV (ZCMV), respectively, as shown in Fig. 3. In SVPWM, the most commonly used approach is to use a symmetric sequence formed by multiple vectors. Different vectors often have different CMV values, thereby CMV will switch in high frequencies per control period (T_s), resulting in high *dv/dt* values of the CMV. Therefore, in addition to the magnitude of the CMV, its *dv/dt* values also need to be suppressed.

Assuming that the reference voltage $\boldsymbol{V}_{\mathbf{ref}}$ is located in the yellow area in Fig. 3. The CMV formed by the seven-segment sequences in CSVPWM is shown in Fig. 4(a). It can be observed that the magnitude of the CMV is 1/4 V_{dc}, and the CMV changes six times per T_s. Therefore, CSVPWM cannot suppress the CMV effectively. The reduced CMV SVPWM method uses five-segment sequences to suppress the CMV. Its CMV changes four times between NCMV and PCMV, and its magnitude is 1/6 V_{dc} per T_s as shown in Fig. 4(b). Therefore, the magnitude of the CMV is suppressed compared to conventional methods. However, the *dv/dt* of the CMV needs to be further considered. To address the above issue, two different sequences are designed as shown in Fig. 4(c) and (d). In the new subsector, the CMV is also changed four times in both subsectors, but the range is between ZCMV and PCMV or ZCMV and NCMV per T_s, which further reduces the *dv/dt* of the CMV. The proposed space vector diagram with novel subsectors is shown in Fig. 5.

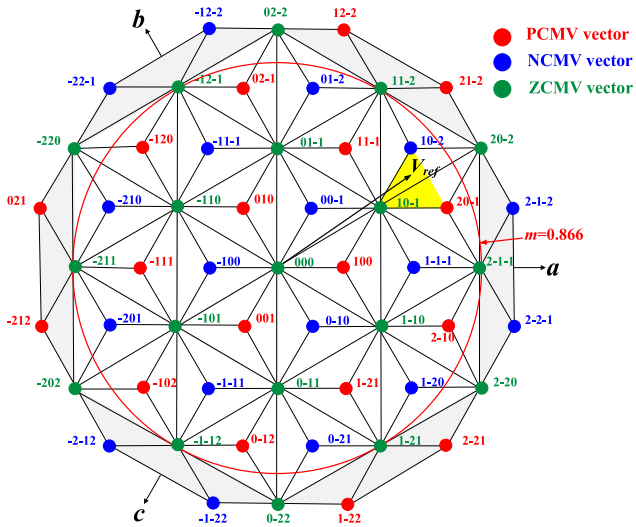


Fig. 5. Proposed novel subsectors.

B. Determine Vectors

In SVPWM, the common approach to divide and select the sub-sector is based on the coordinates of vectors. Conventional methods simplify the coordinates of the vector and the sector determination through various coordinate transformations. However, this requires a look-up table containing information such as vector coordinates and states. When facing other topologies with different voltage levels, the look-up table needs to be upgraded. Other simplified SVPWM methods can be used to different multilevel converters with look-up tables, but their

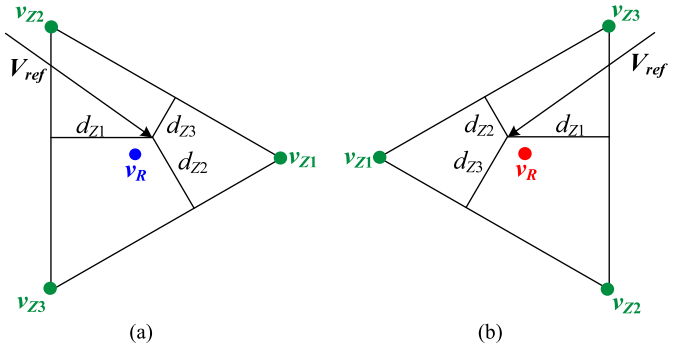


Fig. 6. Two types of triangular sector. (a) S_r. (b) S_l.

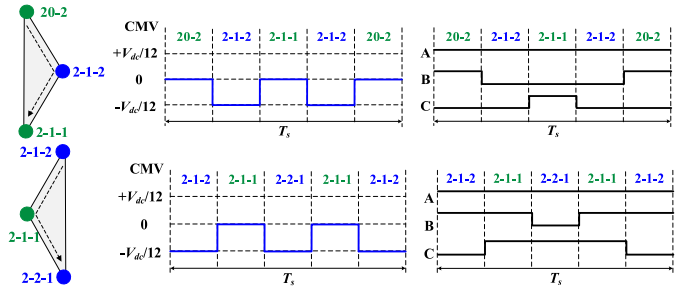


Fig. 7. Principle of CMV suppression in −30° to +30° sector.

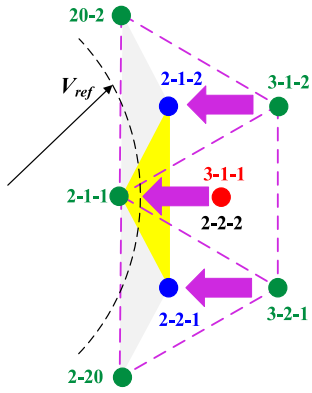


Fig. 8. State combinations in −30° to +30° sector after adding a saturation to suppress the CMV.

subsectors are still based on conventional equilateral triangles rather than obtuse triangles. To address the above issue, a natural *abc*-coordinate system is proposed in this article.

The direction of *abc* coordinate system is shown in Fig. 5. Here, an interesting conclusion can be found: The coordinates of the ZCMV vector are the same as their state combinations in the natural *abc* coordinate system. In other words, as long as the coordinates of ZCMV vectors are determined, their corresponding state combinations can also be determined. Through this idea, the relationship between state combinations and coordinates of ZCMV vectors is revealed.

The round-down value u_{fx} of u_{rx} is expressed as

$$u_{fx} = floor(u_{rx})(x = a, b, c) \tag{3}$$

where floor () is the round-down function.

There are two types of triangular sector (S_r and S_l) formed by three ZCMV vectors, as shown in Fig. 6, and they can be determined by

$$S = \begin{cases} S_r & \text{if } \sum_{\mathrm{x=a,b,c}} \mathrm{u_{fx}} = -1 \\ S_l & \text{if } \sum_{\mathrm{x=a,b,c}} \mathrm{u_{fx}} \neq -1 \end{cases}. \tag{4}$$

Based on the sector where $\boldsymbol{V_{ref}}$ is located, the coordinates of the three closest ZCMV vectors ($\boldsymbol{v_{Z1}}, \boldsymbol{v_{Z2}}, \boldsymbol{v_{Z3}}$) can be obtained from

$$\begin{array}{ll} \text{if } S = S_r & \text{if } S = S_l \\ \begin{cases} \boldsymbol{v_{Z1}} = (u_{fa} + 1 u_{fb} u_{fc}) \\ \boldsymbol{v_{Z2}} = (u_{fa} u_{fb} + 1 u_{fc}) \\ \boldsymbol{v_{Z3}} = (u_{fa} u_{fb} u_{fc} + 1) \end{cases} & \begin{cases} \boldsymbol{v_{Z1}} = (u_{fa} u_{fb} + 1 u_{fc} + 1) \\ \boldsymbol{v_{Z2}} = (u_{fa} + 1 u_{fb} u_{fc} + 1) \\ \boldsymbol{v_{Z3}} = (u_{fa} + 1 u_{fb} + 1 u_{fc}) \end{cases} \end{array}. \tag{5}$$

As mentioned earlier, once the coordinates of the three ZCMV vectors are determined, their state combinations are obtained simultaneously, so the values in (5) are also the state combinations of the ZCMV vectors.

Case 1: When m <0.866

As shown in Fig. 5, in every equilateral triangle surrounded by three closet ZCMV vectors, there always exists a PCMV or NCMV vector when m<0.866. Define PCMV and NCMV as RCMV. According to the different types of triangular sectors in (4), the state combination of the RCMV vector ($\boldsymbol{v_R}$) can be obtained from

$$\begin{array}{ll} \text{if } S = S_r & \text{if } S = S_l \\ \boldsymbol{v_R} = (u_{fa} u_{fb} u_{fc}) & \boldsymbol{v_R} = (u_{fa} + 1 u_{fb} + 1 u_{fc} + 1). \end{array} \tag{6}$$

Case 2: When m >0.866

The red circle represents $m = 0.866$ as shown in Fig. 5. When m>0.866, which is the gray area in Fig. 3, there exist sequences that also conform to Fig. 4(c) and (d). Take the sector from -30° to +30° as an example, like as shown in Fig. 7.

To suppress CMV without adding additional complex calculations, this article adds a limiter to achieve the above goals. The limiter such as a saturation module is set as

$$|p| = \frac{n-1}{2} \tag{7}$$

where n is the maximum number of voltage levels. For the 5L-ANPC converter, n equals 5 and p equals ±2.

After adding a saturation, for example, the PCMV vector 3-1-1 is changed to 2-1-1 instead of the previous 2-2-2, as shown in Fig. 8, so the high CMV can be avoided. But at this time, the state combination is changed as purple arrows indicated, $\boldsymbol{V_{ref}}$ cannot be accurately synthesized, which will cause little current peak distortions. But $m = 0.866$ is already a relatively high modulation index. And when m just exceeds 0.866, it will only pass through a small part of the yellow triangle in Fig. 8, thereby the current peak distortions will be at least $m = 0.9$. Moreover, GSVPWM is a real-time algorithm; setting a limiter will ensure that the GSVPWM can generate appropriate PWM

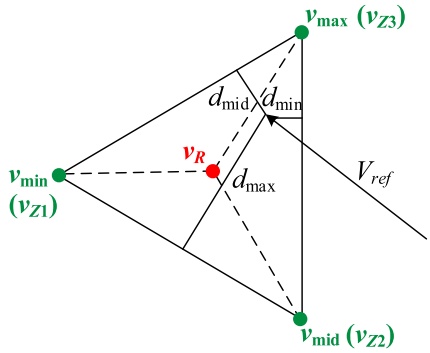


Fig. 9. $v_{\min}$, v_{mid}, and $v_{\max}$ and their duty ratios in S_r.

signals. After adding the limiter in (7), the proposed GSVPWM can operate effectively over the full m range from 0 to 1.

C. Calculate Duty Ratios

Define the difference between u_{fx} and u_{rx} as

$$\Delta u_{fx} = u_{fx} - u_{rx}(x = a, b, c). \tag{8}$$

In fact, the duty ratios of the three ZCMV vectors are proportional to the distance from $\boldsymbol{V_{\mathrm{ref}}}$ to the three sides of the equilateral triangle surrounded by three ZCMV vectors. After (3), the height of this triangle is normalized to 1. Therefore, the duty ratios of the three ZCMV vectors, as shown in Fig. 6, can be expressed as

$$\begin{array}{ll} \text{if} S = S_l & \text{if} S = S_r \\ \begin{cases} d_{Z1} = 1 - \Delta u_{fa} \\ d_{Z2} = 1 - \Delta u_{fb} \\ d_{Z3} = 1 - \Delta u_{fc} \end{cases} & \begin{cases} d_{Z1} = \Delta u_{fa} \\ d_{Z2} = \Delta u_{fb} \\ d_{Z3} = \Delta u_{fc} \end{cases} \end{array}. \tag{9}$$

Each equilateral triangle formed by three ZCMV vectors can be divided into three novel subsectors, as shown in Fig. 5. Therefore, the three vectors for synthesizing $\boldsymbol{V_{\mathrm{ref}}}$ in a novel subsector must be $\boldsymbol{v_R}$ and two ZCMV vectors, which means that one ZCMV vector among $\boldsymbol{v_{Z1}}$, $\boldsymbol{v_{Z2}}$, and $\boldsymbol{v_{Z3}}$ needs to be discarded. In order to achieve this, the duty ratios of $\boldsymbol{v_{Z1}}$, $\boldsymbol{v_{Z2}}$, and $\boldsymbol{v_{Z3}}$ are ordered first, which are expressed as

$$\begin{cases} d_{\min} = \min(d_{Z1}, d_{Z2}, d_{Z3}) \\ d_{\mathrm{mid}} = \mathrm{mid}(d_{Z1}, d_{Z2}, d_{Z3}) \\ d_{\max} = \max(d_{Z1}, d_{Z2}, d_{Z3}) \end{cases}. \tag{10}$$

Define the ZCMV vectors corresponding to the duty ratio $d_{\min}$, d_{mid}, and $d_{\max}$ as $\boldsymbol{v_{\min}}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$ as shown in Fig. 9, respectively. According to (9), the ZCMV vector $\boldsymbol{v_{\min}}$ corresponding to $d_{\min}$ is discarded when synthesizing $\boldsymbol{V_{\mathrm{ref}}}$. In other words, the ZCMV vector $\boldsymbol{v_{\min}}$ with the smallest duty ratio will be discarded. At this time, $\boldsymbol{V_{\mathrm{ref}}}$ is located in the triangular sector formed by $\boldsymbol{v_R}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$. Then, the duty ratios of $\boldsymbol{v_R}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$ need to be derived.

Based on the above analysis, $\boldsymbol{V_{\mathrm{ref}}}$ can be synthesized by $\boldsymbol{v_R}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$. Define their duty ratios as d_R, $d_{Z\mathrm{mid}}$, and $d_{Z\max}$, respectively. According to the voltage-second balance principle, $\boldsymbol{V_{\mathrm{ref}}}$ can be obtained from

$$\begin{cases} d_R + d_{Z\mathrm{mid}} + d_{Z\max} = 1 \\ \boldsymbol{v_R} \cdot d_R + \boldsymbol{v_{\mathrm{mid}}} \cdot d_{Z\mathrm{mid}} + \boldsymbol{v_{\max}} \cdot d_{Z\max} = \boldsymbol{V_{ref}} \end{cases}. \tag{11}$$

The same $\boldsymbol{V_{\mathrm{ref}}}$ can also be synthesized by $\boldsymbol{v_{\min}}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$. According to the voltage-second balance principle, it holds

$$\begin{cases} d_{\max} + d_{\mathrm{mid}} + d_{\min} = 1 \\ \boldsymbol{v_{\max}} \cdot d_{\max} + \mathbf{v_{mid}} \cdot d_{\mathrm{mid}} + \boldsymbol{v_{\min}} \cdot d_{\min} = \boldsymbol{V_{\mathrm{ref}}} \end{cases}. \tag{12}$$

Define $\Delta d_{\max}$ and Δd_{mid} as

$$\begin{cases} \Delta d_{\max} = d_{\max} - d_{\min} \\ \Delta d_{\mathrm{mid}} = d_{\mathrm{mid}} - d_{\min} \end{cases}. \tag{13}$$

Substituting (13) into (12), it holds

$$\begin{aligned} &\boldsymbol{v_{\max}} \cdot d_{\max} + \boldsymbol{v_{\mathrm{mid}}} \cdot d_{\mathrm{mid}} + \boldsymbol{v_{\min}} \cdot d_{\min} \\ &= \boldsymbol{v_{\max}} \cdot (\Delta d_{\max} + d_{\min}) + \boldsymbol{v_{\mathrm{mid}}} \cdot (\Delta d_{\mathrm{mid}} + d_{\min}) \\ &\quad + \boldsymbol{v_{\min}} \cdot d_{\min} \\ &= d_{\min} \cdot (\boldsymbol{v_{\max}} + \boldsymbol{v_{\mathrm{mid}}} + \boldsymbol{v_{\min}}) + \boldsymbol{v_{\max}} \cdot \Delta d_{\max} \\ &\quad + \boldsymbol{v_{\mathrm{mid}}} \cdot \Delta d_{\mathrm{mid}}. \end{aligned} \tag{14}$$

$\boldsymbol{v_R}$ is the center of an equilateral triangle formed by vectors $\boldsymbol{v_{Z1}}$, $\boldsymbol{v_{Z2}}$, and $\boldsymbol{v_{Z3}}$ as shown in Fig. 9, thereby v_R satisfies

$$\boldsymbol{v_R} = \frac{\boldsymbol{v_{\max}} + \boldsymbol{v_{\mathrm{mid}}} + \boldsymbol{v_{\min}}}{3}. \tag{15}$$

Substituting (15) into (14), it yields

$$\begin{aligned} &d_{\min} \cdot (\boldsymbol{v_{\max}} + \boldsymbol{v_{\mathrm{mid}}} + \boldsymbol{v_{\min}}) + \boldsymbol{v_{\max}} \cdot \Delta d_{\max} \\ &\quad + \boldsymbol{v_{\mathrm{mid}}} \cdot \Delta d_{\mathrm{mid}} \\ &= 3d_{\min} \cdot \left(\frac{\boldsymbol{v_{\max}} + \boldsymbol{v_{\mathrm{mid}}} + \boldsymbol{v_{\min}}}{3} \right) + \boldsymbol{v_{\max}} \cdot \Delta d_{\max} \\ &\quad + \boldsymbol{v_{\mathrm{mid}}} \cdot \Delta d_{\mathrm{mid}} \\ &= \boldsymbol{v_R} \cdot 3d_{\min} + \boldsymbol{v_{\mathrm{mid}}} \cdot \Delta d_{\mathrm{mid}} + \boldsymbol{v_{\max}} \cdot \Delta d_{\max}. \end{aligned} \tag{16}$$

Combining (16) and (11), the duty ratios of $\boldsymbol{v_R}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$ are expressed as

$$\begin{cases} d_R = 3d_{\min} \\ d_{Z\mathrm{mid}} = \Delta d_{\mathrm{mid}} = d_{\mathrm{mid}} - d_{\min} \\ d_{Z\max} = \Delta d_{\max} = d_{\max} - d_{\min} \end{cases}. \tag{17}$$

The sum of d_R, $d_{Z\mathrm{mid}}$, and $d_{Z\max}$ is

$$\begin{aligned} &d_R + d_{Z\mathrm{mid}} + d_{Z\max} \\ &\quad = d_{\max} + d_{\mathrm{mid}} + d_{\min} = 1. \end{aligned} \tag{18}$$

According to (13) and (18), $\Delta d_{\max}$ and Δd_{mid} are always non-negative, and the sum of d_R, $d_{Z\mathrm{mid}}$, and $d_{Z\max}$ is 1. Therefore, the duty ratios obtained from (17) are reasonable. By sorting the duty ratios in (10) and requiring a simple calculation in (17), the accurate duty ratios of $\boldsymbol{v_R}$, $\boldsymbol{v_{\mathrm{mid}}}$, and $\boldsymbol{v_{\max}}$ to synthesize $\boldsymbol{V_{\mathrm{ref}}}$ can be obtained. Sector S_l also follows this principle.

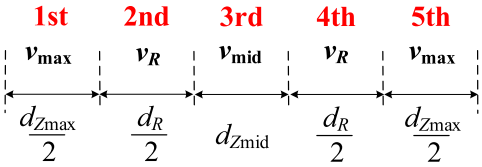


Fig. 10. Order of three candidate vectors in each five-segment sequence.

TABLE I
SWITCHING COMBINATIONS OF 5L-ANPC CONVERTERS

Switching combination	V_{xo}	Switching state	$(S_{x1}, S_{x3}, S_{x5}, S_{x6})$	i_o	i_{xf}
SC_{x1}	$-V_{dc}/2$	-2	(0,0,0,0)	0	0
SC_{x2}	$-V_{dc}/4$	-1	(0,0,0,1)	0	$-i_x$
SC_{x3}			(0,0,1,0)	i_x	i_x
SC_{x4}	0	0	(0,0,1,1)	i_x	0
SC_{x5}			(1,1,0,0)	i_x	0
SC_{x6}	$V_{dc}/4$	1	(1,1,0,1)	i_x	$-i_x$
SC_{x7}			(1,1,1,0)	0	i_x
SC_{x8}	$V_{dc}/2$	2	(1,1,1,1)	0	0

D. Design Five-Segment Sequences

After determining three vectors $\boldsymbol{v_R}$, $\boldsymbol{v_{mid}}$, and $\boldsymbol{v_{max}}$, it is necessary to design their order to reduce switching losses. As analyzed in the previous part, the selected three vectors must be one RCMV vector and two ZCMV vector, which means $\boldsymbol{v_{mid}}$ and $\boldsymbol{v_{max}}$ must be two vectors among $\boldsymbol{v_{Z1}}$, $\boldsymbol{v_{Z2}}$, and $\boldsymbol{v_{Z3}}$. Observing (5) and (6), it can be concluded that whether in S_r or S_l, when $\boldsymbol{v_R}$ is located in the middle of two ZCMV vectors, it can be ensured that the adjacent vector states switch once during each control period, achieving the same switching sequence as shown in Fig. 4(c) and (d). In the symmetric sequence, vector $\boldsymbol{v_{max}}$ is defined as the first vector. Therefore, in a five-segment symmetrical sequence formed by $\boldsymbol{v_R}$, $\boldsymbol{v_{mid}}$, and $\boldsymbol{v_{max}}$, $\boldsymbol{v_R}$ is located in the second and fourth positions; the first and fifth positions are vector $\boldsymbol{v_{max}}$ corresponding to $d_{Z\max}$; the middle position is vector $\boldsymbol{v_{mid}}$ corresponding to $d_{Z\mathrm{mid}}$, as shown in Fig. 10.

E. Capacitor Voltage Balancing

The capacitor voltages in the 5L-ANPC inverter are easy to balance. 5L-ANPC converters have eight switching combinations on each leg as listed in Table I. By switching them, the FC voltage (FCV) and the NP voltage (NPV) can be balanced properly.

The voltage difference between V_{xf} and the required value $V_{\mathrm{dc}}/4$ are expressed as

$$\Delta V_{xf} = V_{xf} - \frac{V_{dc}}{4} (x = a, b, c). \tag{19}$$

The voltage difference between V_n and V_p is expressed as

$$\Delta V_{np} = V_n - V_p. \tag{20}$$

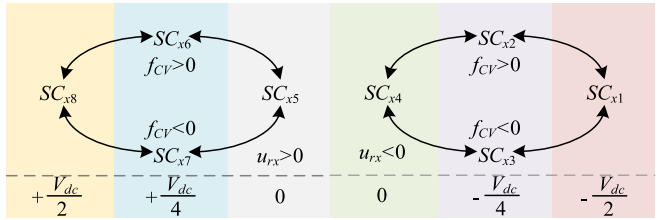


Fig. 11. Principle of selecting switching combinations.

The balancing factors of FCV and NPV are defined as

$$\begin{cases} f_{FC} = \Delta V_{xf} \cdot i_x \\ f_{NP} = \Delta V_{np} \cdot i_x \cdot u_{rx} \end{cases} (x = a, b, c). \tag{21}$$

Based on the sign of (21), the appropriate switching combinations can be selected to balance the NPV and FCV. When $V_{xo} = \pm V_{\mathrm{dc}}/4$, the redundant switching combinations SCx_2 and SCx_3, SCx_6 and SCx_7 have opposite direction of i_{xf}, which can be used to balance FCV. The FCV can only be balanced by its own leg. Therefore, the FCV should have a higher priority than NPV. Only when the FCV is balanced properly, can the NPV be balanced. Thus, a threshold K needs to be set. The above idea can be expressed as

$$f_{CV} = \begin{cases} f_{FC}, |\Delta V_{xf}| \geq K \\ f_{NP}, |\Delta V_{xf}| < K \end{cases} K \geq 0. \tag{22}$$

When $V_{xo} = 0$, the redundant switching combinations SC_{x4} and SC_{x5} need to be further selected. According to Table I, the four power devices (S_{x1}–S_{x4}) on the dc-side work under fundamental frequency, whereas the other four switches (S_{x5}–S_{x8}) around the FC work under high frequency. In order to maintain this advantage, SC_{x4} and SC_{x5} should be distinguished based on the sign of the modulation signal u_{rx}. Besides, the switching losses also need to be reduced by designing the order of switching combinations. For example, switching between SC_{x2} and SC_{x3} is not allowed since both S_{x5} and S_{x6} act; switching between SC_{x1} and SC_{x2} is allowed since only S_{x6} acts. Therefore, the order of the switching combinations and the capacitor voltage balancing strategy as illustrated in Fig. 11.

A flowchart of the GSVPWM strategy is illustrated in Fig. 12, where it is observed that the GSVPWM can be extended to any different multilevel topology by changing the capacitor voltage balancing strategy and setting a suitable parameter p. When the GSVPWM strategy is applied to other multilevel topologies, the SC selection part of the 5L-ANPC can be replaced with the corresponding SC principle specific to the target topology.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental parameters are listed in Table II. The proposed GSVPWM is compared with Method-1 and Method-2 described in [12] and [27], respectively. The simulation is conducted in MATLAB/Simulink. dSPACE is adopted as the main controller, and the experimental platform is shown in Fig. 13. The dead-time is 2 μs, and the CMV is calculated by phase voltages in the experiment.

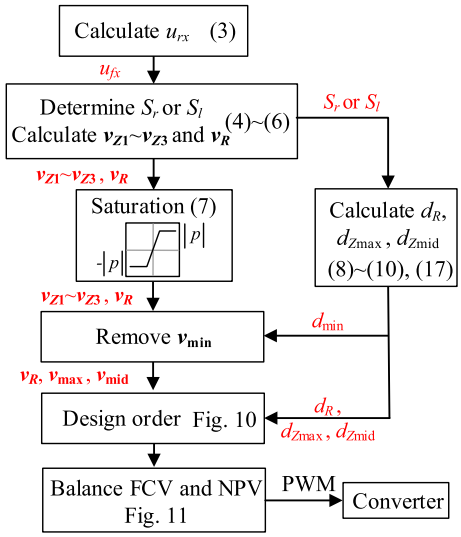


Fig. 12. Flowchart of the GSVPWM method.

TABLE II
PARAMETERS FOR SIMULATIONS AND EXPERIMENTS

DC-link voltage (V_{dc})	100 V
DC-link capacitor (C_p, C_n)	3000 μF
Flying capacitor (C_{xf})	1000 μF
Fundamental frequency (f)	50 Hz
Load (R)	8 Ω
Filter (L)	3.5 mH
Control period (T_s)	100 μs
K in equation (22)	2 V
Parasitic capacitor (C_{pr})	100 nF

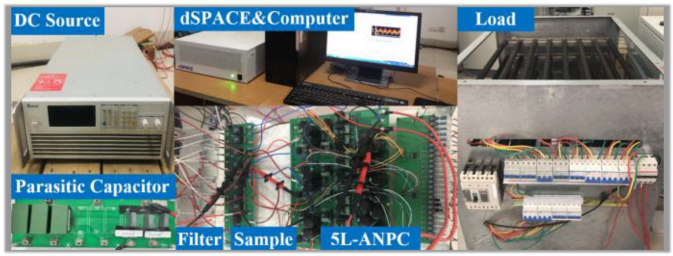


Fig. 13. Experimental platform of the 5L-ANPC converter.

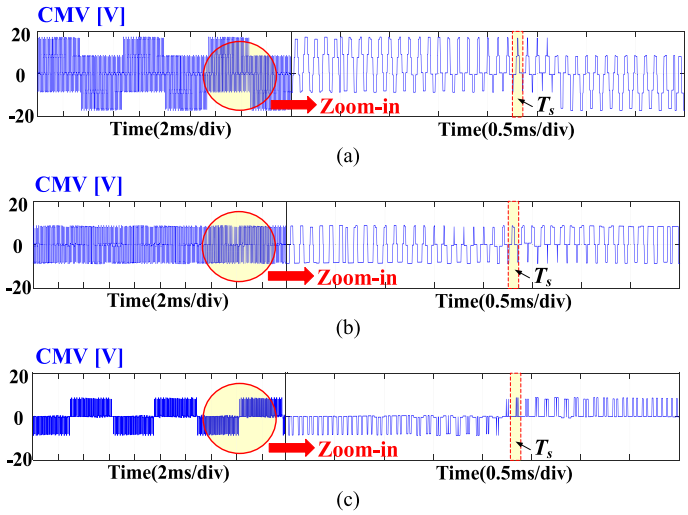


Fig. 14. Simulated results of CMV when $m = 0.4$. (a) Method-1. (b) Method-2. (c) GSVPWM.

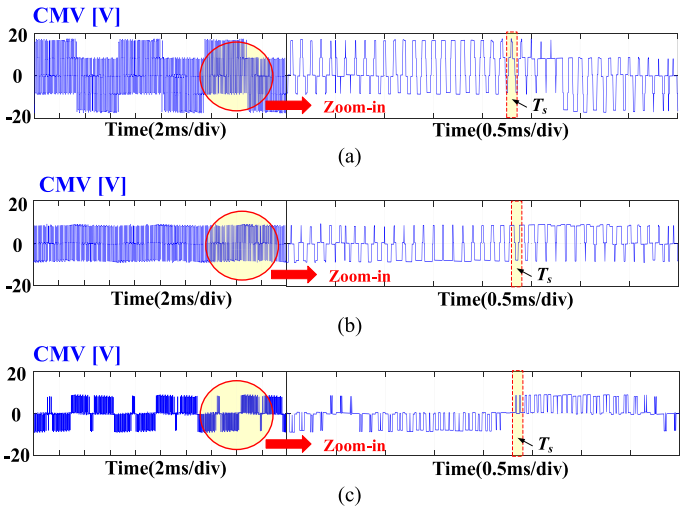


Fig. 15. Simulated results of CMV when $m = 0.8$. (a) Method-1. (b) Method-2. (c) GSVPWM.

A. Simulation Results

1) Analyzing CMV: When $m = 0.4$, Method-1 shows a high magnitude of the CMV, and its CMV changes six times per T_s as shown in Fig. 14(a). Method-2 can reduce the magnitude and the frequency of the CMV compared to Method-1, as shown in Fig. 14(b). Its CMV changes four times per T_s between +8.3 V (+1/12V_{dc}) and -8.3 V (-1/12V_{dc}). The CMV of GSVPWM also changes four times per T_s, as shown in Fig. 14(c), which means the frequency of the CMV of Method-2 and GSVPWM is the same. But the magnitude of the CMV is between +1/12V_{dc} and 0 or -1/12V_{dc} and 0, so its dv/dt values of the CMV are lower than Method-2's.

When m reaches 0.8 as shown in Fig. 15, the magnitude, frequency, and dv/dt values of the CMV of the three methods are similar to the performance when $m = 0.4$. This is because when m<0.866, the candidate vectors that participate in the synthesis of the $\boldsymbol{V}_{\mathbf{ref}}$ have the same CMV values. When m reaches 0.9, the peak values of the CMV of Method-1 and Method-2 increase as shown in Fig. 16(a) and (b). At this time, the number of redundant vectors decreases as m increases. Method-1 and Method-2 are forced to select vectors with high CMV. For example, Method-1 may select 1-2-2 with CMV -1/4V_{dc} while Method-2 may select 2-2-2 with CMV -1/6V_{dc} as shown in Fig. 2. Due to the saturation module in (7) and Fig. 12, GSVPWM can still suppress the magnitude of the CMV, as shown in Fig. 16(c). The dv/dt values of the CMV are also suppressed effectively. Further analysis is displayed in Fig. 17. The modulation signals in (1) are transformed to $\alpha\beta$ coordinate system. GSVPWM can suppress

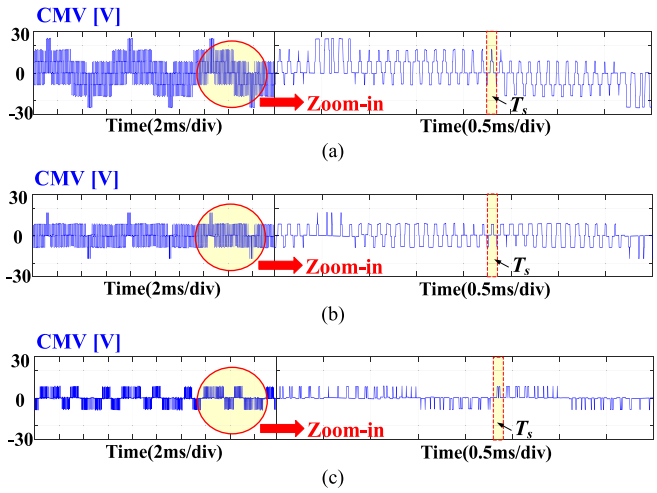


Fig. 16. Simulated results of CMV when $m = 0.9$. (a) Method-1. (b) Method-2. (c) GSVPWM.

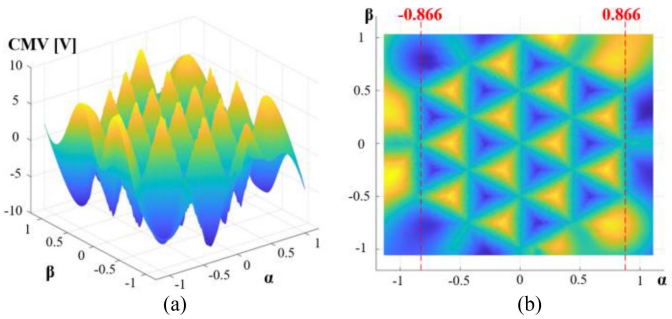


Fig. 17. 3-D plots analysis of the 5L-ANPC converter. (a) 3-D plot of Axis α, β, and CMV. (b) 3-D plot of axes α and β.

TABLE III
COMPARISON BETWEEN THREE SIMPLIFIED SVPWM

Method	Peak CMV	Peak-to-peak CMV	CMV transitions	Coordinate system
Method-1	$V_{dc}/4$	$V_{dc}/4$	6	60° *gh*
Method-2	$V_{dc}/12$	$V_{dc}/6$	4	45° $\alpha'\beta'$
GSVPWM	$V_{dc}/12$	$V_{dc}/12$	4	*abc*

CMV between +1/12V_{dc} and -1/12V_{dc} for 5L-ANPC, and the CMV values are between +8.3 and -8.3 V. The CMV is always suppressed between the above values when m is from 0 to 1, as shown in Fig. 17(a), and the space vector diagram, as shown in Fig. 17(b), is the same as Fig. 5 when m<0.866.

The peak CMV, peak-to-peak CMV, number of CMV transitions within each T_s, as well as the employed coordinate systems for the three methods, are summarized in Table III. It can be observed that GSVPWM operates directly in the *abc* coordinate system, eliminating the need for coordinate transformations. Moreover, GSVPWM exhibits the lowest peak CMV, peak-to-peak CMV, and CMV transition count among the compared methods. Therefore, GSVPWM effectively suppresses both the magnitude and the *dv*/*dt* of the CMV.

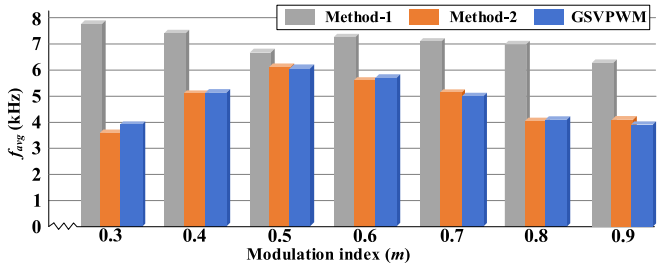


Fig. 18. Average switching frequency of three SVPWM methods.

TABLE IV
SWITCHING LOSS P_{sw} (W) OF THREE METHODS UNDER DIFFERENT MODULATION INDICES

m	0.3	0.4	0.5	0.6	0.7	0.8	0.9
Method-1	1.56	1.49	1.33	1.61	1.66	1.67	1.64
Method-2	0.78	0.98	1.29	1.22	1.23	1.01	0.98
GSVPWM	0.86	1.01	1.20	1.26	1.19	1.00	0.82

2) Steady-State Performance: The average switching frequency (f_{avg}) of 5L-ANPC can be defined as

$$f_{avg} = \frac{f_{sam}}{24N} \sum_{i=0}^{N-1} S_w(i) \tag{23}$$

where $N = f_{sam}/f$; f_{sam} is the sampling frequency ($1/T_s$); $S_w(i)$ is the switching frequency per T_s; 24 means the number of power devices in 5L-ANPC converters [29].

According to (23), the f_{avg} of three SVPWM methods is illustrated in Fig. 18. It can be concluded that the f_{avg} of Method-1 is the largest, since it uses seven-segment sequences as shown in Fig. 4(a). The f_{avg} of Method-2 is similar to that of GSVPWM, because they both use five-segment sequences as shown in Fig. 4(b)–(d). When m is very high such as m = 0.9, f_{avg} of GSVPWM will be smaller than that of Method-2. At this time, the limiter in (7) will transfer vectors with high CMV values to other vectors with lower CMV values, resulting in fewer vectors participating in the synthesis of $\boldsymbol{V}_{\mathbf{ref}}$.

To further analyze switching losses, IGBT switch IKW40T120 is selected. According to [30] and [31], P_{sw} is expressed as

$$\begin{aligned} P_{sw} &= P_{sw\_T} + P_{sw\_d} \\ &= f_s \times 6.5 \times 10^{-3} \times \left(\frac{I_{sw}}{40}\right) \times \left(\frac{V_{sw}}{1200}\right). \end{aligned} \tag{24}$$

According to (24), P_{sw} is positively correlated with the actual switching frequency. P_{sw} of the three methods, obtained from PLECS simulations, are summarized in Table IV. It can be observed that the variation trend of P_{sw} basically follows that of the f_{avg}. Although at some modulation indices, especially at low values, Fig. 18 and Table IV show that the f_{avg} and P_{sw} of GSVPWM are higher than those of Method-2, this may be because the verification is carried out on the 5L-ANPC topology. As shown in Table I and Fig. 11, 5L-ANPC requires frequent changes in switching combinations to balance the capacitor

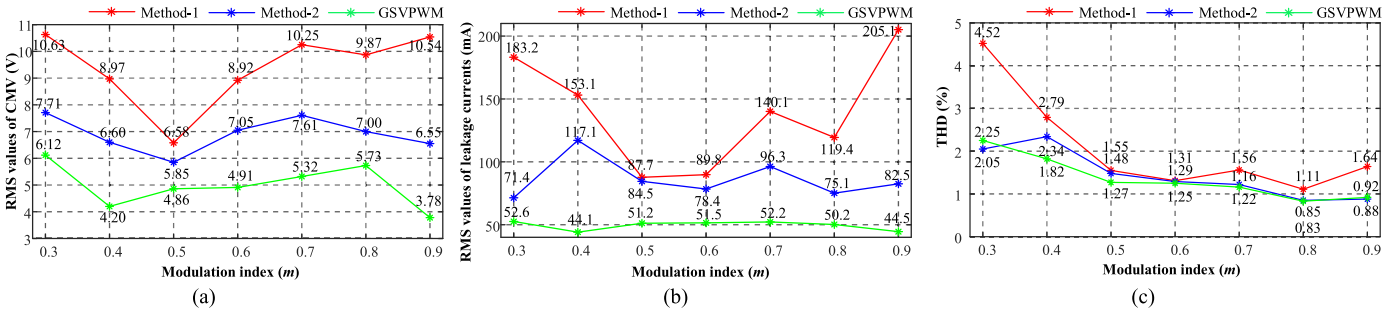


Fig. 19. Simulated results of the RMS values of CMV, leakage currents, and output current THD values. (a) RMS values of CMV. (b) RMS values of leakage currents. (c) THD values.

voltages. Since the two methods adopt different subsector divisions, the selected switching combinations and the instantaneous capacitor voltages are not the same, which leads to these slight differences. Overall, among the three methods, Method-1 exhibits the highest $P_{\rm sw}$, while Method-2 and the proposed GSVPWM yield similar $P_{\rm sw}$ values.

To study the leakage currents, a parasitic capacitor $C_{\rm pr}$, as shown in Table II, is connected between points o and n in Fig. 1 according to [25]. The leakage current is affected by the magnitude and *dv/dt* values of CMV. The RMS values of the CMV, leakage currents, and output current THD values are shown in Fig. 19.

Method-1 does not consider the CMV, thereby its RMS values of CMV and leakage currents are the largest. Compared to Method-1, Method-2 uses vectors with small CMV values to reduce the magnitude and *dv/dt* values of the CMV, thereby its RMS values of the CMV and leakage currents are smaller. Compared to Method-2, the proposed GSVPWM still uses vectors with small CMV values. Specifically, their magnitude of the CMV is between $\pm V_{\rm dc}/12$, and the CMV switches four times per T_s. But GSVPWM further uses the novel subsectors to reduce the *dv/dt* values of the CMV. Thus, GSVPWM has the smallest RMS values of the CMV and leakage currents. As analyzed earlier, when m is high enough, in order to suppress the CMV, GSVPWM transfers the vectors with high CMV values to lower ones. Thus, its current THD will increase at least $m = 0.9$ in Fig. 19. But the THD is not very high. Meanwhile, the RMS values of CMV and leakage currents for the other two methods are still high, whereas they decrease in GSVPWM.

As shown in Table IV, when m exceeds 0.9, the $P_{\rm sw}$ of GSVPWM becomes significantly lower than that of Method-2. This indirectly indicates that GSVPWM employs fewer vectors to synthesize the reference voltage, thereby sacrificing part of the current quality in exchange for lower switching losses. However, as illustrated in Fig. 19(c), the THD of the two methods remains close at this point. This demonstrates that GSVPWM can more effectively suppress leakage current as shown in Fig. 19(b), thus compensating for the errors introduced during vector synthesis. Consequently, GSVPWM can effectively reduce the magnitude and *dv/dt* values of CMV, resulting in the smallest RMS values of CMV and leakage currents.

It is necessary to note that if the inverter does not include a common-mode loop, the existence of CMV does not affect the system. In this case, the output current THD of Method-1 and

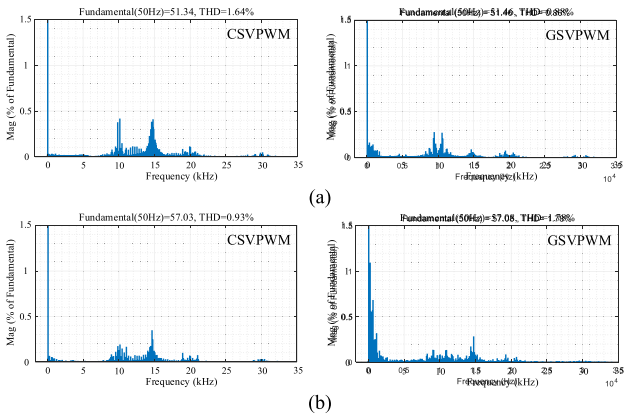


Fig. 20. Simulated FFT results of the output voltage V_{ao}. (a). $m = 0.9$. (b). $m = 1$.

Method-2 is lower than that of GSVPWM, since both Method-1 and Method-2 synthesize the reference voltage using the nearest three vectors, whereas GSVPWM does not [32]. In certain motor drive systems or transformless photovoltaic topologies, high-frequency CMV can induce the leakage current, which in turn affects the quality of the output current. Under such conditions, the output current THD of Method-1 and Method-2 becomes higher than that of GSVPWM. Many existing strategies focus on improving output current quality, such as [33] and [34]; however, they are not suitable for applications where leakage current is present. Due to the lack of effective CMV suppression, the output current harmonic distortion increases. Moreover, these strategies are not applicable to different multilevel inverter topologies. In addition, existing generic modulation strategies, such as Method-1 and Method-2, fail to simultaneously suppress both the amplitude and the *dv/dt* of the CMV.

3) Analyzing Output Voltage: In order to perform a comparative analysis of the output voltage V_{ao} in GSVPWM, a CSVPWM based on [35] for 5L-ANPC converters is selected for comparison. The current THD is the same as the voltage THD when connecting the resistance. The THD results are shown in Fig. 20. As shown in Fig. 20(a), the THD of V_{ao} for CSVPWM and GSVPWM is 1.64% and 0.88%, respectively. High-frequency harmonics caused by leakage currents are observed in CSVPWM, resulting in a higher THD of V_{ao} compared to GSVPWM. At $m = 1$ as shown in Fig. 20(b), due to current peak distortion in GSVPWM, low-frequency harmonics appear

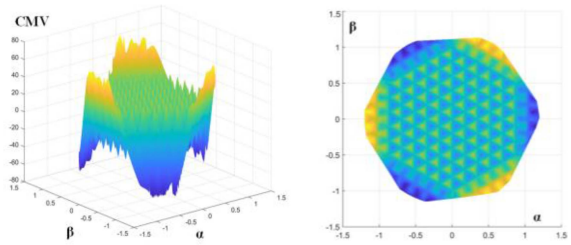


Fig. 21. 3-D plots analysis of the 11-level CHB converter. (a) 3-D plot of Axis α, β, and CMV. (b) 3-D plot of axes α and β.

in its fast Fourier transform (FFT) diagram. But GSVPWM is still able to achieve high-quality output voltage, with a THD of V_{ao} equal to 1.78%. Moreover, when $m = 1$, both methods yield a V_{ao} amplitude of 57 V, indicating that the voltage utilization reaches 1 in GSVPWM. Therefore, the proposed GSVPWM can operate normally over the full modulation index range from 0 to 1. GSVPWM can maintain high-quality output current over a wide range of modulation indices at the same time.

4) Scalability Evaluation: To demonstrate the scalability of the GSVPWM, an 11-level cascaded H-bridge (CHB) is built in MATLAB/Simulink. Each H-bridge is clamped by a dc voltage source, which can avoid the influence of capacitor voltages. According to Fig. 12, n equals 11 and p equals 5 at this time. Each dc voltage source is 100 V, and other parameters are given in Table I. The eleven-level CHB converter consists of five H-bridges on each phase. Therefore, the equivalent dc-link voltage is 1000 V. A 3-D plot is shown in Fig. 21. It can be observed that the distribution of sectors is consistent with the theory in Fig. 5. For an 11-level CHB, except for ZCMV, the minimum value of CMV is ± 33 V (100/3 V). GSVPWM can suppress the magnitude of the CMV within ± 33 V in a large-scale m. As m continues to increase, especially when it approaches 1, it can be observed that the magnitude of CMV is ± 66 V as shown in Fig. 21(a). The higher CMV values are located near the six vertices of the hexagon in the space vector diagram, as shown in Fig. 21(b). This is because there is no redundant vector with the smallest CMV values at this time. The saturation module in (7) will limit the calculated vector to other vectors with the second-lowest CMV values, indicating that (7) can suppress the CMV.

In conclusion, GSVPWM can be applied to different multilevel converters. It can effectively suppress both the magnitude and *dv/dt* values of the CMV.

B. Experiment Results

5) Steady-State Results: When $m = 0.4$ as shown in Fig. 22, V_{ao} shows three-level waveforms between −25 V and +25 V, and V_{ab} shows five-level waveforms between −50 V and +50 V of the three methods. FCV and NPV are balanced around 25 and 50 V, respectively. The THD of i_a in Method-1 is 2.92%, as the leakage currents are the largest as shown in Fig. 22(a). Method-2 reduces both the magnitude and the *dv/dt* values of the CMV as analyzed in Fig. 4(b). Therefore, its leakage currents are reduced, and its current THD is reduced to 2.83% as shown in Fig. 22(b). GSVPWM can further suppress the *dv/dt* values of the CMV, thereby suppressing its leakage currents, and the current THD is the smallest 2.24% as shown in Fig. 22(c). V_{ao} in Method-2 and GSVPWM have some certain clamping states, as shown in Fig. 22(b) and (c), because they both use five-segment sequences, and one of the phase states is fixed, as shown in Fig. 4(b)–(d).

When $m = 0.8$, the steady-state performance of the three methods is all good as shown in Fig. 23. V_{ao} shows five-level waveforms from −50 to +50 V, and V_{ab} shows nine-level waveforms from −100 to +100 V. Their output current THD values are 1.53%, 1.32%, and 1.35% for Method-1, Method-2, and GSVPWM, respectively. The THD of GSVPWM is slightly higher than that of Method-2. Because Method-2 uses three nearest vectors located in an equilateral triangle, while GSVPWM uses three vectors located in an obtuse triangle. But at this time, the leakage currents of GSVPWM are the smallest, as shown in Fig. 23(c).

From the steady-state experimental results, it can be concluded that for different modulation indices, the FCV and NPV are balanced properly. As a real-time algorithm, GSVPWM demonstrates good steady-state performance. Its phase-voltage, line-voltage, and output currents are consistent with the corresponding 5L-ANPC converters. The output current quality is high, and the leakage current is effectively suppressed.

6) Dynamic Results: Experimental results under dynamic conditions are shown in Fig. 24. When m is changed from 0.4 to 0.8, NPV and FCV are balanced properly without significant voltage fluctuations, indicating that the balancing strategy in Fig. 11 is effective. As a real-time algorithm, a sudden change in modulation index will not lead to any calculation errors in GSVPWM. It has a similar dynamic response to the conventional method using look-up tables.

7) CMV dv/dt Value Evaluation: When $m = 0.8$, the CMV of Method-1 has five levels: ±16.6 V, ±8.3 V, and 0 as shown in Fig. 25(a). Its CMV is between −8.3 and +16.6 V, or −16.6 and +8.3 V. Specifically, in each T_s, its CMV has four voltage levels: ±8.3 V, 0 and +16.6 V or ±8.3 V, 0 and −16.6 V, thereby the magnitude, frequency, and *dv/dt* values of the CMV are the highest. For Method-2, only RCMV and ZCMV vectors are used, thereby its CMV is between −8.3 and +8.3 V with three voltage levels: ±8.3 V and 0 per T_s as shown in Fig. 25(b). Similarly, GSVPWM adopts the same vectors as Method-2, and its CMV is also within −8.3 and 8.3 V. But GSVPWM further reduces the *dv/dt* values of the CMV compared to Method-2. Its CMV shows only two voltage levels: 0 and +8.3 V or 0 and −8.3 V since it uses NCMV and ZCMV vectors or PCMV and ZCMV vectors as shown in Fig. 25(c).

When $m = 0.9$, both Method-1 and Method-2 exhibit new CMV values of ±24.9 and ±16.6 V, as shown in Fig. 26(a) and (b), respectively. Due to less options for redundant switching combinations, the vectors with higher CMV values are forced to be selected such as −122 in Method-1 and −222 in Method-2 like shown in Fig. 2. As shown in Fig. 26(c), the CMV of GSVPWM still switches between 0 and +8.3 V or 0 and −8.3 V, since the saturation in (7) can suppress the CMV.

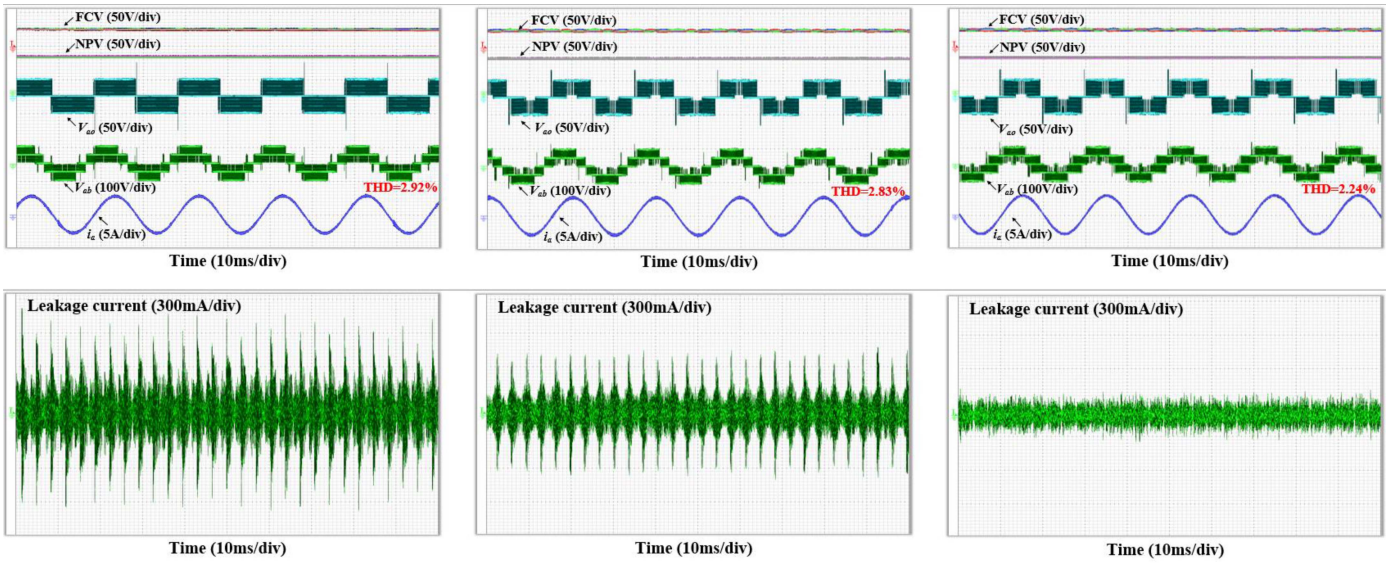


Fig. 22. Steady-state experimental results when $m = 0.4$. (a) Method-1. (b) Method-2. (c) GSVPWM.

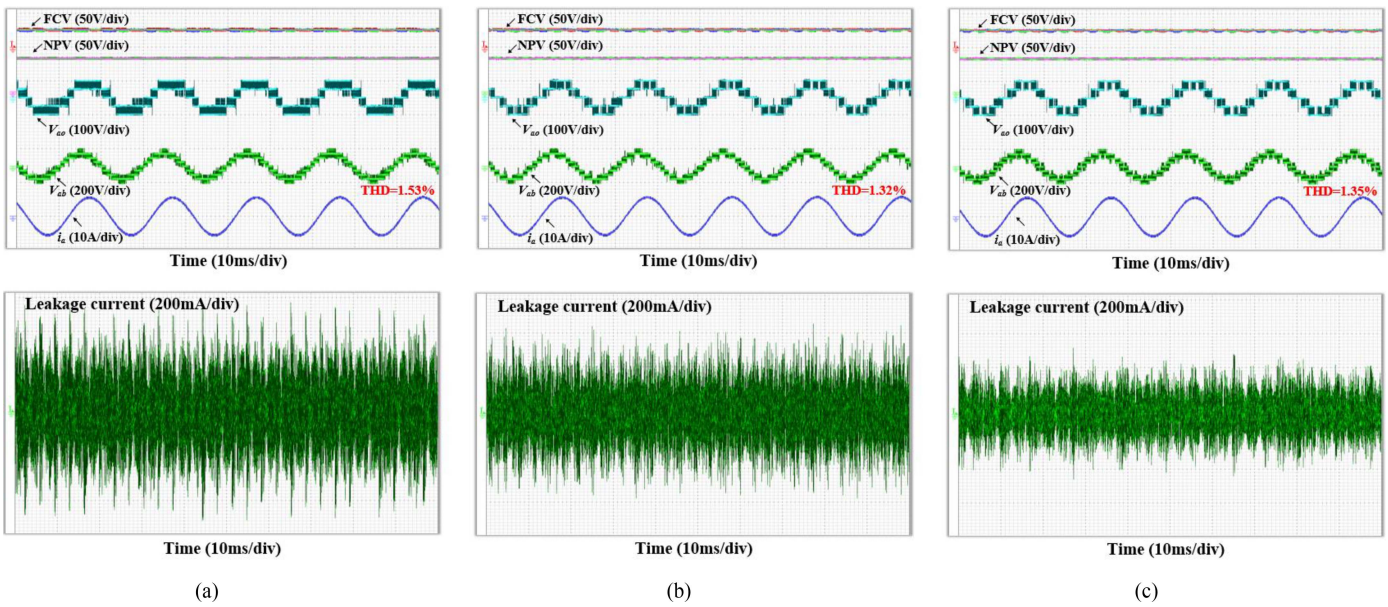


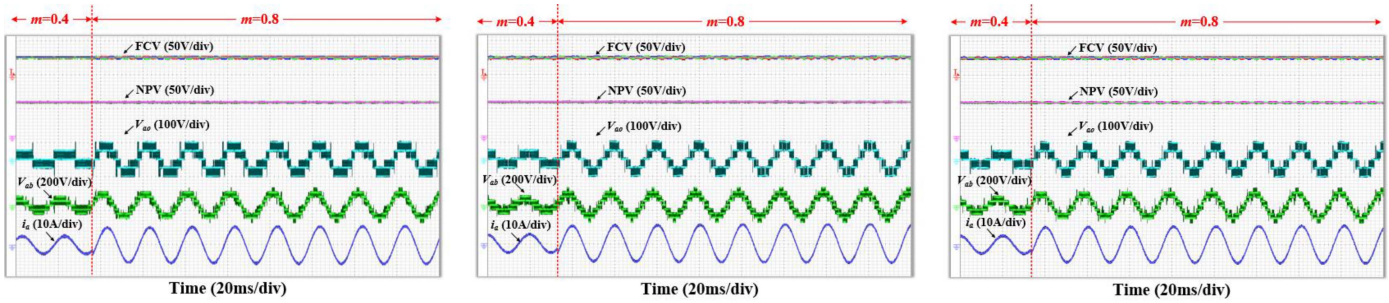
Fig. 23. Steady-state experimental results when $m = 0.8$. (a) Method-1. (b) Method-2. (c) GSVPWM.

According to [36], due to dead-time, SC transitions that are prohibited in Fig. 11 may occur across adjacent T_s, resulting in additional CMV spikes. All three methods exhibit the above phenomenon. The impact of dead-time on CMV varies among different multilevel inverters, depending on the designed switching combinations. However, dead-time does not alter the distribution of the vectors in the space vector diagram. As shown in the experimental results, the CMV generated by GSVPWM is still primarily distributed between $-V_{\rm dc}/12$ and 0 or between $V_{\rm dc}/12$ and 0, while Method-1 and Method-2 still show larger peak-to-peak CMV values.

In conclusion, GSVPWM can reduce the CMV magnitude values by using ZCMV and RCMV vectors. It further suppresses the *dv*/*dt* values of the CMV by using the novel subsectors. These above functions are all achieved through the proposed simplified real-time algorithm.

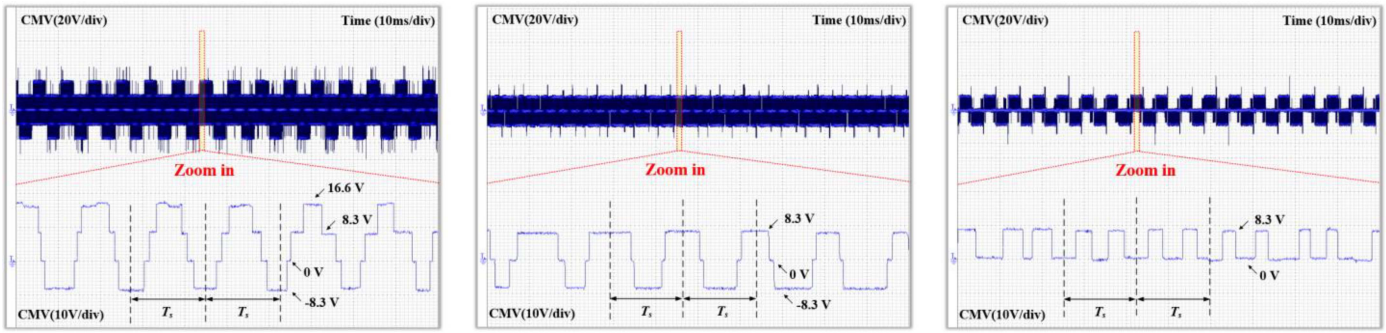
V. Conclusion

A novel GSVPWM modulation strategy based on a natural coordinate system is proposed in this article to suppress both the magnitude and the *dv*/*dt* of the CMV in multilevel converters.



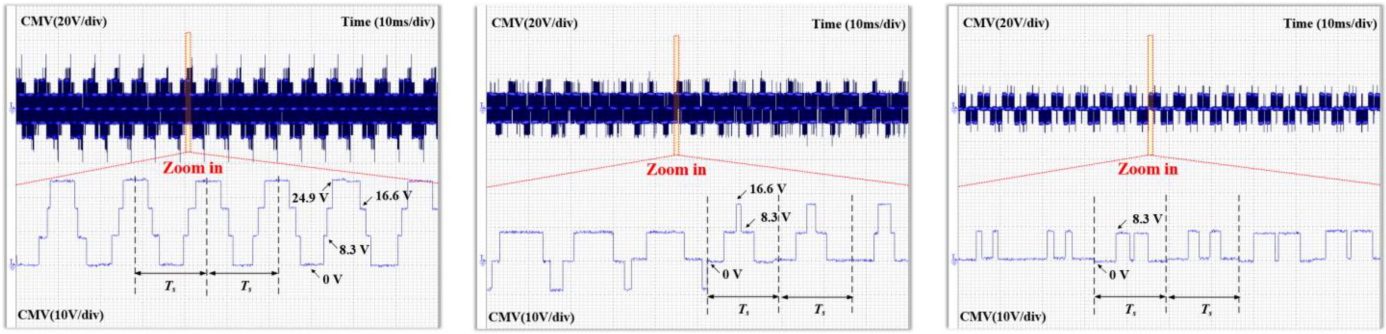
(a) (b) (c)

Fig. 24. Dynamic experimental results. (a) Method-1. (b) Method-2. (c) GSVPWM.



(a) (b) (c)

Fig. 25. Experimental results for CMV analysis when $m = 0.8$. (a) Method-1. (b) Method-2. (c) GSVPWM.



(a) (b) (c)

Fig. 26. Experimental results for CMV analysis when $m = 0.9$. (a) Method-1. (b) Method-2. (c) GSVPWM.

The proposed method calculates duty ratios, determines switching states, and arranges the vector sequence online, without relying on look-up tables. Furthermore, it eliminates the need for complex operations such as square roots, trigonometric functions, or coordinate transformations. GSVPWM operates effectively over a wide modulation index range. Compared with conventional simplified CMV suppression SVPWM strategies, GSVPWM reduces the peak-to-peak CMV by 50% without increasing its amplitude and effectively avoids high CMV levels of $\pm 1/6\ V_{\mathrm{dc}}$ under high modulation conditions. GSVPWM can operate effectively over the full modulation index range from 0 to 1. When the modulation index approaches the boundary of the maximum linear modulation range, GSVPWM sacrifices a certain degree of output current quality in exchange for lower switching losses. But the output current THD still remains low at this point, and GSVPWM can provide the best CMV and leakage current suppression performance. By tuning the parameter n of the voltage level in (7), GSVPWM can be flexibly adapted to various multilevel converter topologies without incurring additional computational burden. These advantages make GSVPWM a practically viable and promising solution for medium- and high-voltage applications.

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