A Dynamic-R_{ON}-Reduced Bidirectional GaN Load Switch With Inrush Current Protection and Spike Suppression

Po-Jui Chiu, Xiao-Quan Wu, Chi-Yu Chen, Yu-Ting Huang, Chien-Wei Cho, Tz-Wun Wang, Sheng-Hsi Hung, Ke-Horng Chen, *Fellow, IEEE*, Ying-Hsi Lin, Shian-Ru Lin, Tsung-Yen Tsai, and Hann-Huei Tsai, *Member, IEEE*

***Abstract*—The proposed bidirectional load switch enables bidirectional current conduction while effectively blocking reverse current, providing efficient and reliable power management. It operates with a maximum input voltage (V_{IN}) of 48 V and supports load currents (I_{Load}) up to 25 A, achieving a low ON-resistance (R_{on}) of 11.2 mΩ. A driving current limiter is implemented to regulate the gate-driving strength and suppress inrush current, allowing the bidirectional GaN (Bi-GaN) switch to turn ON smoothly. This results in a rising propagation delay (T_{pdr}) of 347.4 μs and a rise time (T_r) of 936.7 μs, reducing inrush current by 91.4%. Additionally, the spike-reduced turn-OFF circuit enables fast turn-OFF with a 409.7 ns falling propagation delay (T_{pdf}) and 483.6 ns fall time (T_f), reducing voltage overshoot by 89.5% to protect on-chip devices. The Bi-GaN device also adopts a split-source field plate structure, limiting the R_{on} increase to only 28.5% after 168 h of stress testing, thereby ensuring long-term reliability and performance stability.**

***Index Terms*—Bidirectional load switch (BLS), current collapse, driving current limiter (DCL), dynamic ON-resistance (RON) reduction, electric vehicle power systems, field plate (FP), gallium nitride (GaN), gate driver (GD) for bidirectional GaN switch, spike-reduced turn-OFF (SRT).**

I. Introduction

IMPLEMENTING high-side battery switching in 48V electric vehicle (EV) power systems requires an advanced load switch (LS) design that supports both bidirectional current conduction and reverse current blocking. These features are essential for efficient and safe power management under various operating conditions. During the battery charging phase, a single charger sequentially charges multiple battery cells, as illustrated in Fig. 1. To enable this functionality, the LS positioned between the charger and battery cells must provide reverse current blocking capability when turned OFF, preventing unintended discharge from the charged battery. In the discharging phase of the battery, the LS must facilitate the current conduction from the battery to the load to meet the power demands of the EV. Dual-mode operation highlights the importance of bidirectional current transfer, ensuring effective management of charging currents directed to battery cells while maintaining a stable path for discharging currents to power the load. As a result, the LS design is crucial to optimize system efficiency, preserve battery health, and ensure reliable operation under varying load conditions.

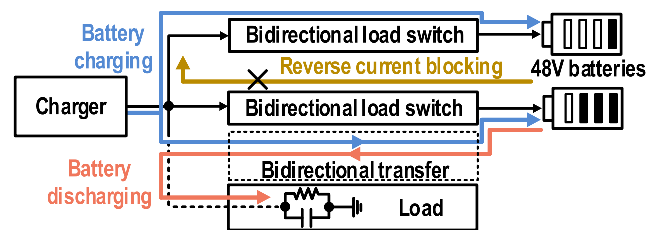


Fig. 1. Application of bidirectional load switch.

Conventional LSs [1], [2], [3], [4], [5], [6] typically use a single power switch (PS) to conduct current between two terminals. However, when the PS is turned OFF, the body diode within the device allows the reverse current to flow from the second terminal to the first, which poses a challenge for effective current blocking. To address this limitation, LS architectures with back-to-back (B2B) PS configurations have been introduced in [7], [8], and [9]. In these designs, the oppositely oriented body diodes effectively block reverse currents. However, these LS designs lack full bidirectional current transfer capability, as their gate drivers (GDs) function only when the voltage at one specified terminal is higher than the other. Recent advances have led to the development of bidirectional load switches (BLSs) [10], [11], [12], which block reverse current and enable bidirectional current transfer. These BLS designs commonly incorporate B2B PS configurations to achieve their functionality. However, this configuration doubles the ON-resistance

Received 21 July 2025; revised 14 October 2025; accepted 28 November 2025. Date of publication 2 December 2025; date of current version 25 February 2026. This work was supported by the National Science and Technology Council under Grant 114-2640-E-007-008, Grant 114-2640-E-006-008, Grant 114-2221- E-A49-158-MY3, Grant 114-2622-E-A49-019, Grant 113-2622-E-A49-004, Grant 112-2221-E-A49-145-MY3, and Grant 112-2221-E-A49-016-MY3. Recommended for publication by Associate Editor D. Dong. *(Corresponding author: Ke-Horng Chen.)*

Po-Jui Chiu, Xiao-Quan Wu, Chi-Yu Chen, Yu-Ting Huang, Chien-Wei Cho, Tz-Wun Wang, Sheng-Hsi Hung, and Ke-Horng Chen are with the Institute of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: khchen@nycu.edu.tw).

Ying-Hsi Lin, Shian-Ru Lin, and Tsung-Yen Tsai are with Realtek Semiconductor Corporation, Hsinchu 30010, Taiwan.

Hann-Huei Tsai is with Taiwan Semiconductor Research Institute (TSRI), Hsinchu 300091, Taiwan.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3639306.

Digital Object Identifier 10.1109/TPEL.2025.3639306

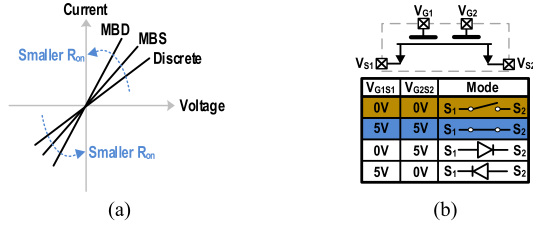


Fig. 2. (a) R_{on} comparison of discrete, MBS, and MBD topologies. (b) Mode table of MBD.

(R_{on}) due to the series connection of two switches, resulting in higher conduction losses. To mitigate these losses, gallium nitride (GaN) devices have emerged as a preferred choice for PS implementation due to their inherently low R_{on}. Among the latest innovations, monolithic bidirectional GaN (Bi-GaN) technology [13], [14], [15] significantly reduces R_{on} compared to traditional discrete B2B GaN PS designs, as illustrated in Fig. 2(a). Bi-GaN devices featuring a common drain/source (MBD/MBS) structure emulate the functionality of B2B GaN switches but with reduced R_{on} due to the common drain/source terminals. As shown in Fig. 2(b), Bi-GaN operates in two modes: In the first mode ($V_{\mathrm{G1S1}} = V_{\mathrm{G2S2}} = 0$V), the device blocks current in both directions. The second mode ($\mathrm{V}_{\mathrm{G1S1}} = \mathrm{V}_{\mathrm{G2S2}} = 5$V) enables bidirectional current conduction. These attributes make Bi-GaN an ideal solution for BLS applications, offering reduced conduction losses, improved bidirectional capability, and enhanced integration in compact designs.

Fig. 3 illustrates the structures of 100V MBS and MBD configurations, where the length from the gate to the drain (L_{gd}) is approximately three times the length from the gate to the source (L_{gs}), which is a critical consideration for optimizing device performance. Compared to discrete B2B GaN topologies, monolithic integration offers significant advantages regarding device size and R_{on}. Specifically, the MBS configuration achieves a 13% reduction in size, while the MBD configuration achieves a 38% reduction. Given its proportional relationship of R_{on} with L_{gs} and L_{gd}, size optimization directly contributes to lowering R_{on}, thus improving conduction efficiency and enabling compact integration for power management applications.

Although the MBS topology in Fig. 4 offers the potential for further integration, its GD design introduces unique challenges. The MBS topology allows both gates to be driven by the same GD, allowing the two gates to be merged into a single control node [13], [14]. However, during the turn-OFF process, the MBS topology may result in overstress conditions due to the absence of an available source terminal for biasing, as shown in Fig. 5(a), where the input control signal (V_{PWM}) transitions from high to low, prompting the GD to pull the gate voltage (V_G) to ground. As the load resistor (R_{Load}) gradually discharges the charge on the source terminal, the gate-to-source voltage (V_{GS}) experiences a sharp drop, potentially exceeding the gate-to-source breakdown voltage. Such an overstress can jeopardize the reliability and longevity of the device. To mitigate this issue, an additional turn-OFF selector must dynamically manage the gate terminal during the turn-OFF process. The selector ensures that the gate terminal is shorted to the lower voltage of either the first terminal (V_{D1}) or the second terminal (V_{D2}), effectively preventing overstress conditions in Fig. 5(b). While this solution solves the risk of breakdown, it comes at the cost of increased control complexity, as the turn-OFF selector requires precise timing and coordination to maintain reliable operation. Using two drivers without tying the gates is another topology to drive the MBS. However, an additional turn-OFF selector is still required in this design to determine which terminal is V_{OUT}, as V_G must connect to V_{OUT} during turn-OFF to prevent the overstress problem shown in Fig. 5(a). Therefore, the topology shown in Fig. 4 and the topology using two drivers without tying the gates both require an extra turn-OFF selector, which increases the complexity of the GD design of MBS. This is one reason why MBS is not preferable for implementing BLS.

In summary, Bi-GaN configurations offer compelling benefits in size reduction and R_{on} minimization compared to discrete B2B designs, with MBD providing the most significant improvements. However, the MBS topology introduces unique challenges during the turn-OFF process, necessitating a turn-OFF selector to ensure reliability. The tradeoff between integration, control complexity, and robustness underscores the importance of continued innovation in designing Bi-GaN devices to realize their full potential in advanced power management systems.

Considering the characteristics of Bi-GaN devices and the requirements for GD design, this article adopts MBD as the primary PS to implement BLS, achieving low cost, high efficiency, and a simplified GD design.

The rest of this article is organized as follows. Section II discusses the challenges in GD design and introduces the proposed GD architecture for the BLS. Section III addresses issues associated with Bi-GaN devices and presents methods to enhance their performance. In Section IV, the measurement results and a comparison table are provided. Finally, Section V concludes the article.

II. Gate Driver for Bidirectional Load Switch

A. *Architecture and Challenges of Bi-GaN Gate Driver*

Building on the previous GD design for a single GaN PS [16], the corresponding GD architecture for MBD topology is illustrated in Fig. 6. To achieve full turn-ON of the MBD, a large bootstrap capacitor ($C_{\mathrm{boot}x}$) is connected between the gate (V_{Gx}) and the source (V_{Sx}). While the approach ensures adequate driving strength for the MBD, it introduces additional design complexity compared to the GD for a single GaN PS. The MBD GD requires an extra level shifter to elevate the V_{PWM} into the voltage domain spanning from V_{Sx} to the bootstrapped voltage ($V_{\mathrm{boot}x}$). Furthermore, an additional charge pump circuit is required to maintain the voltage across $C_{\mathrm{boot}x}$ sufficiently high to sustain operation. The charge pump uses bulky capacitors to handle the increased charge demand, which occupies a significant area. The complexity further escalates for dual-gate MBD designs, as each gate requires a dedicated $C_{\mathrm{boot}x}$, level shifter, and charge pump circuit. The duplication doubles the area consumption and increases the power and design overhead.

In this article, the proposed GD for the monolithic Bi-GaN eliminates the need for level shifters, offering a more simplified

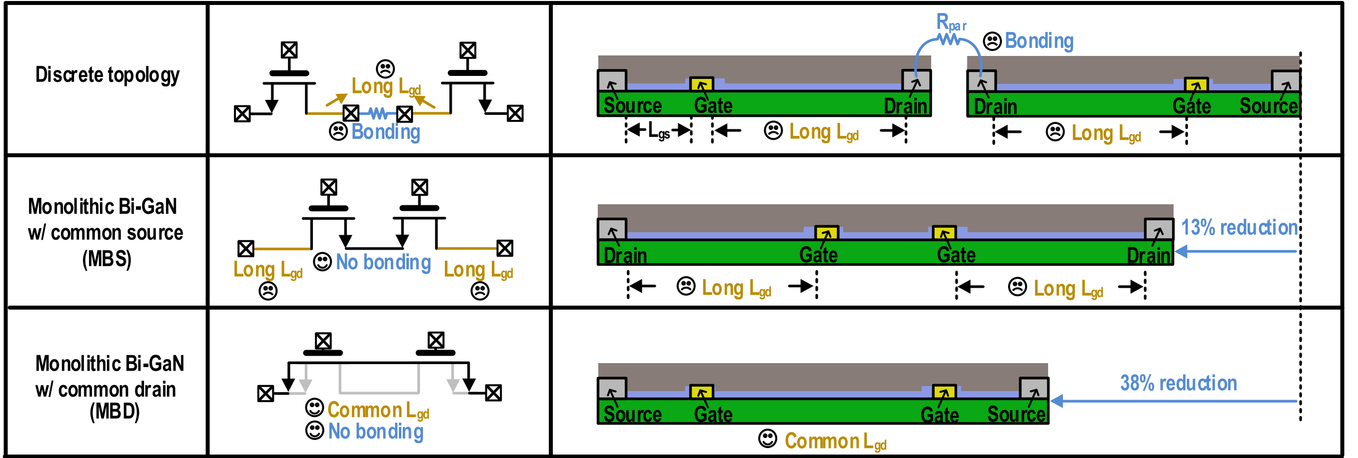


Fig. 3. Comparison of different Bi-GaN devices.

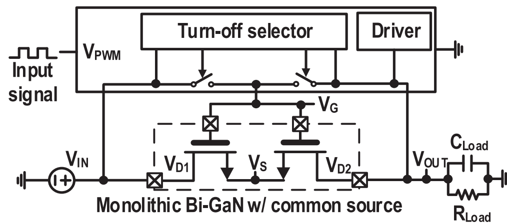


Fig. 4. Architecture of MBS gate driver.

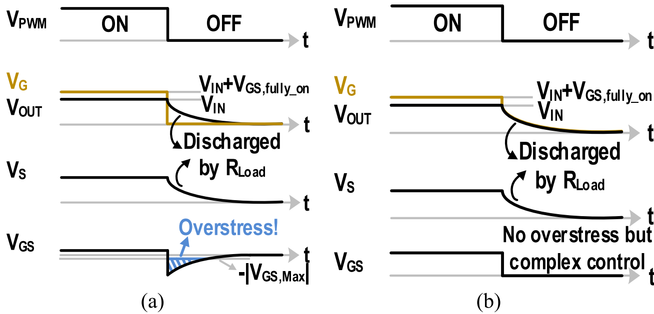


Fig. 5. Problems in gate driver design with MBS. (a) V_{GS} is overstressed without a turn-OFF selector. (b) No overstress but complex control of the turn-OFF selector.

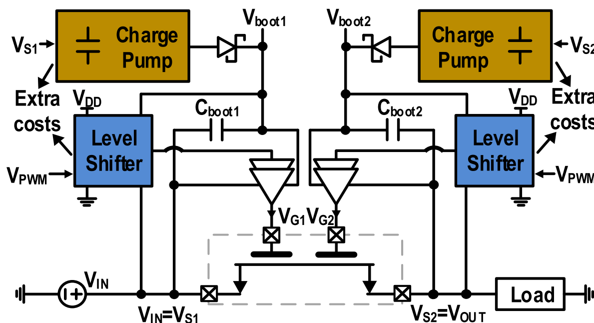


Fig. 6. Architecture of conventional gate driver for MBD.

design [17] compared to traditional GD architectures. As illustrated in Fig. 7, the design requires only two $C_{\mathrm{boot}x}$s in total, one for each gate terminal, thereby reducing the component count. Furthermore, the proposed GD incorporates a driving current limiter (DCL) and spike-reduced turn-OFF (SRT) circuits to address critical challenges associated with switching and transient effects. DCL effectively mitigates the inrush current, which is a common issue when turning ON LS, by controlling the strength of the driving current. Additionally, the SRT circuit is designed to reduce voltage spikes during the turn-OFF process, thereby protecting the ON-chip devices from potential damage caused by overshoot voltages. The voltage spikes resulting from parasitic inductances or rapid switching transitions pose a significant risk to ON-chip devices. By minimizing voltage spikes, the SRT circuit improves the reliability and robustness of the system

$$I_{\mathrm{OUT}} = I_{\mathrm{Load}} + I_{\mathrm{Inrush}} \tag{1}$$

$$I_{\mathrm{Load}} = \frac{V_{\mathrm{OUT}}}{R_{\mathrm{Load}}} \tag{2}$$

$$I_{\mathrm{Inrush}} = C_{\mathrm{Load}} * \frac{dV_{\mathrm{OUT}}}{dt}. \tag{3}$$

Fig. 8(a) shows the occurrence of an inrush current during the turn-ON process in the BLS. The clock signal V_{CLK} is activated by V_{PWM}. V_{CLK_B} is an inverted signal of V_{CLK} through an inverter. Both V_{CLK} and $V_{\mathrm{CLK_B}}$ are reset to the low state when V_{PWM} is in the low state. V_{CLK} and V_{CLK_B} determine whether $C_{\mathrm{boot}x}$s are charging by the higher voltage between V_{S1} and V_{S2} or discharging to V_{Gx}. When V_{CLK} is high and V_{CLK_B} is low, C_{boot1} charges V_{Gx}, and C_{boot2} is charged by the higher voltage between V_{S1} and V_{S2}. However, C_{boot1} slowly discharges by $I_{\mathrm{LK}\,Gx}$, leading to insufficient voltage to fully turn ON the BLS, as shown in Fig. 9(a). When V_{CLK} transitions from high to low and V_{CLK_B} transitions from low to high, C_{boot1} is charged by the higher voltage between V_{S1} and V_{S2}, and the fully charged C_{boot2} charges V_{Gx} to maintain a fully-ON voltage of the BLS. These steps continue until V_{PWM} transitions from high to low, at

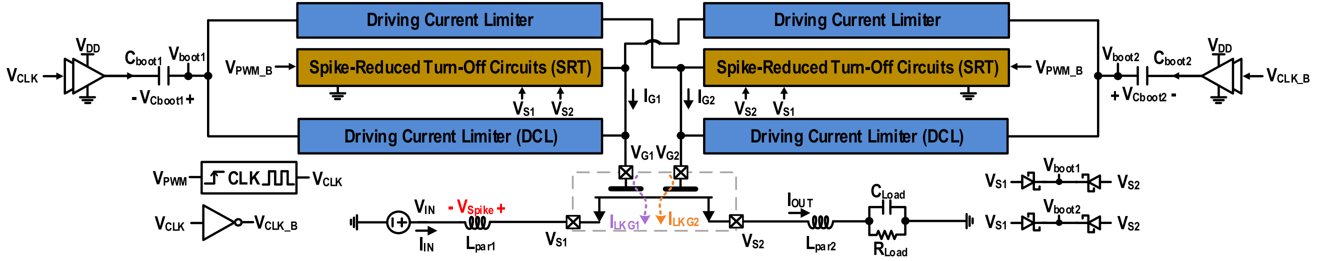


Fig. 7. Architecture of proposed Bi-GaN driver.

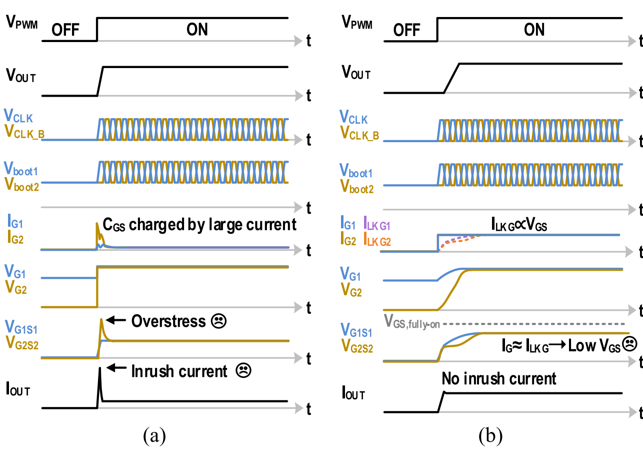


Fig. 8. (a) Inrush current and overstress occur without soft-start. (b) Bi-GaN cannot be fully turned ON with a small driving current.

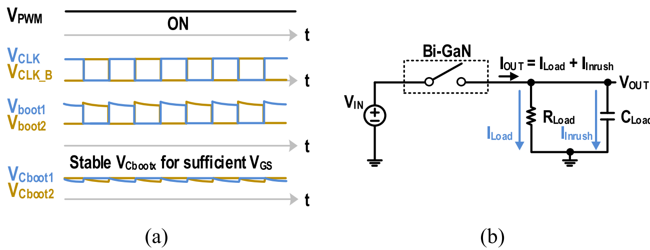


Fig. 9. (a) Complementary CLK signals to maintain stable $V_{Cboot x}$. (b) Simplified model of bidirectional load switch.

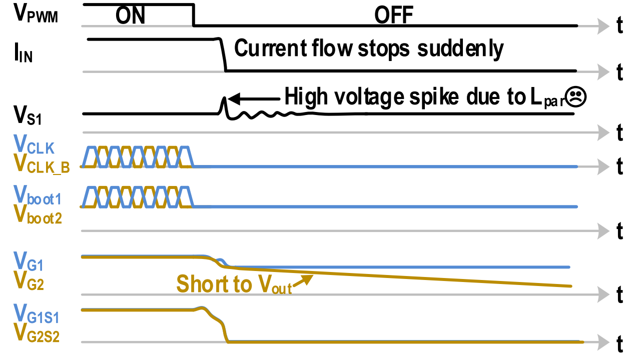


Fig. 10. Spike on V_{S1} during turn-OFF.

which point both V_{CLK} and V_{CLK_B} are reset to the low state. As V_{PWM} transitions from low to high, V_{Gx} is then charged by the higher voltage between V_{boot1} and V_{boot2}. V_{CLK} and V_{CLK_B} then drive the capacitors to fully charge, ensuring that the gate-to-source voltage (V_{GxSx}) of the Bi-GaN device reaches the desired level, allowing it to turn ON effectively. However, during this turn-ON process, an inrush current occurs as the load capacitor (C_{Load}) is charged from 0 V to V_{IN}. As illustrated in Fig. 9(b), the current stress in the Bi-GaN device is determined using (1)–(3).

The sudden influx of current can cause significant stress on the device, especially when the load capacitor presents a large capacitance. Large current spikes may damage the device, leading to device degradation or even permanent damage. Furthermore, V_{G2S2} experiences overstress during this transition because V_{OUT} is initially 0 V. As the GD attempts to charge the gate, a large voltage difference is applied to V_{G2S2}, which can exceed the rated gate-to-source voltage, risking damage to the Bi-GaN device.

According to (3), the inrush current is directly proportional to the rising slope of V_{OUT}. Thus, slowing down the turn-ON speed of the Bi-GaN device helps reduce inrush current. Fig. 8(b) demonstrates the implementation of a GD soft-start technique using a small constant current. When V_{PWM} is transitioned from low to high, the V_{Gx} of Bi-GaN is charged by a small current, causing V_{Gx} to rise gradually. The soft-start addresses the issues of inrush current and overstress typically observed during the rapid turn-ON process, thereby enhancing the protection and stability of the Bi-GaN device during the turn-ON phase. However, while the soft-start technique effectively mitigates the inrush current and overstress issues, it introduces a new challenge related to the gate leakage current ($I_{\mathrm{LK}\,Gx}$) of the GaN device. $I_{\mathrm{LK}\,Gx}$ is a parasitic current that flows through the gate terminal and is proportional to the V_{GS}. As V_{Gx} increases during the soft-start process, $I_{\mathrm{LK}\,Gx}$ also increases. At a certain point, when $I_{\mathrm{LK}\,Gx}$ becomes comparable to the small driving current (I_{Gx}) provided by GD, V_{Gx} ceases to rise further. Therefore, V_{GxSx} of the Bi-GaN device is clamped below the fully-ON voltage level ($V_{GS,\ \mathrm{fully\text{-}on}}$), increasing the R_{on} and leading to higher conduction losses. Thus, while the soft-start technique offers a solution to the issues of inrush current and overstress during turn-ON, the gate leakage current introduces a tradeoff, preventing the Bi-GaN device from achieving optimal performance.

Fig. 10 illustrates the challenges during the turn-OFF process of the Bi-GaN device. When V_{PWM} is transitioned from high to

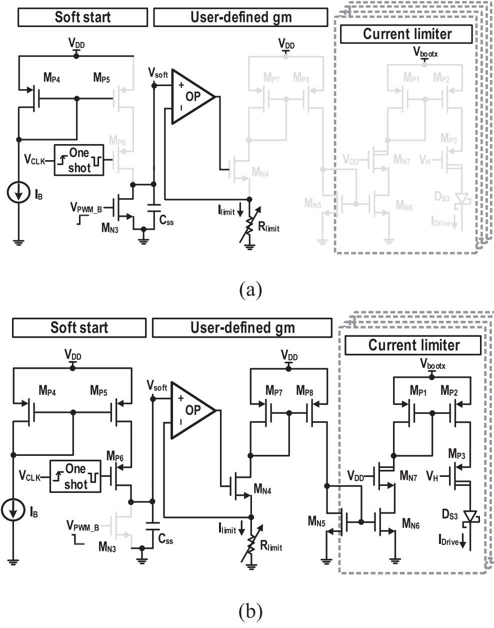


Fig. 11. Architecture of DCL circuit. (a) Operation of DCL when $V_{\mathrm{PWM_}B}$ is in the high state. (b) Operation of DCL when $V_{\mathrm{PWM_}B}$ is in the low state.

low, the Bi-GaN is turned OFF, and the flow of the input current is abruptly interrupted. The sudden stop of the current creates a steep current rate of change (*di/dt*) that interacts with the input parasitic inductance ($L_{\mathrm{par}x}$). Therefore, a high voltage spike in (4) is induced at the input terminal of the Bi-GaN device. The voltage spike poses significant risks to the GD circuitry

$$V_{\mathrm{Spike}} = L_{\mathrm{par1}} \frac{dI_{\mathrm{IN}}}{dt}. \tag{4}$$

The magnitude of the spike is directly proportional to the parasitic inductance and the *di/dt*, which are influenced by factors such as the switching speed. If the voltage spike exceeds the breakdown voltage of the GD or other ON-chip components, it can cause permanent damage or degradation to the device. Furthermore, repeated exposure to such spikes may reduce the reliability and operational lifetime of the Bi-GaN device and its associated circuitry.

In conclusion, the turn-ON and turn-OFF process plays a crucial role in the operation of the Bi-GaN-based LS. However, it presents challenges such as inrush current, I_{LKG}, and *di/dt*-induced voltage spikes. Addressing these issues underscores the need for effective switching techniques to enhance system reliability and safeguard the GD.

B. Driving Current Limiter

Fig. 11 illustrates the architecture of the proposed DCL, designed to effectively mitigate the inrush current and ensure the full turn-ON of the Bi-GaN power device. The DCL integrates a soft-start mechanism and a user-defined transconductance stage to achieve precise control over the GD current. When V_{PWM} is low, transistor M_{N3} pulls V_{soft} down to 0 V, thereby disabling the current limiter, as illustrated in Fig. 11(a). As shown in

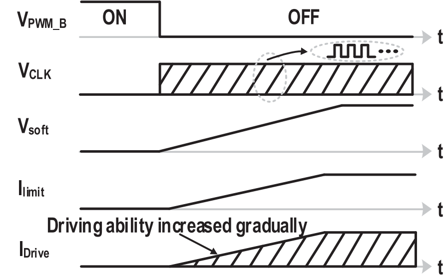


Fig. 12. Operation of driving current limiter.

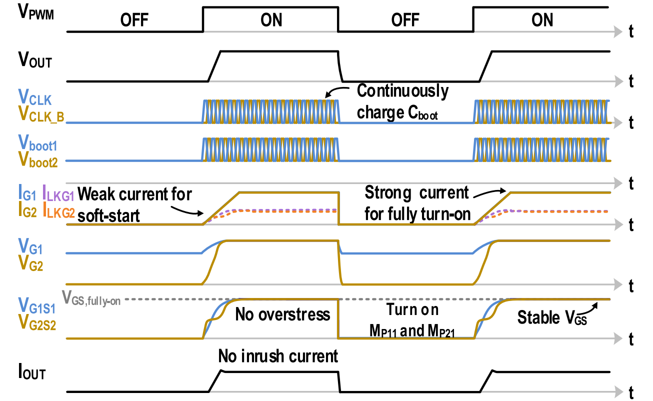


Fig. 13. Operation of the proposed driver with DCL.

Fig. 12, when the V_{PWM} signal transitions from low to high, M_{N3} turns OFF, and M_{P6} turns ON and OFF repetitively to charge the soft start capacitor (C_{SS}) slowly, causing the control voltage V_{soft} to ramp up gradually. The user-defined transconductance converts V_{soft} into the corresponding limit current I_{limit}, which is subsequently mirrored to the current-limiting stage. The source terminals of M_{P1} and M_{P2} are connected to the bootstrap voltage $V_{\mathrm{boot}x}$, thereby constraining the driving current I_{Drive} within the limits of I_{limit}. Regulated I_{Drive} ensures a controlled and gradual increase in the gate current I_{Gx}, which charges V_{Gx} smoothly. Consequently, the operation alleviates inrush current and prevents overstress on the Bi-GaN device during the turn-ON process, as verified by the transient response shown in Fig. 13. When the soft-start phase ends, V_{soft} remains at a constant level. A larger I_{limit} allows a stronger I_{Gx} to compensate for the gate leakage current $I_{\mathrm{LK}\,Gx}$. This ensures that the Bi-GaN device is fully turned ON, thereby minimizing R_{on} and conduction losses.

C. Spike-Reduced Turn-off Circuits

Fig. 14 shows the schematic of the proposed SRT, designed to suppress voltage overshoot during the turn-OFF transition of Bi-GaN. When V_{PWM} is high, transistors M_{N11} and M_{N21} turn OFF, driving $V_{\mathrm{SG,\ MP11}}$ and $V_{\mathrm{SG,\ MP21}}$ to 0 V and thereby switching M_{P11} and M_{P21} OFF, as shown in Fig. 14(a). When the control signal V_{PWM} switches from high to low, NMOS transistors M_{N11} and M_{N21} are activated, pulling the gate voltages of M_{P11} and M_{P21} low to short V_{Gx} to V_{Sx}, effectively turning OFF the Bi-GaN. During this event, a voltage spike at node V_{S1}

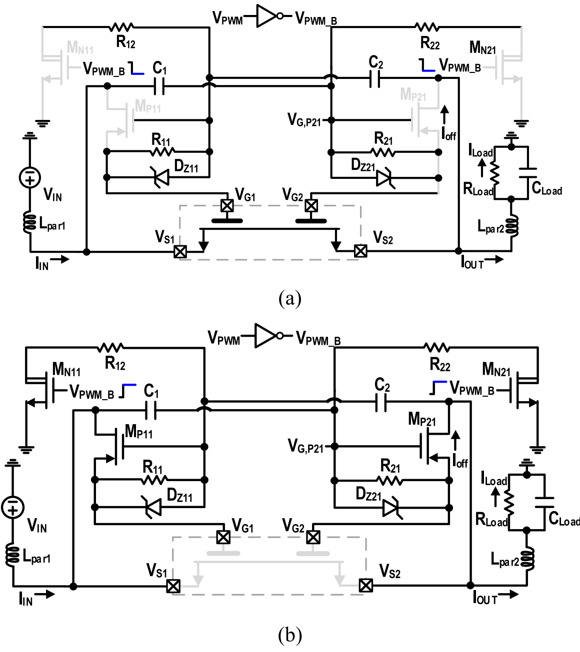


Fig. 14. Architecture of SRT circuit. (a) Operation of SRT when V_{PWM_B} is in the low state. (b) Operation of SRT when V_{PWM_B} is in the high state.

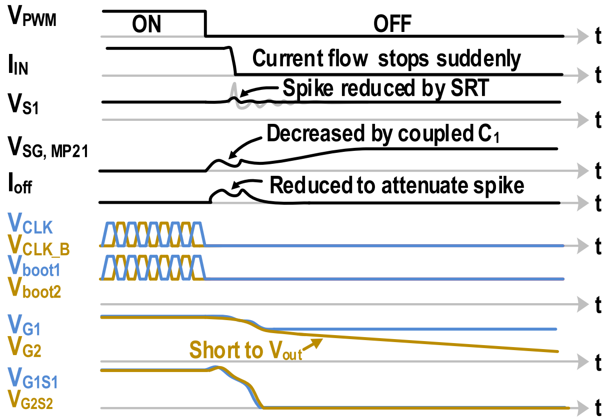


Fig. 15. Operation of the proposed SRT.

is capacitively coupled to the gate of M_{P21} through capacitor C_1, dynamically lowering its source-to-gate voltage ($V_{\mathrm{SG,MP21}}$). This reduction modulates and decreases the Bi-GaN's turn-OFF current (I_{off}), slowing the discharge of the gate capacitance of Bi-GaN. As a result, the turn-OFF process is decelerated, effectively reducing the voltage spike at V_{S1}, as shown in Fig. 15. This controlled turn-OFF improves Bi-GaN reliability by minimizing electrical overstress from fast switching.

III. Bidirectional GaN Switch

A. Mechanism of Current Collapse in MBD

Although the low R_{on} of the Bi-GaN device helps minimize conduction losses, its long-term stability deteriorates under sustained high-voltage stress. Over time, R_{on} gradually increases, resulting in reduced efficiency of the BLS. As shown

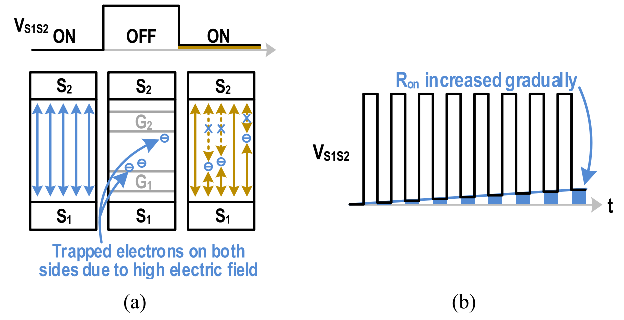


Fig. 16. (a) R_{on} increases after stress at high voltage. (b) R_{on} increases with time.

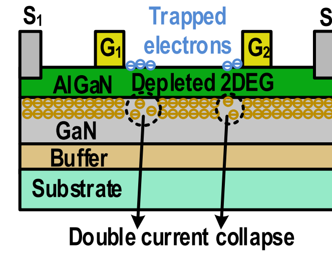


Fig. 17. Dual gates of MBD double the impact of the current collapse.

in Fig. 16(a), this degradation is linked to the "current collapse" phenomenon [18], [19], [20], [21], [22] commonly seen in GaN devices. The effect is caused by electron trapping in the insulating layer, triggered by strong electric fields between the gate and drain terminals. During the ON state of a GaN HEMT, a conductive channel is formed to carry current. When the V_{GS} is lowered, the device turns OFF, and the drain voltage rises. In this period, the high electric field between the gate and drain induces electron trapping in the insulator. These trapped charges persist and partially screen the channel, thereby impeding current conduction during the subsequent ON state and resulting in an increased dynamic R_{on}. Prolonged high-voltage stress causes increased electron trapping, which depletes the two-dimensional electron gas (2DEG) and obstructs current conduction. The reduction in 2DEG density weakens channel conductivity and obstructs current flow, resulting in a transient increase in dynamic R_{on}, as illustrated in Fig. 16(b). The increase in R_{on} becomes more pronounced with higher gate-to-source voltage stress [23]. Additionally, the dual-gate structure of the MBD architecture intensifies the current collapse effect. As shown in Fig. 17, charge trapping occurs beneath both gate terminals simultaneously, doubling the impact on R_{on}. This exacerbates the degradation of the conduction performance of the device, accelerating the rise in R_{on} and leading to a further decline in efficiency over time.

B. Dynamic-R_{on}-Reduced Bidirectional GaN Switch

Fig. 18 illustrates the structure of GaN high electron mobility transistors (HEMTs) incorporating various field plate (FP) configurations. Conventional GaN HEMT with a gate field plate (GFP) [24], [25] exhibits a pronounced electric field

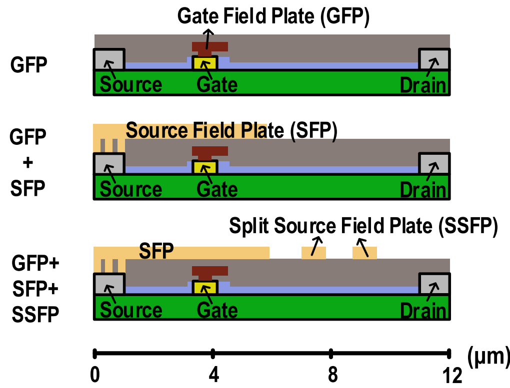


Fig. 18. GaN HEMTs with different field plates.

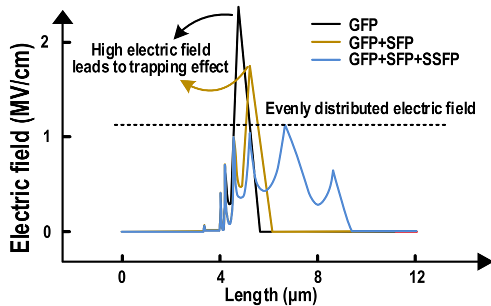
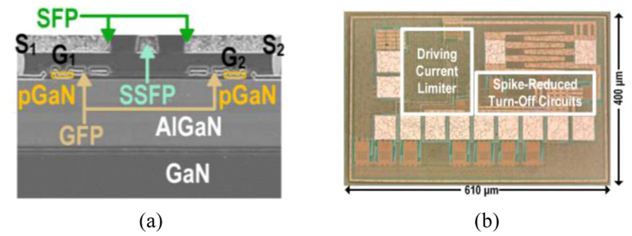


Fig. 19. Electric field distribution in GaN HEMTs with different field plates.

concentration at the edge of the gate, as shown in Fig. 19. The peak electric field contributes to device degradation and current collapse in high-power operation. To address this issue, the GaN HEMT with an additional source field plate (SFP) [26], [27] demonstrates an improvement by slightly suppressing the electric field peak. The presence of the SFP causes the peak electric field to shift from the gate edge to the edge of the SFP, thereby mitigating the field stress on the gate and improving overall device reliability. However, while the introduction of the SFP alleviates some field concentration, the redistribution of the electric field remains nonuniform, leading to residual peaks that can still impact performance under high-voltage conditions. The proposed split source field plate (SSFP) structure consists of a segmented extension of the SFP, further modulating the electric field distribution. The segmentation ensures a more gradual transition of the electric field across the SFP and SSFP edges, thereby reducing the magnitude of the peak electric field and achieving a more uniform field profile, as shown in Fig. 19. The bidirectional control of the Bi-GaN device is enabled by the symmetric source/drain architecture and the underlying AlGaN/GaN heterostructure. The 2DEG channel can be modulated by the gate potential, thereby allowing bidirectional conduction while maintaining normally-OFF characteristics. The device is fabricated on a 6-inch GaN-on-Si wafer, which comprises a low-resistivity silicon substrate, a GaN buffer/transition layer, and a p-GaN gate layer. The SFPs and SSFPs are implemented with ~1.5-μm-thick Aluminum-Copper interconnects to ensure robust current handling. The GFP employs a Schottky contact metal with a thickness of about one-fifth of the SFP, directly



(a) (b)

Fig. 20. (a) SEM cross-sectional image of the Bi-GaN in the 0.5 μm process. (b) Chip micrograph of Bi-GaN gate driver.

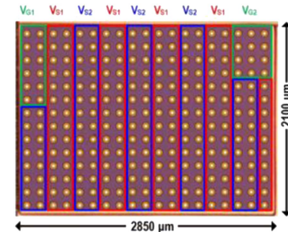


Fig. 21. Package of Bi-GaN.

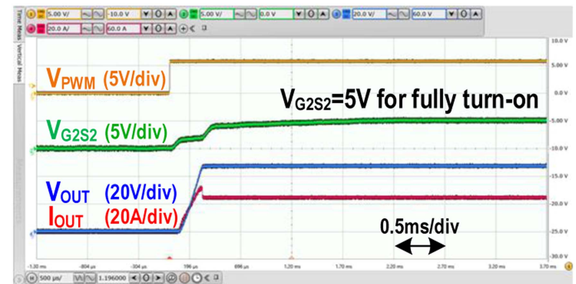


Fig. 22. Turn-ON operation.

Fig. 23 Turn-OFF operation.

interfacing with the p-GaN layer and incorporating Nickel Silicide to improve electrical performance and reliability.

IV. Measurement Results

Fig. 20(a) shows the scanning electron microscope (SEM) cross-sectional image of the Bi-GaN in the 0.5 μm process, and Fig. 20(b) shows the silicon driver in the 0.18 μm BCD process. Fig. 21 shows the chip micrograph of a package of the Bi-GaN to drive a large current. Figs. 22 and 23 show the measured waveforms of turn-ON and turn-OFF operations under 48 V V_{IN} and 25 A I_{Load} with 10 μF C_{Load}. Fig. 22 shows that Bi-GaN is fully

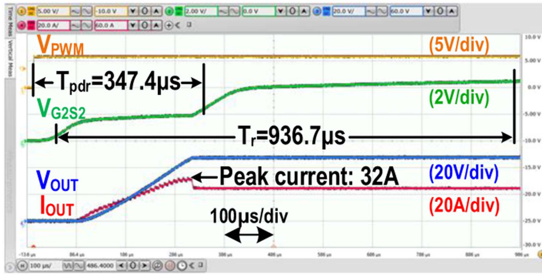


Fig. 24. Zoom-in turn-ON operation.

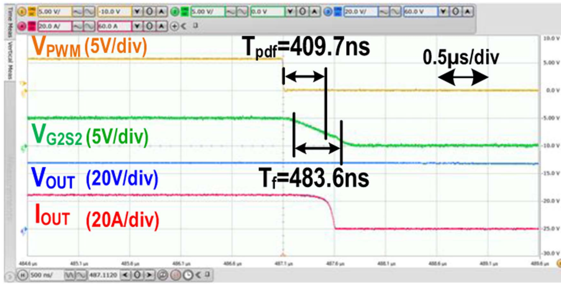


Fig. 25. Zoom-in turn-OFF operation.

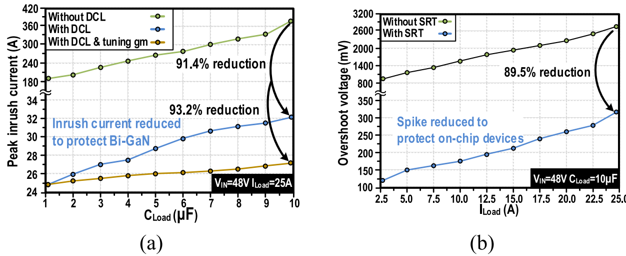


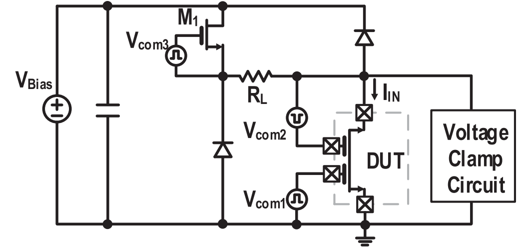
Fig. 26. (a) Inrush current versus C_{Load} with and without DCL. (b) Overshoot on V_{S1} versus I_{Load} with and without SRT.

turned ON with 5V V_{G2S2}. Figs. 24 and 25 show the zoomed-in turn-ON and turn-OFF operations. The proposed GD with Bi-GaN has a 347.4 μs rising propagation delay (T_{pdr}) and a 936.7 μs rising time (T_r) to turn ON Bi-GaN smoothly for delay (T_{pdf}) and a 483.6 ns falling time (T_f) to turn OFF Bi-GaN immediately for reverse current blocking. Fig. 26(a) demonstrates that utilizing DCL reduces the inrush current by 91.4% under a maximum load capacitance (C_{Load}) of 10 μF. Additionally, fine-tuning the user-defined transconductance achieves a further 1.8% reduction in the inrush current.

Fig. 26(b) shows that the implementation of the SRT effectively suppresses the overshoot on V_{S1}, achieving an overshoot suppression of 89. 5% under a maximum load current (I_{Load}) of 25 A. The reduction in voltage stress enhances the reliability of the on-chip power devices by preventing potential overstress. Also, it preserves the fast turn-OFF characteristics essential for high-performance switching operations.

Fig. 28 presents the wafer distributions of the measured R_{on} for the MBD fabricated with different FP structures, with each structure consisting of 50 measured samples. The R_{on} values of the conventional SFP MBD and the proposed SSFP MBD are nearly identical. However, after undergoing a 168-hour burn-in test, the R_{on} of the proposed SSFP MBD increases by only 28.5%, which is significantly lower than typically observed in conventional structures under similar stress conditions. This mitigation in the dynamic R_{on} of Bi-GaN effectively mitigates the conduction loss, enhancing the overall efficiency and reliability of the device during the on-state operation of the BLS. The dynamic R_{on} measurement circuit follows the setup shown in Fig. 3 of [21], as shown in Fig. 27(a). R_{on} is obtained from the ON-state voltage V_{S1S2} and current I_{IN}. M_1 is used to control the device under test (DUT) trapping time. R_L sets the current level when the DUT is in the ON-state. Static R_{on} is measured by applying the control signal shown in Fig. 27(b), where DUT is continuously ON and M_1 is controlled by a single pulse. Dynamic R_{on} is measured by applying the control signal shown in Fig. 27(c). The DUT is first turned OFF with M_1 applying a bias voltage (V_{Bias}) across it (trapping), then turned ON again to allow current conduction (detrapping). By varying the OFF period (t_1-t_2) and ON period (t_2-t_3), R_{on} under different trapping and detrapping conditions can be evaluated. The burn-in test to measure dynamic R_{on} is conducted over 168 h from t_1 to t_2. The R_{on} is measured 1 μs after t_2.

Fig. 29(a) illustrates the test bench setup designed to evaluate the turn-ON and turn-OFF propagation delays, where capacitors



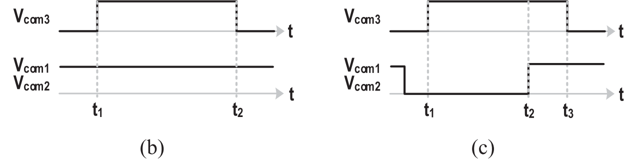


Fig. 27. (a) Dynamic R_{on} measurement circuit. (b) Control signal to measure static R_{on}. (c) Control signal to measure dynamic R_{on}.

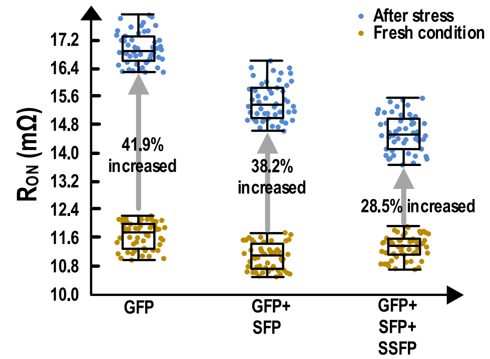
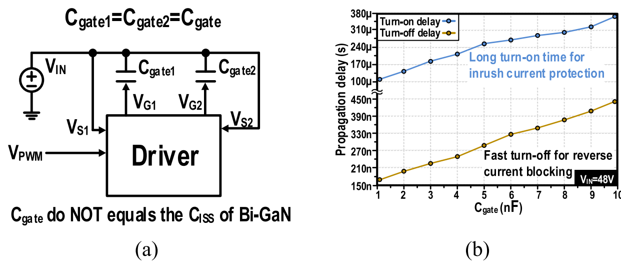


Fig. 28. Distributions of R_{on} for the MBD with different field plates.

TABLE I
COMPARISON TABLE WITH STATE-OF-THE-ART

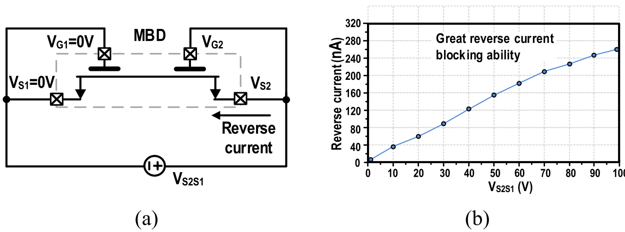
Design	This article	SiP32101 [10]	NX5P3001 [11]	AP22953 [12]	ADP198 [7]	MIC94080 [4]
Technology	Si: 0.18μm BCD; GaN: 0.5μm	N/A	N/A	N/A	N/A	N/A
Topology	Silicon driver + Bi-GaN switch	Silicon driver + PMOS switch	Silicon driver + NMOS switch	Silicon driver + NMOS switch	Silicon driver + PMOS switch	Silicon driver + PMOS switch
V_{IN_max} / I_{Load_max}	48V / 25A	5.5V / 7A	30V, *6.75V / 3A	5.9V / 3.5A	7V / 1A	6V / 2A
T_{pdr} / T_{pdf}	347.4 μs / 409.7 ns	80 μs / 120 μs	160 μs / 34.6 ms	15 ms / 5.22 μs	450 μs / N/A	0.4 μs / 60 ns
T_r / T_f	936.7 μs / 483.6 ns	1000 μs / 100 μs	1100 μs / 33 ms	N/A	650 μs / N/A	60 ns / 20 ns
R_{on}	11.2 mΩ	6.5 mΩ	62 mΩ	39 mΩ	40 mΩ	67 mΩ
(Dynamic R_{on})/R_{on}	1.285	N/A	N/A	N/A	N/A	N/A
Package Size	4.8 mm³	1.22 mm³	1.15 mm³	1.64 mm³	2.2 mm³	0.4 mm³
**FoM	22.3	4.9	1.3	0.3	0.08	0.4
Temp. Range	-40°C ~ 125°C	-40°C ~ 85°C	-40°C ~ 85°C	-40°C ~ 85°C	-40°C ~ 125°C	-40°C ~ 125°C
Inrush Current Protection	Yes	Yes	Yes	Yes	Yes	No
Spike Reduced Turn-off	Yes	No	No	No	No	No
Reverse Current Blocking	Yes	Yes	Yes	Yes	Yes	No
Bidirectional Transfer	Yes	Yes	Yes	Yes	No	No

*Two different maximum input voltage in two terminals; **FoM= (V_{IN_max}*I_{Load_max})/(R_{on}*Package Size) (Unit: V*A/mΩ*mm³))



(a) (b)

Fig. 29. (a) Test bench of delay versus C_{gate}. (b) Turn-ON and turn-OFF delay versus C_{gate}.



(a) (b)

Fig. 30. (a) Test bench of reverse current versus V_{S2S1}. (b) Reverse current versus V_{S2S1}.

C_{gate1} and C_{gate2} serve as gate capacitances to simulate various gate driving conditions. Fig. 29(b) presents the measured turn-ON and turn-OFF delays for different C_{gate} values. The extended turn-ON time, resulting from the DCL, effectively prevents the Bi-GaN from experiencing inrush current. Meanwhile, the fast turn-OFF time ensures prompt reverse current blocking. Fig. 30(a) depicts the test setup for evaluating the reverse current behavior of the Bi-GaN under different voltage conditions from

Fig. 31. Measurement setup of the charger system with proposed MBD BLS.

the second terminal to the first (V_{S2S1}). Fig. 30(b) shows the measured reverse current under different V_{S2S1}. V_{G1S1} and V_{G2S2} are both 0 V, and V_{G1} is 0 V in the reverse blocking test. The reverse current is less than 280 nA under 100 V V_{S2S1}, the reverse blocking capability effectively guarantees the safe operation of the BLS.

Fig. 31 shows the measurement setup of the charger system with the proposed MBD BLS. Fig. 32 presents the measured power efficiency of the charger system incorporating either the discrete B2B GaN BLS or the proposed MBD BLS. The results demonstrate that the proposed MBD BLS achieves a consistent improvement in system efficiency across the tested operating range. Specifically, a maximum enhancement of 0.9% in power efficiency is observed compared to discrete GaN BLS.

Table I gives that the proposed BLS has a maximum V_{IN} of 48 V and I_{Load} of 25 A with a low R_{on} of 11.2 mΩ by adopting Bi-GaN as the main PS. The inrush current protection with dynamic driving current control allows the GD to fully turn ON Bi-GaN for minimized R_{on} without the risk of overcurrent. The SRT blocks the reverse current fast without damaging the on-chip devices.

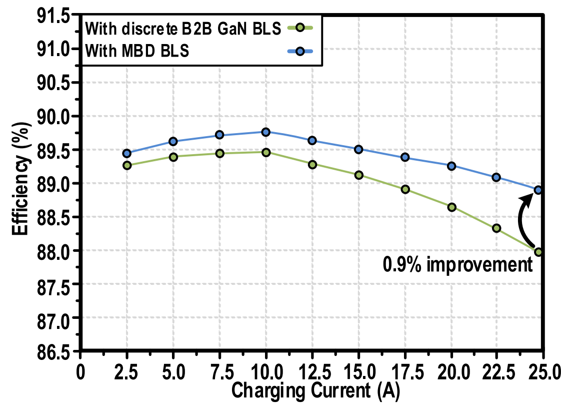


Fig. 32. Power efficiency of the charger system with discrete B2B GaN BLS and with proposed MBD BLS.

V. Conclusion

This article proposes a BLS that enables both bidirectional current flow and reverse current blocking. The proposed BLS supports a maximum input voltage of 48 V and a load current of 25 A, achieving an ON-resistance R_{on} of 11.2 mΩ. To regulate the turn-ON behavior of the Bi-GaN switch, a DCL is introduced, providing a turn-ON propagation delay T_{pdr} of 347.4 μs and a rise time T_r of 936.7 μs, effectively reducing inrush current by 91.4%. An SRT circuit dynamically adjusts the turn-OFF speed, enabling rapid deactivation with a T_{pdf} of 409.7 ns and a fall time T_f of 483.6 ns, reducing voltage overshoot by 89.5%. In addition, the Bi-GaN device with an SSFP structure mitigates the current collapse effect under extended high-voltage stress, limiting R_{on} degradation to 28.5% after 168 h of continuous operation.

Acknowledgment

The authors gratefully acknowledge the valuable support provided by Win-San (Vince) Khwa, Dr. Meng-Fan (Marvin) Chang, and the Joint Development Project (JDP) with Taiwan Semiconductor Manufacturing Company (TSMC) Ltd. The authors also thank Chen-Yen Ho from the MediaTek Advanced Research Center (MARC) for his important contributions.

References

[1] Analog Devices, "12 V, 2 A logic controlled high-side power switch," ADP1290 datasheet, Dec. 2014.
[2] Rohm Semiconductor, "1ch ultra small high side load switch," BUS1DJC0GWZ datasheet, Mar. 2014.
[3] Onsemi, "Integrated load switch," FDC6324L datasheet, Dec. 2021.
[4] Microchip, "67 mΩ $R_{DS(ON)}$ 2A high-side load switch in 0.85 mm x 0.85 mm FTDFN package," MIC94080 datasheet, Aug. 2018.
[5] NXP, "Logic controlled high-side power switch," NX5P2924D datasheet, Jun. 2020.
[6] Texas Instruments, "4.5-V, 1.5-A, 7.5-mΩ on-resistance fast turn-on load switch with regulated inrush current," TPS22999 datasheet, Nov. 2023.
[7] Analog Devices, "Logic controlled, 1 A, high-side load switch with reverse current blocking," ADP198 datasheet, Oct. 2011.
[8] Diodes Incorporated, "Single slew rate controlled load switch with true reverse current blocking," AP22913 datasheet, May 2021.
[9] Richtek, "70mΩ/55mΩ, 3A/2.5A/2A/1.5A/1A/0.5A High-side power switches with flag," RT9742 datasheet, Jan. 2020.
[10] Vishay, "6.5 mΩ, bidirectional switch in compact WCSP," SiP32101 datasheet, Apr. 2022.
[11] NXP, "Bidirectional high-side power switch for charger and USB-OTG applications," NX5P3001 datasheet, May 2023.
[12] Diodes Incorporated, "Switch for V_{BUS} line with overvoltage, surge, and ESD protection," AP22953 datasheet, Jan. 2022.
[13] Innoscience, "40V Bi-directional GaN enhancement-mode power transistor," INN040W048A datasheet, Aug. 2023.
[14] Nexperia, "40 V, 4.8 mOhm bi-directional gallium nitride (GaN) FET in a 2.1 mm x 2.1 mm wafer level chip-scale package (WLCSP)," GANB4R8-040CBA datasheet, Aug. 2024.
[15] G. Wang, H. Wen, W. Liu, and F. Li, "Physical structure, characteristics, and applications of monolithic bidirectional switches: A comprehensive review," *IEEE Trans. Power Electron.*, vol. 40, no. 7, pp. 9187–9199, Jul. 2025.
[16] X. Mu et al., "Floating-domain integrated GaN driver techniques for DC–DC converters: A review," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 9, pp. 3790–3805, Sep. 2023.
[17] P.-J. Chiu et al., "32.6 A dynamic-R_{ON}-diminished bidirectional GaN load switch with inrush current protection and spike attenuation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2025, pp. 538–540.
[18] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932–2941, Dec. 2006.
[19] J. P. Kozak et al., "Stability, reliability, and robustness of GaN power devices: A review," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8442–8471, Jul. 2023.
[20] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic on-resistance in GaN-on-Si HEMTs: Origins, dependencies, and future characterization frameworks," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5581–5588, Jun. 2020.
[21] K. Li, P. L. Evans, and C. M. Johnson, "Characterisation and modeling of gallium nitride power semiconductor devices dynamic on-state resistance," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5262–5273, Jun. 2018.
[22] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017.
[23] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-state resistance test and evaluation of GaN power devices under hard- and soft-switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019.
[24] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current collapse suppression by gate field-Plate in AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1379–1381, Nov. 2013.
[25] H. Huang, Y. C. Liang, G. S. Samudra, T.-F. Chang, and C.-F. Huang, "Effects of gate field plates on the surface state related current collapse in AlGaN/GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2164–2173, May 2014.
[26] A. Brannick, N. A. Zakhleniuk, B. K. Ridley, J. R. Shealy, W. J. Schaff, and L. F. Eastman, "Influence of field plate on the transient operation of the AlGaN/GaN HEMT," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 436–438, May 2009.
[27] W. Saito et al., "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 659–661, Jul. 2010.

Po-Jui Chiu was born in Taiwan in 2000. He received the B.S. degree in electronics and electrical engineering in 2023 from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree in electronics and electrical engineering.

He is a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU. His research interests include monolithic GaN-based integrated circuits, gate driver design, and bandgap reference circuits. He has authored four papers at the IEEE International Solid-State Circuits Conference in 2023, 2024, and 2025, and one paper at the International Electron Devices Meeting in 2023.

Xiao-Quan Wu was born in Taiwan in 2002. He received B.S. degrees in electronics and electrical engineering in 2024 from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree in electronics and electrical engineering.

He is a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU. He has authored or coauthored three papers at the International Solid-State Circuits Conference in 2024 and 2025, and two papers at the Symposium on VLSI Technology & Circuits in 2024. His research focuses on monolithic GaN-based integrated circuits.

Chi-Yu Chen was born in Taiwan in 2000. He received the B.S. degree in electronics and electrical engineering in 2023 from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree in electronics and electrical engineering.

He is a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU. He has authored four papers at the IEEE International Solid-State Circuits Conference in 2023, 2024, and 2025, and one paper at the International Electron Devices Meeting in 2023. His research interests include monolithic GaN-based integrated circuits, gate driver design, and LLC resonant converter design.

Yu-Ting Huang was born in Taiwan in 2001. He received B.S. degrees in electronics and electrical engineering from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, in 2024, where he is currently working toward the Ph.D. degree in electronics and electrical engineering.

He is a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU He has authored or coauthored three papers at the International Solid-State Circuits Conference in 2024 and 2025, and two papers at the Symposium on VLSI Technology & Circuits in 2024. His research focuses on monolithic GaN-based integrated circuits.

Chien-Wei Cho was born in Taiwan in 2002. He received the B.S. degree in electronics and electrical engineering in 2024 from the Department of Electronics and Electrical Engineering, National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, where he is currently working toward the M.S. degree in electrical and control engineering.

He is currently a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU.

Tz-Wun Wang received the B.S. and Ph.D. degrees in electronics and electrical engineering from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, in 2022 and 2024, respectively.

He was a Member of the Mixed-Signal and Power Management IC Laboratory, NYCU, where his research focused on monolithic GaN-based integrated circuit and device design, as well as power management IC design. From 2022 to 2024, he has authored or coauthored five papers at the International Solid-State Circuits Conference and one at the International Electron Devices Meeting in 2023. He is currently a Principal Engineer with Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

Sheng-Hsi Hung was born in Taipei, Taiwan. He received the M.S. degrees in electronics and electrical engineering from the National Yang Ming Chiao Tung University, Hsinchu, Taiwan, in 2010, and Ph.D. degree in electrical and control engineering from the Institute of Electrical and Control Engineering, Taichung City, Taiwan, in 2024.

He has authored or coauthored five papers at the International Solid-State Circuits Conference from 2022 to 2025, and one International Electron Devices Meeting in 2023. His research interests include high-frequency power conversion techniques and high-density module packaging and integration, and wide bandgap semiconductors design.

Ke-Horng Chen (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

He is currently a Chair Professor and an Associate Dean of the College of Electrical and Computer Engineering at National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan. He was the Chief Technology Officer with the Industrial Technology Research Institute in 2022. He leads the Mixed-Signal and Power IC Laboratory, NYCU, where his research focuses on advanced power management integrated circuit (PMIC) design. He is the author of the textbook *Power Management Techniques for Integrated Circuit Design* (IEEE Press and John Wiley, May 2016), which is widely used by students and engineers across Taiwan as a reference and design guide. Since joining NYCU in 2004, following industry experience as an IC design engineer in several leading firms. He has cultivated deep academic–industrial collaborations with major companies such as Realtek, Richtek, and Novatek. Over the past decade, he has led more than 80 collaborative research projects, securing over 65 million TWD in funding. His team's research has resulted in more than 50 U.S. patents and more than 50 Taiwan patents. He and his group have published approximately 300 papers in top-tier journals and international conferences. Notably, his team pioneered the first design methodology for single-inductor multiple-output (SIMO) converters, which significantly improve silicon area efficiency, power efficiency, and reduce cross-regulation issues. He has supervised more than 30 Ph.D. students and 210 M.S. students. At NYCU, he oversees the undergraduate program and three graduate programs—Electrical and Computer Engineering, Control Engineering, and Communications Engineering—comprising 82 full-time faculty, 16 adjunct faculty, 10 professional staff, and 1423 students (705 graduate and 718 undergraduate).

Dr. Chen is currently the Board of Directors of the IEEE Taipei Section. He was the Chair of the IEEE Circuits and Systems Society Taipei Chapter from 2015 to 2016, earning the Outstanding Chapter Award. He has been an Associate Editor for several major journals, including IEEE TRANSACTIONS ON POWER ELECTRONICS (since 2011), IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS (since 2022), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I (2014–2019), and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (2012–2013). His contributions to international conferences include serving on the Technical Program Committees of ISSCC (2021–2024), ESSCIRC (2011–2022), and CICC (2016). He was the General Co-Chair of the 2018 *International Workshop on Power Supply on Chip (PwrSoC)*, a premier event on integrated power conversion technologies. He was the recipient of received numerous prestigious awards, including: IEEE TPEL Associate Editor Excellence Award (2023); IEEE ISSCC Takuo Sugano Award for Outstanding Far-East Paper (2023); IEEE Taipei Section Outstanding Chapter Chair Award; Ministry of Science and Technology Outstanding Research Awards (2019, 2022); Outstanding Engineering Professor Award from the Chinese Institute of Engineers (2019); Hsing Yun Award for Education (2023); Nagamori Award (2023); National Invention and Creation Silver Award (2023); Pan Wen-Yuan Foundation Outstanding Research Award (2024); and MediaTek Advanced Research Center Outstanding Research Award (2025). As of 2025, He and his group have authored or coauthored a total of 30 papers at the IEEE International Solid-State Circuits Conference (ISSCC), including seven papers in the 2023 conference alone. He has also authored or coauthored two papers at the International Electron Devices Meeting (IEDM) in 2023 and 2025.

Ying-Hsi Lin received the B.S. degree in control engineering and electrical engineering from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, in 1993, and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1995.

He began his career in 1995 as a Researcher with the Computer & Communication Research Laboratory of the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. In 1998, he was a Project Leader, focusing on the design of complementary metal-oxide-semiconductor (CMOS) radio frequency (RF) and high-speed mixed-signal circuits. During his time at ITRI's Computer & Communications Laboratory, he worked extensively on CMOS RF and mixed-signal integrated circuit design for computer and communication applications. In October 1999, he was with Realtek Semiconductor Corp., as an RF Manager. There, he led several R&D projects in CMOS RF technologies, including Bluetooth, wireless local area networks (WLAN) covering 802.11a/b/g/n standards, WLAN for consumer electronics, and ultrawideband systems. He was also involved in planning the mass production of CMOS RF ICs. His technical expertise spans a wide range of circuit and system-level design, including RF synthesizers, low-noise amplifiers, mixers, modulators, power amplifiers, filters, programmable gain amplifiers, mixed-signal circuits, electrostatic discharge protection, RF device modeling, RF system calibration, and overall communication system architecture. In 2010, he was the Vice President and took charge of Realtek's Research & Design Center in Hsinchu, Taiwan. He holds more than 30 patents in the field of mixed-signal and RF IC design. Between 2015 and 2022, he published 107 journal papers and 12 papers at the International Solid-State Circuits Conference, demonstrating his continued leadership in cutting-edge semiconductor innovation.

Shian-Ru Lin was born in Nantou, Taiwan, in 1978. He received the B.S. degree in electronic engineering from National Taiwan University of Science and Technology, Taipei, Taiwan, in 2000, and the M.S. degree in electronic engineering from National Taiwan University, Taipei, Taiwan, in 2003.

In 2003, he was with the R&D Center, Realtek Semiconductor Corp., Hsinchu, Taiwan, where he is currently the Director. His research interests span a broad range of analog and mixed-signal circuit design, including high-speed and high-resolution data converters, timing recovery for communication systems, high-efficiency line drivers, and power management integrated circuits.

Tsung-Yen Tsai was born in Pingtung, Taiwan. He received the B.S. degree in control engineering and electrical engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2004, and the M.S. degree in communication engineering from National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, in 2006.

In 2006, he was an Analog Circuit Designer with Realtek Semiconductor Corporation, Hsinchu, Taiwan, where he has been actively involved in a variety of projects, including GPS, Bluetooth, and wireless LAN systems such as 802.11a/b/g, 802.11n, and 802.11ac. His research interests include current-mode digital-to-analog converters and switching regulators for system-on-chip applications.

Hann-Huei Tsai (Member, IEEE) was born in Taipei, Taiwan, in 1970. He received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan City, Taiwan, in 1992 and 1994, respectively.

Since 2025, he has been the Vice Chairman of the Taiwan Semiconductor Research Institute, part of the National Applied Research Laboratories.