A Current Sharing Strategy With Model Predictive Control for Multiphase Parallel *LLC*-Buck Converters

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***Abstract*—Input-series-output-parallel (ISOP) *LLC*-Buck converters are widely used in energy storage systems for their high efficiency and wide voltage gain range. However, parameter mismatches among parallel modules often cause power imbalance and degraded current sharing. This article proposes a model predictive control (MPC) based current sharing strategy for multiphase *LLC*-Buck converters. A current-sharing error model is established to analyze the impact of mismatched parameters, including resonant components, magnetizing inductance, switch characteristics, and Buck inductor resistance. Based on this, a fixed-frequency, single-step MPC algorithm is developed, incorporating real-time reference updates and an observer to correct model deviations. Compared with the widely used average current control, the proposed method enhances dynamic response, robustness, and current balance. A 500 W two-phase *LLC*-Buck prototype (48 V to 3.2 V) is built, and both simulation and experimental results validate the approach, achieving current sharing errors of 0.84% at half-load and 0.27% at full-load.**

***Index Terms*—Current-sharing, input-series output-parallel (ISOP), *LLC*-Buck converter, model prediction control (MPC).**

I. Introduction

With the improvement of integration and efficiency requirements in energy storage scenarios, input-series-output-parallel (ISOP) *LLC*-Buck converters have become a preferred choice due to their high efficiency and easy integration [1]. The *LLC* stage operates in open-loop as a direct current transformer (DCX) to achieve efficient energy transfer. In contrast, the Buck stage operates in closed-loop to regulate the output voltage [2], [3]. As system capacity increases and the output becomes low-voltage and high-current, the stress on power switches becomes a limiting factor. Multiphase parallel converters offer an effective and reliable solution to this issue [4], [5].

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However, in multiphase parallel systems, mismatches in circuit parameters—such as resonant inductance, capacitance, and passive components—often cause current imbalance [6], [7], [8], [9]. Accordingly, various current sharing strategies have been proposed to address this issue. For *LLC* converters, frequency regulation [10] and phase-shift control [11] are commonly used, but often lead to ripple inconsistency or limited adaptability.

Passive methods using common inductance or capacitance [12], [13], [14] are simple and scalable, yet their accuracy declines when parameter deviations are large. For Buck converters, typical strategies include average current, peak current, droop, and master-slave control [15], [16], [17], [18], [19], [20], which often requires multiple current sensors and raises system cost. A single-sensor method is proposed in [21] and [22], but it has limited dynamic performance and flexibility. For *LLC*-Buck combined topologies, research remains limited. A method in [23] adjusts the Buck inductor current to achieve current sharing, but assumes identical voltage gains across *LLC* modules and ignores parameter mismatches, limiting practical effectiveness. A recent study proposes a capacitive differential wireless power transfer architecture using a switched-capacitor-based converter to achieve balanced power delivery in multiport systems [24], offering valuable insights for extending current-sharing techniques to high-voltage, multioutput topologies.

Neural-network-based feedforward control can effectively regulate power flow in multiport converters without requiring precise circuit parameters [25]. Meanwhile, model predictive control (MPC) has gained attention in dc–dc converters for its simple structure, fast dynamic response, and strong robustness [26]. By predicting future system behavior and minimizing a defined cost function, MPC generates optimal control actions. It is generally categorized into continuous control set MPC (CCS-MPC) and finite control set MPC (FCS-MPC). While FCS-MPC enables direct switch control, it suffers from high computational complexity and variable switching frequency [27], whereas CCS-MPC offers fixed frequency and lower complexity, making it more suitable for multiphase systems [28].

Despite its advantages, MPC is sensitive to model accuracy, which poses challenges in parameter-varying conditions. Traditional approaches extend the prediction horizon [29] to improve accuracy, but this leads to increased computational complexity and reduced dynamic response speed. Recent approaches introduce model correction techniques. For instance, integral terms [30], perturbation variables [31], and duty-cycle-based weight factor tuning [32], [33], [34] have been proposed to improve

accuracy and stability. However, few of these techniques are applied in multiphase current sharing scenarios. Existing research on current-sharing control of *LLC*-Buck converters still has two key limitations: First, most methods (such as frequency regulation in [8] and PI-based average current control in [13]) do not quantify the impact of parameter mismatch on current-sharing accuracy—they fail to specify robustness indicators under ±10% deviation of *LLC* resonant inductance and ±20% deviation of Buck inductance, which is insufficient to support engineering design in industrial scenarios. Second, traditional passive current-sharing (see [20], [21], [22]) or single-loop PI control, when extended to multiphase systems, suffers from slow dynamic response or requires additional current sensors. To address the limitations above, a current sharing control strategy based on CCS-MPC is proposed in this article for multiphase ISOP *LLC*-Buck converters. A current error model is established, and a single-step predictive controller with fixed switching frequency is developed. The converter model is embedded into a dynamic current reference, enabling coordinated voltage and current control. To enhance robustness against parameter variations, a Luenberger observer is introduced to compensate for model deviations, and its stability region is analytically derived.

The main contributions of this work are summarized as follows.

1) To address the current imbalance caused by circuit parameter mismatches in multiphase ISOP *LLC*-Buck converters, a system-level model and current-sharing error model were established. The impact of key parameter mismatches—including resonant components and passive device tolerances—on current sharing performance was thoroughly analyzed.
2) To reduce control complexity and improve current regulation accuracy, a single-step, fixed-frequency CCS-MPC strategy was proposed. In this method, the converter model was integrated into a dynamically updated current reference, enabling effective voltage regulation and accurate current sharing under fixed switching frequency.
3) To enhance robustness against modeling inaccuracies and parameter deviations, a Luenberger observer was incorporated into the control framework. The observer's stability range was analytically derived, and reliable current sharing performance was achieved even under significant model uncertainty.

The rest of this article is organized as follows. Section II presents the circuit model and sensitivity analysis. Section III introduces the proposed MPC-based current sharing control strategy. Section IV provides simulation and experimental validation, respectively. Finally, Section V concludes this article.

II. Proposed Model Predictive Control Current Sharing Method

To mitigate the impact of circuit parameter mismatches on current sharing performance, a single-step model predictive current sharing method with fixed switching frequency is proposed. The overall control block diagram of the m-phase parallel *LLC*-Buck converter is illustrated in Fig. 1. The proposed control system mainly consists of a current prediction model and a dynamic current reference model, which incorporates both the current sharing model and the output voltage reference.

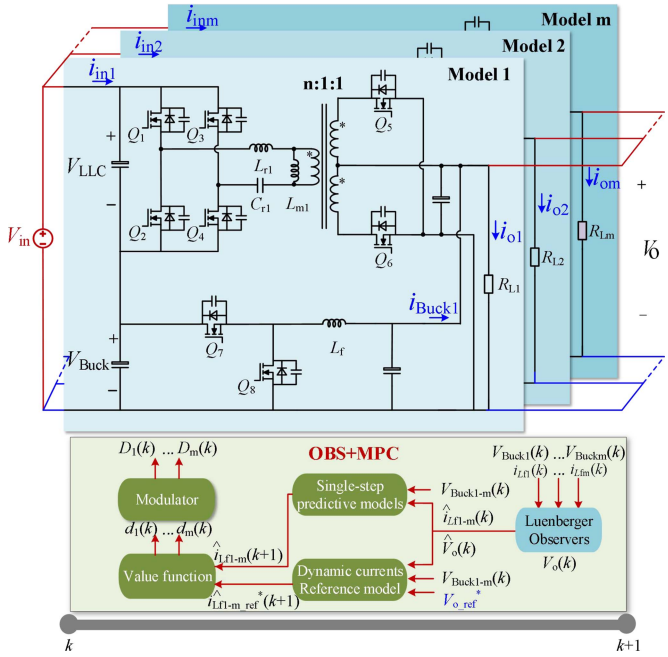

Fig. 1. Overall control block diagram of the m-phase parallel *LLC*-Buck converter.

To reduce sampling errors and suppress prediction deviations caused by parameter inconsistencies in the circuit model, a Luenberger observer is introduced. The observer output is employed to dynamically compensate both the current prediction model and the dynamic reference model in real time. Through the optimization of the value function, error-free tracking of each module's state variables and reference signals is achieved, thereby enabling both precise voltage regulation and highly accurate current sharing control.

To investigate the current sharing mechanism, a detailed analysis of multimodule parallel operation is carried out. This serves as a crucial preparatory step for the subsequent development and implementation of the model predictive current sharing method.

A. *Current-Sharing Error Modeling for Multiphase Parallel* LLC-*Buck Converters*

Fig. 2 illustrates a two-phase parallel *LLC*-Buck converter. Taking one module as an example, the symbols in Fig. 2 are defined as follows: L_{r1}, C_{r1}, and L_{m1} denote the resonant inductor, resonant capacitor, and magnetizing inductor of the *LLC* stage, respectively. L_{f1} represents the freewheeling inductor of the Buck stage. C_{in11}, C_{in12}, C_{o11}, and C_{o12} are the input and output capacitors of the *LLC* and Buck stages, respectively. V_{in} and V_o are the input and output voltages of the converter, while V_{LLC1} and V_{Buck1} are the input voltages of the *LLC* and Buck stages. i_{Cin11} and i_{Cin12} are the currents through the input capacitors of the *LLC* and Buck stages, and i_{Co11} and

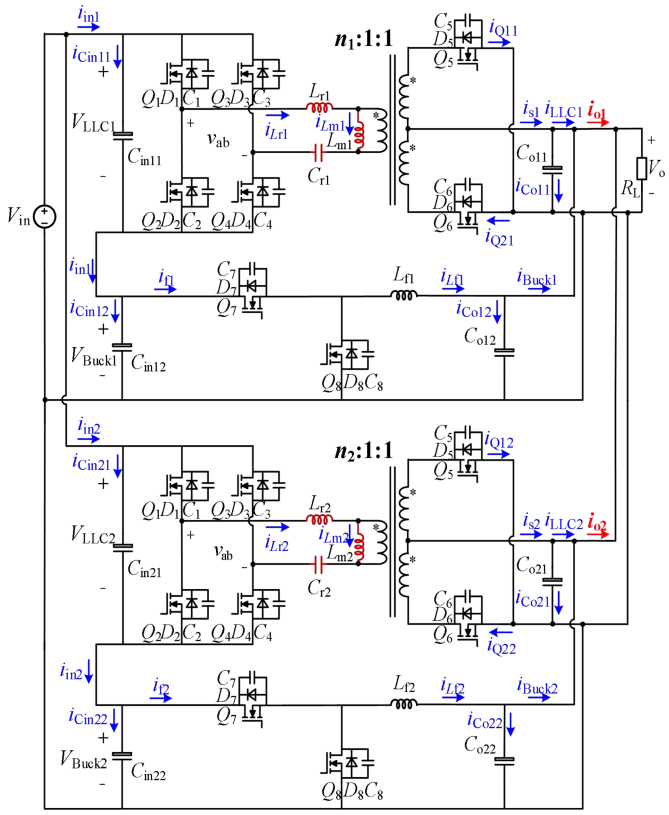

Fig. 2. Two-phase parallel *LLC*-Buck converter.

i_{Co12} are the corresponding output capacitor currents. i_{s1} and i_{Lf1} are the currents before the *LLC* output capacitor and after the Buck inductor, respectively. i_{LLC1} and i_{Buck1} denote the output currents of the *LLC* and Buck stages. i_{Lr1} and i_{Lm1} are the resonant and magnetizing currents of the *LLC* stage. i_{f1} is the input current of the Buck stage, and i_{o1} is the output current of the converter. The transformer turns ratio is denoted by n_1. The expression format of the second-phase model is consistent with that of the first-phase model.

Owing to the ISOP structure, the voltage and current relationships of the *LLC* and Buck stages are expressed as

$$\begin{cases} i_{LLC1} = i_{Co11} + i_{s1} \\ i_{Buck1} = i_{Co12} + i_{Lf1} \\ i_{o1} = i_{LLC1} + i_{Buck1} \end{cases} \tag{1}$$

$$\begin{cases} i_{Cin11} + i_{Lr1} = i_{Cin12} + i_{f1} \\ V_{in} = V_{LLC1} + V_{Buck1} \end{cases}. \tag{2}$$

It should be emphasized that KCL holds under all operating modes. In the freewheeling mode, the input capacitor current of the *LLC* stage is nearly zero, and the node equation reduces to $i_{Lr1} = i_{Cin12} + i_{f1}$. However, this mode occupies only about 5–10% of the switching period and has a negligible influence on the steady-state current distribution. In contrast, the resonant mode dominates the conduction interval and captures the essential current-sharing behavior. Therefore, the steady-state current-sharing error analysis in this article is derived from the KCL equation of the resonant mode.

Since the *LLC* resonant stage inherently operates with a voltage gain of unity in DCX mode, deviations arise in practical implementations due to component tolerances within the resonant network and variations in transformer design parameters across different modules. Consequently, the input–output voltage and current relationships of the *LLC* stage are accurately described by the expressions

$$\begin{cases} V_{LLC1} = n_1 V_o / M_{LLC1} \\ i_{s1} = n_1 (i_{Lr1} - i_{Lm1}) / M_{LLC1} \end{cases} \tag{3}$$

where M_{LLC} is the resonator gain of the *LLC*.

Neglecting the transmission loss, the Buck power relationship can be expressed as

$$V_{Buck1} i_{f1} = V_o i_{Lf1}. \tag{4}$$

During steady-state operation, the *LLC* converter mainly operates in the resonant mode (the freewheeling mode has a short duration and small current amplitude). Thus, deriving the output current i_{o1} based on the KCL relationship of the resonant mode can accurately reflect the steady-state current distribution law of the system. Since the magnetizing inductor L_m is much larger than the resonant inductor L_r, this results in a low proportion of the magnetizing current to the total primary current. Additionally, the i_{Lm} mismatch among multiple modules is small, and its impact on the current sharing error is negligible; thus, i_{Lm} is temporarily not considered. Thus, based on (1)–(4), the output current i_{o1} can be obtained as follows:

$$\begin{aligned} i_{o1} &= i_{s1} - i_{Co11} + i_{Lf1} - i_{Co12} \\ &= n_1 i_{Lr1} / M_{LLC1} + \frac{Vin - n_1 V_o / M_{LLC1}}{V_o} i_{f1} \\ &\quad - C_{o11} \frac{dV_o}{dt} - C_{o12} \frac{dV_o}{dt} \\ &= \frac{n_1}{M_{LLC1}} (i_{Cin12} - i_{Cin11}) + \frac{V_{in}}{V_o} i_{f1} \\ &\quad - (C_{o11} + C_{o12}) \frac{dV_o}{dt} \end{aligned} \tag{5}$$

where i_{Cin11} and i_{Cin12} in (5) are expressed as follows:

$$i_{Cin11} = C_{in11} \frac{dV_{LLC1}}{dt} = \frac{n_1 C_{in11}}{M_{LLC1}} \frac{dV_o}{dt} \tag{6}$$

$$i_{Cin12} = C_{in12} \frac{dV_{Buck1}}{dt} = C_{in12} \frac{dV_{in}}{dt} - \frac{n_1 C_{in12}}{M_{LLC1}} \frac{dV_o}{dt}. \tag{7}$$

By combining (5)–(7), the output current i_o can be simplified as

$$\begin{aligned} i_{o1} = \frac{n_1}{M_{LLC1}} \Bigg(& C_{in12} \frac{dV_{in}}{dt} - C_{in12} \frac{n_1}{M_{LLC1}} \frac{dV_o}{dt} \\ & - C_{in11} \frac{n_1}{M_{LL}} \frac{dV_o}{dt} \Bigg) - (C_{o11} + C_{o12}) \frac{dV_o}{dt} + \frac{V_{in}}{V_{Buck1}} i_{Lf1}. \end{aligned} \tag{8}$$

Under steady-state operating conditions, where all differential terms converge to zero, the resultant steady-state output current

can be mathematically expressed as

$$i_{o1} = \frac{V_{in}}{V_{Buck1}} i_{Lf1} = \frac{V_{in}}{V_{in} - n_1 V_o / M_{LLC1}} i_{Lf1}. \quad (9)$$

When operating in CCM, and considering the ON-resistance R_{s1} of the power switch and the internal resistance R_{L1} of the freewheeling inductor in the synchronous Buck converter, the output current i_{o1} of the Buck converter stage is derived according to the analytical formulation presented in [35] as follows:

$$\begin{aligned} i_{o1} &= \frac{V_{in}}{V_{in} - n_1 V_o / M_{LLC1}} \cdot \frac{V_{Buck1} D_1 - V_o}{(R_{s1} + R_{L1})} \\ &= \frac{V_{in}}{V_{in} - n_1 V_o / M_{LLC1}} \cdot \frac{(V_{in} - n_1 V_o / M_{LLC1}) D_1 - V_o}{(R_{s1} + R_{L1})} \end{aligned} \quad (10)$$

where D_1 denotes the duty cycle of the power switch in the Buck stage.

From (10), the output current of each converter in the two-phase parallel system is given by

$$\begin{cases} i_{o1} = \frac{V_{in}}{V_{in} - n_1 V_o / M_{LLC1}} \cdot \frac{(V_{in} - n_1 V_o / M_{LLC1}) D_1 - V_o}{(R_{s1} + R_{L1})} \\ i_{o2} = \frac{V_{in}}{V_{in} - n_2 V_o / M_{LLC2}} \cdot \frac{(V_{in} - n_2 V_o / M_{LLC2}) D_2 - V_o}{(R_{s2} + R_{L2})}. \end{cases} \quad (11)$$

Under identical duty cycle control ($D_1 = D_2$), the voltage gains of the two *LLC* units differ due to inherent design variations. In practical implementations, the internal resistances of power switches and inductors in the Buck stages cannot be precisely matched. As a result, the output currents of the modules deviate from each other.

The current sharing error between the two modules is defined

$$\delta_o = \text{abs}\left(\frac{i_{o1} - i_{o2}}{i_{o1} + i_{o2}} \right). \quad (12)$$

When δ_o equals zero, the output currents of the two modules are balanced. As δ_o increases, the current sharing error becomes more pronounced. A value of δ_o equal to one indicates that only one module is supplying current, resulting in a complete imbalance. According to (11), the factors contributing to the current sharing error can be categorized into two main aspects. The first involves the voltage gain M_{LLC} and the transformer turns ratio n of the *LLC* units. The second pertains to the internal resistances R_s and R_L associated with the power switch and the freewheeling inductor in the Buck stage.

To facilitate the development of the proposed MPC current sharing strategy, a sensitivity analysis is performed to examine how parameter mismatches affect the current distribution among modules.

B. Sensitivity Analysis of Parameter Mismatches on Current-Sharing Performance

Since a planar transformer structure is adopted and the transformer turns ratio is identical, its impact on current sharing can be neglected. Therefore, the current sharing error is primarily influenced by mismatches in L_r, C_r, L_m, R_s, and R_L. To quantitatively analyze the impact of these mismatches, dimensionless parameters a, b, c, e, f, and g are defined to represent the relative deviation of each corresponding component between the two modules

$$\begin{cases} L_{r2} = aL_{r1} & C_{r2} = bC_{r1} & L_{m2} = cL_{m1} \\ R_{s2} = eR_{s1} & R_{L2} = fR_{L1} & L_{f2} = gL_{f1} \end{cases}. \quad (13)$$

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE SYSTEM

Quantity	Symbol	Value
Input voltage	V_{in}	48 V
Output voltage	V_o	3.2 V
Switching frequency of the LLC/Buck stage	f_s/f_b	300 kHz/50 kHz
Total rated output power	P_N	500 W(250×2)
Resonant inductance	L_r	2.5 μH
Resonant capacitor	C_r	111 nF
Magnetizing inductance	L_m	25.6 μH
Turn ratio of the transformer	n	12
Equivalent on-state resistance of the power switch	R_s	1 mΩ
Parasitic resistance of the output inductor	R_L	7.5 mΩ

Based on the circuit parameters specified in Table I, this article conducts a comprehensive quantitative analysis of parameter mismatch effects on current sharing performance, with detailed results presented in Fig. 3 that illustrate both individual and combined impacts of component variations.

1) *Sensitivity Analysis of Resonant Inductance Mismatch in LLC Stage:* Fig. 3(a) illustrates the relationship between resonant inductance mismatch and current sharing error, assuming matched parameters in the Buck stage. When parameters b and c are greater than 1, the current sharing error initially decreases and then increases with the variation of a. For $a > 1$, the error increases monotonically. Furthermore, higher values of b and c lead to more significant current sharing errors. Specifically, when $a = b = c = 1.1$, the current sharing error reaches 96.5%.
2) *Sensitivity Analysis of Resonant Capacitance Mismatch in LLC Stage:* Fig. 3(b) shows the relationship between resonant capacitance mismatch and current sharing error, with Buck stage parameters remaining matched. When parameters a and c are greater than 1, the current sharing error initially decreases and then increases as b varies. For $b > 1$, the error increases continuously. In addition, higher values of a and c result in larger current sharing errors.
3) *Sensitivity Analysis of Magnetizing Inductance Mismatch in LLC Stage:* Fig. 3(c) illustrates the impact of magnetizing inductance mismatch on current sharing error, with matched Buck stage parameters. As parameter c increases, the current sharing error remains essentially unchanged.
4) *Sensitivity Analysis of Inductance Mismatch in Buck Converter:* Fig. 3(f) shows the effect of mismatch in Buck inductance parameters on system current sharing error, assuming matched *LLC* stage parameters. As parameter

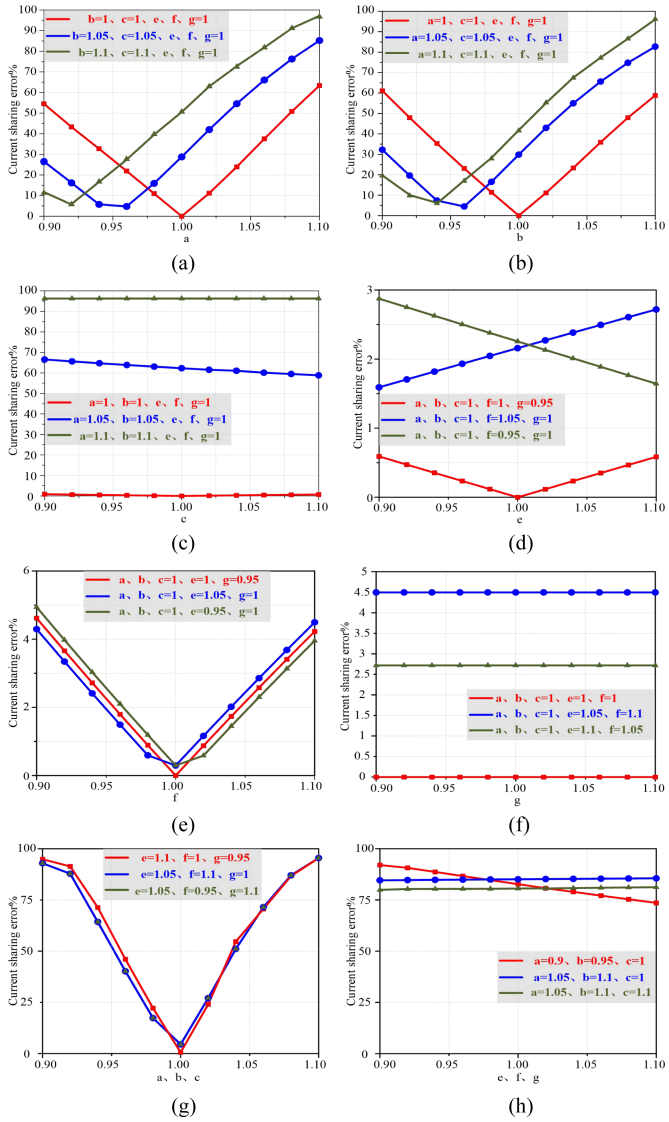

Fig. 3. Relationship curve of the current sharing error. (a) Effect of resonant inductance mismatch in the *LLC* stage. (b) Effect of resonant capacitance mismatch in the *LLC* stage. (c) Effect of magnetizing inductance mismatch in the *LLC* stage. (d) Effect of power switch parasitic resistance mismatch in the Buck stage. (e) Effect of inductor parasitic resistance mismatch in the Buck stage. (f) Effect of inductance mismatch in the Buck stage. (g) Effect of overall parameter mismatch on the *LLC* side. (h) Effect of overall parameter mismatch on the Buck side. (Test conditions: Input voltage $V_{\text{in}} = 48$ V, output voltage $V_{\text{o}} = 3.2$ V, ambient temperature 25 °C, *LLC* switching frequency $f_{\text{s}} = 300$ kHz, Buck switching frequency $f_{\text{b}} = 50$ kHz).

g increases, the current sharing error remains nearly constant.

5) *Sensitivity Analysis of Parasitic Resistance Mismatch in Buck Power Switch:* Fig. 3(d) illustrates the impact of power switch parasitic resistance mismatch on the current sharing error. As observed in Fig. 3(f), parameter g does not influence the current sharing performance. When $f = 0.95$, the current sharing error decreases with increasing e; when $f = 1.05$, the error increases with e; and when $f = 1$, the error first decreases and then increases as e changes. For example, when $e = 0.9$, $f = 0.95$, and $g = 0.95$, the resulting current sharing error is 2.85%.

6) *Sensitivity Analysis of Inductor Parasitic Resistance Mismatch in Buck Converters:* Fig. 3(e) shows the impact of inductance parasitic resistance mismatch on the system's current sharing error. As f increases, the current sharing error first decreases and then increases. A larger e leads to a greater current sharing error. For instance, when $e = 0.95$, $f = 0.9$, and $g = 1$, the current sharing error reaches 4.96%.

7) *Sensitivity Analysis of System Parameter Mismatch:* Fig. 3(g) illustrates the effect of parameter mismatches in the *LLC* unit on current sharing error. As a, b, and c increase, the current sharing error initially decreases and then increases. The variations in these parameters significantly affect the current sharing performance, with the error ranging from 0% to 96.5% as a, b, and c vary from 0.9 to 1.1. Fig. 3(h) presents the influence of the Buck unit parameter mismatch on current sharing error. When a, $b > 1$, the current sharing error remains relatively constant with changes in e, f, and g. When a, $b < 1$, the error decreases with increasing e, f, and g. These Buck-side parameters exhibit a comparatively lower impact, with current sharing error varying from 74.3% to 90.2% as e, f, and g change from 0.9 to 1.1.

In conclusion, the following observations can be made.

1) Variations in the inductance value have a negligible impact on current sharing error.
2) Deviations in magnetizing inductance result in only minor changes to the current sharing error, indicating a certain level of system tolerance.
3) The impact of parameter mismatch in the *LLC* unit is significantly greater than that in the Buck unit.

Specifically, a 5% deviation in the resonant parameters of the *LLC* stage leads to a current sharing error exceeding 30%, whereas a 10% deviation in the Buck stage parameters results in a maximum error of only 5%, demonstrating the critical importance of accurate *LLC* parameter design.

III. Modeling and Optimization Design

Since the *LLC* stage operates in DCX mode, current sharing is primarily achieved by adjusting the duty cycle of the Buck stage. Based on the notations shown in Fig. 2, the continuous-time domain model of the Buck unit can be expressed in terms of the inductor current i_{Lf} and output capacitor voltage u_{o} as follows:

$$L_{\text{f}} \frac{di_{\text{Lf}}(t)}{dt} = (V_{\text{Buck}}(t)d(t) - V_{\text{o}}(t)) \tag{14}$$

$$C_{\text{o2}} \frac{du_{\text{o}}(t)}{dt} = \left(i_{\text{Lf}}(t) - \frac{V_{\text{o}}(t)}{R_{\text{o2}}}\right) \tag{15}$$

where $d(t)$ denotes the control input of the system, corresponding to the switching state of transistor Q_7. $Q_7 = 1$ indicates the switch is ON, and $Q_7 = 0$ indicates it is OFF. R_{o2} represents the equivalent load resistance, C_{o2} is the output capacitance of the Buck stage, and T_{s} denotes the switching period. $V_{\text{Buck}}(t)$ is the input voltage applied to the Buck stage.

Based on the continuous-time model, a discrete-time representation of the Buck stage is derived using the first-order Euler

approximation method

$$i_{Lf}(k+1)=\frac{V_{\mathrm{Buck}}(k)d(k)T_{\mathrm{s}}-V_{\mathrm{o}}(\mathrm{k})T_{\mathrm{s}}}{L_{\mathrm{f}}}+i_{\mathrm{Lf}}(k) \tag{16}$$

$$V_{\mathrm{o}}(k+1)=\frac{V_{\mathrm{o}}(k)T_{\mathrm{s}}}{R_{\mathrm{o2}}C_{\mathrm{o2}}}-\frac{i_{\mathrm{Lf}}(k)T_{\mathrm{s}}}{C_{\mathrm{o2}}}+V_{\mathrm{o}}(k) \tag{17}$$

where T_{s} is the sampling period, which also serves as the switching period of the Buck unit. $i_{\mathrm{Lf}}(k)$, $V_{\mathrm{Buck}}(\mathrm{k})$, and $V_{\mathrm{o}}(\mathrm{k})$ represent the sampled inductor current, input voltage, and output voltage of the Buck stage at the time instant kT_{s}, respectively. The output capacitor voltage is equal to the output voltage. $d(k)$ denotes the duty cycle of the Buck switch at kT_{s}, and $i_{\mathrm{Lf}}(k+1)$ is the predicted inductor current at the next sampling instant $(k+1)T_{\mathrm{s}}$ moment.

A. Direct Current MPC Formulation

To achieve effective current sharing and ensure a stable load current, a standard current tracking error-based cost function is formulated

$$J(k)=\sum_{1}^{N}\left[{i_{\mathrm{Lf}}}^{*}(k+i)-i_{\mathrm{Lf}}(k+i\,|k)\right]^{2} \tag{18}$$

where $i_{\mathrm{Lf}}{*}(k+i)$ denotes the reference value of the Buck inductor current at time $k+i$, and $i_{\mathrm{Lf}}(k+i\,\big|\,, k)$ represents the predicted value at the same time. A larger prediction index i expands the prediction horizon, enhancing system stability but increasing model complexity. N defines the total prediction horizon; while a larger N improves stability, it also imposes a greater computational load on the predictive controller, potentially reducing response speed. In this article, both N and i are set to 1. To achieve accurate voltage regulation with low computational burden, a properly designed dynamic current reference is required to coordinate voltage control and current sharing.

Herein, the control frequency of the proposed CCS-MPC control strategy is synchronized with the switching frequency of the Buck stage, which is 50 kHz (corresponding to a discrete sampling period $T_{\mathrm{s}}=20\ \mu$s). It matches the switching timing of the Buck stage to avoid control conflicts among multiple modules.

B. Design of the Proposed Dynamic Current Reference

Due to variations in the voltage gain of each *LLC* unit, the input voltage applied to each equivalent Buck stage in the m-phase parallel system differs accordingly

$$V_{\mathrm{Buck1}}\neq\cdots\neq V_{\mathrm{Buckm}}. \tag{19}$$

Let the rated power of each phase cascaded *LLC*-Buck converter be denoted as P_{N}, and assume that the input power of each module is equal

$$P_{\mathrm{N1}}=\cdots=P_{\mathrm{Ni}}=\cdots=P_{\mathrm{Nm}}=P_{\mathrm{N}} \tag{20}$$

where P_{Ni} denotes the rated input power of the ith module. Based on the input–output characteristics of the cascaded *LLC*-Buck converter, the power delivered by the Buck stage of phase i is given by

$$P_{\mathrm{Bucki}}=\frac{V_{\mathrm{Bucki}}}{V_{\mathrm{in}}}P_{\mathrm{N}} \tag{21}$$

where P_{Bucki} denotes the input power of the ith phase Buck unit, and V_{Bucki} represents the input voltage of the ith phase Buck unit. Therefore, the equivalent output load R_{oi} of the ith phase Buck can be expressed as

$$R_{\mathrm{oi}}=\frac{{V_{\mathrm{o}}}^{2}}{P_{\mathrm{Bucki}}}. \tag{22}$$

From (21) to (22), the ratio of the equivalent output load for each phase of the Buck unit is

$$\begin{aligned}R_{\mathrm{o1}}:\ldots:R_{\mathrm{om}}&=\frac{{V_{\mathrm{o}}}^{2}}{P_{\mathrm{Buck1}}}:\ldots:\frac{{V_{\mathrm{o}}}^{2}}{P_{\mathrm{Buckm}}}\\&=\frac{1}{V_{\mathrm{buck1}}}:\ldots:\frac{1}{V_{\mathrm{buckm}}}.\end{aligned} \tag{23}$$

The equivalent output of the Buck unit in the m-phase parallel system can be expressed as

$$\sum_{1}^{\mathrm{m}}i_{\mathrm{Lfi}}=\sum_{1}^{m}i_{\mathrm{c2i}}+\frac{V_{\mathrm{o}}}{R_{\mathrm{o-Buck}}} \tag{24}$$

where i_{c2i} represents the output capacitor current of each module's Buck unit, the overall equivalent load of the Buck in the m-phase system is

$$R_{\mathrm{o-Buck}}=\frac{V_{\mathrm{o}}}{\sum_{1}^{m}i_{\mathrm{Lfi}}-\sum_{1}^{m}i_{\mathrm{C2i}}} \tag{25}$$

where $R_{\mathrm{o\text{-}buck}}$ denotes the output resistance of the Buck converters in all modules.

Therefore, the equivalent output load of the ith module's Buck unit can be expressed as

$$R_{\mathrm{o-Bucki}}=\frac{\sum_{1}^{m}V_{\mathrm{Bucki}}}{V_{\mathrm{Bucki}}}R_{\mathrm{o-Buck}}. \tag{26}$$

The dynamic reference value of the inductor current of the ith module Buck unit is

$${i_{\mathrm{Bucki}}}^{*}=\frac{{V_{\mathrm{o}}}^{*}}{R_{\mathrm{o-Bucki}}} \tag{27}$$

where ${i_{\mathrm{Bucki}}}^{*}$ and ${V_{o}}^{*}$ represent the output current and output voltage reference values of the ith module's Buck unit. Since the outputs of each module are connected in parallel, ${V_{\mathrm{o}}}^{*}$ also serves as the overall output voltage reference for the system. To achieve current sharing in parallel systems, the following can be derived:

$$I_{\mathrm{o1}}=I_{\mathrm{o2}}=\cdots=I_{\mathrm{om}}. \tag{28}$$

Based on (9), given that the input voltages of modules in the m-phase parallel system are equal, the condition for achieving current sharing among the modules can be expressed as

$$\frac{I_{Buck1}}{V_{\mathrm{Buck1}}}=\frac{I_{Buck2}}{V_{\mathrm{Buck2}}}=\cdots=\frac{I_{Buckm}}{V_{\mathrm{Buckm}}}. \tag{29}$$

If the output current value of the *i*th Buck unit is represented by (27), then the current reference value of the other modules is

$$i_{\mathrm{Buckj}}{}^{*} = \frac{i_{\mathrm{Bucki}}{}^{*}}{V_{\mathrm{Bucki}}} V_{\mathrm{Buckj}} \qquad i \neq j \tag{30}$$

where $i_{\mathrm{Buckj}}{}^{*}$ denotes the output current reference of the *j*th Buck unit with $i \neq j$. During the dynamic adjustment process, the reference values of each module vary over time. Accordingly, the dynamic current references of each module, after discrete-time processing, can be expressed as

$$\begin{cases} i_{\mathrm{Bucki}}{}^{*}(k+1) = \dfrac{V_{\mathrm{o}}{}^{*} V_{\mathrm{Bucki}}(k)\left(\sum_{1}^{m} i_{\mathrm{Lfi}}(k) + \sum_{1}^{m} C_{\mathrm{oi2}} \frac{V_{\mathrm{o}}(k) - V_{\mathrm{o}}(k-1)}{T_{\mathrm{s}}}\right)}{V_{\mathrm{o}}(k) \sum_{1}^{m} V_{\mathrm{Bucki}}(k)} \\ i_{\mathrm{Buckj}}{}^{*}(k+1) = \frac{i_{\mathrm{Bucki}}{}^{*}(k+1)}{V_{\mathrm{Bucki}}(k)} V_{\mathrm{Buckj}}(k) \end{cases} \tag{31}$$

where the core function is to ensure that the reference value of the inductor current of each phase Buck stage not only tracks the output voltage demand (V_{o}^{*}) but also meets the current sharing demand ($i_{\mathrm{Bucki}}^{*} = i_{\mathrm{Buckj}}^{*}$) under fixed switching frequency.

C. Design of Observer-Based Strategy (OBS)

In practical engineering applications, deviations in passive component parameters and limited measurement accuracy can lead to discrepancies between actual values and their sampled counterparts. These discrepancies introduce uncertainty into the state variables of both the dynamic reference model and the predictive model. To address this issue, an observer is implemented to estimate and correct the predicted state variables and reference trajectories. Specifically, a Luenberger observer is designed by incorporating output error feedback to enhance state estimation accuracy and improve the overall robustness of the model.

Based on (16), (17), the discrete-time state-space representation of the Buck unit is formulated in matrix form as follows:

$$\begin{aligned} x(k+1) &= A_{\mathrm{L}} x(k) + B_{\mathrm{L}}(k) u(k) + E_{\mathrm{L}} w(k) \\ y(k) &= C_{\mathrm{L}} x(k) \end{aligned} \tag{32}$$

where $x(k)$ denotes the state variables of the Buck unit, $u(k)$ represents the switching state of the power device, $\omega(\mathrm{k})$ is the output current of the Buck unit, and $y(k)$ is the output variable of the Buck unit. The matrices in the model are given as follows:

$$\begin{aligned} x(k) &= \begin{bmatrix} i_{\mathrm{Lf}}(k) & V_{\mathrm{o}}(k) \end{bmatrix}^{\mathrm{T}} u(k) = \begin{cases} 1 & Q_7 = 1 \\ 0 & Q_7 = 0 \end{cases} \\ w(k) &= i_{\mathrm{Buck}}(k) \quad y(k) = \begin{bmatrix} i_{\mathrm{Lf}}(k) & V_{\mathrm{o}}(k) \end{bmatrix}^{\mathrm{T}} \\ A_{\mathrm{L}} &= \begin{bmatrix} 1 & -\frac{T_{\mathrm{s}}}{L_{\mathrm{f}}} \\ \frac{T_{\mathrm{s}}}{C_{\mathrm{o2}}} & 1 \end{bmatrix} B_{\mathrm{L}} = \begin{bmatrix} \frac{T_{\mathrm{s}} V_{\mathrm{Buck}}(k)}{L_{\mathrm{f}}} & 0 \end{bmatrix}^{\mathrm{T}} \\ C_{\mathrm{L}} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} E_{\mathrm{L}} = \begin{bmatrix} 0 & -\frac{T_{\mathrm{s}}}{C_{\mathrm{o2}}} \end{bmatrix}^{\mathrm{T}}. \end{aligned} \tag{33, 34}$$

A standard Luenberger observer is designed, which can be formulated as

$$\begin{aligned} \hat{x}(k+1) &= A_{\mathrm{L}} \hat{x}(k) + B_{\mathrm{L}}(k) u(k) + E_{\mathrm{L}} w(k) + L(y(k) - \hat{y}(k)) \\ \hat{y}(k) &= C_{\mathrm{L}} \hat{x}(k) \end{aligned} \tag{35}$$

where represents the estimated state variables of the Buck unit, $\hat{\mathrm{y}}(\mathrm{k})$ is the estimated output, and L is the observer gain matrix to be determined. Define the estimation error as $\bar{e}(\mathrm{k}) = \mathrm{x}(\mathrm{k}) - \hat{\mathrm{x}}(\mathrm{k})$. By combining (32) and (35), the following expression is obtained:

$$\bar{e}(k+1) = (A_{\mathrm{L}} - LC_{\mathrm{L}}) \bar{x}(k+1). \tag{36}$$

According to the stability criterion, a matrix (A_{L}-LC_{L}) is stable if all eigenvalues of the matrix (A_{L}-LC_{L}) lie within the unit circle. This ensures that the estimation error diminishes over time, providing reliable state information for the controller. Therefore, the estimated values provided by the observer in (35) can be used to replace the corresponding predicted quantities in (32) and the reference values in (31), enabling correction for parameter uncertainties and improving system robustness. Fig. 4 illustrates the detailed control block diagram.

D. Stable Analyse

1) OBS Stability Analysis: The gain matrix of the observer is given by (A_{L}-LC_{L}). The observer is stable if the absolute values of all eigenvalues of the gain matrix are less than 1. Accordingly, the characteristic matrix of the system can be expressed as

$$\lambda I - (A_{\mathrm{L}} - LC_{\mathrm{L}}) = \begin{bmatrix} \lambda + L_1 - 1 & L_2 + \frac{T_{\mathrm{s}}}{L_{\mathrm{f}}} \\ L_2 - \frac{T_{\mathrm{s}}}{C_{\mathrm{o2}}} & \lambda + L_1 - 1 \end{bmatrix} \tag{37}$$

where I is the 2×2 identity matrix.

L_1 and L_2 are the parameters of the gain matrix in the Luenberger observer, which can be expressed as

$$L = \begin{bmatrix} L_1 & L_2 \\ L_2 & L_1 \end{bmatrix}. \tag{38}$$

λ denotes the eigenvalue of the system's gain matrix, which can be obtained by solving the characteristic matrix

$$\begin{cases} \lambda_1 = \sqrt{(L_2 - \frac{T_{\mathrm{s}}}{C_{\mathrm{o2}}})(L_2 + \frac{T_{\mathrm{s}}}{L_{\mathrm{f}}})} - L_1 + 1 \\ \lambda_2 = -\sqrt{(L_2 - \frac{T_{\mathrm{s}}}{C_{\mathrm{o2}}})(L_2 + \frac{T_{\mathrm{s}}}{L_{\mathrm{f}}})} - L_1 + 1. \end{cases} \tag{39}$$

Based on the parameters listed in Table I, the stability range of the observer can be determined, as shown in Fig. 5.

The selection of L_1 and L_2 governs the attenuation rate of the observer, thereby influencing the overshoot and dynamic response of the system voltage and current. Based on the parameters listed in Table I, and maintaining all other parameters constant ($a = 1.05, b = 1.1, e = 0.8, f = 1.2, g = 1.1$), a two-phase parallel system simulation platform is developed. By defining $\gamma = L_1/L_2$, the overshoot and response speed of the system voltages and currents under varying γ values are illustrated in Fig. 6.

Simulation results indicate that as γ increases, the output current response speed improves and overshoot decreases, whereas the output voltage response slows and overshoot increases. From (35), a larger L_1 corresponds to greater weighting of the Buck inductor current estimation by the observer, accelerating error attenuation and enhancing current stability.

The output current settles within 420 μs with overshoot under 12.5%, while the output voltage settles within 2.4 ms with overshoot below 9.3%. Thus, L_1 and L_2 must be properly

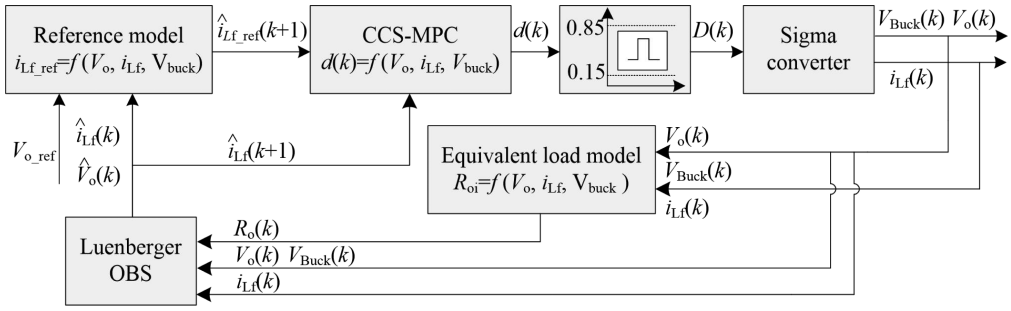

Fig. 4. Proposed control block diagram.

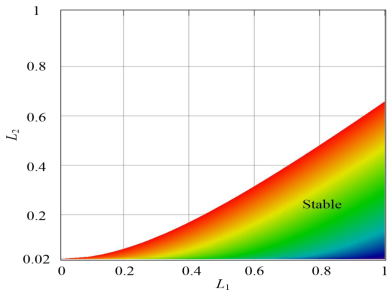

Fig. 5. Observer stability range.

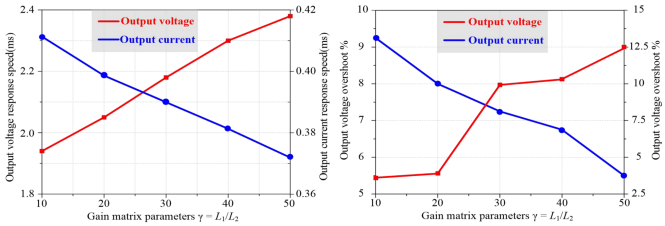

Fig. 6. Influence of gain matrix parameters on the dynamic performance of the system. (a) $\gamma = L_1/L_2$ is the relationship between voltage and current response speed. (b) $\gamma = L_1/L_2$ is the relationship between voltage and current overshoot.

chosen to balance system performance and satisfy application requirements.

2) Cost Function Stability Analysis: The cost function determines the optimal control law of the system. To ensure that the estimated inductor current can effectively track its reference value, it is necessary to derive the optimal duty cycle of the switching signal that minimizes the value function. Therefore, the explicit solution for the duty cycle is obtained by taking the first-order partial derivative of the value function with respect to $d(k)$. To verify that this duty cycle corresponds to a minimum of the cost function, the second-order partial derivative of the value function with respect to $d(k)$ is further calculated

$$\frac{\partial^2 J(k)}{\partial^2 d(k)} = \left(\frac{T_s V_{\text{Buck}}(k)}{L_f}\right)^2 \geq 0. \tag{40}$$

From (40), it can be seen that the second-order partial derivative of the cost function $J(k)$ with respect to $d(k)$ is always positive, indicating that the first-order partial derivative is monotonically increasing. Therefore, the optimal control duty cycle corresponds to the minimum of the cost function. Substituting this optimal duty cycle back into the cost function yields a value of zero. This confirms that the estimated inductor current state accurately tracks the reference value at each iteration, resulting in zero tracking error.

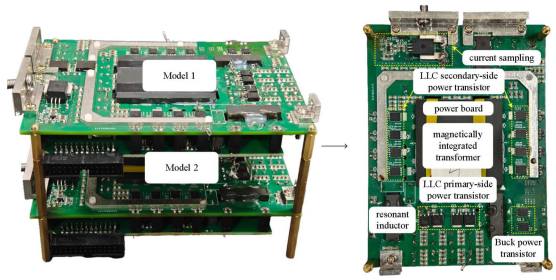

Fig. 7. Experimental platform. (Model 1 is a module with nominal parameters, and Model 2 is a module with parameter mismatches (L_r deviates by 5% and C_r deviates by 10% from nominal values)).

IV. Experimental Verification

To verify the effectiveness of the proposed method, a two-phase parallel experimental platform is constructed, as shown in Fig. 7. The rated inductance of the Buck converter is 22 μH. To reduce conduction losses, *LLC* primary-side power MOSFETS adopt HSU8048, *LLC* secondary-side and Buck power MOSFETS use CSD17573Q5B, with their built-in body diodes serving instead of external diodes in both the *LLC* and Buck stages. The input capacitance of both the *LLC* and Buck stages is 880 μF, and the output capacitance is 1000 μF. The experimental parameters of the prototype are listed in Table I. For the second prototype, parameter mismatches are introduced with $a = 1.05$ and $b = 1.05$.

The magnetizing inductance depends on the planar transformer's air gap, which cannot be precisely controlled. The transformer turns ratio is fixed by the PCB process and generally remains consistent. Parasitic resistances of the Buck stage's power switch and inductor are hard to measure and assumed to vary due to manufacturing tolerances. To achieve desired voltage and current transient responses, the observer gains are set to $L_1 = 0.4$ and $L_2 = 0.02$ in both simulation and experiments. The predictive model uses an inductance $L_f = 22$ μH and an output capacitance $C_{o2} = 1000$ μF.

Furthermore, the control frequency is set to 50 kHz, synchronized with the Buck stage switching. The computational

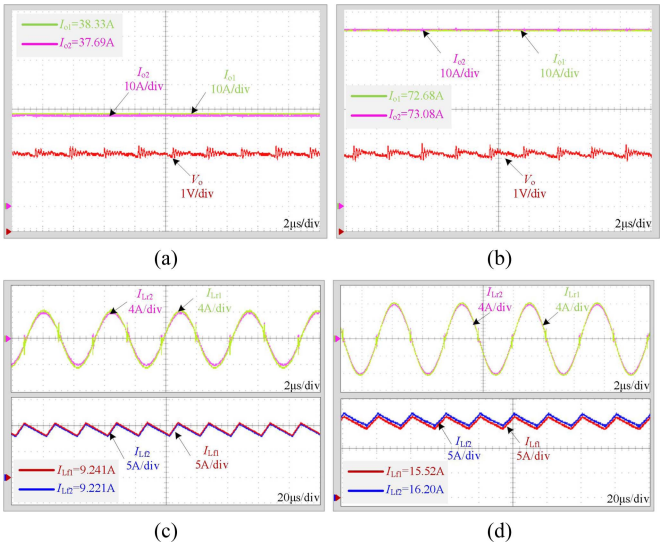

Fig. 8. Key waveforms of the two-phase parallel *LLC*-Buck converter under half-load and full-load conditions. (a) Output waveform at half load. (b) Output waveform at full load. (c) Current waveform at half load. (d) Current waveform at full load. (Half load: 250 W, Full load: 500 W; Input voltage $V_{\text{in}} = 48$ V, Ambient temperature 25 °C).

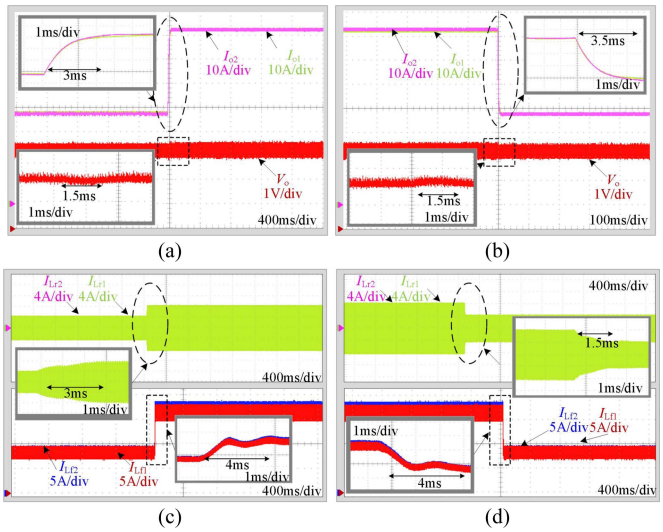

Fig. 9. Key waveforms during dynamic load changes. (a) Output waveform during half-load to full-load switching. (b) Output waveform during full-load to half-load switching. (c) Current waveform during half-load to full-load switching. (d) Current waveform during full-load to half-load switching. (Half load to full load: 250 W→500 W; Full load to half load: 500 W→250 W; Input voltage $V_{\text{in}} = 48$ V).

requirements of the OBS+MPC controller were evaluated on a 200 MHz DSP platform. Each cycle takes approximately 3 μs, which is well below the 20 μs control period, ensuring real-time feasibility in practical implementation.

The key waveforms of the two-phase parallel *LLC*-Buck converter are presented in Fig. 8. Under half-load (250 W) operation, the output currents of the two modules are $I_{\text{o1}} = 38.33$ A and $I_{\text{o2}} = 37.69$ A, respectively. Under full-load conditions, the output currents increase to $I_{\text{o1}} = 72.68$ A and $I_{\text{o2}} = 73.08$ A. The corresponding current sharing error is calculated as follows:

$$\begin{cases} \delta_{\text{o-half-load}} = \frac{38.33-37.69}{38.33+37.69} = 0.84\% \\ \delta_{\text{o-full-load}} = \frac{73.08-72.68}{73.08+72.68} = 0.27\%. \end{cases} \tag{41}$$

When the system operates in steady state, the dynamic response during load transients is illustrated in Fig. 9. As shown in Fig. 9(a) and (b), the two modules maintain effective current sharing during load switching, and the output voltage is regulated at 3.2 V. The dynamic response time of the output current is approximately 3 ms, while the output voltage stabilizes within 1.5 ms. The *LLC* resonant current settles within 3 ms, and the Buck inductor current reaches a new steady state in approximately 4 ms. Notably, all key waveforms exhibit no overshoot during the load transition.

Fig. 10 is the steady-state temperature diagram of the prototype. As can be seen from the diagram, the maximum temperature of the core power devices on the single power board is 62.8 °C with an average temperature of 54.7 °C, and the maximum temperature of the overall prototype is 72.0 °C with an average temperature of 50.2 °C; both temperatures are far below the 150 °C junction temperature limit of the power devices.

To verify the superiority of the proposed method, comparative experiments were conducted under identical conditions. The key current-sharing waveforms obtained using a conventional

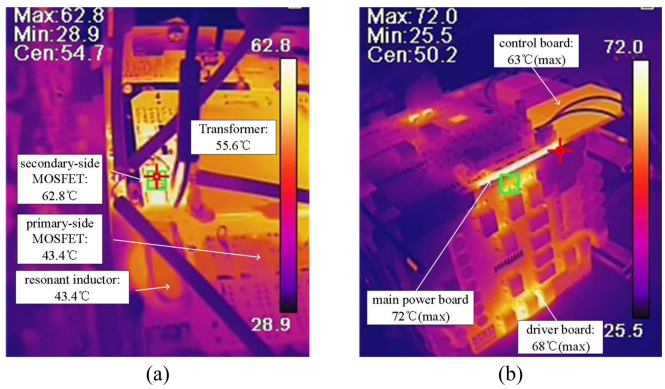

Fig. 10. Steady-state temperature diagram. (a) Single power board (b) Bidirectional parallel prototype.

PI controller are shown in Fig. 11. Under half-load conditions, the output currents of the two modules are $I_{\text{o1}} = 38.45$ A and $I_{\text{o2}} = 37.37$ A. At full load, the output currents are $I_{\text{o1}} = 72.75$ A and $I_{\text{o2}} = 71.04$ A. The resulting current sharing error is

$$\begin{cases} \delta_{\text{o-half-load}} = \frac{38.45-37.37}{38.45+37.37} = 1.42\% \\ \delta_{\text{o-full-load}} = \frac{72.75-71.40}{72.75+71.40} = 0.94\%. \end{cases} \tag{42}$$

Fig. 12 shows the dynamic waveforms under PI control during load transients. As seen in Fig. 12(a) and (b), current sharing is maintained during switching, and the output voltage stabilizes at 3.2 V. However, the output current response time is about 4.8 ms, which is slower than that of the proposed method. The output voltage settles in 1.5 ms, and the *LLC* resonant current stabilizes within 4 ms. Notably, the Buck inductor current exhibits spikes during transitions, with a settling time of approximately 10 ms, indicating slower dynamic performance and reduced overall system stability.

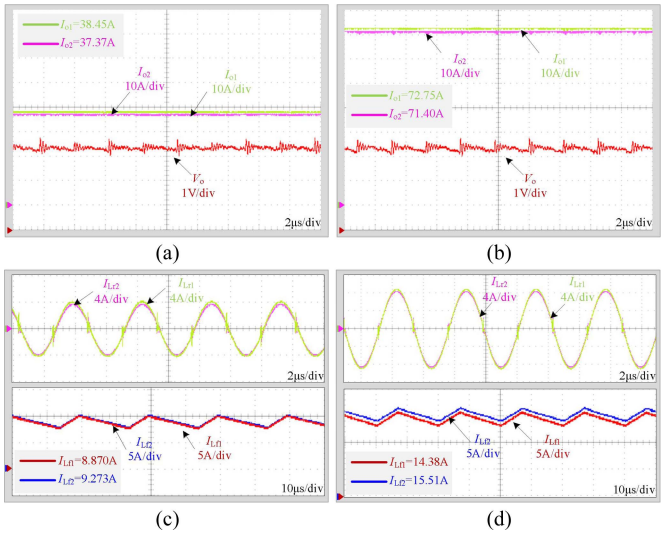

Fig. 11. Key waveforms of the two-phase parallel *LLC*-Buck converter under PI control at half-load and full-load conditions. (a) Output waveform at half load. (b) Output waveform at full load. (c) Current waveform at half load. (d) Current waveform at full load. (PI controller parameters: $K_{\mathrm{p}} = 0.8$, $K_{\mathrm{i}} = 10$; Load: half-load 250 W/full-load 500 W).

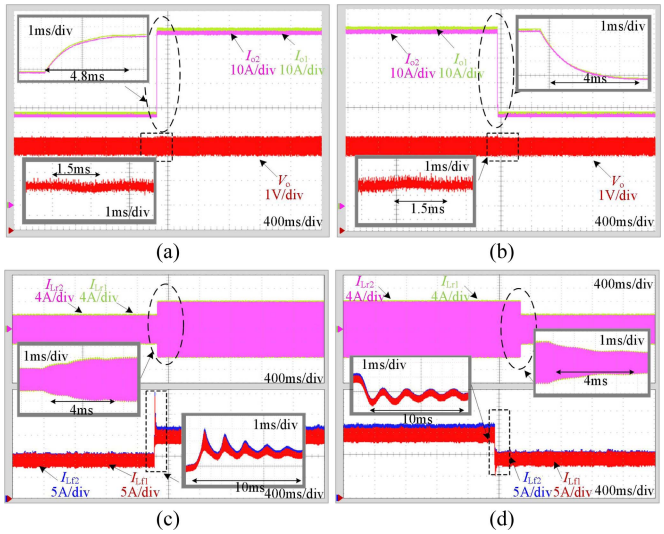

Fig. 12. Key waveforms during dynamic load changes under PI control. (a) Output waveform during half-load to full-load transition. (b) Output waveform during full-load to half-load transition. (c) Current waveform during half-load to full-load transition. (d) Current waveform during full-load to half-load transition. (Half load to full load: 250 W→500 W; Full load to half load: 500 W→250 W; Input voltage $V_{\mathrm{in}} = 48$ V).

To evaluate the robustness of the proposed method, the inductance and capacitance parameters used in the Buck unit prediction model are deliberately modified without altering the actual circuit parameters, with $L_{\mathrm{f}} = 10\ \mu$H and $C_{\mathrm{o2}} = 500\ \mu$F. The observer gain matrix remains $L_1 = 0.44$ and $L_2 = 0.02$. The key experimental waveforms are shown in Fig. 13. Under half-load conditions, the output currents of the two modules are $I_{\mathrm{o1}} = 36.81$ A and $I_{\mathrm{o2}} = 37.55$ A; under full-load conditions, the output currents are $I_{\mathrm{o1}} = 71.09$ A and $I_{\mathrm{o2}} = 70.74$ A. The

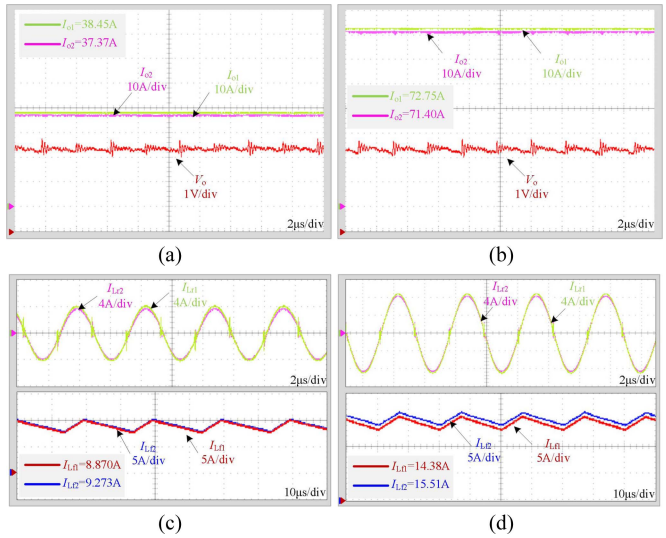

Fig. 13. Key waveforms of the two-phase parallel *LLC*-Buck converter under OBS+MPC control with 50% parameter deviation. (a) Output waveform at half load. (b) Output waveform at full load. (c) Current waveform at half load. (d) Current waveform at full load. (Prediction model parameter deviation: $L_{\mathrm{f}} = 10\ \mu$H (nominal value: 22 μH), $C_{\mathrm{o2}} = 500\ \mu$F (nominal value: 1000 μF); Load: Half load 250 W / Full load 500 W).

resulting current sharing error is

$$\begin{cases} \delta_{\mathrm{o-half-load}} = \dfrac{37.55-36.81}{37.55+36.81} = 1.00\% \\ \delta_{\mathrm{o-full-load}} = \dfrac{71.09-70.74}{71.09+70.74} = 0.25\%. \end{cases} \tag{43}$$

Under full-load conditions, the current sharing error is 0.25%, indicating accurate current sharing. The average Buck inductor currents are $I_{\mathrm{Lf1}} = 16.36$ A and $I_{\mathrm{Lf2}} = 16.87$ A. These results confirm that the controller remains effective even with up to 50% deviation in model parameters.

Fig. 14 shows the dynamic waveforms under model parameter deviations. As seen in Fig. 14(a) and (b), current sharing is maintained during load transients, and the output voltage stabilizes at 3.2 V. Due to the mismatch, the current response time increases to 4 ms, and the voltage settles in 3 ms. The *LLC* and Buck currents stabilize within 3 ms and 4 ms, respectively, with larger fluctuations and noticeable current spikes observed during load transitions. Despite the reduced stability caused by parameter variations, the controller still achieves effective and reliable current sharing under significant parameter deviations.

The oscillation phenomenon of the output voltage (V_0) and output current (i_{o}) in the figure stems from the inherent ripple coupling of the *LLC*-Buck cascaded topology.

Fig. 15(a)–(c) illustrates the output current and current sharing error of the two modules under three control strategies: OBS+MPC, OBS+MPC with 50% parameter deviation, and conventional PI control. Under OBS+MPC, the current sharing error remains within 3% across the full load range and decreases as the load increases. When the load reaches 40% of the rated value, the current sharing error is reduced to below 1%. In the OBS+MPC(50%) scenario, the current sharing error remains within 4%, demonstrating robustness to model parameter deviations. In contrast, the current sharing error under PI control

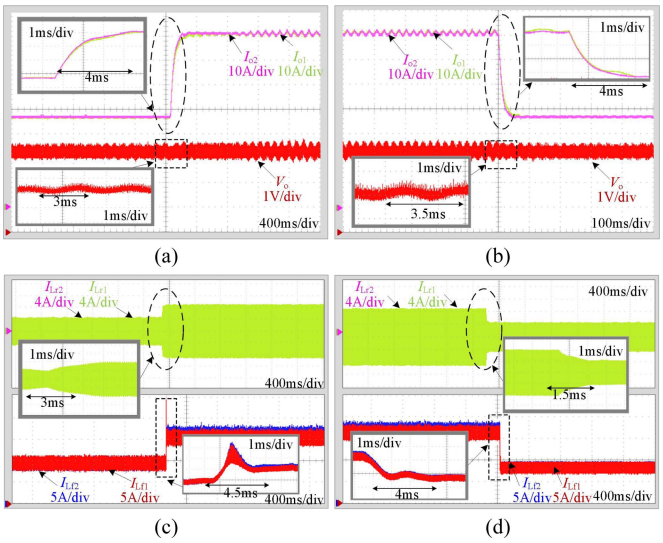

Fig. 14. Key waveforms during dynamic load changes under OBS+MPC control with 50% parameter deviation. (a) Output waveform during half-load to full-load transition. (b) Output waveform during full-load to half-load transition. (c) Current waveform during half-load to full-load transition. (d) Current waveform during full-load to half-load transition. (Observer gains: $L_1 = 0.44$, $L_2 = 0.02$; Load-switching conditions: 250 W→500 W/500 W→250 W).

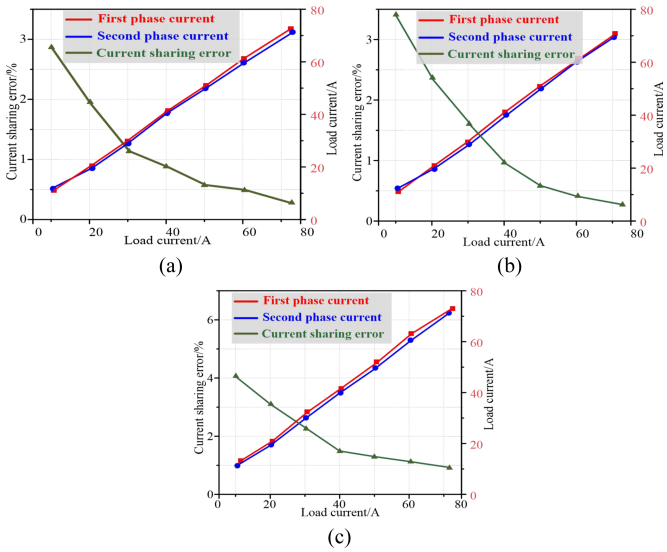

Fig. 15. Output currents of two modules and current sharing error under different control strategies. (a) OBS+MPC. (b) OBS+MPC with 50% parameter deviation. (c) PI control. (Load range: 50 W–500 W, Step size: 50 W; Input voltage $V_{in} = 48$ V, Ambient temperature 25 °C).

remains within 5% across the load range. Although the current sharing error decreases with increasing load in all cases, it is consistently higher under PI control compared to the OBS+MPC and OBS+MPC(50%) methods at the same power level.

The comparison of key experimental results for the three control strategies is summarized in Fig. 16. When the model parameters deviate by 50%, the proposed method still demonstrates excellent current sharing performance, with the current sharing error remaining comparable to that under nominal parameters. However, the response speed of the output voltage and current is moderately reduced, and a current overshoot is observed during

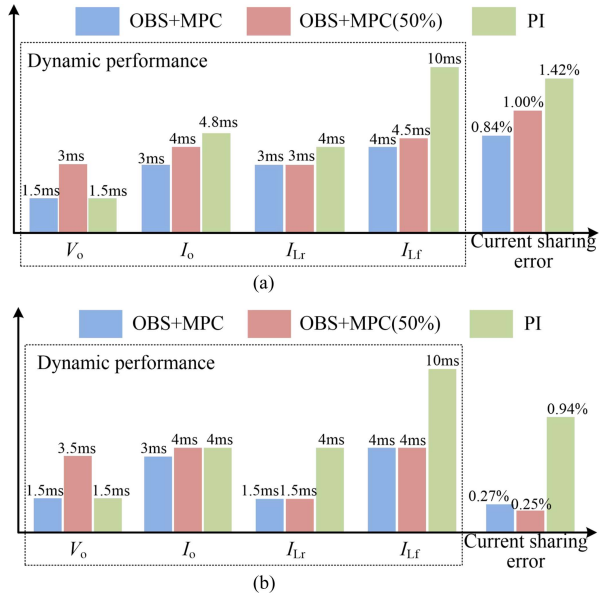

Fig. 16. Comparison of key experimental parameters during load transitions. (a) Half-load to full-load switching. (b) Full-load to half-load switching.

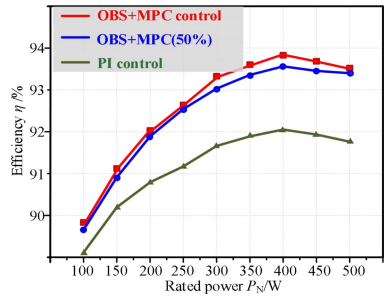

Fig. 17. Efficiency curves of the two-phase parallel sigma converter.

load transients. In contrast, under PI control, the current sharing error is significantly larger than that of the proposed method. Although the output voltage response speed is similar to that of the proposed method, the current response is considerably slower. Specifically, the inductor current of the Buck stage exhibits nearly double the response time, and current overshoot occurs during load transitions.

From Fig. 17, it can be seen that OBS+MPC (both without parameter deviation, peak efficiency 93.8%, and with 50% parameter deviation, peak efficiency 93.2%) has higher efficiency than traditional PI and a smoother efficiency curve, as reflected in the graph.

V. Conclusion

This article establishes a current-sharing error model for multimodule parallel *LLC*-Buck converters. The influence of circuit parameter mismatches between the *LLC* and Buck stages on the system's current-sharing accuracy is analyzed. To improve dynamic response speed, enhance system reliability, and reduce current sharing error, a model predictive current sharing control strategy is proposed. Based on the developed output current

mathematical model, a predictive model and voltage-current reference model are constructed, enabling coordinated voltage and current sharing control through a predefined cost function. To enhance the robustness of the system model, a Luenberger observer is introduced to correct parameter deviations. Two 500 W (250 W×2) *LLC*-Buck converter prototypes were designed, and the feasibility of the proposed current sharing strategy was experimentally validated. Furthermore, comparative results demonstrate that the proposed method outperforms traditional average current control in terms of dynamic performance, robustness, and current sharing accuracy.

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