400/50 V Vertically Mounted *LLC* Module With Enhanced Hold-Up Capability for Datacenters

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***Abstract*—The growing power demands of artificial intelligence- and machine learning-based datacenters drive the need for higher power density in ac–dc power supply units without increasing their physical footprint. In isolated dc–dc stages, *LLC* resonant converters are favored for their high efficiency; however, achieving the large gain required during hold-up events via frequency modulation necessitates modifications to the resonant tank parameters that compromise nominal efficiency, resulting in oversized bulk capacitance. Secondary-side rectifier (SR) phase-shifting control can eliminate the dependence on magnetizing inductance, but extended freewheeling intervals require an increase in switching frequency to limit peak and rms currents, which in turn broadens the frequency range and increases switching losses. This work introduces a selective SR phase-shifting control leveraging matrix transformers to mitigate these challenges. The approach is experimentally validated on a vertically mounted $400/50$ V *LLC* converter module, achieving 98.7% peak efficiency and a surface power density of $1320\ \mathrm{W/in^2}$, while maintaining regulation over a 200–400 V input range. The proposed method enables a 33% reduction in bulk capacitance compared to frequency control, improving both volumetric power density and efficiency in high-performance power supply designs.**

***Index Terms*—DC–DC converter, datacenters, high gain range, *LLC* converter, phase-shift control, synchronous rectifiers.**

I. Introduction

POWER supplies for datacenters are among the most performance-driven, energy-intensive, and cost-sensitive within industrial applications. The growing demand for online services, such as e-commerce, cloud computing, banking, and social media, continues to drive up datacenter energy consumption [1]. In 2018, global datacenters consumed an estimated 205 TWh—around 1% of the world's electricity [2]. While energy usage has nearly doubled over the past decade, overall datacenter efficiency has improved significantly. Given this upward trend in digital infrastructure and global efforts to reduce carbon emissions, enhancing power conversion efficiency at every stage of the power delivery chain has become increasingly critical.

A key contributor to these efficiency gains is the shift in datacenter power architecture. Incoming ac power is typically rectified to a regulated dc bus through a nonisolated boost power factor correction stage, followed by an isolated dc–dc converter. Historically, a 12-V bus powered the servers, resulting in high conduction losses due to large currents. To address this, industry leaders, including Google, Facebook, Cisco, and IBM, have transitioned to a 48–52 V bus architecture, nominally regulated at 50 V. The higher bus voltage reduces i^2R losses and enables direct battery integration onto the bus, minimizing intermediate conversion stages and simplifying power distribution, as shown in Fig. 1. The use of a narrow-range bus also relaxes the gain requirements of downstream converters by allowing battery connection through a regulated dc–dc interface.

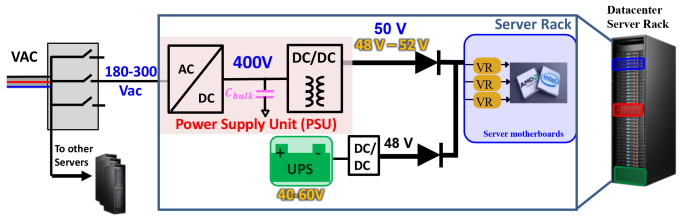

Fig. 1. 50 V bus architecture for datacenters proposed by OCP.

To support this evolving architecture, the open compute project (OCP) introduced the Open Rack V3 specification in 2020, standardizing a 3-kW server power supply unit (PSU) with a peak efficiency of 97.5% in a compact 1 U form factor [3]. Since then, the power rating has nearly doubled to 5.5 kW within a slightly larger footprint [4], with next-generation PSUs projected to scale up to 9–10 kW to meet the surging power demands of high-performance graphical processing units (GPUs). These trends have placed new demands on isolated dc–dc converters—not only in terms of efficiency and power density, but also in thermal management, hold-up capability, and form factor constraints.

The outlined converter requirements present a distinct challenge: achieving galvanic isolation while supporting a high voltage step-down ratio, substantial output current, and compact design—all while maintaining high efficiency. *LLC* resonant converters are particularly well-suited to meet these demands. They offer zero-voltage switching (ZVS) over a wide load range, reduce turn-OFF losses in primary-side switches compared to soft-switching pulsewidth modulation (PWM) converters, and enable zero-current switching (ZCS) for the secondary-side rectifiers (SRs) [5], [6]. These features help minimize switching and conduction losses while improving thermal performance. Furthermore, advancements in Gallium–Nitride (GaN) power

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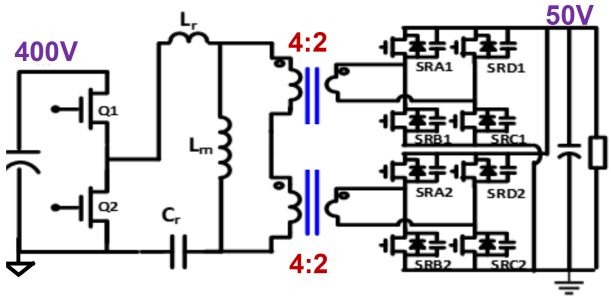


Fig. 2. 3 kW 400/50 V *LLC* converter with matrix transformer.

devices and planar magnetics have enabled higher switching frequencies and improved integration, helping to push the boundaries of converter efficiency and power density. These technological enablers are essential for meeting the stringent requirements of modern datacenter PSUs, particularly as power levels approach 10 kW and vertical space within server racks remains limited.

For high-power converters with large voltage step-down ratios, the resulting secondary-side current is often too high for a single transformer to handle efficiently without excessive conduction losses. In addition, paralleling multiple SRs introduces current-sharing challenges due to layout and termination mismatches. To mitigate these issues, the transformer can be "exploded" into multiple smaller transformers, each carrying a portion of the total power. This approach enables better thermal distribution and reduced winding losses. In such matrix transformers, the elemental transformers are typically configured with their primary windings in series—ensuring equal voltage stress—and their secondary windings paralleled at the output to share current. For example, in the proposed 3 kW 400/50 V *LLC* converter, two transformers with a 4:2 turns ratio are connected in this manner, as illustrated in Fig. 2 [7].

Another critical requirement for the front-end dc-dc stage is to maintain the rated output voltage for a short duration—typically tens of milliseconds—when the ac input supply is interrupted [4]. This is known as the *hold-up time* requirement and ensures continuous operation while the uninterruptible power supply or battery backup takes over, as shown in Fig. 3(a). During this period, energy is drawn from the input-side bulk capacitance, whose voltage decays based on the stored energy and load power. The relationship between the hold-up time and the required bulk capacitance is given by

$$P_{\text{in}} t_{\text{hold}} = \frac{1}{2} C_{\text{bulk}} \left(V_{\text{in,nom}}^2 - V_{\text{in,min}}^2 \right) \tag{1}$$

where P_{in} is the input power, t_{hold} is the required hold-up time, C_{bulk} is the bulk capacitance, $V_{\text{in,nom}}$ is the nominal input voltage, and $V_{\text{in,min}}$ is the minimum voltage to which the capacitor discharges during the hold-up period.

To maintain a constant output voltage V_o as the input voltage drops, the *LLC* converter must increase its voltage gain to a maximum value M_{max}. Assuming a nominal gain of 1 during steady-state operation ($V_{\text{in,nom}} = 2nV_o$, where n is the transformer turns ratio), and that the minimum input voltage is given

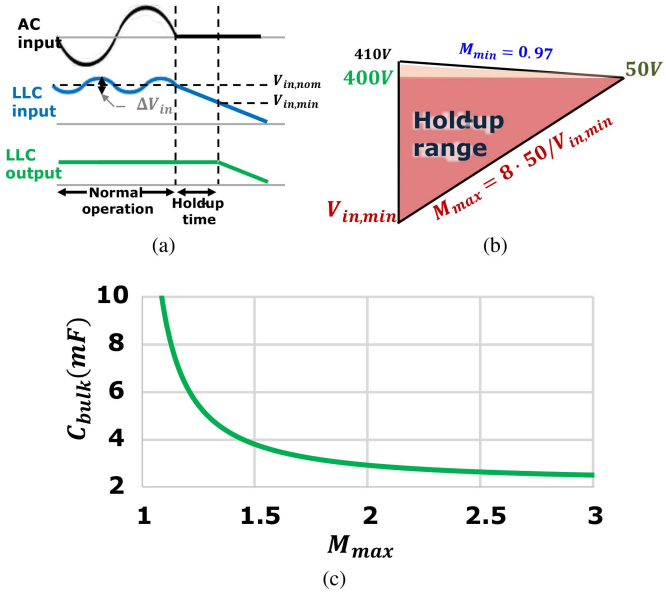


Fig. 3. (a) Hold-up time operation. (b) *LLC* gain requirement. (c) C_{bulk} versus M_{max} for $P_{\text{in}} = 9$ kW, $V_{\text{in,nom}} = 400$ V, and $t_{\text{hold}} = 20$ ms.

by $V_{\text{in,min}} = 2nV_o/M_{\text{max}}$, (1) simplifies to

$$C_{\text{bulk}} = \frac{2P_{\text{in}} t_{\text{hold}}}{V_{\text{in,nom}}^2} \cdot \left(\frac{M_{\text{max}}^2}{M_{\text{max}}^2 - 1} \right). \tag{2}$$

Fig. 3(c) illustrates this relationship for a 9-kW converter with $V_{\text{in,nom}} = 400$ V and $t_{\text{hold}} = 20$ ms. A smaller C_{bulk} stores less energy, causing a faster voltage drop and requiring a higher M_{max} to maintain output regulation. This creates a tradeoff between bulk capacitance and the gain range of the *LLC* converter. Since the bulk capacitor bank typically occupies 20%–30% of the PSU volume, minimizing C_{bulk} by increasing the achievable gain range—without sacrificing nominal efficiency—is critical for improving overall system power density.

Conventionally, the gain of a resonant converter is modulated by varying the switching frequency (f_s) relative to the tank's resonant frequency (f_0), as shown in Fig. 4. In the case of *LLC* converters, a gain of unity is achieved when $f_s = f_0$, gains greater than unity occur when $f_s < f_0$, and gains less than unity occur when $f_s > f_0$. When operating in the high-gain region ($f_s < f_0$), two primary modes of operation occur, as illustrated in Fig. 4(c) and (d). In Mode I, the load remains connected to the resonant tank, allowing energy transfer. Once the magnetizing current i_{Lm} equals the resonant current i_{Lr}, the secondary rectifiers turn OFF, initiating Mode II. In this mode, the transformer is disconnected from the tank, and the magnetizing inductance L_m resonates with L_r and C_r. Due to the larger effective inductance, the tank impedance increases, reducing the rate of energy buildup in the tank.

Achieving higher gains requires increasing the tank energy, which can be done by (1) extending Mode II duration, (2) reducing the resonant capacitor C_r, or (3) reducing the magnetizing inductance L_m. However, each approach has drawbacks. Extending Mode II increases frequency range and results in

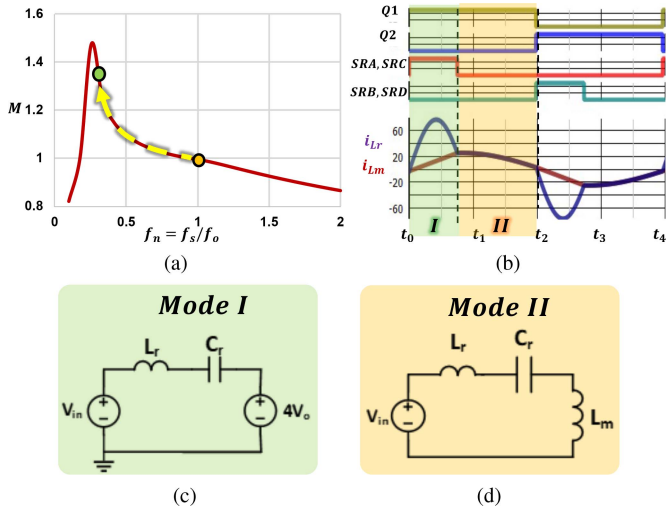


Fig. 4. Frequency modulation. (a) Gain curve and path to boost gain. (b) Key waveforms. (c) Mode 1. (d) Mode 2.

higher rms currents, with limits set by $i_{Lr} = 0$. Reducing C_r increases V_{Cr} more rapidly but, for a fixed f_0, also increases L_r, leading to larger inductor size and higher core losses. Lowering L_m can increase energy transfer rates but causes larger circulating currents during nominal operation. As a result, relying solely on frequency modulation to achieve high gain necessitates tradeoffs, including (a) use of a large L_r, (b) wide frequency excursions, and (c) reduced efficiency at the nominal operating point.

To address the limitations of frequency modulation for gain control, two alternative strategies have been explored in literature: resonant tank modification and PWM control. Resonant tank modification involves dynamically adjusting elements of the *LLC* tank—such as the magnetizing inductance L_m, resonant inductance L_r, and resonant capacitor C_r—during hold-up events. For example, L_m is typically maximized under nominal conditions to minimize circulating current, but an auxiliary circuit can be activated during hold-up to reduce L_m and boost gain [8]. Another method introduces an additional capacitor C_p in series with L_m, effectively lowering the inductive impedance seen by the tank and increasing gain over a narrower frequency span [9]. While these techniques aim to optimize nominal performance, they often require added hardware that is only active during rare hold-up events—leading to underutilized components and potential efficiency penalties during normal operation.

PWM-based control presents another approach to gain extension by modulating the effective transformer voltage seen by the resonant tank (V_{tr}). This is often implemented through control of the SRs. For instance, a matrix transformer configuration using two transformers and full-bridge (FB) rectifiers can operate each bridge in FB, half-bridge (HB), or disabled ("0") modes, depending on how many switches are active [10]. This results in discrete voltage steps at V_{tr}, enabling multiple gain levels. However, smooth transitions between these levels still require accompanying frequency modulation, limiting the standalone effectiveness of this method.

To achieve high gain without relying on inefficient passive components, prior works have explored phase-shifting control of the SRs [11], [12], [13]. In this approach, the SRs of one HB are phase-shifted relative to the primary switches, while the SRs of the other HB remain in-phase. This creates an interval, where V_{tr} is zero, allowing additional energy build-up in the resonant tank and thus a gain boost. Furthermore, as will be detailed in Section II, the Mode II operation can be rendered redundant. Eliminating this mode, as shown in [14], reduces both rms and peak currents. However, such approaches typically require a wide frequency range, leading to increased switching losses and a loss of ZVS under some conditions.

To overcome these limitations, this article proposes a selective SR phase-shift control method that reduces the required frequency range by leveraging the added controllability with matrix transformers. Specifically, phase-shifting is selectively applied to only one of the two transformers, enabling smooth gain control with improved efficiency and reduced component stress.

The rest of this article is organized as follows. Section II discusses the SR phase-shifting control method and its limitations. Section III introduces the proposed selective phase-shifting technique to mitigate those challenges. Section IV details the implementation of the proposed control method on a vertically mounted 3 kW, 400/50 V *LLC* converter with an input voltage range of 200–400 V during hold-up time. In Section V, hardware results are presented. Finally, Section VI concludes this article.

II. Conventional SR Phase-Shift Control

Fig. 5 describes the conventional SR phase-shift control for the *LLC* converter operating at its series resonant frequency f_0. The switching instants of the SRs of one HB (SRC1, SRD1, SRC2, and SRD2) are phase-delayed by α with respect to the primary switches (Q1 and Q2), while the SRs of the other bridge operate in-phase with the primary switches. Here, α can be defined as

$$\alpha = \frac{\text{phase-shifted period } (t_0 - t_1)}{\text{half-switching period } (t_0 - t_3)} \times 180^\circ. \tag{3}$$

In addition, SRA1, SRB1, SRA2, and SRB2 are turned OFF when i_{Lr} equals i_{Lm}, or when the secondary current reaches zero, to prevent reverse conduction.

During t_0–t_1, Q1, SRA1/2, and SRD1/2 are ON, which results in the transformer's secondary winding being shorted, i.e., $V_{\text{tr}} = 0$. This effectively bypasses L_m as well, thereby resulting in a new Mode III operation, as illustrated in Fig. 5(b). In contrast to Mode II, L_m is bypassed in Mode III, reducing the tank impedance to consist of only L_r and C_r, thereby charging the tank at a much faster rate. Moreover, the constraints on L_m are eliminated, since it is no longer part of the resonant tank during the gain increase phase. Since $V_{\text{tr}} = 0$, the resonant tank voltage becomes $V_{\text{tank}} = V_{\text{in}} - 0 = V_{\text{in}}$, resulting in a boost in the resonant tank energy.

During t_1–t_2, Q1, SRA1/2, and SRC1/2 are ON, which results in normal operation (Mode I), with the resonant tank voltage given by $V_{\text{tank}} = V_{\text{in}} - nV_o$. During t_2–t_3, only SRC1/2 is ON on the secondary side, resulting in the load disconnecting from

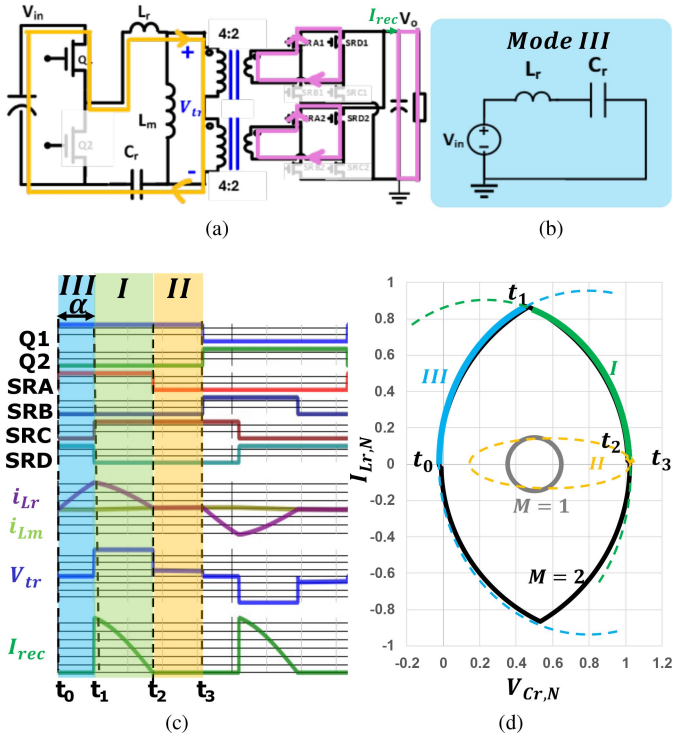


Fig. 5. SR phase-shift control at $f_s = f_0$. (a) Schematic. (b) Circuit for Mode III. (c) Key waveforms. (d) State trajectory.

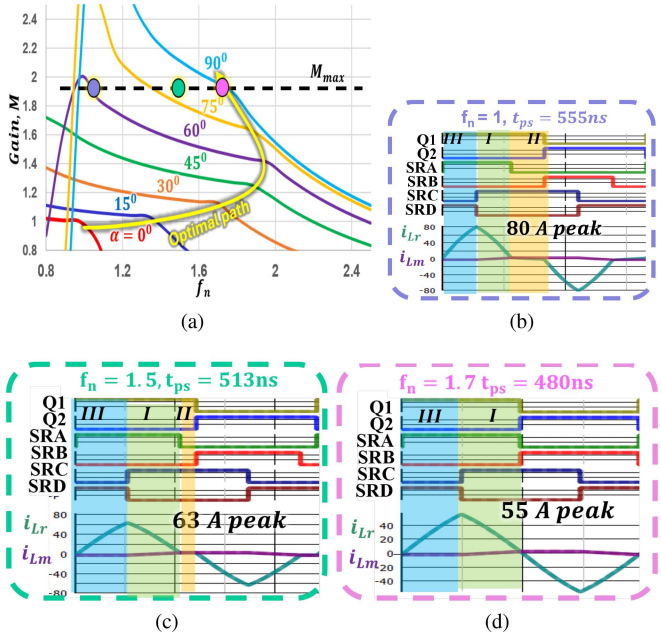


Fig. 6. (a) Gain curves with different α, and waveforms at $M = 2$ when operating at (b) $f_n = 1$, (c) $f_n = 1.5$, and (d) $f_n = 1.7$.

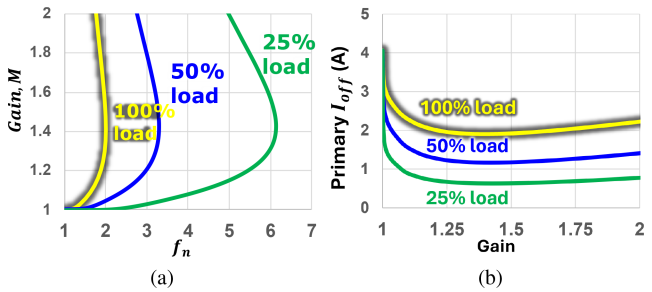


Fig. 7. (a) Increasing frequency range and (b) reducing turn-OFF current with reducing loads while optimally SR phase-shifting.

the transformer, and freewheeling of the resonant current on the primary side (Mode II). This period lasts until Q2 is turned ON at t_4 for the second half-cycle, after which the operation repeats. A similar mode of operation can be observed when $f_s < f_0$ and $f_s > f_0$, highlighting the versatility of this control technique.

The boosted resonant tank energy can also be observed from the state trajectory diagram in Fig. 5(d), where the grey curve represents the state trajectory under nominal conditions ($M = 1$) with no phase shift, and the black curve corresponds to the boosted resonant tank energy for a gain $M = 2$ with applied phase shift. It may be noted that although Mode II occupies a significant portion of the half-switching period in Fig. 5(c), it has a negligible impact on the tank energy transfer, as seen in Fig. 5(d). This results in high primary-side circulating current without a corresponding increase in energy delivered to the load or stored in the tank, thereby reducing efficiency and increasing conduction losses.

To optimize the operation during SR phase-shifting, Zhao et al. [14] proposed a control method described in Fig. 6. Fig. 6(a) shows the gain curves with increasing phase-shift angles α, and Fig. 6(b) shows the key waveforms when switched at $f_n = 1$ as typically operated. However, redundant Mode II increases the primary rms and peak currents ($I_{Lr,\text{pk}} = 80$ A), thereby causing high device and inductor stress. To reduce the duration of Mode II, the frequency of operation is increased, as shown in Fig. 6(c). The increase in switching cycles reduces the phase-shifted period required per cycle, thereby reducing the peak current to 63 A. Furthermore, the duration of Mode II also reduces, thereby reducing the rms current. The frequency can be further increased until Mode II is eliminated, thereby optimizing the operation with a minimum peak current of 55 A, as shown in Fig. 6(d). This process can be repeated across the required gain range to result in the optimal path, as shown in Fig. 6(a). The detailed method to calculate this optimal path is described in Section III.

However, this approach introduces certain limitations. First, under light-load conditions, the load can be charged and discharged within a shorter period, necessitating a wider frequency range, as illustrated in Fig. 7(a). This reduces the peak magnetizing current and, consequently, the primary turn-OFF current, which may lead to a loss of ZVS, as shown in Fig. 7(b).

Second, the phase-shifted SRs are turned OFF under high current, as illustrated in Fig. 8(a). As the phase-shift angle increases, the SR turn-OFF current rises proportionally with the converter gain, reaching nearly 120 A at a gain of 2, as shown in Fig. 8(b). The total SR turn-OFF loss for a hard-switched device,

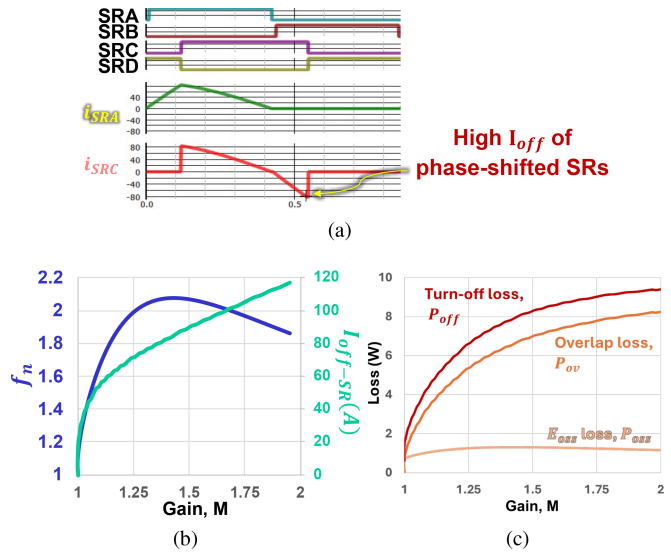


Fig. 8. (a) Waveforms showing high turn-OFF currents for phase-shifted SRs. (b) Frequency and turn-OFF current as a function of gain. (c) Turn-OFF loss with increasing gain.

$P_{\mathrm{SR,off}}$, can be expressed as

$$\begin{aligned} P_{\mathrm{SR,off}} &= P_{\mathrm{SR,ov}} + P_{\mathrm{SR,oss}} \\ P_{\mathrm{SR,ov}} &= \tfrac{1}{2} V_{\mathrm{DS}} I_{\mathrm{off,SR}} t_{\mathrm{ov}} f_s = k_1 I_{\mathrm{off,SR}} f_n \\ P_{\mathrm{SR,oss}} &= \gamma E_{\mathrm{SR,oss}} f_s = k_2 f_n \end{aligned} \tag{4}$$

where $P_{\mathrm{SR,ov}}$ denotes the current–voltage overlap loss, and $P_{\mathrm{SR,oss}}$ represents the capacitive (output-capacitance) switching loss. Here, V_{DS} is the drain–source voltage, $I_{\mathrm{off,SR}}$ is the SR turn-OFF current, t_{ov} is the overlap duration, γ is the unrecovered-energy coefficient, and $E_{\mathrm{SR,oss}}$ is the energy associated with the SR output capacitance. To estimate these losses, several reasonable assumptions are adopted: $V_{\mathrm{DS}} = 50$ V, $t_{\mathrm{ov}} = 5$ ns, $f_o = 300$ kHz, $\gamma = 1$, and $E_{\mathrm{SR,oss}} = 2.1$ μJ (from the device datasheet). These constants can be consolidated into $k_1 = 0.0375$ V and $k_2 = 0.63$ W. Based on these parameters, the SR turn-OFF loss variation with gain is computed and plotted in Fig. 8(c). Although low-voltage GaN devices exhibit much lower intrinsic switching energy than their silicon or high-voltage counterparts, the large SR turn-OFF current substantially increases the overlap-loss component, eventually dominating over the capacitive loss. This steep rise in switching losses can lead to excessive device stress or failure and therefore must be mitigated.

III. Proposed Selective SR Phase-Shift Control

To address the issues outlined in Section II, the primary objective is to reduce the required frequency range. To this end, a selective SR phase-shifting control method is proposed, originally introduced for center-tapped rectifiers in [15]. This method leverages the inherent flexibility of matrix transformers, in which the SRs—and therefore the voltage of each elemental transformer—can be independently controlled.

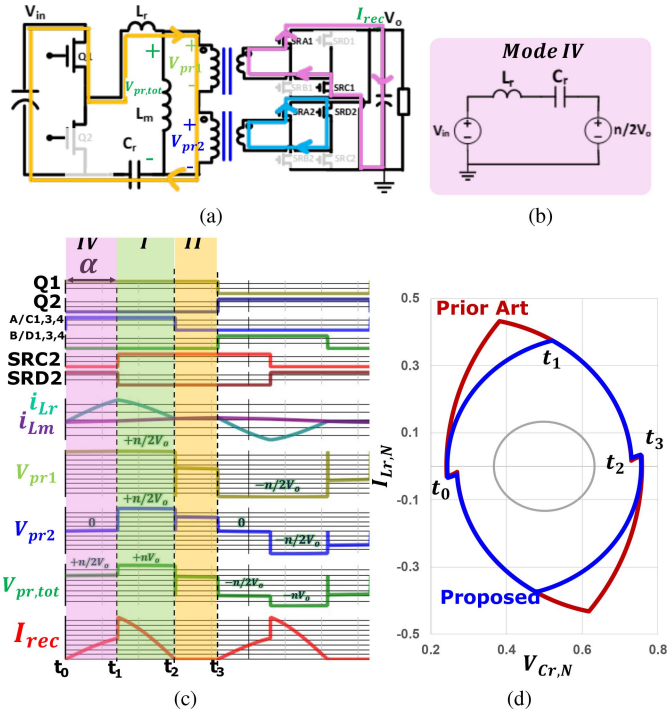


Fig. 9. Selective SR phase-shift control at $f_s = f_0$. (a) Schematic. (b) Circuit for Mode IV. (c) Key waveforms. (d) State trajectory.

Fig. 9 illustrates the proposed selective SR phase-shift control using a matrix configuration of two elemental transformers. All SRs of Transformer 1 are operated in-phase with the corresponding primary devices (Q1 and Q2) and are turned OFF when $i_{\mathrm{Lm}} = i_{\mathrm{Lr}}$ to prevent reverse conduction. For Transformer 2, the SRs of one HB (SRA2 and SRB2) are also operated in-phase with Q1 and Q2, respectively, while the SRs of the other HB (SRC2 and SRD2) are phase-shifted relative to Q1 and Q2. Effectively, the conventional SR phase-shifting operation is applied selectively to only one elemental transformer, while the other operates in the standard in-phase configuration.

The current paths and operating sequence of the proposed control method are illustrated in Fig. 9(a). From t_0–t_1, Q1, SRA1, SRC1, SRA2, and SRD2 are ON. During this period, the voltage across transformer 1 $V_{\mathrm{pr1}} = +nV_o/2$ and that across transformer 2 is $V_{\mathrm{pr2}} = 0$, resulting in a new Mode IV of operation. The effective total transformer voltage is therefore $V_{\mathrm{pr,tot}} = +nV_o/2$. From t_1–t_2, Q1, SRA1, SRC1, SRA2, and SRC2 are ON, corresponding to normal forward conduction through both elemental transformers (Mode I operation). At t_2, when $i_{\mathrm{Lm}} = i_{\mathrm{Lr}}$, SRA1, SRC1, and SRA2 are turned OFF, initiating the freewheeling period (Mode II) from t_2–t_3. After t_3, Q2 turns ONand the second half-cycle begins in a symmetrical fashion.

Mode IV operation offers several advantages over Mode III. First, $V_{\mathrm{pr,tot}} = +nV_o/2$ in Mode IV compared to $V_{\mathrm{pr,tot}} = 0$ in Mode III. This results in a lower voltage across the resonant tank, $V_{\mathrm{tank}} = V_{\mathrm{in}} - V_{\mathrm{pr,tot}}$, which charges the inductor more gradually. This effect can also be seen from the reduced peak $I_{\mathrm{Lr,N}}$ in the state trajectories of Fig. 9(d), where the smaller V_{tank}

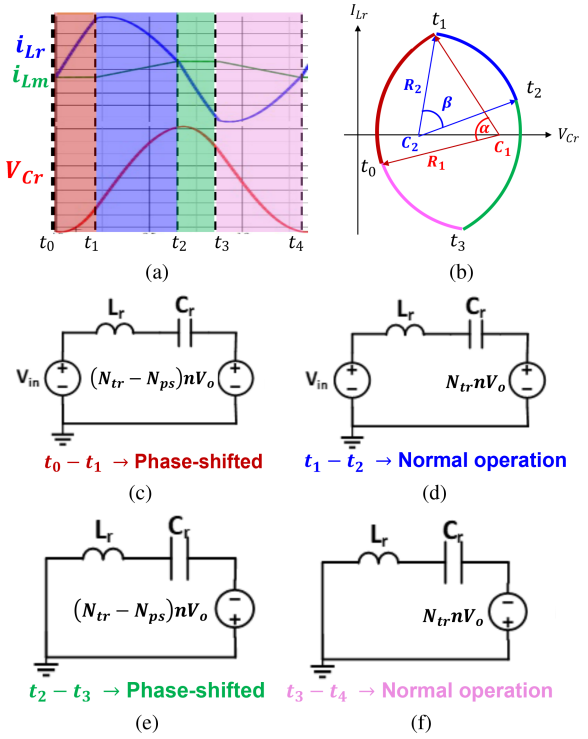


Fig. 10. (a) Key waveforms at the optimal operating condition, (b) corresponding state trajectory, and equivalent circuits during (c) t_0–t_1, (d) t_1–t_2, (e) t_2–t_3, and (f) t_3–t_4.

reduces the radius of the trajectory from t_0–t_1, thereby lowering the peak current.

It should be noted that Mode II persists when operating at $f_s = f_o$, and therefore, a frequency optimization procedure similar to that described in [14] and Section II can be applied. To enable a performance comparison between the proposed method and existing approaches, a generalized mathematical model is formulated to evaluate the resonant tank behavior under various operating conditions. The optimal operating trajectory, along with the corresponding voltages and currents at different gain levels, can be obtained for a general matrix transformer by recognizing that the resonant tank waveforms comprise four distinct periods within each switching cycle, as illustrated in Fig. 10(a). These time intervals can be expressed as functions of the normalized optimal switching frequency $f_{n,\text{opt}}$, the phase-shift angle α, and the normal operation angle β as

$$t_0 - t_2 = \frac{T_s}{2} = \frac{1}{2f_o f_{n,\text{opt}}}, \quad t_0 - t_1 = \frac{\alpha T_s}{2\pi}$$
$$t_1 - t_2 = \frac{\beta T_s}{2\pi}, \quad f_{n,\text{opt}} = \frac{\pi}{\alpha+\beta}. \tag{5}$$

For a matrix transformer consisting of N_{tr} elemental units, each with a turns ratio of $n:1$, phase-shifting is applied to the SRs of N_{ps} transformers. The resulting state trajectories are derived from the equivalent resonant tank voltages during the four distinct time intervals, as illustrated in Fig. 10(c)–(f). From these trajectories, the resonant inductor current i_{Lr}, resonant capacitor voltage v_{Cr}, and magnetizing current i_{Lm} can be formulated as

Mode IV—$t_0 - t_1$:

$$\begin{aligned} i_{\text{Lr1}}(t) &= (V_{\text{in}} - (N_{\text{tr}} - N_{\text{ps}})nV_o - V_{\text{Cr0}})/Z_o \sin(\omega_0 t) \\ &\quad + i_{\text{Lr0}} \cos(\omega_0 t) \\ v_{\text{Cr1}}(t) &= V_{\text{Cr0}} - [V_{\text{in}} - (N_{\text{tr}} - N_{\text{ps}})nV_o] \cos(\omega_0 t) \\ &\quad + Z_o i_{\text{Lr0}} \sin(\omega_0 t) \\ i_{\text{Lm1}}(t) &= ((N_{\text{tr}} - N_{\text{ps}})nV_o/L_m)\, t + i_{\text{Lm0}}. \end{aligned} \tag{6}$$

Mode I—$t_1 - t_2$:

$$\begin{aligned} i_{\text{Lr2}}(t) &= (V_{\text{in}} - N_{\text{tr}}nV_o - V_{\text{Cr1}})/Z_o \sin[\omega_0(t - t_1)] \\ &\quad + i_{\text{Lr1}} \cos[\omega_0(t - t_1)] \\ v_{\text{Cr2}}(t) &= (V_{\text{Cr1}} - N_{\text{tr}}nV_o) \cos[\omega_0(t - t_1)] \\ &\quad + Z_o i_{\text{Lr1}} \sin[\omega_0(t - t_1)] \\ i_{\text{Lm2}}(t) &= (N_{\text{tr}}nV_o/L_m)(t - t_1) + i_{\text{Lm1}}. \end{aligned} \tag{7}$$

Mode IV′—$t_2 - t_3$:

$$\begin{aligned} i_{\text{Lr3}}(t) &= ((N_{\text{tr}} - N_{\text{ps}})nV_o - V_{\text{Cr2}})/Z_o \sin[\omega_0(t - t_2)] \\ &\quad + i_{\text{Lr2}} \cos[\omega_0(t - t_2)] \\ v_{\text{Cr3}}(t) &= V_{\text{Cr2}} - (N_{\text{tr}} - N_{\text{ps}})nV_o \cos[\omega_0(t - t_2)] \\ &\quad + Z_o i_{\text{Lr2}} \sin[\omega_0(t - t_2)] \\ i_{\text{Lm3}}(t) &= (-(N_{\text{tr}} - N_{\text{ps}})nV_o/L_m)(t - t_2) + i_{\text{Lm2}}. \end{aligned} \tag{8}$$

Mode I′—$t_3 - t_4$:

$$\begin{aligned} i_{\text{Lr4}}(t) &= (N_{\text{tr}}nV_o - V_{\text{Cr3}})/Z_o \sin[\omega_0(t - t_3)] \\ &\quad + i_{\text{Lr3}} \cos[\omega_0(t - t_3)] \\ v_{\text{Cr4}}(t) &= (V_{\text{Cr3}} + N_{\text{tr}}nV_o) \cos[\omega_0(t - t_3)] \\ &\quad + Z_o i_{\text{Lr3}} \sin[\omega_0(t - t_3)] \\ i_{\text{Lm4}}(t) &= (-N_{\text{tr}}nV_o/L_m)(t - t_3) + i_{\text{Lm3}}. \end{aligned} \tag{9}$$

Analyzing (6)–(9), it can be observed that the state trajectories form arcs of circles with varying radii and centers, as depicted in Fig. 10(b). Applying the boundary conditions for i_{Lr}, v_{Cr}, and i_{Lm} at t_0, t_1, t_2, and t_3 yields the following six equations:

$$\begin{aligned} i_{\text{Lr1}}(t = t_0) &= i_{\text{Lm1}}(t = t_0) \\ i_{\text{Lm1}}(t = t_1) &= i_{\text{Lm4}}(t = t_4) \\ i_{\text{Lr1}}(t = t_1) &= i_{\text{Lr2}}(t = t_1) \\ i_{\text{Lr2}}(t = t_2) &= -i_{\text{Lr1}}(t = t_0) \\ v_{\text{Cr2}}(t = t_2) &= V_{in} - v_{\text{Cr1}}(t = t_0) \\ v_{\text{Cr1}}(t = t_1) &= v_{\text{Cr2}}(t = t_1). \end{aligned} \tag{10}$$

The average output current can be expressed as

$$\frac{V_o}{R_L} = \frac{2}{T_s}\left[(N_{\text{tr}} - N_{\text{ps}})n \int_{t_0}^{t_1} (i_{\text{Lr1}}(t) - i_{\text{Lm1}}(t))\, dt + N_{\text{tr}}n \int_{t_1}^{t_2} (i_{\text{Lr2}}(t) - i_{\text{Lm2}}(t))\, dt\right]. \tag{11}$$

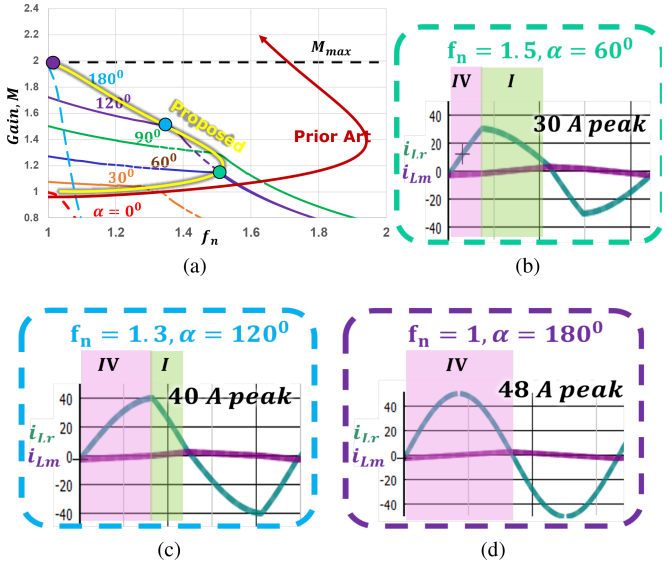


Fig. 11. (a) Gain curves with different α under selective SR phase-shifting, and waveforms at different gain levels during optimal operation. (b) $M = 1.3$. (c) $M = 1.5$. (d) $M = 2$.

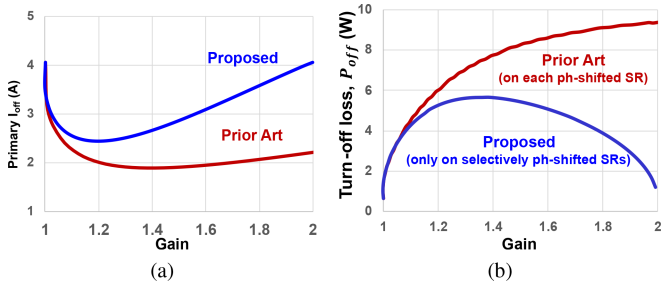


Fig. 12. (a) Higher primary turn-OFF current and (b) lower SR turn-OFF loss with the proposed control compared to the prior-art control.

Owing to the nonlinear nature of (6)–(11), a closed-form analytical solution is not attainable. Instead, the seven governing equations from (10) and (11) are solved numerically using mathematical software to determine the instantaneous currents and voltages. For specified values of V_o, α, and R_L, the corresponding $f_{n,\text{opt}}$ and V_{in} can be computed, yielding the optimal trajectory (yellow curve), as shown in Fig. 11(a). The optimal path for the conventional SR phase-shift control (red curve) is obtained by setting $N_{\text{ps}} = N_{\text{tr}}$. As α increases, the switching frequency is raised to suppress Mode II. When α exceeds 90°, the sinusoidal behavior of Mode IV predominates, and f_n gradually returns to unity at $\alpha = 180^\circ$, as shown in Fig. 11(d). Because Transformer 1 remains connected to the load throughout the entire cycle, $V_{\text{pr,tot}} = nV_o/2$ is maintained, enabling a peak achievable gain of 2. In general, fully phase-shifting the SRs in N_{ps} transformers to $\alpha = 180^0$ yields a peak gain given by

$$M_{\text{pk}} = \frac{2N_{\text{tr}}\, nV_o}{V_{\text{in}}\,(N_{\text{tr}} - N_{\text{ps}})}. \tag{12}$$

It can be observed from Fig. 11(a) that the proposed method reduces the frequency range by approximately 50% compared to the conventional approach. In the proposed scheme, the load is supplied not only during Mode I but also partially during the phase-shifted period (Mode IV), thereby reducing the number of switching cycles required to deliver the necessary energy to the load. In contrast, the prior-art method charges only the resonant tank during its phase-shifted period (Mode III), relying solely on Mode I to transfer energy to the load, and thus requiring a greater number of switching cycles. This advantage extends to lighter load conditions, where the frequency range can also be narrowed using the proposed method.

The reduced frequency range offers additional benefits. First, it maintains higher primary turn-OFF currents, thereby mitigating the risk of ZVS loss, as illustrated in Fig. 12(a). Second, the combination of the narrower frequency range and the return to sinusoidal operation at higher gains leads to a reduction in SR turn-OFF losses compared to the conventional method, as shown in Fig. 12(b). Furthermore, only two SR devices are phase-shifted in the proposed scheme, halving the number of devices subjected to turn-OFF loss compared to the four phase-shifted SRs in the prior-art method.

IV. Implementation on a 400/50 V *LLC* Module

The proposed selective SR phase-shifting method is implemented in a 3 kW, 300 kHz, 400/50 V *LLC* converter module employing a matrix of two elemental transformers, wherein the SRs of one bridge in a single elemental transformer are selectively phase-shifted to achieve a peak gain of $M_{\text{pk}} = 2$, and hence an input voltage range of 200–400 V, as discussed in Section III. The topology of the proposed converter is illustrated in Fig. 2, where a turns ratio of 8:2 is selected to optimize the tradeoff between transformer core loss and winding loss [7]. Consequently, each elemental transformer has a turns ratio of 4:2, with the primaries connected in series and the secondaries connected in parallel.

Extensive research has focused on developing high-density, high-efficiency 400/50 V *LLC* converters using printed circuit board (PCB)-based magnetics [6], [16], [17]. While planar magnetics enable low-profile designs, they often require larger surface areas, limiting space for other PSU components and underutilizing the available 1 U (40 mm) vertical profile. As the rated power increases, these surface-area constraints become more pronounced, creating a need for an alternative form factor that enhances surface power density and fully exploits the available vertical height, while maintaining the manufacturability and repeatability of PCB windings.

To address these challenges, the *LLC* converter in this work is implemented as a vertically mounted module. This approach reduces the surface area occupied, supports future power expansion, and enables double-sided cooling by arranging components, as shown in Fig. 13(a). The input and output terminals are positioned along the bottom edge of the module for direct plug-in to the motherboard. The resonant inductor L_r and the two transformers are integrated into a single magnetic structure, with a common magnetic flux return leg along the top edge. The inductor and transformer legs incorporate air gaps to adjust their respective inductances, while the ungapped return leg provides

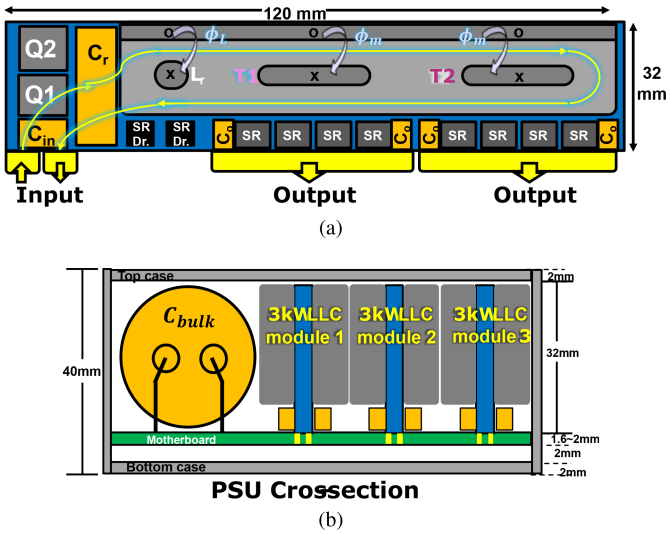


Fig. 13. (a) Vertically mounted module form factor. (b) Possible arrangement of multiple modules in parallel for 9 kW power.

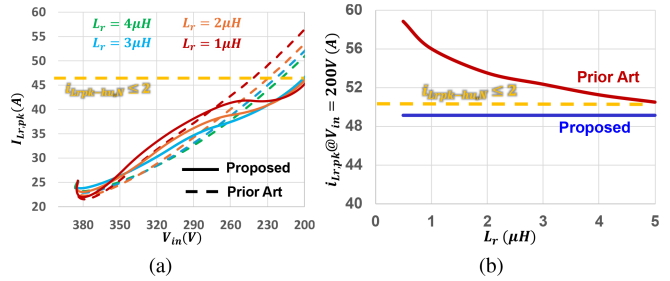


Fig. 14. (a) Peak i_{Lr} versus V_{in} at $V_o = 48$ V with varying L_r for both the prior-art and proposed methods. (b) Change in peak i_{Lr} at $V_{in} = 200$ V versus L_r for both the prior-art and proposed methods.

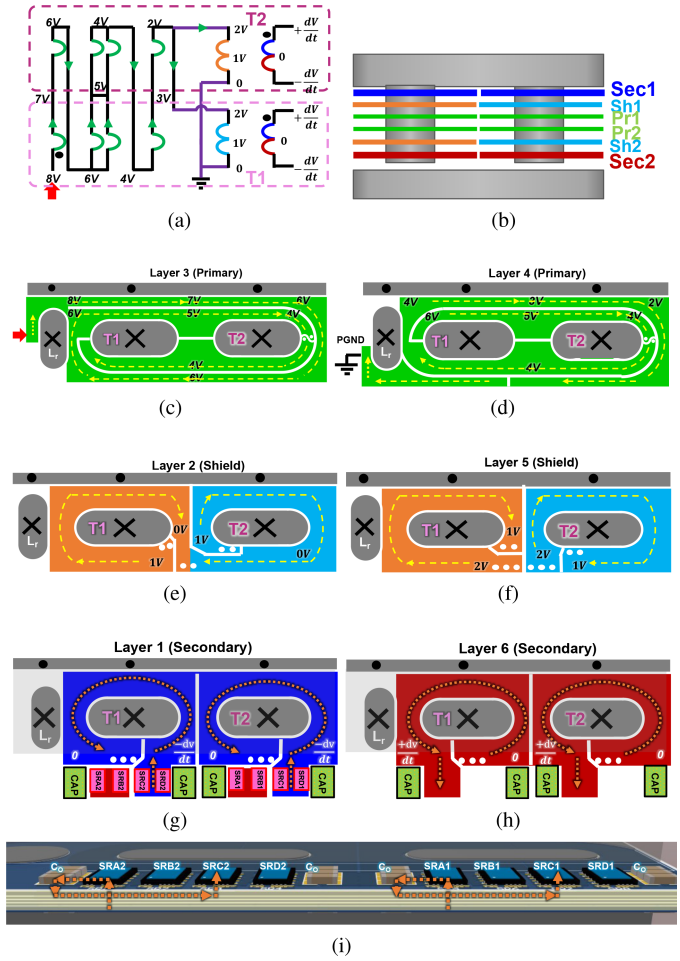


Fig. 15. PCB arrangement. (a) Transformer winding schematic. (b) PCB stack-up. (c) Pr1. (d) Pr2. (e) Sh1. (f) Sh2. (g) Sec1. (h) Sec2 layers. (i) secondary current flow through SR FB termination structure.

the lowest reluctance path for the magnetic flux from each leg. Multiple such modules can be paralleled, with adjacent input and output terminals simplifying interconnection, as illustrated in Fig. 13(b), enabling a total rated power of 9 kW.

The selection of resonant tank parameters is critical to achieving high efficiency while ensuring that the required gain is attainable without overstressing the converter. Unlike frequency modulation control, where the achievable gain is strongly dependent on L_m, the SR phase-shift control decouples gain from L_m. This allows L_m to be designed purely for minimizing device conduction losses at nominal operation. Following the optimization reported for a similar power and voltage conversion in [6], $L_m = 26$ μH is chosen for operation at 300 kHz.

The resonant inductance L_r significantly influences both the peak resonant inductor current $i_{\mathrm{Lr,pk}}$ and the required frequency range during hold-up operation, and thus must be selected carefully. Based on the mathematical model in Section III, $i_{\mathrm{Lr,pk}}$ is evaluated for decreasing V_{in} at $V_o = 48$ V (i.e., increasing gain), as shown in Fig. 14(a). The dotted $i_{\mathrm{Lr,pk}}$ curves representing conventional SR phase-shift control rise with gain because the required α, and hence the circulating current, increases for a given L_r. Since $i_{\mathrm{Lr,pk}} = i_{\mathrm{Lr}}(t_1)$ and the characteristic impedance $Z_o = \sqrt{L_r/C_r}$ decreases with increasing L_r (with C_r reduced accordingly to maintain f_o), it can be observed from (6) that the peak current decreases as L_r increases. Furthermore, a lower Z_o accelerates resonant tank charging and discharging, resulting in shorter switching cycles and a higher operating frequency range. However, increasing L_r also increases the inductor size and losses, requiring a tradeoff between nominal efficiency optimization and component stress during hold-up.

With the proposed control, sinusoidal operation is restored at $V_{\mathrm{in}} = 200$ V, making $i_{\mathrm{Lr,pk}}$ independent of L_r [see Fig. 14(b)]. The operating frequency range still grows with L_r and must be considered. Here, $i_{\mathrm{Lr,pk-hu,N}}$ is limited to 2 to avoid core saturation. Under conventional control, this requires $L_r = 5$ μH. The proposed method removes this limitation, and $L_r = 1$ μH is selected as a balanced choice between inductor size, loss, and frequency range.

The six-layer PCB winding stack-up is illustrated in Fig. 15(b), where the primary and secondary layers are interleaved, with shield layers inserted between them to suppress common-mode (CM) noise. Typically, the shield layers are designed identical to the secondary windings, and the node at

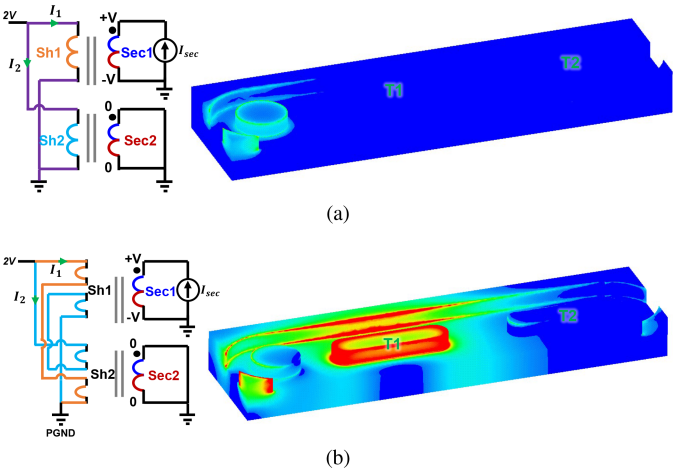


Fig. 16. (a) Conventionally paralleled shield windings resulting in undesirable magnetic-flux induction. (b) Interwound shield windings ensuring symmetry and proper magnetic-flux induction.

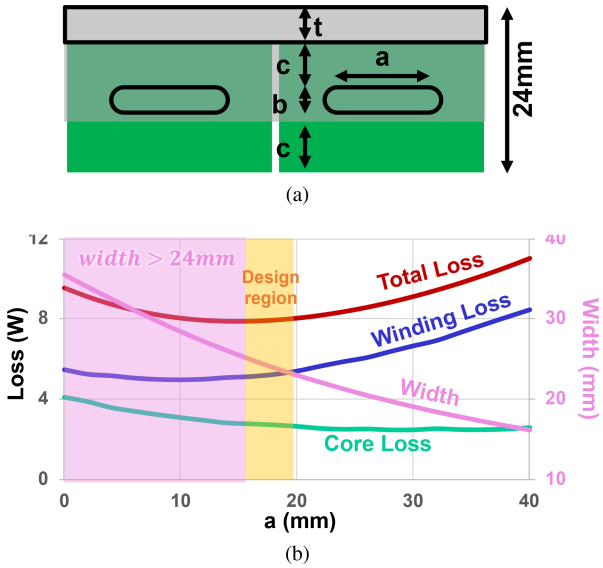


Fig. 17. (a) Transformer dimension parameter and profile constraint. (b) Selection of the design region based on minimum loss and limited profile.

zero potential is connected to the primary ground, as described in [18]. In this configuration, the identical shield and secondary windings remain equipotential, thereby mitigating CM currents through their interwinding capacitance, and instead redirecting them back to the primary ground to which the shield layers are connected. However, eddy currents are induced in the shield layers, which can increase the total winding loss. To better utilize the shield layers while reducing current stress on the primary layers, the shield layers are connected in series with the primary windings, effectively reducing the number of turns in the primary layers and hence lowering winding losses, as outlined in [7] and shown in Fig. 15(c)–(f). Although this increases the potential on the shield layers by $1V_o$, the effective reduction in winding loss outweighs the reduction in CM noise mitigation.

The secondary current paths, as depicted in Fig. 15(g)–(i), demonstrate the series connection of the two secondary layers and the FB rectifier layout, which minimizes termination loop length while placing all devices on the same side to enable shared cooling.

While the parallel connection of the shield layers in Fig. 15(a) effectively reduces CM noise and winding losses, it presents a drawback during the selective SR phase-shifting operation. When only one transformer is shorted, the resulting difference in potential between T1 and T2 drives unequal currents through the parallel shield windings. These unequal currents induce asymmetric voltages on the shield layers, which in turn disturb the normal operation of the other transformer, as shown in Fig. 16(a). To resolve this, the shield layers are interwound around both transformers, as illustrated in Fig. 16(b). This interleaving ensures symmetrical proximity to the secondary windings, thereby inducing equal currents in the shield layers and maintaining proper operation across both transformers.

Considering the case and motherboard thickness, the 40 mm PSU profile constraint limits the module height to 32 mm. Since the SR termination occupies approximately 8 mm, the transformer height must be restricted to 24 mm. At the same time, the core and winding dimensions must be optimized to minimize transformer losses for the given footprint. To meet both objectives, the core leg elongation a is swept at a fixed footprint, following the approach in [16]. Increasing a reduces the overall converter width and lowers the core loss through reduced flux density and eddy-current losses. However, it also increases the winding length, leading to higher winding loss. The design point is therefore chosen near the valley of the total transformer loss curve at half load (to maximize peak efficiency), while remaining within the 24 mm profile constraint, as shown in Fig. 17(b).

TABLE I
LLC CONVERTER PARAMETERS

Parameter	Value
Voltage rating	400/50 V
$P_{o,\max}$	3000 W
f_s	330 kHz
Primary device	2× CGD CGD65C025SP2
Secondary device	8× Innoscience INN100EQ016
Core material	DMEGC DMR59
L_m	27 μH
L_r	1 μH
Hold-up voltage range	200 – 400 V
Power density	1300 W/in^3
Surface density	1330 W/in^2

V. HARDWARE VERIFICATION

The proposed selective SR phase-shifting method is implemented in the 3 kW, 300 kHz, 400/50 V vertically mounted *LLC* converter module with a matrix of two elemental transformers, where the SRs of one bridge in an elemental transformer are selectively phase-shifted to achieve a peak gain of 2, as discussed in Section II. Table I lists the parameters of the 400/50 V *LLC* converter hardware prototype, and Fig. 18 shows the hardware prototype for the module. The converter operates at $f_0 = 330$ kHz during nominal operation and achieves a power

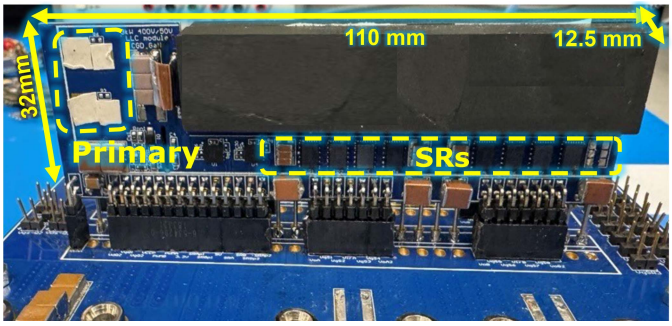
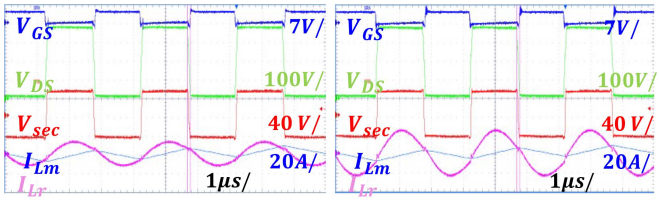
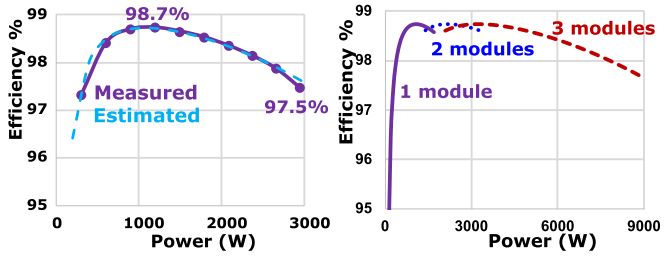


Fig. 18. 3 kW 400/50 V vertically mounted *LLC* module.



(a) (b)

Fig. 19. Waveforms at 400/50 V. (a) 50% load. (b) 100% load.



(a) (b)

Fig. 20. Converter efficiency at 400/50 V. (a) 3 kW operation. (b) 9 kW operation.

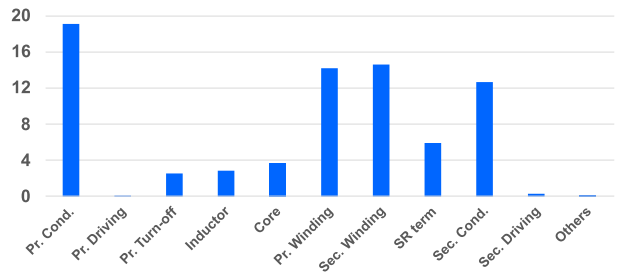
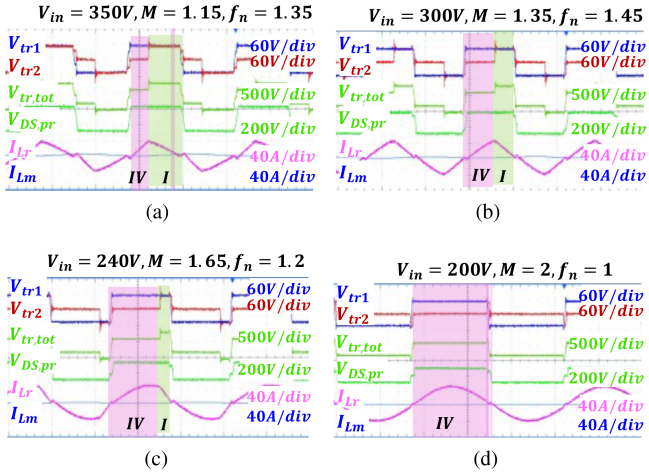


Fig. 21. Converter loss breakdown at full load of 3 kW.

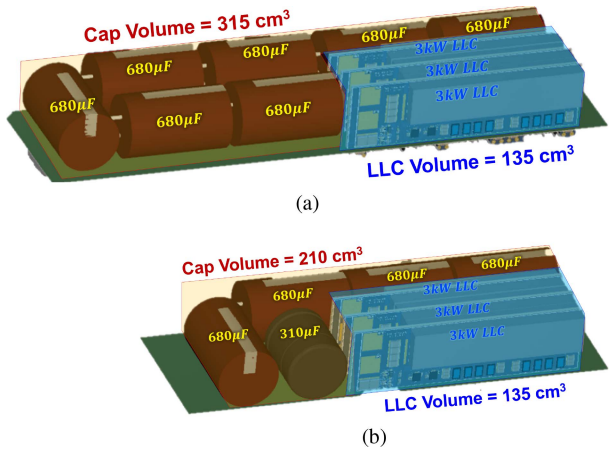
density of 1300 W/in^3 and a surface density of 1330 W/in^2, enabling multiple modules to be paralleled for high-power, high-density PSUs.

To facilitate high efficiency, GaN devices are used for both the primary and secondary sides. Fig. 19 shows the operating waveforms at 400/50 V at half load and full load, where ZVS is maintained across the load range. The measured efficiency, excluding driving losses, is shown in Fig. 20(a), with a peak



(a) (b) (c) (d)

Fig. 22. Key waveforms during hold-up time using selective SR phase-shifting at full load and $V_o = 50$V. (a) $M = 1.15$. (b) $M = 1.35$. (c) $M = 1.65$. (d) $M = 2$.



(a) (b)

Fig. 23. Estimated area occupation and layout of bulk capacitance and DC–DC converters in a 9-kW PSU under (a) frequency control and (b) selective SR phase-shift control.

efficiency of 98.7% and a full-load efficiency of 97.5%. Furthermore, Fig. 20(b) plots the projected efficiency with three modules in parallel for up to 9 kW, where phase-shedding can be implemented to boost the light-load efficiency.

Fig. 21 shows the loss breakdown of the converter at full load, where the majority of losses originate from current-dependent device conduction and winding losses, as expected.

During hold-up, the phase-shift angle on the SRs of the selectively phase-shifted transformer is progressively increased, while the switching frequency is initially raised and subsequently reduced back to f_o to follow the optimal trajectory described in Fig. 11(a). Fig. 22 illustrates the key waveforms as V_{in} decreases and the gain correspondingly increases to maintain the output voltage at 50 V under full-load conditions. Consistent with the analytical model, the maximum normalized frequency f_n reaches approximately 1.5 before returning to unity. Aside from the dead time, only Modes I and IV remain in operation, thereby minimizing the circulating current in the resonant

TABLE II
COMPARISON OF VARIOUS CONTROL METHODS TO BOOST *LLC* GAIN

Parameter	Freq. Ctrl.	SR PS Ctrl.	Proposed
Max. Gain, $M_{\max}$	1.35	2	2
Min. V_{in} (V)	296	200	200
Bulk Cap. @ full load	4.8 mF	3 mF	3 mF
Max. f_n range @ full load	0.28–1	1–1.9	1–1.5
$i_{Lr,pk}$ / $i_{\text{Lr, pk, nom}}$	3.83	2.46	2.04
Max. $i_{SR,off}$ (A)	0	120.1	83.7

PS: Phase-Shift

tank, which in turn reduces conduction losses and improves efficiency during the hold-up period. Furthermore, the results clearly demonstrate safe operation while achieving the required peak gain.

VI. CONCLUSION

Due to the rapid growth of artificial intelligence and machine learning, datacenter power demands are increasing exponentially, while the available space for power delivery remains largely unchanged. Consequently, the power density of ac–dc PSUs must increase to meet these demands. A major contributor to PSU volume is the bulk capacitance, which supplies energy during hold-up time when the *LLC* converter must operate at a high-voltage gain.

With frequency control, the achievable gain is constrained by L_m and L_r, and an efficiency-optimized design, such as the one presented in this article, can only reach a peak gain of 1.35, as shown in Fig. 4(a) and listed in Table II. From Fig. 3(c), this corresponds to $C_{\text{bulk}} = 4.8$ mF, occupying nearly three times the volume of the *LLC* converter, as illustrated in Fig. 23(a). Furthermore, a wide frequency range down to $f_n = 0.28$ is required, resulting in significantly higher peak and rms primary currents to deliver more energy per switching cycle. Nevertheless, the SRs maintain ZCS operation as they operate in discontinuous conduction mode.

To increase the achievable gain independently of L_m, SR phase-shifting can be employed while maintaining operation near the resonant frequency. For an enhanced maximum gain of 2, the required C_{bulk} reduces to 3 mF—a 33% reduction in capacitor volume compared to frequency control, as shown in Fig. 23(b) and listed in Table II. However, in the conventional SR phase-shift approach, the circulating-energy interval (Mode II) occupies a substantial portion of the switching cycle without contributing to useful power transfer. Eliminating Mode II necessitates increasing the switching frequency, which widens the frequency range and reduces the primary turn-OFF current, but simultaneously increases SR turn-OFF losses, particularly under light-load conditions.

This article introduces a *selective SR phase-shift control* technique that leverages matrix transformers, where phase-shifting is applied to only one elemental transformer. The other transformer continues to deliver load current during the phase-shift interval, thereby reducing the required frequency range, increasing primary turn-OFF current, and lowering SR switching losses compared to the conventional SR phase-shift control, while still achieving a maximum gain of 2, as listed in Table II. The method also allows the use of a smaller L_r without incurring excessive peak currents.

The proposed concept is experimentally validated on a vertically mounted 400/50 V LLC converter module with two elemental transformers, achieving a power density of 1300 W/in^3 and a surface power density of 1330 W/in^2, with full-load ZVS and a 200–400 V hold-up input range ($M = 2$). This control method provides an efficient and compact solution for achieving high gain in *LLC* converters and can be readily extended to other systems with wide gain requirements, such as onboard chargers and auxiliary power modules (APMs) in electric vehicles.

Overall, this work demonstrates a promising new control direction for high-current *LLC* converters requiring wide gain operation, particularly for hold-up management in datacenter PSUs. The proposed selective SR phase-shift approach can also be adapted to other high-performance applications, such as APMs in electric vehicles and other distributed power architectures. Future research may focus on maintaining high efficiency across the entire gain range by ensuring ZVS under lighter load conditions, possibly through adaptive frequency limiting or slight detuning above the optimal switching frequency $f_{n,\text{opt}}$. Further investigations could also explore achieving gain levels beyond $M = 2$ by extending the selective phase-shift concept to additional transformers or alternative interleaving strategies, thereby broadening the applicability of this approach to next-generation high-density power systems.

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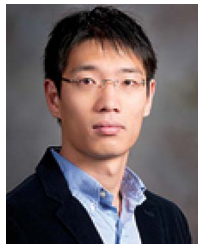

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