ZVS Analysis and Dead Time Selection of a Multiwinding Transformer-Based Multiport AC–DC PFC Converter

Himanshu Bhusan Sandhibigraha, *Graduate Student Member, IEEE*, and Vishnu Mahadeva Iyer, *Senior Member, IEEE*

***Abstract*—This article proposes a circuit-theoretic approach to analyze a multiwinding transformer-based multiport isolated ac–dc power factor correction (PFC) converter, with a focus on soft-switching performance. In isolated converters, the energy stored in the leakage fields of the high-frequency transformer plays a critical role in enabling zero voltage switching (ZVS) by discharging the device output capacitors prior to their turn ON. Accurate modeling of this energy is essential to estimate the ZVS range over a fundamental ac line cycle. The leakage energy is modeled using leakage inductors, and the extended cantilever model (ECM) offers a physically meaningful framework for capturing this energy in multiwinding transformers. However, the ECM becomes increasingly complex and less tractable as the number of windings exceeds three, hindering its direct application for soft-switching analysis. To address this, a unified equivalent model is developed using circuit-theoretic simplifications based on inherent symmetries in the multiport converter. This model is then used to perform a comprehensive soft-switching analysis that accounts for converter design parameters, parasitic elements, operating modes, and load variations. It is demonstrated that the ZVS range can be extended over the fundamental ac line cycle by selecting an optimal dead time. The theoretical findings are supported by circuit simulations using device models. Further, experimental results from a 1.2-kW hardware prototype of the multiport converter are presented to validate the findings.**

***Index Terms*—AC–DC conversion, active clamp, multiport converter, multiwinding transformer, power factor correction (PFC), soft switching, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

ISOLATED ac–dc conversion systems are employed in a wide variety of applications, such as electric vehicle (EV) charging infrastructure [1], [2], power supplies for data centers [3], ac–dc microgrids, and renewable energy storage systems [4]. In such applications, having a multiport converter is advantageous as compared to a multiconverter system, as it can integrate multiple sources and load subsystems without increasing the number of power converters [5]. A multiport converter can reduce the overall size and cost of the system due to component sharing among the ports. An isolated ac–dc conversion system can be broadly categorized into two types: isolated back-end (IBE)-based and isolated front-end (IFE)-based.

An IBE-based multiport ac–dc converter can be realized using a conventional two-port nonisolated front-end power factor correction (PFC) converter that shapes input current and regulates the intermediate dc link voltage [6]. This is cascaded by multiple isolated dc–dc converters, which cater to load subsystems at each port while ensuring isolation between the output ports and the input [7], [8]. Each of the isolated dc–dc converters uses a dedicated two-winding transformer for galvanic isolation. Alternatively, a multiwinding transformer-based realization can achieve galvanic isolation between each port while reducing the number of power conversion stages [9]. In the IBE-based realization, the front-end PFC stage is usually hard switched, while the isolated dc–dc stage is soft switched.

An IFE-based multiport ac–dc converter is realized using an isolated front-end converter that shapes input current and generates a folded ac voltage at the intermediate dc link while ensuring galvanic isolation between the ac and dc ports [10], [11]. This can be cascaded by multiple nonisolated dc–dc converters to cater to load subsystems at each port. However, this approach does not ensure isolation between each output port. To achieve galvanic isolation between each output port, either multiple isolated dc–dc converters may be employed, or a multiwinding transformer-based multiport isolated dc–dc converter may be used [12]. These approaches result in isolation being incorporated in both the front-end and back-end stages, which counteract the efforts toward reducing size and increasing power density. Consequently, such solutions are less prevalent in the literature.

Alternatively, several current-fed isolated front-end ac–dc PFC converters featuring one input and one output port have been proposed in the literature [14], [15]. A multiwinding transformer-based multiport ac–dc PFC converter was proposed

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The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: himanshubs@iisc.ac.in; vishnumi@iisc.ac.in).

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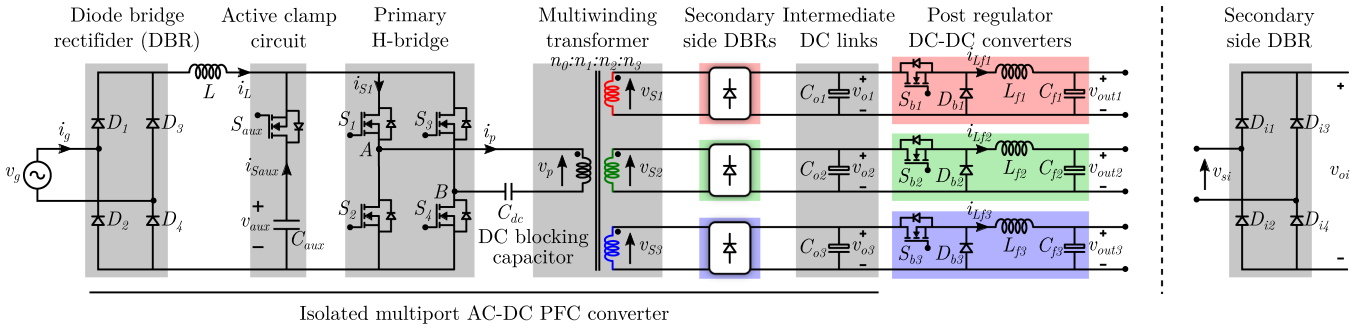


Fig. 1. Multiwinding transformer-based multiport isolated AC–DC PFC converter proposed in our prior work [13].

for EV charging applications in our prior work [13]. The converter comprises an isolated multiport soft-switched current-fed front-end ac–dc PFC converter, which shapes the input current and generates regulated dc voltages at the intermediate dc links. Since the intermediate dc link voltages are not controlled independently, a nonisolated post regulator is connected to each intermediate dc link to independently control the power flow to the load subsystems at each output port, as shown in Fig. 1. The multiport isolated ac–dc PFC stage is controlled in a manner similar to a boost PFC converter, while the post regulators are independently controlled. For an EV charging application, the proposed multiport converter enables simultaneous charging of multiple EVs with diverse battery specifications. The multiwinding transformer in the PFC stage ensures galvanic isolation between each charging port and the input ac port. As compared to a traditional IFE-based multiport system, the proposed approach has two key advantages. The first advantage is that every port is galvanically isolated from every other port. Furthermore, in the proposed converter, the voltage blocked by the switches during their OFF state does not vary over a fundamental line cycle. This simplifies the modulation scheme and closed-loop controller design and removes the need for any complex optimization in the modulation scheme to ensure soft-switching. In addition, the primary side switches of the front-end PFC stage simultaneously handle input current shaping and the generation of high-frequency voltage for the high-frequency transformer, resulting in a lower switch count than in an IBE-based solution.

The focus of this article is to analyze the zero voltage switching (ZVS) bounds of the proposed multiport isolated current-fed ac–dc PFC converter. Zero-voltage turn ON is achieved when the output capacitance of a switch is fully discharged before it is gated ON [16], [17]. Typically, in converters employing a transformer for galvanic isolation, this discharge is facilitated by the energy stored in the leakage field between the primary and secondary windings of the transformer, which is modeled as a leakage inductance in the equivalent circuit. In the proposed converter, both the energy stored in the PFC inductor and the leakage fields of the multiwinding transformer contribute to the discharge process. However, the available energy for discharge varies over the fundamental line cycle due to the nature of ac–dc conversion, making the zero-voltage turn ON dependent on the instant of the fundamental line cycle. As a result, there exists a range of the fundamental line cycle, within which zero-voltage turn ON of the switches is feasible. Maximizing this range requires a detailed soft-switching analysis. Another challenge lies in modeling the leakage energy in multiwinding transformers. For a multiwinding transformer, an extended cantilever model (ECM) offers a physically meaningful and intuitive framework for capturing the magnetic coupling and leakage interactions [18]. However, for transformers with more than three windings, the complexity of the ECM hinders its direct use for soft-switching analysis.

To address these challenges, this work proposes a circuit-theoretic simplification of the ECM, leveraging the inherent operational symmetry of the proposed converter. Since each output port is identical from a topological and functional view, the transformer ac port voltages and currents exhibit predictable symmetrical behavior. This symmetry enables a systematic reduction in the number of independent inductive elements in the equivalent circuit model of the multiwinding transformer, resulting in a compact yet accurate representation. This simplified model forms the foundation for the soft-switching analysis. A comprehensive soft-switching analysis is carried out for the switching transitions to establish the conditions for zero-voltage turn ON, and derive expressions for the minimum and maximum permissible dead times at each point in the fundamental line cycle. The insights and outcomes of the analysis are used to recommend optimal dead times to maximize the ZVS range over a fundamental line cycle.

The key contributions of this article are listed as follow.

1) Leveraging the ECM to represent the multiwinding transformer and gain insights into the multiport converter operation.
2) Analyzing the multiport converter's operating modes and the effect of loading on the leakage energy of the multiwinding transformer.
3) Introducing a circuit-theoretic reduction that simplifies the ECM into a unified, compact equivalent model valid across all operating modes.
4) Developing a comprehensive soft-switching analysis framework to examine switching transitions, establish zero-voltage turn-ON conditions, and derive expressions for the minimum and maximum permissible dead times to achieve soft-switching.
5) Providing recommendations for optimal dead time selection to maximize the ZVS range, considering converter design parameters, operating modes, and load variations.

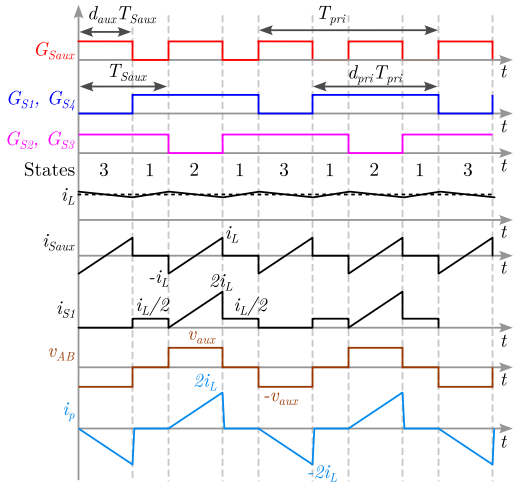


Fig. 2. Modulation scheme and theoretical steady-state waveforms.

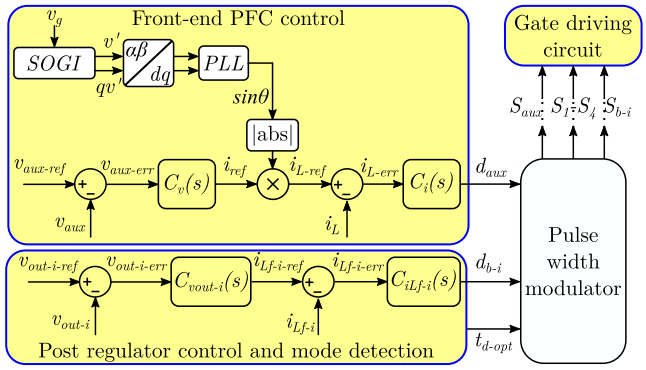


Fig. 3. Closed-loop control scheme of the converter showing front-end multiport PFC converter and one of the post regulator control loops.

II. Converter Operation

A. Modulation Scheme

The primary side H-bridge switches $S_1 - S_4$ are operated in synchronization with the auxiliary switch S_{aux}, to apply a positive voltage v_g, or a negative voltage $v_g - v_{\text{aux}}$, across the PFC inductor L, in a controlled manner as shown in Fig. 2. The duty ratio of the switches is varied to control the pulsewidth of the voltages applied. The duty ratio is varied as commanded by the closed-loop controller to shape the PFC inductor current i_L into a rectified sine wave in phase with the grid voltage. The circuit on the primary side traverses through states 1, 2, and 3 as the switches are turned ON and OFF. In state 1, the PFC inductor current i_L flows through all the bridge switches $S_1 - S_4$ and the currents $i_{S\text{aux}}$, i_p are zero. At the beginning of state 2, the mismatch in currents i_L and i_p, forces current i_L to flow through the body diode of S_{aux}. Thus, the current through the auxiliary capacitor is $i_{C\text{aux}} = i_{S\text{aux}} = -i_L$. For the ampere-second balance to hold good for the capacitor C_{aux}, the final value of axuiliary capacitor current at the end of state 2 is i_L and final value of primary current is $2i_L$. A similar analysis can be done for state 3. The idealized steady-state currents and voltages are shown in Fig. 2. With three secondary ports, the converter exhibits five distinct modes of operation, depending on the loading of each port:

1) *Mode I:* All three ports are equally loaded.
2) *Mode II:* All three ports are unequally loaded.
3) *Mode III:* Two of the three ports are equally loaded.
4) *Mode IV:* Two of the three ports are unequally loaded.
5) *Mode V:* Only one of the three ports is loaded.

B. Closed-Loop Control Scheme

The converter operates in grid-connected mode under closed-loop control. Two cascaded control loops are implemented for each of the following stages: the front-end multiport PFC stage, and each of the three buck post-regulators (Buck 1, Buck 2, and Buck 3) as shown in Fig. 3. For the front-end PFC stage, a standard boost PFC control approach is used: the outer voltage loop regulates the auxiliary capacitor voltage v_{aux} to a fixed value greater than the page of grid voltage v_g, and generates the current reference magnitude i_{ref}, for the inner current control loop. The inner loop regulates the PFC inductor current i_L to follow a rectified sinusoidal waveform. Each buck converter employs an outer voltage loop for output regulation and an inner current loop for controlling the buck inductor current.

The intermediate dc links are not independently regulated. Only the auxiliary capacitor voltage v_{aux} is directly regulated, and due to the symmetrical transformer construction, the intermediate dc link voltages v_{o1}, v_{o2}, v_{o3} naturally converge to approximately the same value. All postregulator dc–dc stages operate independently to facilitate constant current-constant voltage (CC-CV) charging at each output port.

C. Switching Transitions

The converter undergoes four unique switching transitions involving the auxiliary switch S_{aux}, and bridge switches, $S_1 - S_4$, whenever there is a state change. The transitions can be listed as follows.

1) Transition 1: turn OFF of S_{aux}, turn ON of S_2 and S_3 (S_1 and S_4 being ON).
2) Transition 2: turn OFF of S_1 and S_4, turn ON of S_{aux} (S_2 and S_3 being ON).
3) Transition 3: turn OFF of S_{aux}, turn ON of S_1 and S_4 (S_2 and S_3 being ON).
4) Transition 4: turn OFF of S_2 and S_3, turn ON of S_{aux} (S_1 and S_4 being ON).

Transitions 1 and 3 are associated with bridge switch turn ON and are categorized into *transition type I*. Transitions 2 and 4 are associated with the auxiliary switch turn ON and are categorized into *transition type II*. One transition from each category will be analyzed in Section III. In the multiport converter, the energy stored in the PFC inductor L, and the leakage inductors of the multiwinding transformer are responsible for discharging the device output capacitors and enabling soft switching of the primary side switches, $S_1 - S_4$ and S_{aux}. It is essential to estimate an equivalent inductor and its associated energy for soft-switching analysis of the transitions.

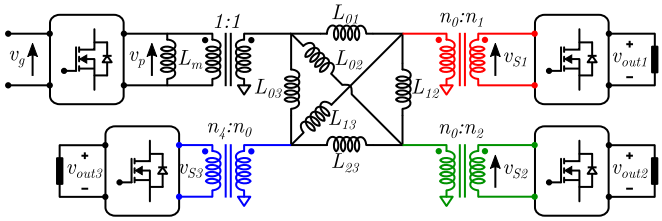


Fig. 4. ECM for a four-winding transformer.

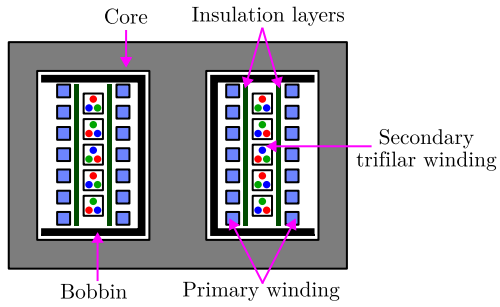


Fig. 5. Cross-sectional view of the transformer window and the winding pattern of the four-winding transformer.

D. Multiwinding Transformer Modeling

A multiwinding transformer is modeled using an ECM as shown in Fig. 4. The parameters of the model can be obtained from open-circuit and short-circuit measurements [18]. However, for transformers with four or more windings, the ECM results in a circuit with complex, nonplanar interconnections, making both analysis and interpretation cumbersome. Although a graphically planar topological dual has been proposed for four-winding transformers in [19], the resulting equivalent circuit remains nonintuitive and analytically complex for soft-switching studies. Moreover, the energy stored in the leakage fields varies dynamically with converter operating modes and port load conditions, necessitating a modeling approach that is both analytically manageable and physically meaningful.

The proposed converter is intended for an EV charging application with three identical ports. Achieving such port-level symmetry requires that the transformer's secondary windings exhibit identical electrical and magnetic characteristics. Accordingly, the transformer is constructed with equal turns on each secondary winding ($n_1 = n_2 = n_3$) and implemented using a trifilar winding configuration, as shown in Fig. 5. The trifilar winding on the secondary side is one of the ways to introduce symmetry. The transformer turns ratios are therefore expressed as

$$n_0 : n_1 = n_0 : n_2 = n_0 : n_3 = n : 1 \tag{1}$$

Due to the trifilar winding pattern, each of the secondary windings is symmetric with respect to the primary winding, and each of the secondary windings is symmetric with respect to each other. This assumption holds good when the primary and secondary winding cross-sectional areas are much smaller than the window height as well as the separation between primary and secondary windings, ensuring identical magnetic coupling between the primary and each of the secondaries. This will also hold good for planar geometries, provided that the secondary trace cross-sectional area remains small relative to the window height and sufficient spacing with respect to the primary winding is maintained. For low-profile planar designs where these conditions do not naturally hold, symmetry can still be deliberately enforced through careful layout and winding strategy at the design stage. By virtue of this symmetry, it can therefore be considered that the inductors modeled between the primary and each of the secondary windings are identical, i.e., $L_{01} = L_{02} = L_{03} = L_1$. Similarly, the inductors between each of the secondary windings can be considered to be the same, i.e., $L_{12} = L_{23} = L_{13} = L_2$ as shown in Fig. 6(a). Also, it is assumed that the value of the magnetizing inductance L_m is sufficiently larger than that of L_1 or L_2, and is omitted from the model.

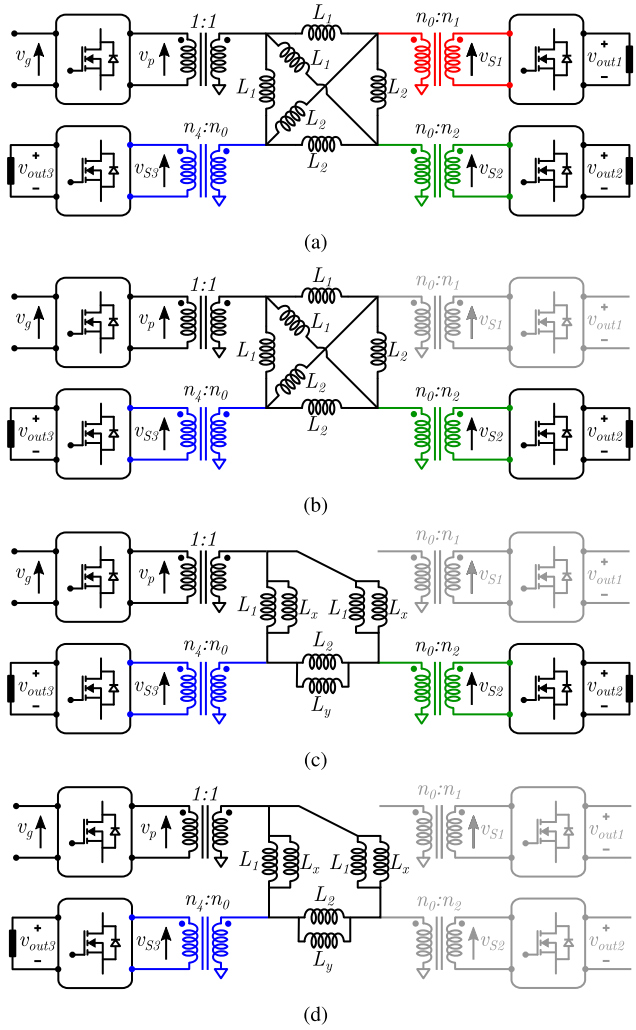


Fig. 6. Extended cantilever model for (a) mode I, (b) modes III and IV, (c) modes III and IV transformed, and (d) mode V.

Fig. 6(a) shows the transformer model for operating mode I, where all three ports are equally loaded. In this mode, the voltage drops across the inductors labeled as L_1 are the same, and the voltage drops across the inductors labeled as L_2 are zero.

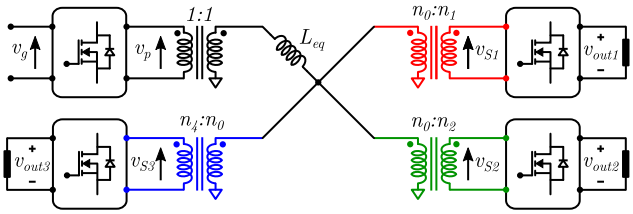


Fig. 7. Equivalent inductance representation of the multiwinding transformer. For modes I, III, and V, the L_{eq} is defined, while for modes II and IV, the representation of equivalent inductance is an approximation, where the value of L_{eq} lies within a range as listed in Table I.

Therefore, the inductors L_2 can be omitted from the model. This also results in the three output voltages being the same, i.e., $v_{o1} = v_{o2} = v_{o3}$. The effect of the three inductors can be modeled by a single equivalent inductor as

$$L_{eq} = L_1/3 \tag{2}$$

When one of the ports is unloaded, the transformer circuit model in Fig. 6(b) can be reduced to a circuit as shown in Fig. 6(c). The value of inductors L_x and L_y can be obtained by star-delta transformation and can be expressed as

$$L_x = 2L_1 + L_2 \tag{3}$$

$$L_y = \frac{L_2}{L_1}(2L_1 + L_2) \tag{4}$$

For symmetric loading of two ports (mode III), the voltage drop across the combination of L_2 and L_y is zero, and hence the parallel combination of L_2 and L_y can be omitted. Similar to mode I, this also results in two port voltages being equal, i.e., $v_{o2} = v_{o3}$. The equivalent inductance L_{eq} for operating mode III can be expressed as

$$L_{eq} = 0.5\frac{L_1 L_x}{L_1 + L_x} = \frac{L_1(L_1 + 0.5L_2)}{3L_1 + L_2} \tag{5}$$

Similarly for mode V shown in Fig. 6(d), L_{eq} can be expressed as

$$L_{eq} = \frac{L_1(L_1 + L_2)}{3L_1 + L_2} \tag{6}$$

At the end of states 2 and 3, the transformer primary current i_p falls to zero with a finite slope. The slope of the current during this is dependent on the output voltages v_{o1}, v_{o2}, v_{o3}, and the equivalent inductance L_{eq}. For modes I, III, and V, a single slope can be defined as

$$\frac{di_p}{dt} = \frac{-nv_o}{L_{eq}} \tag{7}$$

where nv_o is the reflected output voltage at the other end of the equivalent inductor L_{eq}. The transformer model can then be reduced to that with a single equivalent inductance L_{eq} as shown in Fig. 7. For unequal loading modes II and IV, the output voltages v_{o1}, v_{o2}, v_{o3}, and the voltage drops across the leakage inductors are different. In such cases, the falling slope of i_p changes as the current through the port with the lowest loading falls to zero, while the other ports are still conducting. Also, there are multiple values of the reflected voltage, depending

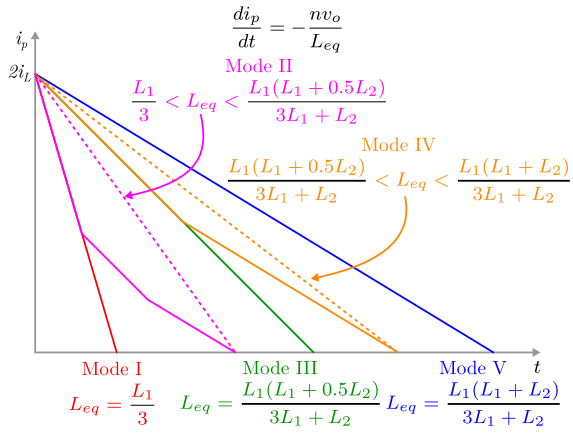


Fig. 8. Transformer primary current i_p during its falling interval showing the variation of slopes with respect to converter operating modes.

on the number of ports under conduction. Therefore, a single equivalent inductance cannot be defined for operation modes II and IV. However, an approximate equivalent inductance may be considered by approximating the slope to a single value. Fig. 8 shows the current during their falling interval for different modes, where the total power for each mode is considered to be the same. The value of the approximate equivalent inductance for modes II and IV can lie within a range bounded by the limiting modes of I, III, and V, depending on the ratio of unequal loading, as listed in Table I.

III. ZVS Analysis

This section presents the analysis for the switching transitions for the multiport converter using the equivalent inductance model developed. The assumptions considered for the analysis are listed below.

1) All the circuits are referred to the primary side.
2) The PFC inductor L is replaced by an ideal current source with a value $I_{L(\theta)}$, which stays constant over a switching cycle, but varies over a fundamental line cycle as a function of $\theta = \omega t$.
3) The auxiliary capacitor C_{aux} and the output capacitor C_o are replaced by an ideal voltage sources with voltages $V_{\text{aux}(\theta)}$ and $V_{o(\theta)}$, respectively.
4) All device capacitances are replaced by their charge-equivalent capacitance $C_{q,eq}$.
5) The transformer magnetizing inductance $L_m \gg L_{eq}$ is omitted.
6) For turn-OFF transitions, it is assumed that the device current flows through its respective output capacitance once the device is gated OFF.

A. Transition Type I

This corresponds to the turn OFF of the auxiliary switch S_{aux} and turn ON of any of the diagonal bridge switches $S_1 - S_4$. Here, the turn ON of switches S_2 and S_3 is analyzed, which can be extended to S_1 and S_4. The analysis is split into two intervals based on the circuit elements participating in the transition.

TABLE I
OPERATING MODES AND EQUIVALENT INDUCTANCE

Operating Mode	Voltages	Equivalent Inductance
I: Three ports equally loaded	$nv_{o1} = nv_{o2} = nv_{o3} = nv_o$	$\frac{L_1}{3}$
II: Three ports unequally loaded	$nv_{o1} \neq nv_{o2} \neq nv_{o3}$	$\frac{L_1}{3} < L_{eq} < \frac{L_1(L_1+0.5L_2)}{3L_1+L_2}$
III: Ports 2 and 3 loaded equally, port 1 unloaded	$nv_{o2} = nv_{o3} = nv_o$	$\frac{L_1(L_1+0.5L_2)}{3L_1+L_2}$
IV: Ports 2 and 3 loaded unequally, port 1 unloaded	$nv_{o1} \neq nv_{o2} \neq nv_{o3}$	$\frac{L_1(L_1+0.5L_2)}{3L_1+L_2} < L_{eq} < \frac{L_1(L_1+L_2)}{3L_1+L_2}$
V: Port 3 loaded, ports 1 and 2 unloaded	$nv_{o3} = nv_o$	$\frac{L_1(L_1+L_2)}{3L_1+L_2}$

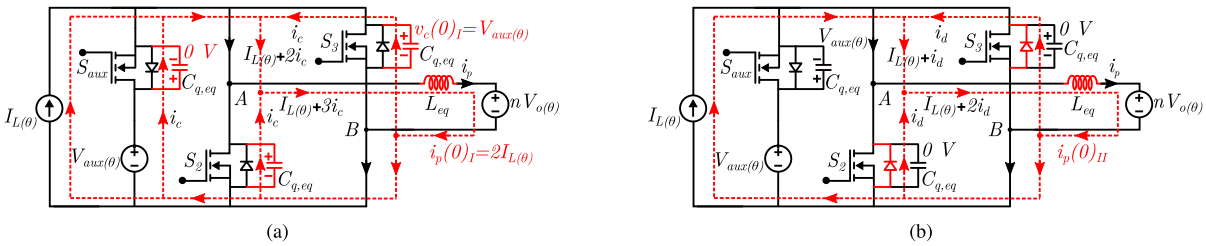


Fig. 9. Circuits under consideration for analysis of transition type I (a) interval I and (b) interval II.

Interval I: The start of interval I is marked by gating OFF of the auxiliary switch S_{aux} as shown in Fig. 9(a). As soon as S_{aux} is gated OFF, the charge equivalent device capacitors $C_{q,eq}$ of switches S_{aux}, S_2, S_3 start to resonate with the equivalent leakage inductor L_{eq}. The initial conditions are highlighted in red in Fig. 9(b). The interval I is governed by the following equations:

$$C_{q,eq}\frac{dv_c}{dt} = C_{q,eq}v_c' = -i_c \tag{8}$$

$$v_c - L_{eq}\frac{di_p}{dt} = nV_{o(\theta)} \tag{9}$$

where $i_p = I_{L(\theta)} + 3i_c$, and v_c is the voltage across device capacitors.

As $i_L = I_{L(\theta)}$ remains fairly constant through the transition, therefore $\frac{dI_{L(\theta)}}{dt} = 0$. On substituting this condition and (8) in (9), we get

$$v_c + 3L_{eq}C_{q,eq}\frac{d^2v_c}{dt^2} = nV_{o(\theta)}. \tag{10}$$

On solving (10), we get

$$v_c = nV_{o(\theta)} + \sqrt{a^2+b^2}\sin\left(\omega_0 t + \pi + \tan^{-1}\frac{b}{a}\right) \tag{11}$$

where $\omega_0 = \sqrt{\frac{1}{L_{eq}C_{q,eq}}}$, $a = \frac{v_c'(0)}{\omega_0} = \frac{-i_c(0)}{\omega_0 C_{q,eq}}$, $b = v_c(0)_I - nV_{o(\theta)} = V_{\text{aux}(\theta)} - nV_{o(\theta)}$.

The equivalent leakage inductor current i_p can be computed from (8) and (11), which is

$$i_p = I_{L(\theta)} - 3\left(\omega_0 C_{q,eq}\sqrt{a^2+b^2}\cos\left(\omega_0 t + \pi + \tan^{-1}\frac{b}{a}\right)\right) \tag{12}$$

This interval implies the discharging of output capacitors of devices S_2 and S_3 and charging of the output capacitor of S_{aux}. Once the capacitors of devices S_2 and S_3 have been discharged to zero, they can be turned ON with zero voltage. The minimum time to be allowed to let the voltage $v_c(t)$ discharge to zero is the minimum dead time to be provided between turning OFF the auxiliary switch S_{aux} and turning on of S_2, S_3. The minimum dead time $t_{d\text{min}}$ is computed by equating (11) to zero and expressed as

$$t_{d\text{min}} = \frac{1}{\omega_0}\left(\sin^{-1}\left(\frac{nV_{o(\theta)}}{\sqrt{a^2+b^2}}\right) - \tan^{-1}\frac{b}{a}\right) \tag{13}$$

The equivalent leakage inductor current i_p at the end of interval I can be computed by substituting $t = t_{d\text{min}}$ in (12), which serves as the initial condition $i_p(0)_{II}$ for interval II.

Interval II: Interval II starts with the commutation of the current from output capacitors of devices S_2, S_3 to the respective body diodes of the devices as shown in Fig. 9(b). Here, the voltage applied by the bridge v_{AB} is zero, and the voltage across the equivalent leakage inductor L_{eq} is negative $-nV_{o(\theta)}$. As a result, the current i_p starts to fall linearly from $i_p(0)_{II}$. In this interval, the difference of currents $I_{L(\theta)}$ and i_p flows through the body diodes of switches S_2 and S_3 equally, which is expressed as

$$i_d = \frac{i_p - I_{L(\theta)}}{2} \tag{14}$$

If the current through the respective body diodes is allowed to fall beyond zero, it will charge the output capacitors of the devices S_2 and S_3. This results in a partial or complete hard turn ON. Therefore, the switches S_2 and S_3 need to be gated ON before the current i_d falls to zero. The maximum allowed time

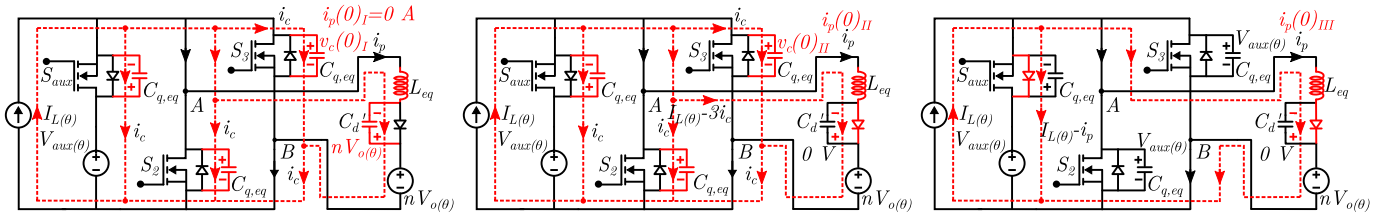


Fig. 10. Circuits under consideration for the analysis of transition type II (a) interval 1, (b) interval 2, and (c) interval 3.

t_{diode} is expressed as

$$t_{\text{diode}} = L_{eq}\frac{i_p(0)_{II} - I_{L(\theta)}}{nV_{o(\theta)}} \tag{15}$$

The maximum dead time that can be allowed between the turn OFF of the auxiliary switch S_{aux} and zero voltage turn ON of the bridge switches $S_2,\ S_3$, can be expressed as

$$t_{d\max} = t_{d\min} + t_{\text{diode}} \tag{16}$$

It can be observed from (13) that $\sin^{-1}(\frac{nV_{o(\theta)}}{\sqrt{a^2+b^2}})$ is only defined if $nV_{o(\theta)} < \sqrt{a^2+b^2}$. As the values, $a,\ b$ depend on initial conditions $i_c(0), v_c(0)_I$, which vary with fundamental angle θ therefore, there exists a minimum fundamental angle $\theta_{\min}$ below which $nV_{o(\theta)} > \sqrt{a^2+b^2}$. The limiting case is where $nV_{o(\theta)} = \sqrt{a^2+b^2}$ and $t_{d\min}$ for this case is

$$t_{d\min-\lim} = \frac{1}{\omega_0}\left(\frac{\pi}{2} - \tan^{-1}\frac{b}{a}\right) \tag{17}$$

This is also the instant where the currents are just enough to discharge the capacitors. On substituting the condition, $nV_{o(\theta)} = \sqrt{a^2+b^2}$ in (12), it can be seen that at the end of interval I, the currents $i_p = I_{L(\theta)}$, which implies $t_{\text{diode}} = 0$. Hence, at $\theta_{\min}$, $t_{d\min} = t_{d\max}$.

B. Transition type II

Transition type II corresponds to the turn OFF of diagonal bridge switches (S_1, S_4 or S_2, S_3) and the turn ON of the auxiliary switch S_{aux}. This analysis focuses on turn OFF of S_2 and S_3, which also applies to S_1 and S_4.

Transition type II begins with the turn OFF of bridge switches $S_2,\ S_3$ and progresses through intervals I, II, and III. Prior to this transition, the equivalent leakage inductor current i_p and secondary winding current are zero, causing all secondary diodes D_{i1}-D_{i4} to block half the output voltage $v_o/2$. For current to start flowing through the secondary winding and diodes, the parasitic capacitors across the diagonal diodes (D_{i1}, D_{i4}) must discharge and those across $D_{i2},\ D_{i3}$ must get charged to v_o. The effect of charging and discharging of diode capacitances is considered by including the series combination of two diodes $C'_d = 3\times 0.5C_{d,eq}/n^2$, as shown in Fig. 10(a).

Interval I: Interval I starts with the resonance between the capacitors $C_{q,eq}$ across devices $S_{\text{aux}},\ S_2,\ S_3$, effective secondary side capacitance reflected to the primary side C'_d and equivalent leakage inductor L_{eq}.

By solving the circuit, we get the following:

$$i_c = I_{L(\theta)}\frac{C_{q,eq}}{C'_d+3C_{q,eq}} + \frac{I_{L(\theta)}}{3}\frac{C'_d}{C'_d+3C_{q,eq}}\cos(\omega_1 t) \tag{18}$$

$$v_c = \left[\frac{I_{L(\theta)}C_{q,eq}}{C'_d+3C_{q,eq}}t + \frac{I_{L(\theta)}C'_d}{C'_d+3C_{q,eq}}\frac{\sin(\omega_1 t)}{3\omega_1}\right]\frac{1}{C_{q,eq}} \tag{19}$$

$$v_{cd} = nV_{o(\theta)} - \frac{I_{L(\theta)}}{C_{q,eq}+3C'_d}\left[t - \frac{\sin(\omega_1 t)}{\omega_1}\right] \tag{20}$$

where $\omega_1 = \sqrt{\frac{1}{L_{eq}C_{eq}}}$, $C_{eq} = \frac{3C_{q,eq}C'_d}{3C_{q,eq}+C'_d}$, and v_{cd} is the voltage across the equivalent secondary diode capacitance C'_d.

Interval I ends with the secondary side diode capacitance discharging to zero. The time t_{dis} taken to discharge C'_d is found by equating $v_{cd} = 0$. The values of capacitor currents$i_c = i_c(0)_{II}$, and voltages $v_c = v_c(0)_{II}$, at the end of interval I can be found by substituting t_{dis} into (18) and (19), respectively, which serve as initial conditions for interval II.

The circuit then progresses through intervals II and III (similar to intervals I and II for transition type I) as shown in Fig. 10(b), (c). Interval II ends with charging of $C_{q,eq}$ to voltage $v_c = V_{\text{aux}(\theta)}$. At the end of this interval, the body diode of the auxiliary switch S_{aux} starts to conduct. The total time taken by intervals I and II together is the minimum dead time to be allowed for soft turn ON of the auxiliary switchS_{aux}

$$t_{d\min} = t_{\text{dis}} + t_{II} \tag{21}$$

where t_{II} is the time taken in interval II. For soft turn ON, the auxiliary switch has to be gated ON before $i_{d\text{aux}}$ reaches zero. The maximum dead time can be computed by using (16) with appropriate initial conditions corresponding to transition type II. From (18), it can be noticed that during interval I of type II transition, the expression of the current i_c has a dc component $I_{L(\theta)}\frac{C_{q,eq}}{C'_d+3C_{q,eq}}$. This results in minimum dead time going to infinity as the current $I_{L(\theta)}$ goes to zero. This implies that ZVS for S_{aux} is achievable even at very low fundamental angles, where $I_{L(\theta)} \to 0$, provided sufficient dead time is allowed. However, excessively long dead times would increase diode conduction intervals, causing higher conduction losses due to the relatively large forward voltage drop of SiC/GaN body diodes. Also, in practice, such long dead times, in the order of the switching period, are not feasible, as it would lead to pulse skipping. This will modify the voltage vectors applied across the boost PFC

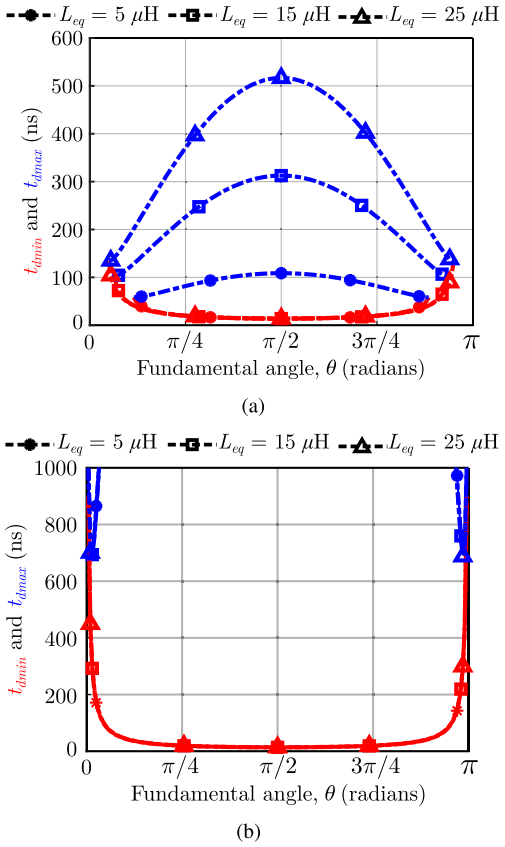


Fig. 11. Plots showing the minimum and maximum dead times for variation of equivalent leakage inductance L_{eq} for transitions of (a) type I and (b) type II.

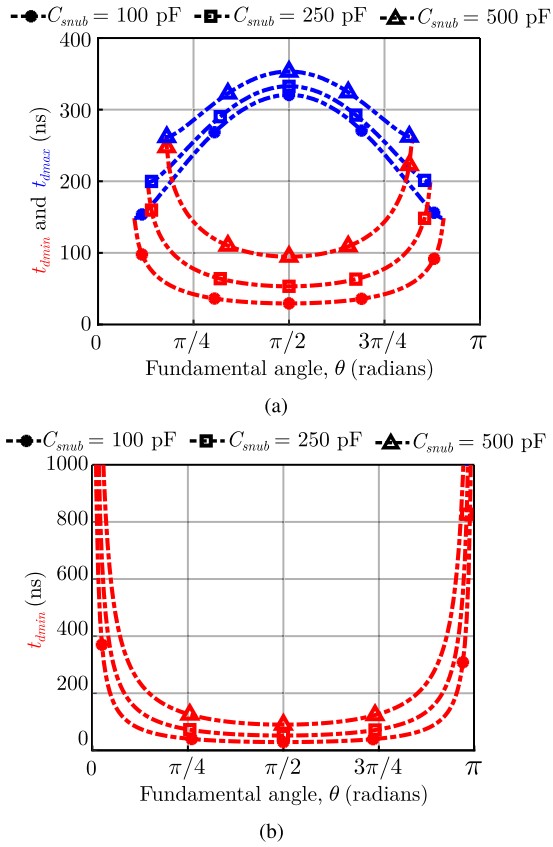


Fig. 12. Plots showing the minimum and maximum dead times for variation of snubber capacitance C_{snub} for transitions of (a) type I and (b) type II.

inductor L, thus affecting the current shaping at lower fundamental angles. Therefore, for practical feasibility and digital implementation considerations, the dead time for turn ON of S_{aux} can be kept the same as that for the bridge switches, which will be elucidated in the later sections.

IV. ZVS Range and Dead Time Selection

This section presents the dead time bounds of the converter and their variation with the converter design parameters. It is considered that the converter is interfaced with a 230 V, 50 Hz grid and it is operating in mode I at rated power, $P_o = 1.2$ kW, where each port is operating at 400 W, at an output voltage, $v_{o1} = v_{o2} = v_{o3} = 100$ V. The transformer turns ratio is 29:8:8:8. The value of linear charge equivalent output capacitance $C_{q,eq}$ is computed to be 90 pF for a blocking voltage of 400 V, using the datasheet information [20], using the approach elucidated in [21]. The diode capacitance $C_{d,eq} = 20$ pF, has been obtained from the datasheet [22].

A. Leakage Inductor L_{eq}

As seen in the previous section, the value of equivalent leakage inductance plays a role in the computation of minimum and maximum permissible dead times for the transitions. Also, for a given output voltage $v_{o1} = v_{o2} = v_{o3} = v_o$, the auxiliary capacitor voltage v_{aux} can be expressed as

$$v_{\text{aux}} = nv_o/\left(1 - \frac{2I_m}{V_m}\frac{L_{eq}}{T_s}\right) \tag{22}$$

where V_m and I_m are the peak values of grid voltage v_g and grid current i_g, respectively. Fig. 11(a) and (b) shows the variation in the computed dead times for different values of leakage inductance L_{eq} for type I and type II transitions, respectively. It can be seen from Fig. 11(a) that the minimum angle θ_{min} reduces as the equivalent inductance L_{eq} increases. Therefore, the soft switching range for type I transitions increases with increasing L_{eq}. The variation of computed dead times for type II transitions with respect to L_{eq} is not as pronounced as that of type I.

B. Snubber Capacitor C_{snub}

A snubber capacitor C_{snub} across the devices will add to its output capacitance, altering the charging/discharging times. Fig. 12(a) and (b) shows the plots of minimum and maximum dead time over the fundamental line cycle for different values of C_{snub} across the devices. An equivalent inductance $L_{eq} = 15$ μH is considered for the analysis.

Further, it is known that the addition of snubber capacitance C_{snub} slows down the rate of rise of voltage across the devices, aiding in zero current turn OFF of the device. LTspice simulations shown in Fig. 13 validate the same for $i_L = 5.22$ A at

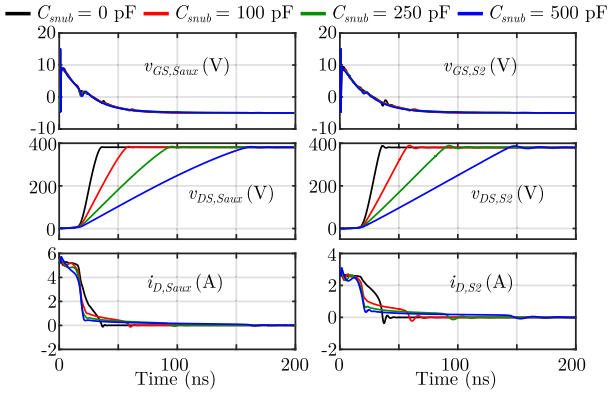
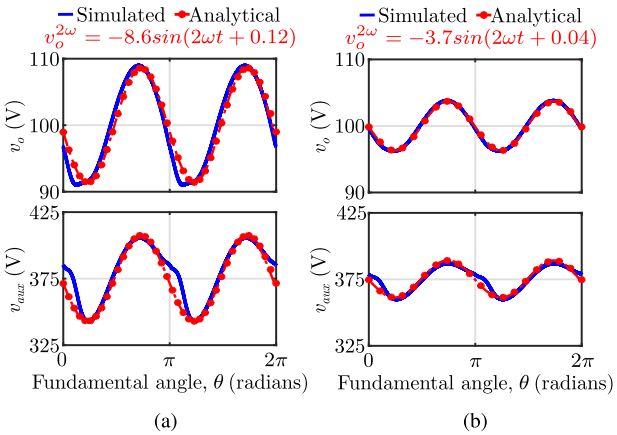


Fig. 13. Simulation results showing the impact of snubber capacitor variation on zero- current turn-OFF of switches S_{aux} and S_2 for $i_L = 5.22$ A.



(a) (b)

Fig. 14. Comparison of double line frequency voltage ripple for (a) $C_{o1} = C_{o2} = C_{o3} = 500$ μF. (b) $C_{o1} = C_{o2} = C_{o3} = 1500$ μF.

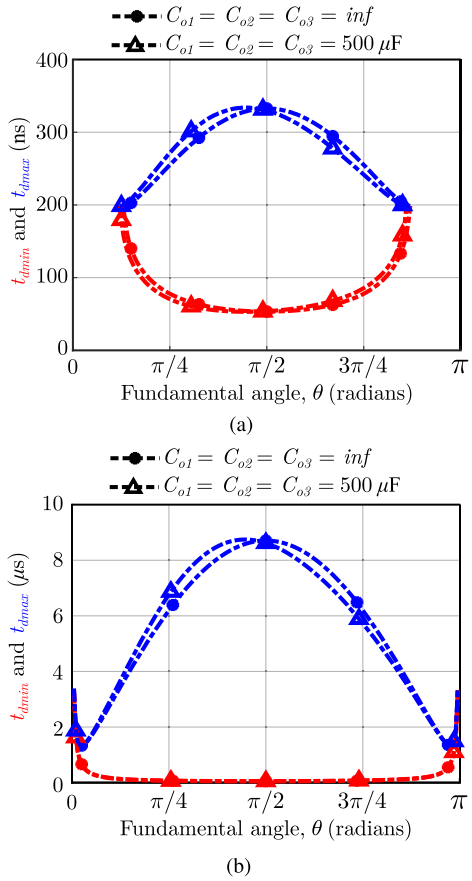


Fig. 15. Plots showing the minimum and maximum dead times for variation of output capacitance C_{o1}, C_{o2}, C_{o3} for transitions (a) type I and (b) type II.

$\theta = \pi/4$ rad. It can be seen that with increasing C_{snub}, there is improvement in the zero current turn OFF, but the minimum fundamental angle θ_{min} also increases, thus shrinking the soft switching range. Hence, there exists a tradeoff between achieving zero current turn OFF and extending the ZVS range over a fundamental cycle.

C. Output Capacitors C_{o1}, C_{o2}, C_{o3}

The output capacitors C_{o1}, C_{o2}, and C_{o3} handle most of the double line frequency power, resulting in a double line frequency voltage ripple in voltages v_{o1}, v_{o2}, v_{o3}. and v_{aux}. This affects the initial and final device capacitor voltages during switching transitions. The double line frequency voltage $v_o^{2\omega}$ can be computed by equating the net double line frequency power at the input with that handled by the converter.

$$P_{\text{in}}^{2\omega} = P_L^{2\omega} + P_{\text{aux}}^{2\omega} + P_{co}^{2\omega} + P_o^{2\omega} \tag{23}$$

where $P_{\text{in}}^{2\omega} = -\frac{V_m I_m}{2}\cos 2\omega t$, $P_L^{2\omega}$, $P_{\text{aux}}^{2\omega}$, $P_{co}^{2\omega}$, $P_o^{2\omega}$ are double line frequency power handled by PFC inductor L, auxiliary capacitor C_{aux}, output capacitors, and resistive loads.

Fig. 14 shows the output voltage v_o and auxiliary voltage v_{aux} waveforms obtained from analysis along with simulated waveforms. The difference in theoretical and simulated v_{aux} waveforms is attributed to the zero crossing distortion and the drop across the leakage inductor, where the relation (22) does not hold well. The capacitors C_{o1}, C_{o2}, C_{o3} must be chosen such that $v_{\text{aux}} > V_m$ is satisfied for PFC operation. Fig. 15(a) and (b) shows the deadtimes for an ideal case (no double line frequency voltage), and $C_{o1} = C_{o2} = C_{o3} = 500$ μF. The shift in the computed dead times captures the effect of the variation of output capacitors. An equivalent inductance $L_{eq} = 15$ μF and snubber capacitance $C_{\text{snub}} = 250$ pF are considered for the analysis.

D. Effect of Parasitic Capacitance

Any parasitic capacitance, such as PCB parasitic capacitance C_{par}, across the primary H bridge or transformer intrawinding capacitances C_p, C_s can affect the switching transitions. Here we present the effect of these parasitic capacitors during a type II transition from state 1 to state 2. Fig 16(a) shows the circuit at the start of the transition, where the bridge switches S_2, S_3 are gated OFF, and Fig. 16(b) shows the circuit at the end of mode I of the transition, where the secondary side diodes start to conduct.

It can be observed that the PCB parasitic capacitance C_{par} and the transformer primary intrawinding capacitance C_s, get charged along with the output capacitance of the bridge

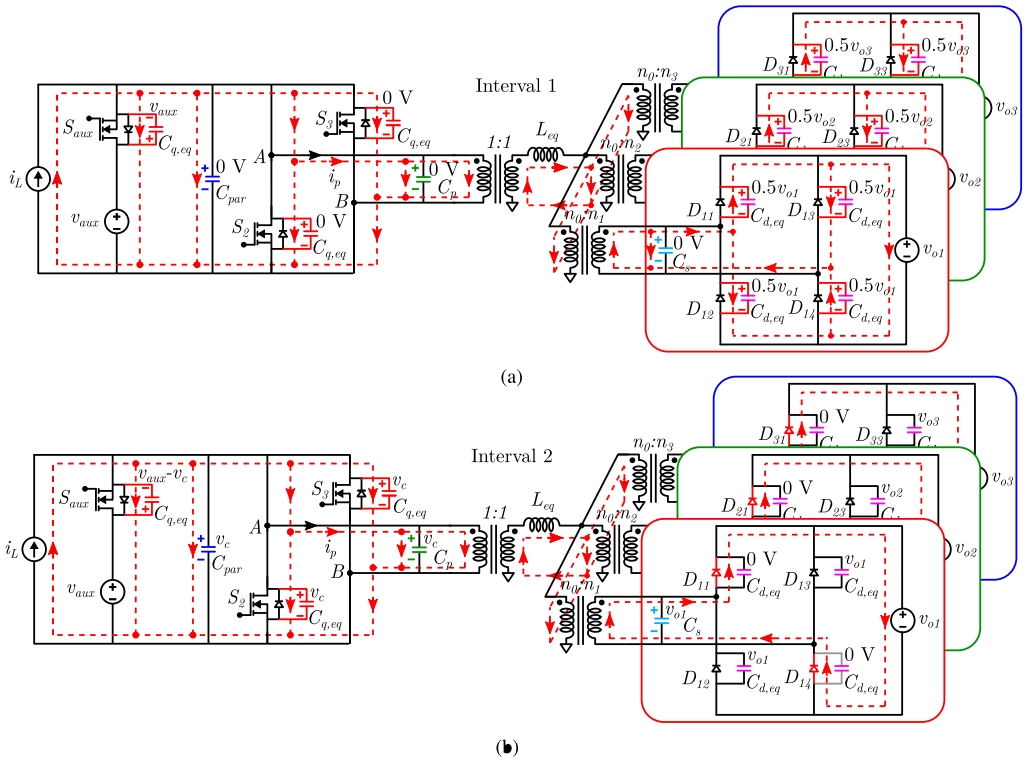


Fig. 16. Circuit during transition type II (state 1 to state 2) (a) during interval 1 and (b) at the end of interval 2.

switches S_2, S_3, while the output capacitance of S_{aux} discharges. Therefore, the effect of these two capacitors is the same as that of adding a distributed snubber capacitor across the switches. Similarly, on the secondary side, the effect is similar to the addition of a snubber capacitor across the diodes. Here, the value of the added capacitor depends on the operating mode and number of bridges participating in the transition, and must be appropriately used while computing the dead time.

To quantify the impact of parasitic capacitances, measurements were performed using an N4L phase-sensitive multimeter with the IAI4 impedance analysis interface. A bare, unpopulated board was used for this purpose. To determine the effective capacitance across each device, the capacitance between the drain and source terminals was measured while shorting the drain-source terminals of the other switch in the same leg. This approach ensures that the measured capacitance reflects the effective value seen during the switching operation, considering the PCB layout and the modulation strategy employed. In addition, the capacitance across the nodes A-B and the transformer primary has also been measured, and the measured values are listed in Table II.

E. Optimal Dead Time Selection

The plot in Fig. 17(a) shows the variation of the dead time bounds for type I transition for output power variation while operating within mode I. The converter specifications and parameters considered are listed in Table III. It can be seen that the ZVS range can be maximized over the fundamental cycle

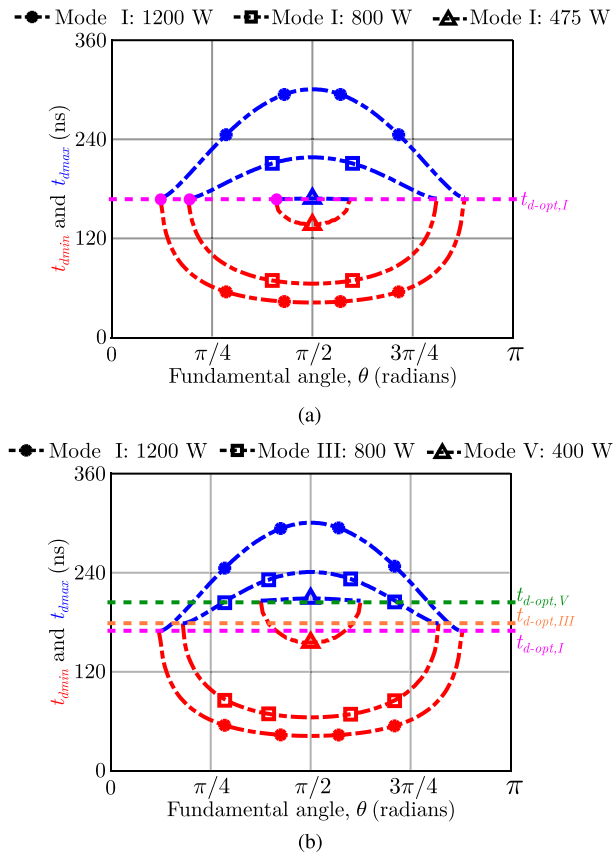


Fig. 17. Transition type I dead time variation for (a) different values of output power and (b) different modes of operation.

TABLE II
PARASITIC CAPACITANCE MEASUREMENTS

Measured across	Value
Drain-source of S_1 (drain-source of S_2 shorted)	173 pF
Drain-source of S_2 (drain-source of S_1 shorted)	168 pF
Drain-source of S_3 (drain-source of S_4 shorted)	172 pF
Drain-source of S_4 (drain-source of S_3 shorted)	167 pF
Drain-source of S_{aux}	157 pF
Nodes A-B (refer Fig. 1)	9 pF
Transformer primary	40 pF

TABLE III
SYSTEM SPECIFICATIONS AND DESIGN PARAMETERS

Specification/Parameter	Value
Grid voltage (RMS), V_g	230 V
Grid frequency	50 Hz
Switching frequency, $f_{S\text{aux}}$	50 kHz
Rated power, P_o	1.2 kW
Rated output voltage, V_o	100 V
PFC inductor, L	3 mH
Auxiliary capacitor, C_{aux}	50 μF
Output capacitors, C_{o1}, C_{o2}, C_{o3}	1500 μF (each)
DC blocking capacitor, C_{dc}	15 μF
Transformer turns ratio, $n_0 : n_1 : n_2 : n_3$	29:8:8:8
Leakage inductance, L_1	40.8 μH
Leakage inductance, L_2	43.2 μH
PCB parasitic capacitance, C_{par}	506 pF
Transformer primary side capacitance, C_p	40 pF

by choosing the dead time $t_{d-opt,I}$, which is the same as the dead time for the limiting case as in (17). It can also be seen that the optimal dead time does not change with power within a given mode. This is because the magnitude of the PFC inductor current i_L at a given fundamental angle reduces with the power reduction. Therefore, it results in a horizontal shrinking of the ZVS range over a fundamental angle. As a limiting case does not exist for type II transitions, the same value of dead time $t_{d-opt,I}$ can be chosen for type II transitions as well.

Fig. 17(b) shows the dead time variation for type I transition for different operating modes I, III, and V. L_{eq} and the operating power change with changes in the operating mode. Therefore, it is recommended that the optimal dead time corresponding to the mode of operation be chosen to extend the ZVS range over a fundamental line cycle. For modes II and IV, it is seen that the value of L_{eq} lies within the values limited by L_{eq} corresponding to modes I, III, and V. Also, it can be seen from Fig. 8 that the value of L_{eq} for modes increases from mode I to V. Choosing a dead time corresponding to a lower value of

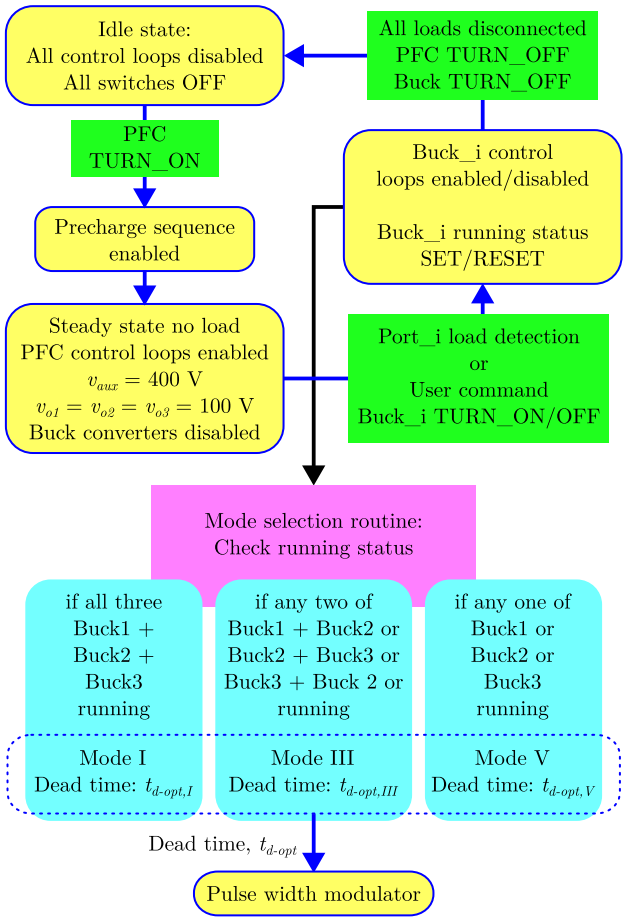


Fig. 18. State machine sequence and mode selection routine.

L_{eq} at the same operating power ensures a wider ZVS range due to the steeper nature of $t_{d-\text{min}}$ curve. Therefore, for mode II operation, $t_{d-\text{opt},I}$ is recommended, and for mode IV operation, $t_{d-\text{opt},III}$ is recommended to extend the ZVS range.

F. Mode Selection Routine

The converter is controlled through a digitally implemented state machine that manages mode transitions based on the real-time connection status of each port. The postregulator stages are turned ON or OFF depending on whether a load is connected at a given port, and this status is tracked using global variables in the embedded software as shown in Fig. 18. Mode changes, such as those caused by dynamic load connection or disconnection, are detected through these variables. As the state machine is executed in each switching cycle, i.e., 20 μs, therefore, the mode changes are detected and the optimal dead time is updated into the pulse width modulation scheme within a switching cycle. During a mode transition, the operating point shifts from one optimal dead-time line to another within a finite time governed by the controller bandwidths or converter ramp sequence. Let us consider a case of sudden port disconnection. For a voltage control loop bandwidth of 10 Hz and an inner current control loop bandwidth of 1 kHz, the mode transition takes around 100 ms, which corresponds to five fundamental cycles as shown

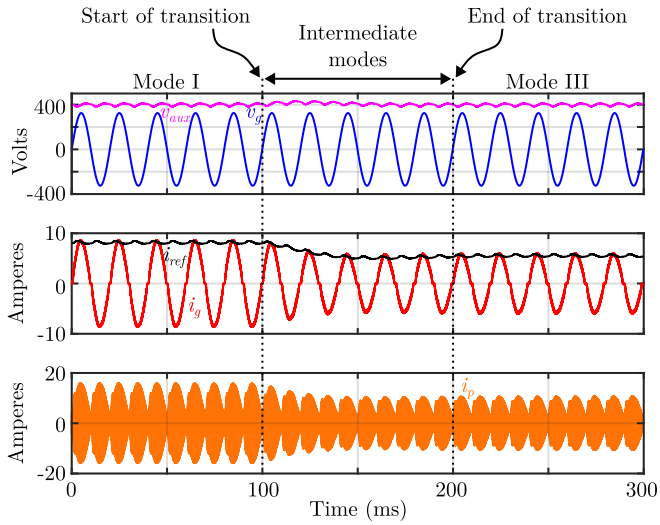


Fig. 19. Simulation results for a sudden port disconnection—transition from Mode I to III.

TABLE IV
OPTIMAL DEAD TIME VARIATION FOR L_{eq} AND C_{SNUB} VARIATION

	Nominal Value	Variation	**% variation**
L_{eq}	13.70 μH	12.33 – 15 μH	$\pm 10\%$
$t_{d,\text{opt}}$	170 ns	161 – 177 ns	$< 6\%$
C_{snub}	182 pF	164 – 200 pF	$\pm 10\%$
$t_{d,\text{opt}}$	170 ns	164 – 175 ns	$< 4\%$

in Fig. 19. Upon detection of a mode change, the optimal dead time is updated within a switching cycle. However, the operating point traverses through multiple intermediate curves, where the ZVS range varies due to changes in both the power and equivalent inductance L_{eq}. Consequently, the updated dead time during the transition may not always be an optimal selection, and the ZVS range may not be maximized during the transition. Nevertheless, the converter still operates in ZVS for some part of the fundamental cycle during the transition. The switching losses arising due to nonoptimal dead time selection during the transition result in negligible additional losses and do not lead to any significant thermal stress. Hence, the converter maintains reliable operation even under dynamic load conditions or mode changes.

G. Impact of Design Tolerances

For a given design, the optimal dead time can vary due to fabrication tolerances in the multiwinding transformer (leading to L_{eq} variations) and the PCB (leading to C_{snub} variations). Table IV lists the optimal dead time variation for $\pm 10\%$ variation in L_{eq} and C_{snub}. Table IV summarizes the variation in optimal dead time for $\pm 10\%$ deviations in L_{eq} and C_{snub}. The results show that the optimal dead time changes by less than 6% for leakage inductance variation and less than 4% for snubber capacitance variation. Furthermore, the ZVS range over the fundamental angle remains largely unaffected within these

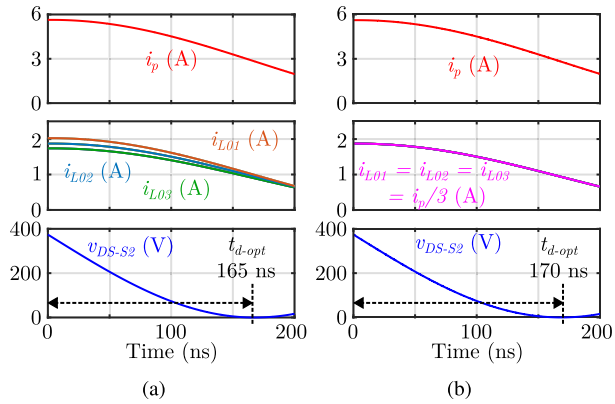


Fig. 20. Results of switching transition with (a) $\pm 10\%$ variations in the inductor values, $L_{01} = 1.1L_{02}$, $L_{03} = 0.9L_{02}$ and (b) symmetric distribution, $L_{01} = L_{02} = L_{03}$.

tolerance limits. The optimal dead time is also insensitive to temperature, since the magnetic core material exhibits negligible temperature dependence in the operating range of interest, and the device output capacitance shows minimal variation with temperature [23], [24].

In practice, minor asymmetries may exist in the transformer construction, resulting in $L_{01} \neq L_{02} \neq L_{03} \neq L_1$ and $L_{12} \neq L_{23} \neq L_{13} \neq L_2$. As long as $L_{01} = L_{02} = L_{03} = L_1$, the voltage drops across them for symmetric loading cases (modes I, III, and V) remain the same. This results in zero voltage drop across L_{12}, L_{23}, L_{13}. Any variations in these inductances will not influence the branch currents, leaving the ZVS analysis unaffected. However, when $L_{01} \neq L_{02} \neq L_{03} \neq L_1$, the current distribution among the branches becomes unequal, leading to multiple distinct slopes in the net primary current during the falling interval. This behavior resembles the unbalanced power condition observed in Modes II and IV as shown in Fig. 8. Circuit simulations show that for a $\pm 10\%$ variation in inductance values, i.e., $L_{01} = 1.1L_{02}$, $L_{03} = 0.9L_{02}$, the optimal dead time changes marginally from 170 ns for symmetric case to 165 ns, which is $< 3\%$ variation as shown in Fig. 20(a) and (b). Larger asymmetries may lead to higher deviations from the analytical model; however, such variations are beyond typical design tolerances. Therefore, within practical design limits, the proposed dead-time selection and ZVS analysis remain valid and effective.

V. RESULTS AND DISCUSSION

A 1.2-kW hardware prototype shown in Fig. 21 has been constructed in the laboratory with the design parameters and specifications listed in Table III. The multiwinding transformer is realized using an E65/32/27 ferrite N87 grade core set from TDK. The PFC inductor is realized using Sendust MKS610125 toroidal cores from Mirrack. Experiments have been carried out in grid-connected mode at 1.2 kW with a resistive load. Fig. 22(a) shows the steady state waveforms of grid voltage v_g, grid current i_g, auxiliary and output capacitor voltages v_{aux} and v_{o1}. The grid current has been shaped into a nearly sinusoidal waveform in

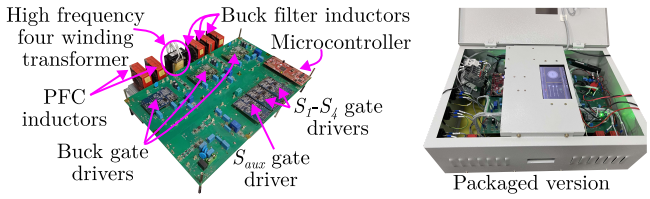


Fig. 21. 1.2 kW hardware prototype of the proposed multiwinding transformer-based multiport isolated AC-DC PFC converter.

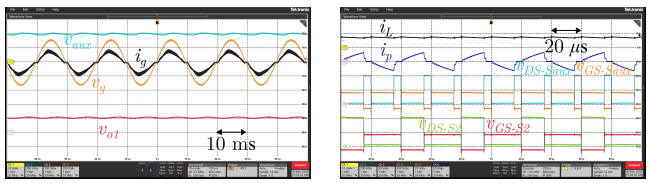


Fig. 22. (a) Experimental waveforms at steady state showing grid voltage v_g [200 V/div], auxiliary capacitor voltage v_{aux} [200 V/div], intermediate dc link voltage v_{o1} [100 V/div], grid current i_g [10 A/div]. (b) PFC inductor current, i_L [10 A/div], transformer primary current, i_p [20 A/div], transformer primary voltage, v_{AB} [500 V/div], gate-source voltages, $v_{GS-S\text{aux}}$, v_{GS-S2} [20 V/div], drain-source voltages, $v_{DS-S\text{aux}}$, v_{DS-S2} [200 V/div], currents, i_L [10 A/div] and i_p [20 A/div].

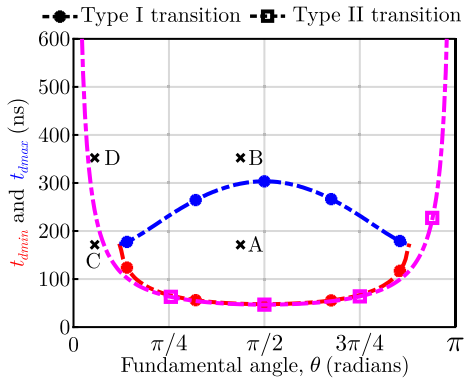


Fig. 23. Operating points and dead times for mode I operation at 1200 W.

phase with grid voltage, while the output voltage is regulated to 100 V. It is seen that the low-frequency harmonics in the grid current are within the permissible limits as defined in the IEC61000-3-2 (A) standard. Fig. 22(b) shows the steady-state high-frequency waveforms from the converter.

In order to validate the analysis, four operating points are selected corresponding to two different fundamental angles and two dead times. Fig. 23 shows the four points: A, B, C, and D, along with the dead time bounds for type I and type II transitions as predicted by the analysis. The dead times have been computed for mode I operation with the system specifications and parameters listed in Table III. From the measured parasitic capacitances in Table II, the resulting snubber capacitance across each device was $C_{\text{snub}} \approx 182$ pF, which was sufficient to ensure zero current turn OFF. Therefore, no additional snubber capacitor has been added in the hardware prototype.

1) A: $i_L = 7$ A at $\theta \approx 72°$ with dead time of 170 ns.

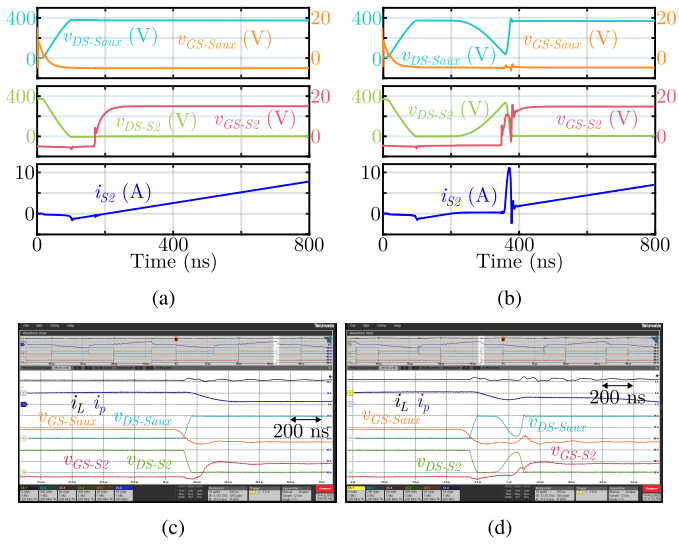


Fig. 24. LTspice simulation results for type I transition showing turn ON of S_2 at: (a) operating point A and (b) operating point B. Experimental results for type I transition corresponding to turn ON of bridge switch, S_2 showing gate-source voltages $v_{GS-S\text{aux}}$, v_{GS-S2} [20 V/div], drain-source voltages, $v_{DS-S\text{aux}}$, v_{DS-S2} [200 V/div], currents, i_L [5 A/div] and i_p [10 A/div] at: (c) operating point A and (d) operating point B.

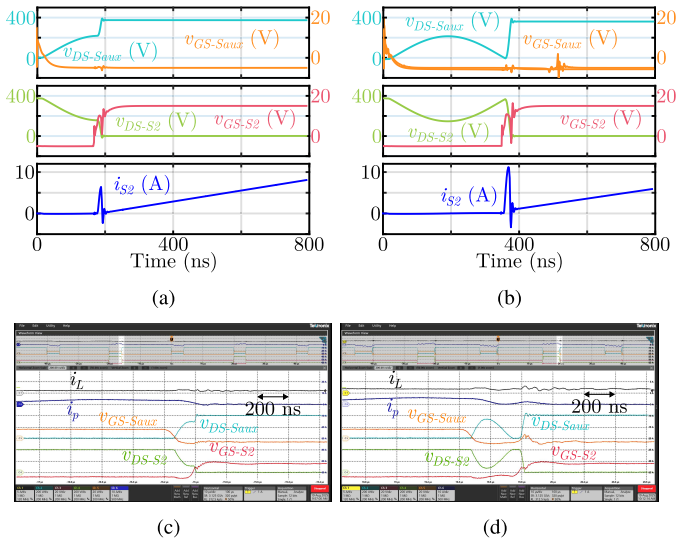


Fig. 25. LTspice simulation results for type I transition showing turn ON of S_2 at: (a) operating point C and (b) operating point D. Experimental results for type I transition corresponding to turn ON of bridge switch, S_2 showing gate-source voltages, $v_{GS-S\text{aux}}$, v_{GS-S2} [20 V/div], drain-source voltages, $v_{DS-S\text{aux}}$, v_{DS-S2} [200 V/div], currents, i_L [5 A/div] and i_p [10 A/div] at: (c) operating point C and (d) operating point D.

2) B: $i_L = 7$ A at $\theta \approx 72°$ with dead time of 350 ns.
3) C: $i_L = 1.5$ A at $\theta \approx 12°$ with dead time of 170 ns.
4) D: $i_L = 1.5$ A at $\theta \approx 12°$ with dead time of 350 ns.

Figs. 24 and 25 show the waveforms for type I transition, where turn ON of S_2 is under consideration. Fig. 24(a) and (b) shows the simulation results to capture the impact of dead time variation for transition type I for operating points A and B, respectively. Here, for point B exceeding the maximum permissible dead time results in a hard switching transition. The

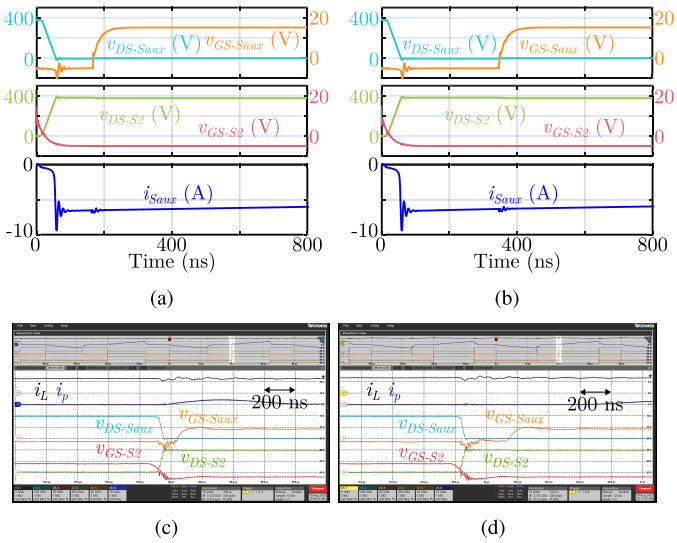


Fig. 26. LTspice simulation results for transition type II showing turn ON of S_{aux} at: (a) operating point A (b) operating point B. Experimental results for type II transition corresponding to turn-ON of auxiliary switch, S_{aux} showing gate-source voltages, $v_{GS-S\text{aux}}$, v_{GS-S2} [20V/div], drain-source voltages, $v_{DS-S\text{aux}}$, v_{DS-S2} [200V/div], currents, i_L [5A/div] and i_p [10A/div] at: (a) operating point A (b) operating point B.

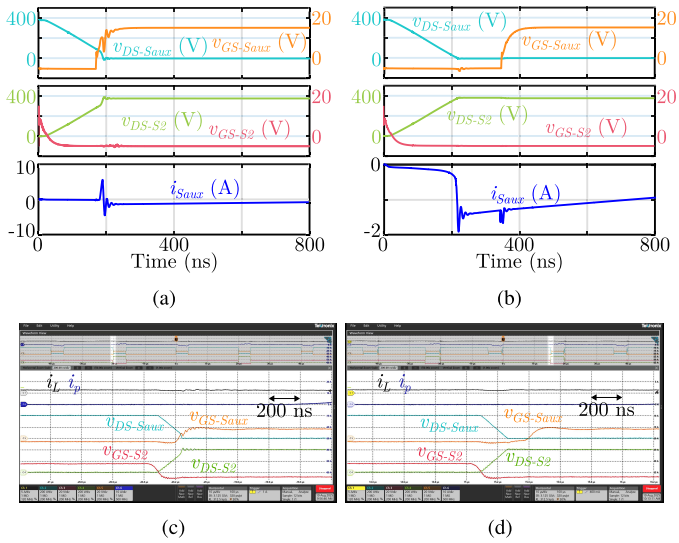


Fig. 27. LTspice simulation results for transition type II showing turn ON of S_{aux} at: (a) operating point C (b) operating point D. Experimental results for type II transition corresponding to turn ON of auxiliary switch, S_{aux} showing gate-source voltages, $v_{GS-S\text{aux}}$, v_{GS-S2} [20 V/div], drain-source voltages, $v_{DS-S\text{aux}}$, v_{DS-S2} [200 V/div], currents, i_L [5 A/div] and i_p [10 A/div] at: (c) operating point C (d) operating point D.

same is validated experimentally as shown in Fig. 24(c) and (d). Fig. 25 shows the simulation and experimental results for type I transition for points C and D. Here, there is no feasible dead time for which S_2 undergoes soft turn ON, as predicted by the analysis.

Unlike transition type I, the maximum permissible dead time for soft turn ON of S_{aux} is in the range of microseconds. This is shown in the simulation results, Fig. 26(a) and (b), where choosing a 350 ns dead time also results in a soft turn ON (point B). The same is validated experimentally as shown in Fig. 26(c) and (d). Also, for transition type II, a minimum dead time exists as compared to transition type I. Fig. 27(a) and (b) show the simulated waveforms where choosing 170 ns dead time results in a partial hard turn ON. Fig. 27(c) and (d) shows the experimental validation for the same. This corresponds to point C lying just outside the ZVS range, while point D lies within the ZVS range for the type II transition.

The analysis and results presented were with identical gate driving circuits for all switches. A mismatch, such as an additional capacitance across the gate-source terminals of S_2 slows the rate of rise and fall of v_{GS-S2} compared to v_{GS-S3} (for transition type II). As a result, the rise of drain-source voltages across the switches is governed by the switch with slower gate driving, affecting the discharging of the capacitor across S_{aux}. This leads to a reduction in the actual dead time that gets implemented between the turn-OFF of $S_2 - S_3$ and the turn ON of S_{aux}. This is captured in the experimental waveforms in Fig. 28(a) and (b), where an extra capacitor is added across gate-source terminals of S_2.

The analytically obtained loss distributions for mode I operation for rated power of 1200 W and different dead times are shown in Fig. 29. At rated power of 1200 W, the analytical

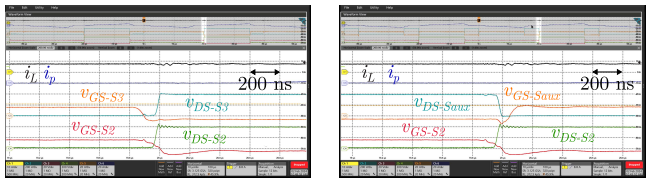


Fig. 28. Experimental waveforms of (a) gate-source voltages, v_{GS-S2}, v_{GS-S3} [20 V/div], drain-source voltages, v_{DS-S2}, v_{DS-S3} [200 V/div] and (b) gate-source voltages, v_{GS-S2}, $v_{GS-S\text{aux}}$ [20 V/div], drain-source voltages, v_{DS-S2}, $v_{DS-S\text{aux}}$ [200 V/div], and currents, i_L [10 A/div], i_p [20 A/div].

loss distribution with different dead times shows that selecting the optimal dead time, $t_{d,opt} = 170$ ns, yields an efficiency of 94.39% , compared to 94.01% with nonoptimal dead time ($t_d = 350$ ns). This corresponds to a 0.38% improvement, or 4.6 W of reduced losses, attributed to soft-switching. Similarly, at 800 W, the benefit from optimal dead time is 0.4% . From the analytical loss split, it is evident that conduction losses dominate in the present design, with the secondary-side diode bridges alone accounting for nearly 36% of total conduction losses. Moreover, the present prototype employs enamelled copper windings (17.5 SWG and 20 SWG) for the multiwinding transformer and PFC inductor, which contribute to higher conduction loss. Replacing these with Litz wires would reduce conduction losses further, thereby increasing the relative share of switching losses. Hence, the efficiency gains from ZVS are expected to be much more significant in conduction-loss-optimized converters operating at higher switching frequencies, as well as in legacy Silicon MOSFET/IGBT-based designs, where switching losses increase more steeply. Under such conditions, the proposed methodology for optimal dead time selection and ZVS extension becomes essential for achieving higher efficiency.

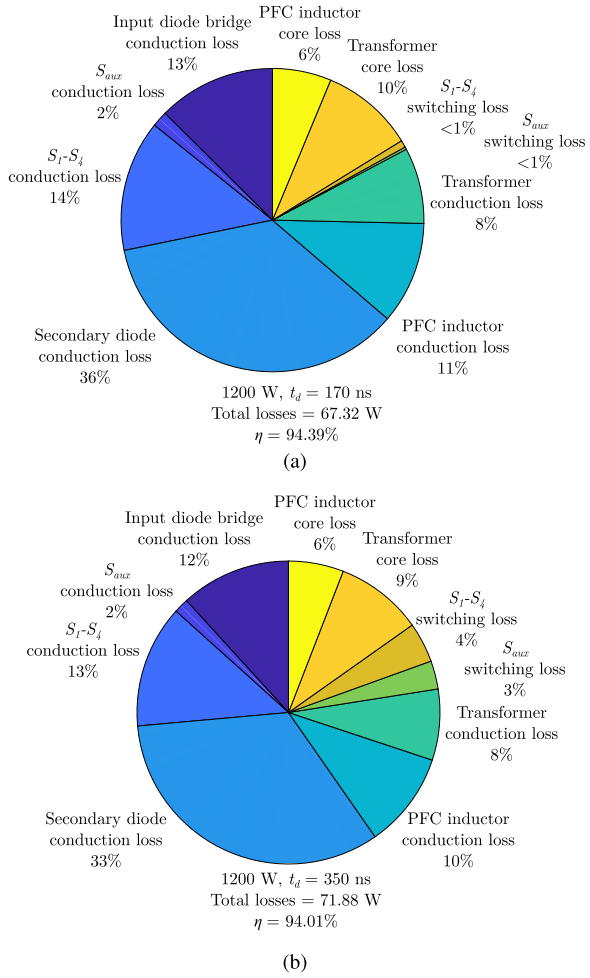


Fig. 29. Analytical loss distribution for mode I operation at 1200 W (a) $t_d = 170$ ns and (b) $t_d = 350$ ns.

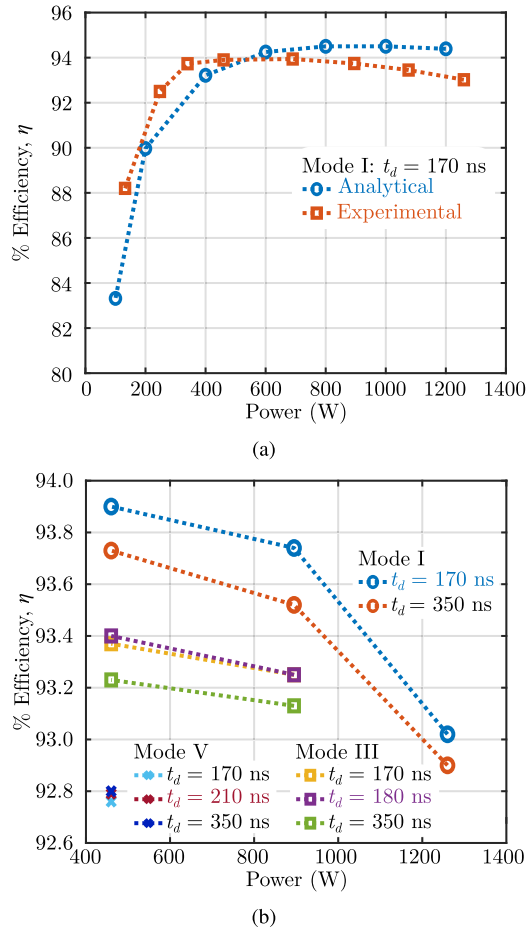


Fig. 30. (a) Analytical versus experimental efficiency for mode I operation with $t_d = 170$ ns. (b) Experimental efficiencies for various modes with different choices of dead time and optimal dead times highlighted.

The validity of the analytical loss model is verified by comparing it against the experimental efficiency as shown in Fig. 30(a). The analytical efficiency trends match closely with the experimental values. The analytical loss model does not account for losses in relays, connectors, and cables, which contribute to higher conduction losses at higher powers; therefore, there is a slight discrepancy between the analytical and experimental efficiency plots.

Experimental validation supports this trend, with measured improvements of 0.17% at 1200 W and 0.22% at 895 W for mode I as shown in Fig. 30(b). The difference between analytical and experimental gains is explained by the fact that the analytical model assumes complete hard-switching in the nonoptimal case, when a dead time higher than $t_{d-\max}$ is used. Whereas in practice, choosing a dead time higher than $t_{d-\max}$ results in partial hard switching, where the switching losses are smaller than the complete hard switching case as considered in the analysis. Thus, it is consistent with the conduction loss-dominated nature of the current prototype and confirms that ZVS range is indeed extended. Fig. 30(b) also shows the efficiency improvements by optimal choice of dead times (highlighted) for modes III and V.

VI. Conclusion

In this article, a circuit-theoretic methodology was presented to analyze a multiwinding transformer-based multiport ac–dc PFC converter proposed for EV charging applications. As the energy stored in the leakage fields plays a critical role in enabling soft-switching, the modeling of multiwinding transformers becomes essential. Conventional approaches, such as the ECM though physically intuitive, become excessively complex when applied to multiwinding transformers with more than three windings. To overcome this challenge, a systematic simplification of the ECM was proposed, wherein topological and operational symmetries of the converter arising from the trifilar winding configuration were exploited. As a result, a unified equivalent transformer model valid across varying operating modes and load conditions was derived.

Based on the simplified model, a soft-switching analysis was carried out, and expressions for the minimum and maximum permissible dead times required for achieving zero-voltage turn ON were derived. The analysis accounts for converter design parameters, circuit parasitics, operating modes, and load variations. It was demonstrated that the zero-voltage turn ON range can be extended over a fundamental line cycle through the

optimal selection of dead time, and the resulting improvements in the efficiency have been quantified. The analytical results were validated through circuit simulations conducted in LTspice using manufacturer-level device models, and experimental verification was provided using a 1.2-kW hardware prototype. In addition, the effects of mismatches in the gate driving circuitry on soft-switching performance were investigated through experimental measurements. The presented methodology is applicable to analyze a broader range of multiwinding transformer-based converters and a wide class of current-fed full-bridge converters with active clamp configurations.

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Himanshu Bhusan Sandhibigraha (Graduate Student Member, IEEE) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology (Indian School of Mines), Dhanbad, India, in 2020. He is currently working toward the doctoral degree with the Department of Electrical Engineering, Indian Institute of Science, Bengaluru, India.

He is a Prime Minister Research Fellow. His research interests include reconfigurable ac–dc converters, multiport power converters, soft-switching strategies, power electronic converter modeling, and control.

Vishnu Mahadeva Iyer (Senior Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from the College of Engineering, Trivandrum, India, in 2011, the M.E. degree in electrical engineering from the Indian Institute of Science, Bengaluru, India, in 2013, and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 2020.

He was a Research Engineer with GE Research, Bengaluru, in 2015, and a Lead Engineer with GE Research, Niskayuna, USA, 2020. Since September 2020, he has been an Assistant Professor with the Department of Electrical Engineering at IISc, Bengaluru. His research interests include resonant and soft-switched converters, high-frequency magnetics, stability and control of power converters, and partial power processing.