Three-Level Optimized Pulse Patterns With Bounded Junction Temperature and Relaxed Properties

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***Abstract*—This article proposes the computation of three-level optimized pulse patterns (OPPs) that ensure the safe operation of the semiconductor devices, thereby enabling the full utilization of the converter capabilities. To achieve this, the junction temperature of the semiconductor devices is directly bounded in the proposed OPP optimization problem. In addition, the symmetry properties of the OPPs are relaxed, and multipolar switch positions are allowed to facilitate the redistribution of the thermal stress among the semiconductor devices. This way, the junction temperature requirements can be met without significantly deteriorating the output current ripple. Nevertheless, computing OPPs with relaxed properties can be computationally challenging. To address this, a computationally efficient method based on the concept of virtual angles is employed to render the computation of such OPPs possible. The presented numerical results for medium-voltage drives, consisting of a neutral-point-clamped converter and either an induction machine or an externally excited synchronous machine, demonstrate the benefits of the proposed approach.**

***Index Terms*—Multilevel converters, optimal modulation, power losses, pulsewidth modulation (PWM), reliability, thermal stress.**

I. Introduction

THE semiconductor devices are the most expensive and vulnerable components in high-power electronics [1]. To ensure operation within their safe operating area, the maximum junction temperature limit defined by the manufacturers should always be respected. By guaranteeing safe and reliable operation close to the thermal limits, the instantaneous converter capability can be fully utilized [2], [3].

The junction temperature is typically controlled by manipulating the switching losses. This can be done, e.g., by using adaptive gate drivers that adjust the gate resistance [4], by manipulating the dc voltage [5], or through advanced control and modulation methods.

Different control strategies that directly or indirectly account for the thermal stress of the semiconductor devices have been investigated. For example, the authors in [6] and [7] decreased the switching losses by manipulating the switching frequency using a hysteresis controller and a region-based control method, respectively. More versatile control techniques, such as model predictive control (MPC), can be designed to account for the thermal stress in the objective function of the MPC problem, as shown in [8] and [9], for two-level and three-level converters, respectively. This equips the control scheme with degrees of freedom that enable the adjustment of the tradeoff between current harmonic distortions and thermal performance [10]. For example, Han et al. [11] selected the switching frequency of modulated MPC by considering the tradeoff between the junction temperature swing and the total demand distortion (TDD) of the output current. In [12], the weighting factor that adjusts the tradeoff between electrical and thermal performance of MPC was dynamically adjusted. Finally, the junction temperature reference was designed in [13] by considering the impact of the thermal control on the remaining lifetime of the devices.

Nevertheless, considering the losses in the modulation stage can improve the aforementioned tradeoff. Specifically, the losses can be reduced either by lowering the switching frequency or by employing discontinuous pulsewidth modulation (DPWM) [14]. The level of reduction of the switching frequency can be selected by assessing the ratio between the expected lifetime extension and current TDD deterioration [15]. Regarding DPWM, its thermal performance depends on the timing and duration of phase clamping within the fundamental period [16]. Therefore, by appropriately adjusting them, the switching losses can be kept below a specific bound [17].

A reduction in switching frequency or the use of DPWM, however, results in degraded output current quality. Thus, to improve the tradeoff between output current quality and reliability, Ugur et al. [18] proposed to employ DPWM only when the devices reach a critical end-of-life threshold. To partially mitigate the output current quality deterioration, the authors in [19] and [20] applied DPWM during only a portion of the fundamental period to target solely the most aged device. Similarly, the authors in [21] and [22] proposed using DPWM exclusively on the most aged phase leg.

As an alternative to DPWM, specialized modulation techniques can also be employed to reduce the junction temperature of the most stressed device. For example, when three-level converters are considered, multipolar patterns can be used to redistribute the losses across the devices—at the expense, however, of increased load current TDD, as shown in [23], [24], and [25],

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for low, medium, and high modulation indexes, respectively. Alternatively, carrier-based PWM with zero-sequence voltage injection can also be utilized to shift the losses from the most stressed device to the rest [26].

However, when high-power applications are of interest, as in this work, the tradeoff between the output current quality and the thermal stress of the semiconductor devices produced with the discussed methods can be particularly poor. To achieve a favorable balance between current quality and thermal stress, optimized pulse patterns (OPPs) can be considered, since they achieve low harmonic distortions at low switching-to-fundamental frequency ratios [27]. Moreover, the switching losses produced by OPPs can be further reduced by explicitly accounting for them in the OPP optimization problem. In this direction, Geyer et al. [28] modified the OPP problem to keep the switching power losses bounded while still producing currents of high quality. To enable this favorable tradeoff between losses and current quality, that work adopted the OPP symmetry relaxations proposed in [29]. In doing so, the search space of the optimization problem increased, thus allowing for more degrees of freedom during the OPP computation process. By exploiting this feature, the robustness of such loss-bounded OPPs to changes in the power factor can also be improved [30].

Nevertheless, since the switching losses are merely a proxy for the junction temperatures, it is more beneficial to formulate the OPP problem to directly account for them. To this end, the computation of OPPs for a three-level neutral-point-clamped (NPC) converter with explicit bounds on the junction temperature was proposed in [31]. In that work, however, only unipolar OPPs were considered, which limited the number of candidate solutions, resulting in underutilization of the thermal capacity of the converter at fundamental frequencies lower than the nominal. Multipolar patterns, on the other hand, enable a more effective redistribution of the losses among the switching devices, while they can also have a positive impact on the performance of OPPs, as demonstrated in [29]. Motivated by these observations, Koukoula et al. [32] extended this concept by adopting multipolar switching sequences to effectively relieve the most thermally stressed devices over a wider range of operating points, while still improving the tradeoff between the junction temperature and the output current TDD.

However, allowing for multipolar switching sequences results in an exponential increase in the number of candidate sequences as the ratio between fundamental and switching frequency, i.e., the pulse number, increases. Hence, exhaustively enumerating all available sequences and solving an optimization problem for each one of them would result in prohibitively high computational times. To tackle this challenge, Koukoula et al. [32] reformulated the OPP problem using the concept of virtual angles, initially presented in [33] and later adapted for OPP computation in [34]. By combining the information of switching angles and corresponding switching transitions into one optimization variable, the iteration over all candidate sequences was avoided, thus significantly alleviating the required computational time.

This article expands upon the work in [32] by advancing both the formulation and the practical applicability of the proposed thermally constrained OPPs. First, the formulation of the thermally constrained OPP optimization problem and the solution procedure are rigorously presented, addressing aspects that were only briefly outlined in [32]. Second, the postprocessing step that guarantees a minimum pulse width as well as the procedure for deciding the optimal OPP pulse number are systematically established. Third, the proposed modulation strategy is validated through extensive numerical studies on different medium-voltage (MV) drive systems, clearly demonstrating its capability to operate the converter semiconductor devices close to their thermal limits over a wide range of operating points, while achieving very low current TDD values. Finally, by accounting for the dependency of the junction temperature on the power factor, the robustness concept—initially developed for loss-constrained OPPs in [30]—is adapted to the proposed thermally constrained OPPs through an appropriate modification of the optimization problem. Thanks to this feature, the proposed OPPs maintain the junction temperature below its upper limit across the whole range of examined operating points.

The rest of this article is organized as follows. Section II presents the conventional three-level OPP optimization problem. The computation of the junction temperature, along with the proposed optimal modulation strategy adopted to limit it, is explained in detail in Section III. Section IV provides numerical results across a broad range of operating points and conditions, and examines the robustness of the proposed method to load variations. Finally, Section V concludes this article.

II. Conventional Three-Level OPPs

A 2π-periodic switching signal $u(\theta)$ with $4d$ switching events per fundamental period results in an average device switching frequency $f_{\text{sw}} = df_1$, where f_1 is the fundamental frequency. Therefore, by defining the pulse number as $d = \frac{f_{\text{sw}}}{f_1}$, the switching signal u is characterized by $4d+1$ switch positions $u_j \in \{-1, 0, 1\}$, $j \in \{0, \ldots, 4d\}$, and $4d$ switching angles α_i, $i \in \{1, \ldots, 4d\}$, at which a switching transition $\Delta u_i = u_i - u_{i-1} \in \{-1, 1\}$ occurs. For the computation of the OPP, i.e., the $4d+1$ switch positions and $4d$ switching angles, that produces the lowest current harmonic distortion, an objective function that captures the load current TDD I_{TDD} is formulated. Note that the latter is proportional to the weighted sum of the amplitude of the switching harmonics $\hat{u}_n = \sqrt{a_n^2 + b_n^2}$ when an inductive load is assumed, where a_n and b_n are the Fourier coefficients of the nth OPP harmonic. For an analytical derivation of the current TDD expression see [29].

Conventional OPPs assume three-phase symmetry, quarter- and half-wave symmetry (QaHWS), and unipolar switching while the initial switch position is zero. Therefore, they can be fully described with only d switching angles occurring in the first quarter of the fundamental period, i.e., $\boldsymbol{\alpha} \equiv \boldsymbol{\alpha}_Q = [\alpha_1\ \alpha_2\ \ldots\ \alpha_d]^T \in [0, \pi/2]^d$ with $\alpha_i < \alpha_{i+1}$, $i \in \{1, \ldots, d-1\}$, while the switch positions are deterministic. Consequently, the optimization problem to compute such OPPs is

$$\begin{aligned} \underset{\boldsymbol{\alpha}_Q}{\text{minimize}} \quad & J(\boldsymbol{\alpha}_Q) = \sum_{n=5,7,\ldots} \left(\frac{b_n(\boldsymbol{\alpha}_Q)}{n} \right)^2 \\ \text{subject to} \quad & b_1(\boldsymbol{\alpha}_Q) = m \\ & 0 \leq \alpha_1 < \alpha_2 < \ldots < \alpha_d \leq \frac{\pi}{2} \end{aligned} \tag{1}$$

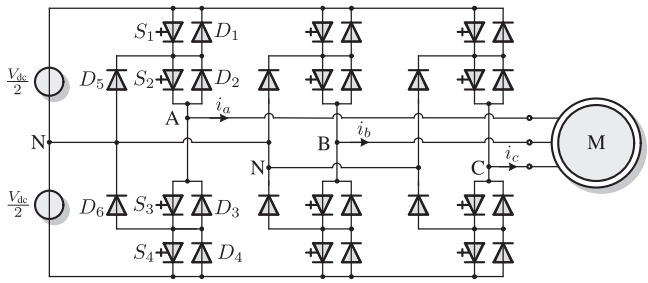

Fig. 1. Three-level NPC converter driving a machine.

TABLE I
SEMICONDUCTOR DEVICE PARAMETERS

GCT 5SHY 55L4500		
Turn-on losses	e_{on}	1.8 J
Turn-off losses	e_{off}	26.5 J
GCT coefficient	a_{GCT}	1.12 V
GCT coefficient	b_{GCT}	$0.26 \cdot 10^{-3}$ V/A
Max. junction temp.	$T_{\text{j,max}}$	125°C
Thermal resistances	R_{1-6}	5.56, 1.53, 0.87, 0.55, 7.0, 2.4 K/kW
Time constants	τ_{1-6}	512, 89.6, 9.1, 2.4, 9000, 3000 ms
Diode 5SDF 20L4520		
Reverse recov. losses	e_{rr}	13.9 J
Diode coefficient	a_{diode}	1.7 V
Diode coefficient	b_{diode}	$0.8 \cdot 10^{-3}$ V/A
Max. junction temp.	$T_{\text{j,max}}$	135°C
Thermal resistances	R_{1-6}	3.71, 1.43, 0.69, 0.18, 2.5, 10.4 K/kW
Time constants	τ_{1-6}	534, 67.0, 7.4, 1.1, 4000, 8000 ms

where $m \in [0, 4/\pi]$ is the desired modulation index, and b_n are the nonzero Fourier coefficients of the OPP given by

$$b_n = \frac{4}{n\pi} \sum_{i=1}^{d} \Delta u_i \cos(n\alpha_i), \quad n = 1, 3, 5, \ldots .$$

Note that the a_n Fourier coefficients and even harmonics are zero due to the QaHWS, while triplen harmonics do not drive harmonic current when a load in Wye configuration with a floating star point is assumed.

III. THERMALLY CONSTRAINED THREE-LEVEL OPPS

A. Junction Temperature Calculation for an NPC Converter

A three-level NPC converter with a machine is shown in Fig. 1. In each phase, there are four active switches S_1 to S_4 with their respective freewheeling diodes D_1 to D_4, and two clamping diodes D_5 and D_6. In this work, the semiconductor devices used are the 5SHY 55L4500 integrated-gate-commutated thyristor (IGCT) [35] and the 5SDF 20L4520 diode [36]. The parameters of the semiconductor devices at rated maximum values of anode–cathode voltage $v_T = 2.8$ kV and anode current $i_T = 4$ kA assuming the maximum allowed junction temperature are given in Table I.[1]

[1]The power losses depend on the junction temperature. When the goal is to guarantee operation within the safe operating area regarding the junction temperature, it is preferable to calculate the power losses assuming the maximum allowable junction temperature, ensuring accuracy under these critical conditions. At lower junction temperatures, this approach overestimates the losses, resulting in higher junction temperature values; however, this has no impact when the focus is on safe operation.

TABLE II
CONDUCTION ENERGY LOSSES IN AN NPC PHASE LEG

Polarity of phase current	Switch position	Conduction energy losses
> 0	1	$e_{\text{con},S_1} + e_{\text{con},S_2}$
	0	$e_{\text{con},S_2} + e_{\text{con},D_5}$
	-1	$e_{\text{con},D_3} + e_{\text{con},D_4}$
< 0	1	$e_{\text{con},D_1} + e_{\text{con},D_2}$
	0	$e_{\text{con},S_3} + e_{\text{con},D_6}$
	-1	$e_{\text{con},S_3} + e_{\text{con},S_4}$

TABLE III
SWITCHING ENERGY LOSSES IN AN NPC PHASE LEG

Polarity of phase current	Switching transition	Switching energy losses
> 0	$0 \to 1$	$e_{\text{on},S_1} + e_{\text{rr},D_5}$
	$1 \to 0$	e_{off,S_1}
	$0 \to -1$	e_{off,S_2}
	$-1 \to 0$	$e_{\text{on},S_2} + e_{\text{rr},D_4}$
< 0	$0 \to 1$	e_{off,S_3}
	$1 \to 0$	$e_{\text{on},S_3} + e_{\text{rr},D_1}$
	$0 \to -1$	$e_{\text{on},S_4} + e_{\text{rr},D_6}$
	$-1 \to 0$	e_{off,S_4}

For a given OPP, the junction temperature of each semiconductor device can be derived from the instantaneous power losses of the device. Due to the three-phase symmetry of the OPP, it suffices to do so in only one phase leg of the NPC converter. In addition, to simplify the computation of the power losses of the semiconductor devices, the total dc-link voltage V_{dc} is assumed constant, and the fluctuations of the neutral-point potential small. As a result, the blocking voltage of each semiconductor device is half the dc-link voltage $v_T = \frac{V_{\text{dc}}}{2}$, and the losses depend only on the instantaneous value of the commutated current. The latter is considered sinusoidal with frequency f_1, i.e., $i(t) = I \sin(2\pi f_1 t - \phi)$, where I is the amplitude of the current and ϕ the angular displacement between the phase current and voltage. Thus, the instantaneous power losses p_{loss} at angle θ are a function of the displacement angle ϕ and can be computed based on the applied OPP as follows.

At each angle θ the devices that conduct the current are determined based on the applied switch position and the polarity of the commutated current, see Table II. Similarly, the devices that produce switching losses at each switching angle α_i are identified based on the polarity of the phase current and the switching transition using Table III. In Tables II and III, $e_{\text{on}}/e_{\text{off}}$ denote the turn-ON/OFF energy losses of the IGCTs, e_{rr} the reverse recovery energy losses of the diodes, while e_{con} are the conduction energy losses.[2]

[2]The detailed computation of the losses was provided in [28] and [30].

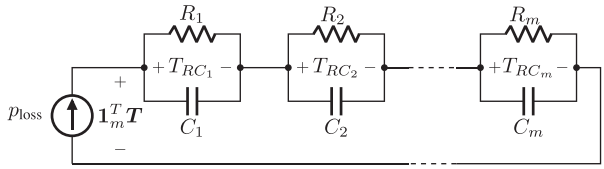

Fig. 2. Foster model of the mth order.

The junction temperature is then computed using the mth-order Foster model (see Fig. 2), where m RC-networks represent the heat transfer path from the junction through the case to the cooling water. In the frequency domain, the junction temperature is given by

$$T_{\text{j}}(s,\phi) = P_{\text{loss}}(s,\phi)\cdot Z_{\text{th}}(s) + T_{\text{w}} \tag{2}$$

where P_{loss} are the instantaneous power losses in the frequency domain, T_{w} is the temperature of the cooling water, and

$$Z_{\text{th}}(s) = \sum_{k=1}^{m} \frac{R_k}{\tau_k s + 1} \tag{3}$$

is the transient thermal resistance with time constant τ_k of the kth RC-network being $\tau_k = R_k C_k$, with $k = 1, 2, \ldots, m$.

In the time domain, the junction temperature T_{j} can be computed with the following system of differential equations

$$\frac{\mathrm{d}\boldsymbol{T}(\theta,\phi)}{\mathrm{d}\theta} = \boldsymbol{F}\boldsymbol{T}(\theta,\phi) + \boldsymbol{G}p_{\text{loss}}(\theta,\phi) \tag{4a}$$

$$T_{\text{j}}(\theta,\phi) = \mathbf{1}_m^T\boldsymbol{T}(\theta,\phi) + T_{\text{w}} \tag{4b}$$

where $\boldsymbol{T} = [T_{RC_1}\ T_{RC_2}\ \ldots\ T_{RC_m}]^T$ is the vector of temperatures T_{RC_k} of the RC-networks, with $k = 1, 2, \ldots, m$, and $\mathbf{1}_m$ is an m-dimensional vector of ones. Finally, the system matrix $\boldsymbol{F}$ and output vector $\boldsymbol{G}$ are

$$\boldsymbol{F} = \begin{bmatrix} -\frac{1}{\tau_1} & 0 & \ldots & 0 \\ 0 & -\frac{1}{\tau_2} & & \vdots \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \ldots & -\frac{1}{\tau_m} \end{bmatrix} \frac{1}{\omega_1}, \text{ and } \boldsymbol{G} = \begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots \\ \frac{1}{C_m} \end{bmatrix} \frac{1}{\omega_1}$$

where ω_1 is the fundamental angular frequency of the OPP.

As shown in [31], the instantaneous value of the temperatures at angle θ can be found by integrating (4a), yielding

$$\boldsymbol{T}(\theta,\phi) = \mathbf{e}^{\boldsymbol{F}\theta}\boldsymbol{T}(0,\phi) + \int_0^{\theta} \mathbf{e}^{\boldsymbol{F}(\theta-\vartheta)}\boldsymbol{G}p_{\text{loss}}(\vartheta,\phi)\,\mathrm{d}\vartheta \tag{5}$$

where $\mathbf{e}$ is the matrix exponential. Due to the 2π-periodicity of the applied OPP, the temperature is also 2π-periodic. Therefore, the initial temperatures $\boldsymbol{T}(0,\phi)$ are given by

$$\boldsymbol{T}(0,\phi) = \left(\boldsymbol{I}_m - \mathbf{e}^{\boldsymbol{F}2\pi}\right)^{-1} \int_0^{2\pi} \mathbf{e}^{\boldsymbol{F}(\theta-\vartheta)}\boldsymbol{G}p_{\text{loss}}(\vartheta,\phi)\,\mathrm{d}\vartheta$$

where $\boldsymbol{I}_m$ is the identity matrix of size m.

Hence, based on the above, the instantaneous junction temperature T_{j} of each device can be expressed as a function of the applied OPP, phase current, and displacement angle ϕ. Therefore, as shown in [31], it can be directly constrained in the OPP optimization problem, as explained in the sequel of this section.

B. Symmetry-Relaxed OPP Problem to Limit the Junction Temperature

Due to the half-wave symmetry (HWS) of OPPs, the devices in the pairs $\{S_1, S_4\}$, $\{D_1, D_4\}$, $\{S_2, S_3\}$, $\{D_2, D_3\}$, and $\{D_5, D_6\}$ have the same losses (see also [28]), and consequently the same junction temperature. Hence, it suffices to constrain the junction temperature of the five semiconductor devices in the upper half of one NPC leg, namely S_1, S_2, D_1, D_2, and D_5. To limit the maximum instantaneous value of the junction temperature of all devices,[3] the constraint

$$T^{\ell}_{\text{j,max}}(\boldsymbol{\alpha},\phi) \le T^{\ell}_{\text{j,lmt}}\ \forall \ell \in \{S_{1,2}, D_{1,2,5}\} \tag{6}$$

is added to optimization problem (1), where $T^{\ell}_{\text{j,lmt}}$ is 125 °C and 135 °C for the IGCTs and diodes, respectively, used in this work. It should be pointed out that, due to the high switching losses of the selected devices, the maximum junction temperature usually occurs after a switching transition. Therefore, the maximum junction temperature $T^{\ell}_{\text{j,max}}$ of each device is assumed to be

$$T^{\ell}_{\text{j,max}}(\boldsymbol{\alpha},\phi) = \max\{T^{\ell}_{\text{j}}(\alpha_i,\phi)\}, i \in \{1,\ldots,4d\} \tag{7}$$

and it is a function of the applied OPP, phase current, and displacement angle ϕ.

OPPs that are computed based on the revised OPP problem—i.e., problem (1) with constraint (6)—can guarantee that the junction temperature remains within the desired limits. Nevertheless, in doing so, the quality of the current TDD is compromised since a tradeoff between T_{j} and I_{TDD} arises. As shown in [31], this tradeoff can be improved by relaxing the symmetry of the OPP and allowing for HWS. This relaxation allows for a more flexible distribution of the switching angles over the half-period. As a result, the increased harmonic distortions caused by additional constraints in the optimization problem can be mitigated, thus enabling an improved I_{TDD}–T_{j} tradeoff.

With the above relaxation, the $2d$ switching angles occurring in the first half of the fundamental period $\boldsymbol{\alpha} \equiv \boldsymbol{\alpha}_H = [\alpha_1\ \alpha_2\ \ldots\ \alpha_{2d}]^T \in [0,\pi]^{2d}$ are needed to fully describe $u(\theta)$. As a result, the optimization problem that accounts for the thermal constraints is revised to the following form [31]:

$$\begin{aligned} \underset{\boldsymbol{\alpha}_H}{\text{minimize}}\quad & J(\boldsymbol{\alpha}_H) = \sum_{n=5,7,11,\ldots} \frac{a_n^2(\boldsymbol{\alpha}_H) + b_n^2(\boldsymbol{\alpha}_H)}{n^2} \\ \text{subject to}\quad & a_1(\boldsymbol{\alpha}_H) = 0,\ b_1(\boldsymbol{\alpha}_H) = m \\ & 0 \le \alpha_1 < \alpha_2 < \ldots < \alpha_{2d} \le \pi \\ & T^{\ell}_{\text{j,max}}(\boldsymbol{\alpha}_H,\phi) \le T^{\ell}_{\text{j,lmt}}\ \forall \ell \in \{S_{1,2}, D_{1,2,5}\} \end{aligned} \tag{8}$$

[3]The junction temperature corresponds to the average temperature across the chip area, under the assumption of a uniform temperature distribution.

where the nonzero a_n and b_n Fourier coefficients are

$$a_n = -\frac{2}{n\pi}\sum_{i=1}^{2d}\Delta u_i \sin(n\alpha_i)\,, \qquad n = 1,3,5,\dots$$

$$b_n = \frac{2}{n\pi}\sum_{i=1}^{2d}\Delta u_i \cos(n\alpha_i)\,, \qquad n = 1,3,5,\dots\,. \tag{9}$$

Note that, as with problem (1), only odd nontriplen harmonics are considered since even harmonics remain zero due to the HWS, while triplen harmonics do not affect the current. Moreover, $a_1 = 0$ such that the phase of the fundamental component is zero.

C. Thermally Constrained Multipolar HWS OPPs

As demonstrated in [32], besides symmetry relaxations, relaxing the polarity of the OPP switch positions can have a beneficial impact on the output current quality while keeping the thermal stress at bay. This means that the single-phase OPP can assume all possible values in the first half of the period, i.e., $u_j \in \{-1,0,1\}$, for $j \in \{0,1,\dots,2d\}$. This is in contrast with unipolar HWS OPPs, where the switch positions in the first half of the fundamental period are

$$u_j = \begin{cases} 0\,, & j = 0,2,\dots,2d \\ 1\,, & j = 1,3,\dots,2d-1\,. \end{cases} \tag{10}$$

Given the above, thermally constrained multipolar HWS OPPs are proposed in this work. To compute such OPPs, the $2d$ optimal switching angles $\boldsymbol{\alpha}_H$ and the $2d+1$ optimal switch positions $\boldsymbol{u}_H = [u_0\, u_1\, \dots\, u_{2d}]^T$ have to be found. Because the switch positions assume integer values, the resulting optimization problem is a mixed-integer nonconvex problem, posing significant computational challenges. To avoid solving the mixed-integer problem directly, problem (8) is typically solved separately for each possible switching sequence $\boldsymbol{u}_H$. This, however, requires the evaluation of $2^{d+1}-1$ sequences $\boldsymbol{u}_H$ for a given pulse number d. Such an exponential increase in the number of candidate sequences indicates a significant increase in the complexity of the—already difficult to solve—nonconvex relaxed OPP problem, making the computation of multipolar HWS OPPs a very challenging task.

This work overcomes this issue by solving the thermally constrained multipolar HWS OPP problem only *once* per initial switch position $u_0 \in \{-1,0,1\}$. To do so, the switching angle $\alpha_i \in [0,\pi]$ and the switching transition $\Delta u_i \in \{-1,1\}$ are combined into one optimization variable, as proposed in [34]. This new variable, referred to as virtual angle γ_i, is defined as

$$\gamma_i = \alpha_i + \frac{1-\Delta u_i}{2}\pi\,. \tag{11}$$

As can be inferred from (11), in contrast to the switching angles α_i which assume values in $[0,\pi]$, the virtual angles γ_i assume values in $[0,2\pi]$. Specifically, the virtual angles $\gamma_i \in [0,\pi]$ correspond to positive switching transitions $\Delta u_i = 1$ with $\gamma_i = \alpha_i$, meaning that

$$\sin(n\gamma_i) = \sin(n\alpha_i) = \Delta u_i \sin(n\alpha_i)$$

and

$$\cos(n\gamma_i) = \cos(n\alpha_i) = \Delta u_i \cos(n\alpha_i)\,.$$

On the other hand, the virtual angles $\gamma_i \in [\pi,2\pi]$ correspond to negative switching transitions $\Delta u_i = -1$ with $\gamma_i = \alpha_i + \pi$, resulting in

$$\begin{aligned}\sin(n\gamma_i) &= \sin(n(\alpha_i+\pi)) = \sin(n\alpha_i)\cos(n\pi) \\ &= -\sin(n\alpha_i) = \Delta u_i \sin(n\alpha_i)\ \forall n \text{ odd}\end{aligned}$$

and

$$\begin{aligned}\cos(n\gamma_i) &= \cos(n(\alpha_i+\pi)) = \cos(n\alpha_i)\cos(n\pi) \\ &= -\cos(n\alpha_i) = \Delta u_i \cos(n\alpha_i)\ \forall n \text{ odd}.\end{aligned}$$

Hence, based on the above, the nonzero a_n and b_n Fourier coefficients of HWS OPPs can be written as a function of γ_i as follows:

$$a_n(\boldsymbol{\gamma}) = -\frac{2}{n\pi}\sum_{i=1}^{2d}\sin(n\gamma_i)\,, \qquad n = 1,3,5,\dots$$

$$b_n(\boldsymbol{\gamma}) = \frac{2}{n\pi}\sum_{i=1}^{2d}\cos(n\gamma_i)\,, \qquad n = 1,3,5,\dots\,.$$

Thus, the objective function can be minimized with respect to the virtual angles.

Following, to fully define the optimization problem, the constraints on the virtual angles need to be designed. Taking into account that the value of γ_i determines the polarity of the switching transition, the number of positive and negative switching transitions in the first half-period can be identified. This is done by observing that the number of positive and negative OPP switching transitions depends on the initial switch position u_0, see Fig. 3. When $u_0 = 0$, d switching transitions are positive and d negative, highlighted with green and red arrows, respectively, in Fig. 3(a). In the case of $u_0 = 1$, $d-1$ switching transitions are positive and $d+1$ negative, see Fig. 3(b). Finally, $d+1$ switching transitions are positive and $d-1$ negative when $u_0 = -1$, see Fig. 3(c). By combining all cases, $d-u_0$ virtual angles relate to positive switching transitions, while $d+u_0$ virtual angles relate to negative switching transitions. Therefore, the virtual angles are arranged in ascending order, i.e., $\gamma_i < \gamma_{i+1}$, $i \in \{1,\dots,2d\}$, and their upper and lower bounds are set to

$$\begin{aligned}&\gamma_i \in [0,\pi],\ i \in \{1,\dots,d-u_0\} \\ &\gamma_i \in [\pi,2\pi],\ i \in \{d-u_0+1,\dots,2d\}.\end{aligned} \tag{12}$$

Finally, unlike conventional OPPs where the unipolar switch positions are deterministic, the multipolar switch positions of the proposed OPPs must be computed during the optimization procedure to ensure they respect the available voltage levels. For that reason, the constraints $-1 \le u_i \le 1$, $i \in \{1,\dots,2d\}$ are added to the optimization problem. To evaluate these constraints, the switching angles and corresponding switch positions need to be derived from the virtual angles during the optimization process.

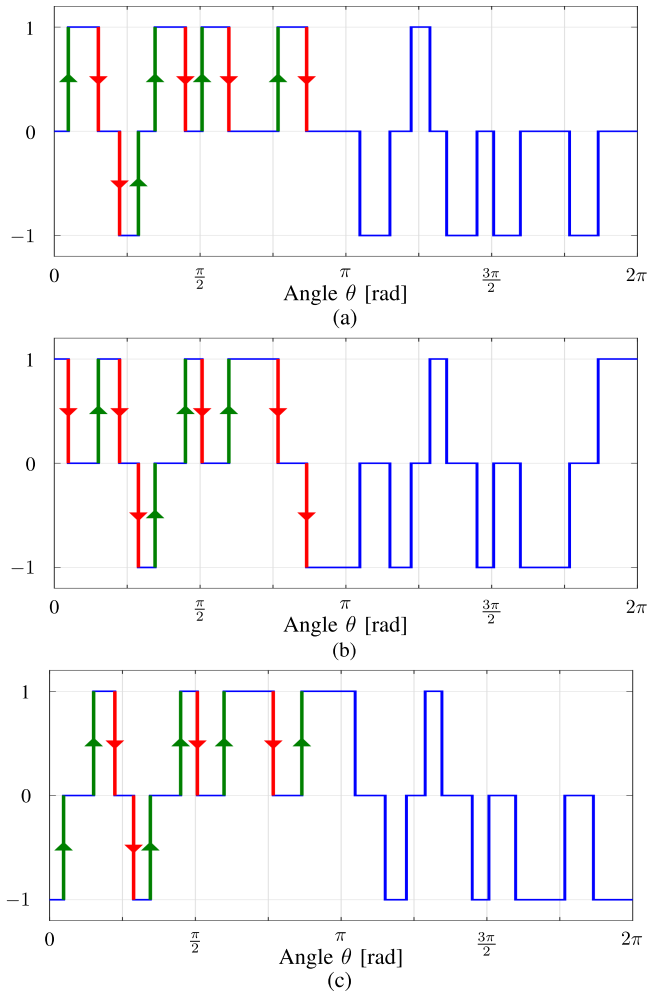

Fig. 3. Multipolar HWS pulse patterns for $d = 5$. (a) With $u_0 = 0$. (b) With $u_0 = 1$. (c) With $u_0 = -1$.

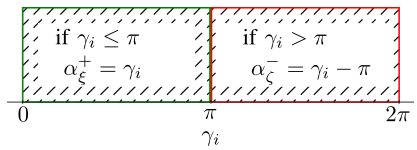

Fig. 4. Derivation of switching angles from the virtual angles.

To do so, first, the switching angles $\alpha_\xi^+, \xi \in \{1, \ldots, d - u_0\}$, corresponding to positive switching transitions, and the switching angles $\alpha_\zeta^-, \zeta \in \{1, \ldots, d + u_0\}$, corresponding to negative switching transitions, are derived from the virtual angles γ_i, $i \in \{1, \ldots, 2d\}$, as visualized in Fig. 4. Then, the switching angles $\boldsymbol{\alpha} = [\alpha_1 \ \ldots \ \alpha_{2d}]^T$ are computed by sorting the sequence $\boldsymbol{A} = [\alpha_1^+ \ \ldots \ \alpha_{d-u_0}^+ \ \alpha_1^- \ \ldots \ \alpha_{d+u_0}^-]^T$ in ascending order. The sequence of switching transitions $\Delta\boldsymbol{u} = [\Delta u_1 \ \ldots \ \Delta u_{2d}]^T$ is constructed by setting $\Delta u_i = 1$ if α_i corresponds to α_ξ^+. Otherwise, the switching transition is $\Delta u_i = -1$ if α_i corresponds to α_ζ^-. Finally, the switch positions u_i are computed by cumulative summing up all the switching transitions starting from the initial switch position u_0 until the transition Δu_i, i.e., $u_i = u_0 + \sum_{j=1}^{i} \Delta u_j$. This procedure of deriving the switching angles α_i and switch positions u_i from the virtual angles γ_i is described in Algorithm 1. After deriving the switch positions u_i from the virtual angles, the constraints $-1 \leq u_i \leq 1$ can be evaluated. An example of the procedure described in Algorithm 1 for the OPP depicted in Fig. 5 is shown in Table IV.

Algorithm 1: Derivation of the Switching Angles and the Switch Positions From the Virtual Angles.

1: Given the virtual angles γ_i, $i \in \{1, \ldots, 2d\}$, construct the sequences of switching angles $\alpha_\xi^+, \xi \in \{1, \ldots, d - u_0\}$, and $\alpha_\zeta^-, \zeta \in \{1, \ldots, d + u_0\}$, based on Fig. 4.
2: Compute the switching angles $\boldsymbol{\alpha} = [\alpha_1 \ \ldots \ \alpha_{2d}]^T$ by sorting the $2d$ angles of $\boldsymbol{A} = [\alpha_1^+ \ \ldots \ \alpha_{d-u_0}^+ \ \alpha_1^- \ \ldots \ \alpha_{d+u_0}^-]^T$ in ascending order.
3: Set Δu_i, $i \in \{1, \ldots, 2d\}$ to $\Delta u_i = 1$ if α_i corresponds to α_ξ^+, otherwise set Δu_i to $\Delta u_i = -1$ if α_i corresponds to α_ζ^-.
4: Calculate u_i by cumulative summing up the corresponding switching transitions up to Δu_i, i.e., $u_i = u_0 + \sum_{j=1}^{i} \Delta u_j$.
Return u_i and α_i for $i \in \{1, \ldots, 2d\}$.

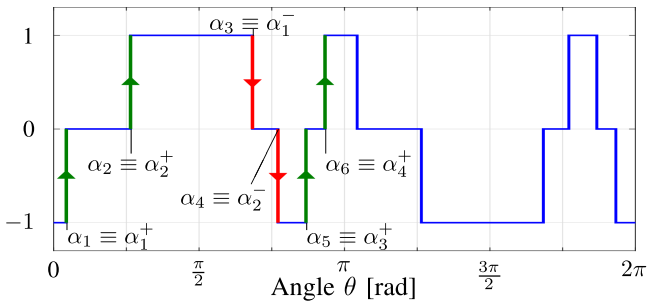

Fig. 5. HWS multipolar OPP with $d = 3$.

TABLE IV
DERIVATION OF SWITCHING ANGLES AND SWITCHING TRANSITIONS FOR THE MULTIPOLAR HWS OPP SHOWN IN FIG. 5

Virtual angles [rad]	
γ_1	0.1367
γ_2	0.8302
γ_3	2.7256
γ_4	2.9309
γ_5	5.2892
γ_6	5.5646

→

Sw. angles [rad]	
α_1^+	0.1367
α_2^+	0.8302
α_3^+	2.7256
α_4^+	2.9309
α_1^-	2.1476
α_2^-	2.4230

$\overset{\text{sort}}{\rightarrow}$

Sw. angles [rad]		Sw. transitions	
$\alpha_1 \equiv \alpha_1^+$	0.1367	Δu_1	+1
$\alpha_2 \equiv \alpha_2^+$	0.8302	Δu_2	+1
$\alpha_3 \equiv \alpha_1^-$	2.1476	Δu_3	−1
$\alpha_4 \equiv \alpha_2^-$	2.4230	Δu_4	−1
$\alpha_5 \equiv \alpha_3^+$	2.7256	Δu_5	+1
$\alpha_6 \equiv \alpha_4^+$	2.9309	Δu_6	+1

$\overset{u_0 \equiv -1}{\Rightarrow}$

Sw. positions	
u_1	0
u_2	1
u_3	0
u_4	−1
u_5	0
u_6	1

Based on the above analysis, the optimization problem for thermally constrained multipolar HWS OPPs becomes

$$\begin{aligned}\underset{\boldsymbol{\gamma}_H}{\text{minimize}} \quad & J(\boldsymbol{\gamma}_H) = \sum_{n=5,7,11,\ldots} \frac{a_n^2(\boldsymbol{\gamma}_H) + b_n^2(\boldsymbol{\gamma}_H)}{n^2} \\ \text{subject to} \quad & a_1(\boldsymbol{\gamma}_H) = 0,\ b_1(\boldsymbol{\gamma}_H) = m \\ & 0 \le \gamma_1 < \gamma_2 < \ldots < \gamma_{d-u_0} \le \pi \\ & \pi \le \gamma_{d-u_0+1} < \gamma_{d-u_0+2} < \ldots < \gamma_{2d} \le 2\pi \\ & -1 \le u_i \le 1\ \forall i \in \{1,\ldots,2d\} \\ & T^{\ell}_{\mathrm{j,max}}(\boldsymbol{\gamma}_H, u_0, \phi) \le T^{\ell}_{\mathrm{j,lmt}}\ \forall \ell \in \{S_{1,2}, D_{1,2,5}\}\end{aligned} \tag{13}$$

where $\boldsymbol{\gamma}_H = [\gamma_1\ \gamma_2\ \ldots\ \gamma_{2d}]^T \in [0, 2\pi]^{2d}$ is the vector of the $2d$ virtual switching angles. Note that the junction temperature constraint is a function not only of the virtual angles but also of the initial switch position $u_0 \in \{-1, 0, 1\}$ because it is needed for the derivation of the switching sequence $\boldsymbol{u}_H$, see Algorithm 1.

Optimization problem (13) is solved with respect to the virtual angles. By doing so, the iteration over all the possible switching sequences is avoided, resulting in significant time savings. However, unlike [31], it cannot be cast in a closed form. After solving (13) for pulse number d, the optimal virtual angles $\boldsymbol{\gamma}^*_{H,d}$ that result in the lowest value of the objective function $J(\boldsymbol{\gamma}_H)$, i.e., $J^*_{H,d} = J(\boldsymbol{\gamma}^*_{H,d})$, are obtained. From those, the optimal switching angles $\boldsymbol{\alpha}^*_{H,d}$ and switching sequence $\boldsymbol{u}^*_{H,d}$ are derived following Algorithm 1.

1) Minimum Pulse Width: In the physical system, a minimum on/off time $\Delta t_{\min}$ is required between two consecutive switching events. In this work, $\Delta t_{\min}$ is set to $50\,\mu$s. To guarantee the minimum ON/OFFtime $\Delta t_{\min}$ requirement of the devices, two consecutive switching angles need to have a minimum difference $\Delta\theta_{\min}$, i.e.,

$$\Delta a_i \ge \Delta\theta_{\min} \quad \forall i \in \{1, 2, \ldots, 2d-1\} \tag{14}$$

where $\Delta a_i = \alpha_{i+1} - \alpha_i$, $\Delta\theta_{\min} = 2\pi\Delta t_{\min}/T_1$, and $T_1 = 1/f_1$ is the fundamental period.

If for a specific modulation index m switching angles $\boldsymbol{\alpha}^*_{H,d}$ do not satisfy condition (14), i.e., a pulse smaller than $\Delta t_{\min}$ exists, (14) needs to be imposed. This is done by solving optimization problem (8), where the Fourier coefficients a_n and b_n are computed assuming a deterministic switching sequence obtained from solving (13), i.e., with $\boldsymbol{u}_H = \boldsymbol{u}^*_{H,d}$. This procedure—described in Algorithm 2—is executed for every modulation index m and a given pulse number d.

2) Optimal Pulse Number: Executing Algorithm 2 ensures that the minimum pulse width is respected. However, patterns with small pulses only slightly longer than $\Delta t_{\min}$ might still be produced. Such pulses can significantly impact the switching losses and, therefore, the junction temperature, without notably affecting the current TDD. As a result, a pulse pattern with a lower pulse number might result in the same current TDD but lower junction temperature. For that reason, the optimization problem needs to be solved for a range of pulse numbers. The OPP with the lowest cost $J^*_{H,d}$, i.e., current TDD, which meets the thermal constraints at a given modulation index is then selected in a postprocessing step.

Algorithm 2: Postprocessing Algorithm.

1: **function** ensureMinPulse($\boldsymbol{\alpha}^*_{H,d}$, $\boldsymbol{u}^*_{H,d}$, $J^*_{H,d}$, d, m)
2: **if** $\exists\ \Delta\alpha_i < \Delta\theta_{\min}, i \in \{1, 2, \ldots, 2d-1\}$ **then**
3: Solve problem (8) with $\boldsymbol{u}_H = \boldsymbol{u}^*_{H,d}$ using $\boldsymbol{\alpha}^*_{H,d}$ among the initial points
4: Update $\boldsymbol{\alpha}^*_{H,d}$, $J^*_{H,d}$ with the optimal solution of (8)
5: **end if**
6: **return** $\boldsymbol{\alpha}^*_{H,d}$, $\boldsymbol{u}^*_{H,d}$, $J^*_{H,d}$
7: **end function**

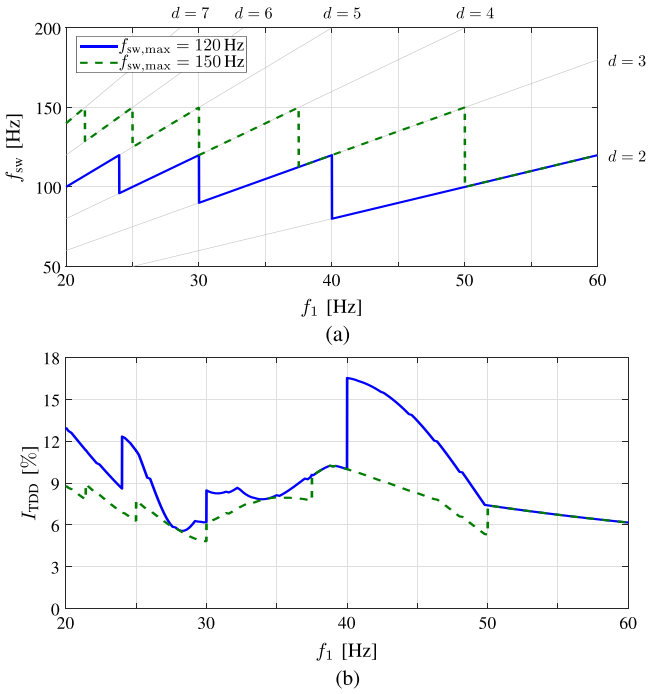

Fig. 6. Conventional approach with $f_{\mathrm{sw,max}} = 120$ Hz (blue solid line) and $f_{\mathrm{sw,max}} = 150$ Hz (green dashed line) over a range of fundamental frequencies. (a) Switching frequency. (b) Current TDD.

IV. Numerical Results

This section shows the optimization results for (a) conventional QaHWS OPPs [see problem (1)]; (b) thermally constrained *unipolar* QaHWS OPPs [see problem (1) with constraint (6)]; (c) thermally constrained *unipolar* HWS OPPs [see problem (8)]; and (d) thermally constrained *multipolar* HWS OPPs [see problem (13)]. OPPs in the "b" category are hereafter referred to as "QaHWS–uni–T_{j} OPPs," those in category "c" as "HWS–uni–T_{j} OPPs," while those in category "d" as "HWS–multi–T_{j} OPPs." All OPPs are computed for an MV drive system consisting of a machine and a three-level NPC converter. Two different machine types are considered, namely an induction machine (IM) and an externally excited synchronous machine (EESM). Both machines have rated voltage 3.3 kV, rated current 2.8 kA and nominal frequency 50 Hz. The total leakage reactance of the IM is 0.25 per unit (p.u.), while the subtransient reactance of the EESM has the same value. The nominal power factor of the IM is 0.82, which corresponds to a displacement angle $\phi = 35°$ (lagging current in motoring operation), while the EESM has a unity nominal power factor corresponding to $\phi = 0°$. Finally, the dc-link voltage of the converter is $V_{\mathrm{dc}} = 4.84$ kV. The parameters

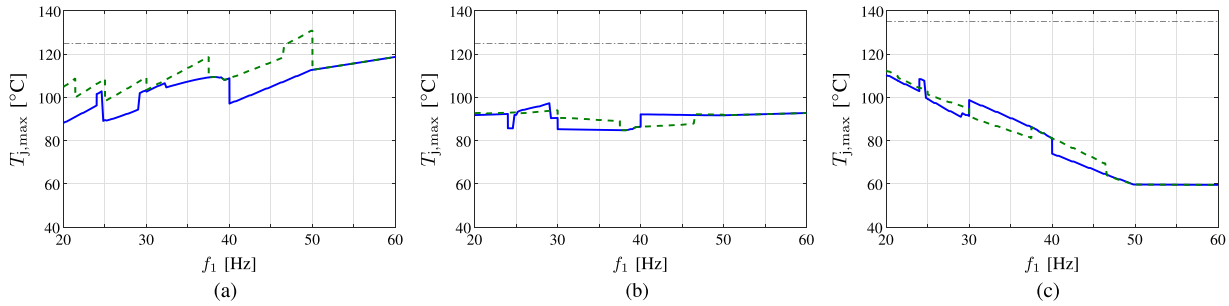

Fig. 7. Maximum junction temperature of conventional approach with $f_{sw,max} = 120$ Hz (blue solid line) and $f_{sw,max} = 150$ Hz (green dashed line) over a range of fundamental frequencies when considering displacement angle $\phi = 35°$. (a) Maximum junction temperature of device S_1. (b) Maximum junction temperature of device S_2. (c) Maximum junction temperature of device D_5.

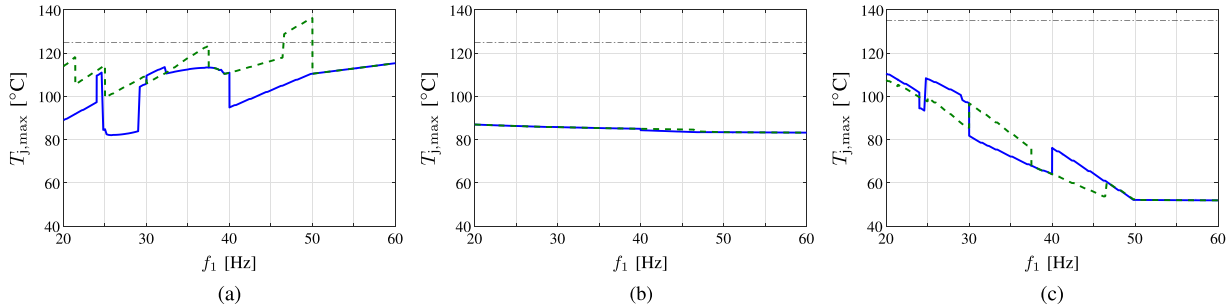

Fig. 8. Maximum junction temperature of conventional approach with $f_{sw,max} = 120$ Hz (blue solid line) and $f_{sw,max} = 150$ Hz (green dashed line) over a range of fundamental frequencies when considering displacement angle $\phi = 0°$. (a) Maximum junction temperature of device S_1. (b) Maximum junction temperature of device S_2. (c) Maximum junction temperature of device D_5.

of the considered semiconductor devices are presented in Table I, while the temperature of the cooling water is $T_w = 37\,°C$.

All OPPs are computed across a range of fundamental frequencies, namely $f_1 \in [20, 60]$ Hz. Note that since the rated frequency of the machine is 50 Hz, the modulation index is proportional to the fundamental frequency up to that frequency, and it remains constant at its nominal value $m_N = 1.113$ for $f_1 \geq 50$ Hz. As explained in Section III-B, only the five devices of the upper half of the NPC leg are considered in the optimization problem due to the symmetry of the OPPs.

A. Conventional Approach

Due to the high switching losses and the need to keep the junction temperature low, MV drives are operated at very low switching frequencies. To achieve these goals, the conventional approach is to keep the switching frequency below the maximum allowable switching frequency. Thus, OPPs with the highest pulse number that keeps the switching frequency below the desired limit, i.e., with pulse number

$$d = \left\lfloor \frac{f_{sw,max}}{f_1} \right\rfloor \tag{15}$$

are selected. The switching frequency and current TDD of the conventional approach for $f_{sw,max} = 120$ Hz are shown in Fig. 6 with a blue solid line. As seen in Fig. 6(a), pulse numbers $d = 2$ to 5 are used in the considered range of fundamental frequencies. The pulse number can be identified in Fig. 6(a) by following the gray lines that correspond to $f_{sw} = df_1$, where the pulse number d is indicated at the side of the figure. Note that there is a step change in the current TDD when changing from one pulse number to another, e.g., I_{TDD} increases from 10% to 16.5% at $f_1 = 40$ Hz when the pulse number changes from three to two.

Two cases are considered for the displacement angle, i.e., $\phi = 35°$ and $\phi = 0°$, corresponding to nominal operation of the IM and EESM, respectively. The junction temperatures of the semiconductor devices for these cases are shown in Figs. 7 and 8, respectively. Note that the junction temperatures of diodes D_1 and D_2 are very low and are therefore not shown here. As can be seen, all semiconductor devices are within the safe operation limits.

If $f_{sw,max}$ was set to 150-Hz higher, then higher pulse numbers would be selected, allowing for lower I_{TDD}, see Fig. 6 . However, in that case, the maximum junction temperature of device S_1 would exceed the safe operating limits for $f_1 \in [47, 50]$ Hz in the case of $\phi = 35°$, see Fig. 7(a), and for $f_1 \in [46.6, 50]$ Hz in the case of $\phi = 0°$, see Fig. 8(a). For that reason, conventional OPPs with $f_{sw,max} = 120$ Hz are used as a baseline in the sequel of this section.

B. Thermally Constrained OPPs

For the numerical results presented in this work, thermally constrained OPPs with pulse numbers up to $d = 12$ are considered. By doing so, enough degrees of freedom are provided in the

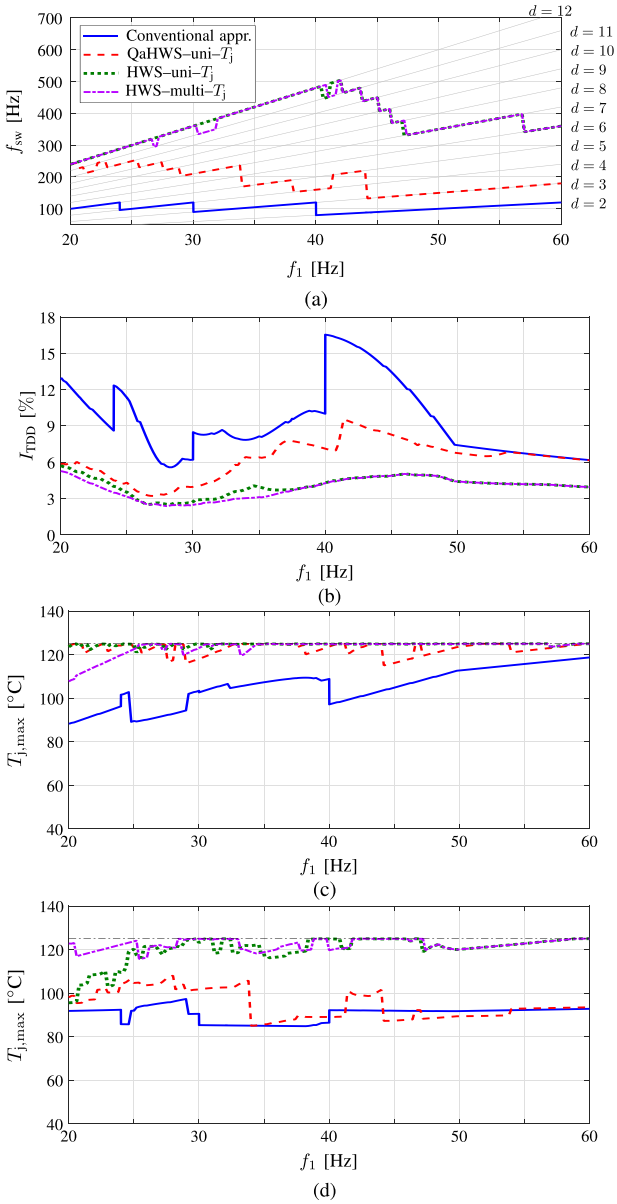

Fig. 9. Conventional approach with $f_{sw,max} = 120$ Hz (blue solid line) and QaHWS and HWS thermally constrained OPPs over a range of fundamental frequencies considering $\phi = 35°$. (a) Switching frequency. (b) Current TDD. (c) Maximum junction temperature of device S_1. (d) Maximum junction temperature of device S_2.

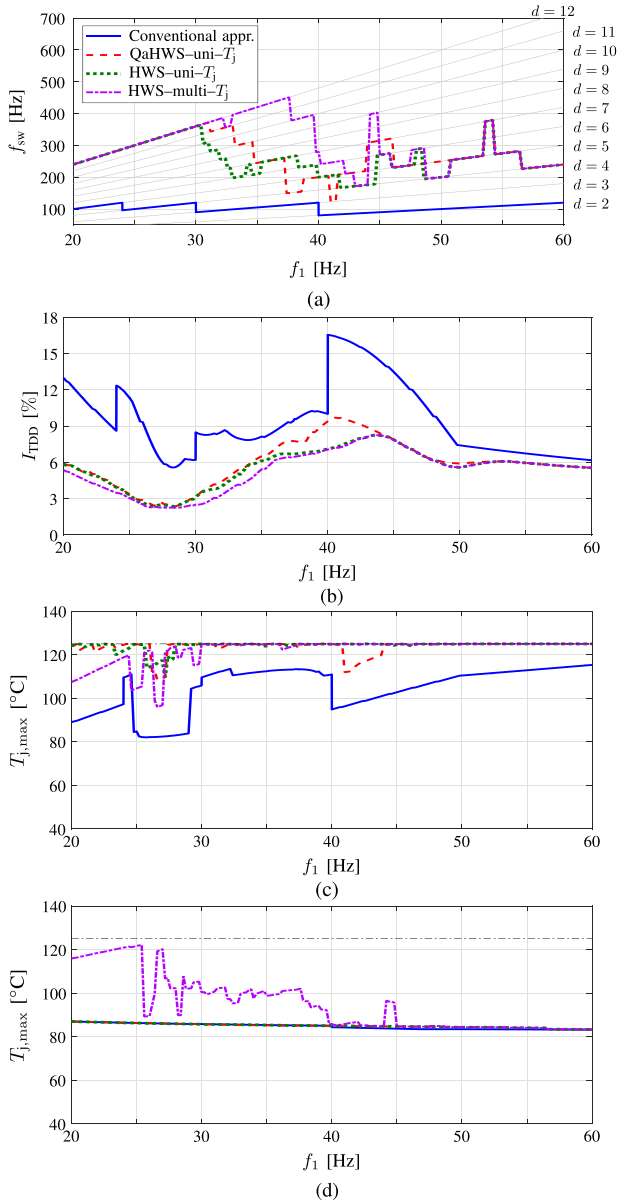

Fig. 10. Conventional approach with $f_{sw,max} = 120$ Hz (blue solid line) and QaHWS and HWS thermally constrained OPPs over a range of fundamental frequencies considering $\phi = 0°$. (a) Switching frequency. (b) Current TDD. (c) Maximum junction temperature of device S_1. (d) Maximum junction temperature of device S_2.

optimization problem to allow for low harmonic distortions in the output current. The optimization problem is solved considering the two aforementioned displacement angles, i.e., $\phi = 35°$ and $\phi = 0°$, which correspond to the nominal operation of the IM and EESM, respectively. Note that for each displacement angle, different OPPs are produced.

Starting from $\phi = 35°$, when considering QaHWS–uni–T_j OPPs, the optimal pulse number varies from 3 to 12 [see Fig. 9(a)], with the resulting switching frequency being up to 250 Hz. As seen in Fig. 9(b), compared to the conventional approach, the current TDD is significantly decreased, with a relative reduction of 64.5% at $f_1 = 24.4$ Hz. This is possible because the devices are pushed to their thermal limits. More specifically, the maximum junction temperature of IGCT S_1 is close to 125 °C for most of the operating points [see Fig. 9(c)], while the maximum junction temperature of S_2 is increased for most fundamental frequencies compared to the conventional approach, see Fig. 9(d). Note that the junction temperature of diodes D_1, D_2, and D_5 are not close to the thermal limits and are therefore not shown in the figure.

When relaxing the symmetry properties, namely using HWS–uni–T_j OPPs, pulse numbers between 6 and 12 are selected as optimal [see Fig. 9(a)], resulting in a switching frequency that reaches up to 500 Hz.[4] As seen in Fig. 9(a), HWS–uni–T_j OPP select higher pulse numbers than QaHWS–uni–T_j OPPs. More specifically, pulse number $d = 12$ is used for $f_1 \in [20, 40.4] \cup$

[4]In practice, due to the $\mathrm{d}i/\mathrm{d}t$ snubbers of the IGCTs, the switching should be limited to 250 Hz to not create significant losses in the driving circuit.

TABLE V
SWITCHING SEQUENCE OF HWS–MULTI–T_j OPPs OVER A RANGE OF FUNDAMENTAL FREQUENCIES CONSIDERING $\phi = 35°$

f_1 [Hz]	$\boldsymbol{u}_H$	d	f_1 [Hz]	$\boldsymbol{u}_H$	d
$[20, 20.4]$	[-1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 1]	12	$[32.4, 33]$	[1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1]	12
$[20.6, 25.2]$	[0 1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 1 0]	12	$[33.2, 37.6]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0]	12
$[25.4, 26]$	[-1 0 -1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1]	12	$[37.8, 40.8]$	[1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1]	12
$[26.2, 26.6]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	12	$[41, 41.6]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0]	11
$[26.8, 27]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0 1 0 1 0 1 0 1 0 1 0]	11	$[41.8, 42]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	12
$[27.2, 28.2]$	[0 1 0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0]	12	$[42.2, 43.6]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	11
$[28.4, 28.6]$	[-1 0 -1 0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 1]	12	$[43.8, 45]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	10
$[28.8, 30.2]$	[0 1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0]	12	$[45.2, 46]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	9
$[30.4, 30.8]$	[1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1]	11	$[46.2, 47.2]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	8
$[31, 31.8]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0]	11	$[47.4, 56.8]$	[0 1 0 1 0 1 0 1 0 1 0 1 0]	7
$[32, 32.2]$	[1 0 1 0 1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1]	12	$[57, 60]$	[0 1 0 1 0 1 0 1 0 1 0]	6

TABLE VI
SWITCHING SEQUENCE OF HWS–MULTI–T_j OPPs OVER A RANGE OF FUNDAMENTAL FREQUENCIES CONSIDERING $\phi = 0°$

f_1 [Hz]	$\boldsymbol{u}_H$	d	f_1 [Hz]	$\boldsymbol{u}_H$	d
$[20, 24.4]$	[0 1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 1 0]	12	$[36.2, 37.6]$	[0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0]	12
$[24.6, 25.4]$	[0 -1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0]	12	$[37.8, 38.2]$	[0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0]	10
$[25.6, 26]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0]	12	$[38.4, 39]$	[1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0 -1]	10
26.2	[0 -1 0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	12	$[39.2, 39.6]$	[1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0 -1 0 -1]	10
$[26.4, 26.6]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0 -1 0]	12	$[39.8, 40]$	[1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1]	7
27	[0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0]	12	$[40.2, 40.8]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0]	6
$[27.2, 27.4]$	[0 1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 1 0]	12	$[41, 41.2]$	[1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1]	6
$[27.6, 28]$	[0 1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 1 0]	12	$[41.4, 42]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0]	6
$[28.2, 28.4]$	[0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0]	12	$[42.2, 42.8]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0]	5
28.6	[1 0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1]	12	$[43, 44]$	[0 1 0 1 0 1 0 1 0]	4
$[28.8, 29.2]$	[1 0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 1 0 1 0 -1]	12	$[44.2, 44.8]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0]	9
$[29.4, 29.8]$	[0 1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0]	12	$[45, 45.8]$	[0 1 0 1 0 1 0 1 0 1 0 1 0]	6
$[30, 30.2]$	[0 -1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0]	12	$[46, 47.4]$	[0 1 0 1 0 1 0 1 0 1 0]	5
$[30.4, 31]$	[1 0 1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1]	12	$[47.6, 48.6]$	[0 1 0 1 0 1 0 1 0 1 0 -1 0]	6
$[31.2, 31.8]$	[0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0]	12	$[48.8, 50.6]$	[0 1 0 1 0 1 0 1 0]	4
$[32, 32.2]$	[1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1]	12	$[50.8, 53.4]$	[0 1 0 1 0 1 0 1 0 1 0]	5
$[32.4, 32.8]$	[1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1]	11	$[53.6, 54.2]$	[0 1 0 1 0 1 0 1 0 1 0 1 0 1 0]	7
$[33, 34]$	[0 1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0]	12	$[54.4, 56.4]$	[0 1 0 1 0 1 0 1 0 1 0]	5
$[34.2, 34.8]$	[0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1 0 -1 0]	12	$[56.6, 60]$	[0 1 0 1 0 1 0 1 0]	4
$[35, 36]$	[1 0 -1 0 -1 0 -1 0 1 0 1 0 1 0 1 0 1 0 -1 0 -1 0 -1 0 -1]	12			

$[41.2, 42]$ Hz, while the same pulse number is used only for $f_1 \in [20, 20.4]$ Hz with QaHWS–uni–T_j OPPs. The relaxation of the symmetry properties allows the switching angles to be more freely distributed within the half-period. As a result, the degrees of freedom provided by the choice of a high pulse number, such as $d = 12$, can be better utilized, leading to improved harmonic performance. A relative improvement of up to 52.1% in the current TDD can be achieved at $f_1 = 37.4$ Hz compared to QaHWS–uni–T_j OPPs. As seen in Fig. 9(c) and (d), the junction temperatures of both S_1 and S_2 are kept close to their thermal limit for most values of the considered fundamental frequencies.

When the switching properties are also relaxed, namely HWS–multi–T_j OPPs are used, the junction temperature constraint can be met while the current TDD is even lower. This is thanks to the additional degrees of freedom of problem (13), as it can choose among multiple switching sequences. Table V shows the switching patterns of HWS–multi–T_j OPPs. As can be observed, multipolar patterns with pulse number $d = 11$ are used for $f_1 \in [26.8, 27] \cup [30.4, 31.8] \cup [41, 41.6]$ Hz, while multipolar patterns with pulse number $d = 12$ are used for $f_1 \in [20, 26] \cup [27.2, 30.2] \cup [32, 40.8]$ Hz. For fundamental frequencies $f_1 > 41.6$ Hz, unipolar patterns with different pulse numbers are chosen. As can be inferred, multipolar patterns are suboptimal at high fundamental frequencies. Nevertheless, the relaxation of the symmetry still enables a reduction in the I_TDD compared to the conventional approach.

Similar observations can be made when unit power factor is considered, i.e., $\phi = 0°$. By constraining the junction temperature, the physical requirements can be met for the whole range of examined operating points. At the same time, QaHWS–uni–T_j OPPs can reduce the current TDD by up to 72% compared to the conventional method, see Fig. 10(b). As seen in Fig. 10(a), QaHWS–uni–T_j OPPs with pulse numbers 3 to 12 are used, resulting in switching frequencies above 250 Hz. Nevertheless, when relaxing the quarter-wave symmetry, the current TDD can be reduced by up to an additional 25.1%, see Fig. 10(b). If multipolar patterns are also allowed, the current TDD can be improved even further. HWS–multi–T_j OPPs result in up to 28% lower I_TDD compared to HWS–uni–T_j OPPs. Similar to the case with $\phi = 35°$, multipolar OPPs are used only at medium fundamental frequencies, i.e., $f_1 \in [20, 43] \cup [44, 45] \cup [47.4, 48.6]$ Hz, with this displacement angle, see Table VI; multipolar patterns are suboptimal at higher fundamental frequencies.

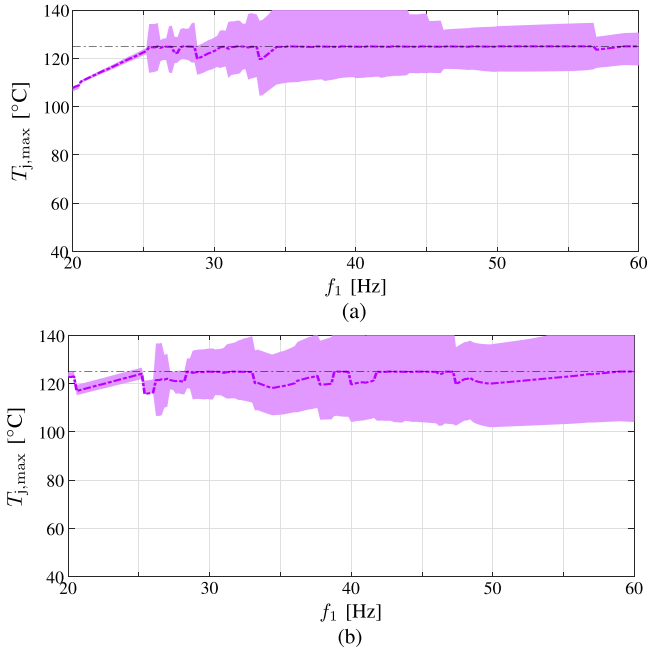

Fig. 11. HWS–multi–T_j OPPs optimized for $\phi = 35°$, considering a displacement angle variation of $\Delta\phi = \pm 10°$ around the nominal value. The (purple) dashed-dotted line shows the maximum junction temperature at $\phi = 35°$, while the (purple) shaded area indicates its variation. (a) Maximum junction temperature of device S_1. (b) Maximum junction temperature of device S_2.

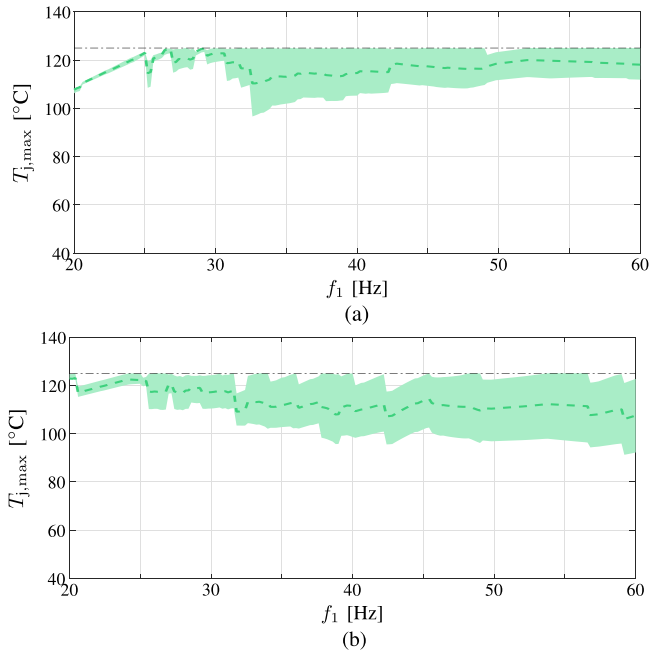

Fig. 12. Robust HWS–multi–T_j OPPs optimized for $\phi = 35°$, considering a displacement angle variation of $\Delta\phi = \pm 10°$ around the nominal value. The (green) dashed line shows the maximum junction temperature at $\phi = 35°$, while the (green) shaded area indicates its variation. (a) Maximum junction temperature of device S_1. (b) Maximum junction temperature of device S_2.

Overall, thermally constrained OPPs with relaxed properties allow for full utilization of the thermal capabilities of the converter over a wide range of operating points, while having superior harmonic performance compared to the conventional approach. The benefits provided by these OPPs can be reaped thanks to the proposed reformulation of the optimization problem, which facilitates their computation without significantly increasing the computational burden.

C. Robust Thermally Constrained OPPs

The thermally constrained OPPs presented in Section IV-B are optimized for a specific displacement angle ϕ. By doing so, they can operate very close to the thermal limits of the semiconductor devices for that specific ϕ. However, when they are used at a displacement angle different from the one they were optimized for, they might result in junction temperatures above the thermal limits, rendering them unsuitable. As an example, Fig. 11 shows the maximum junction temperature of S_1 and S_2 when the HWS–multi–T_j OPPs optimized for $\phi = 35°$ are used with varying $\phi \in [25°, 45°]$. As can be inferred, these OPPs cannot be used with a varying power factor because the resulting junction temperature exceeds the limit of 125 °C, and can reach up to 140 °C.

To tackle this issue, a modification to constraint (6), inspired by [30], is proposed. More specifically, the maximum junction temperature of all devices at $\phi \pm \Delta\phi$, where $\Delta\phi$ is a variation in ϕ, are also constrained, resulting in the modified constraint

$$T^{\ell}_{j,max}(\boldsymbol{\alpha}, \phi) \leq T^{\ell}_{j,lmt} \; \forall \ell \in \{S_{1,2}, D_{1,2,5}\} \text{ and}$$

$$T^{\ell}_{j,max}(\boldsymbol{\alpha}, \phi - \Delta\phi) \leq T^{\ell}_{j,lmt} \; \forall \ell \in \{S_{1,2}, D_{1,2,5}\} \text{ and}$$

$$T^{\ell}_{j,max}(\boldsymbol{\alpha}, \phi + \Delta\phi) \leq T^{\ell}_{j,lmt} \; \forall \ell \in \{S_{1,2}, D_{1,2,5}\}. \quad (16)$$

Thus, by using constraint (16) instead of (6) in optimization problem (8), robust thermally constrained *unipolar* HWS OPPs—hereafter referred to as "robust HWS–uni–T_j OPPs"—are computed. Similarly, by replacing constraint (6) with (16) in optimization problem (13), robust thermally constrained *multipolar* HWS OPPs—referred to as "robust HWS–multi–T_j OPPs"—are computed. These robust thermally constrained OPPs are compared to the HWS–multi–T_j OPPs in the remainder of this section.

As seen in Fig. 12, robust HWS–multi–T_j OPPs respect the thermal limits for the whole range of fundamental frequencies and considered range of power factors. This robustness feature, however, comes at the expense of increased harmonic distortions, see Fig. 13(b). Robust HWS–multi–T_j OPPs have up to 40% higher TDD compared to HWS–multi–T_j OPPs. This is because the robust thermally constrained OPPs choose lower pulse numbers compared to HWS–multi–T_j OPPs. This implies that, to achieve the desired robustness feature, the switching frequency needs to be limited. Still, compared to robust HWS–uni–T_j OPPs, robust HWS–multi–T_j OPPs can decrease the I_{TDD} by up to 19.6%. Alas, this improvement is only possible at medium fundamental frequencies up to $f_1 = 38$ Hz. Similar to the simple thermally constrained OPPs, unipolar patterns are preferred at high fundamental frequencies.

Given the above discussion, a tradeoff between robustness to power factor variations and harmonic performance arises. Robust thermally constrained HWS multipolar OPPs offer a

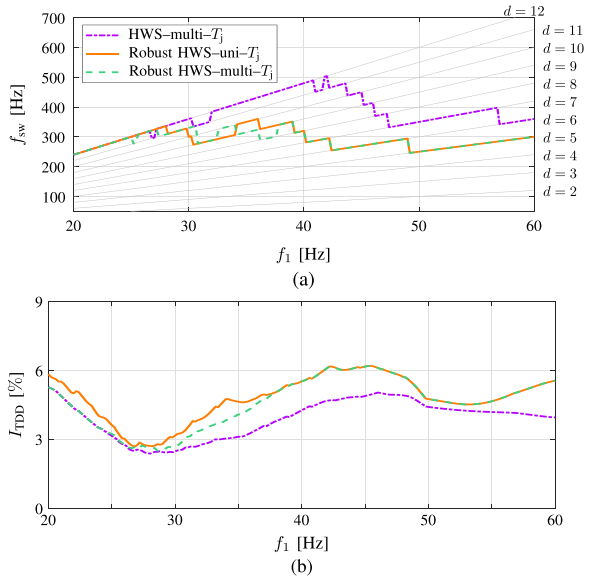

Fig. 13. HWS thermally constrained OPPs with and without the robustness feature, considering $\phi = 35°$. The (purple) dashed-dotted line corresponds to HWS–multi–T_j OPPs, the (orange) solid line to the robust HWS–uni–T_j OPPs, and the (green) dashed line to robust HWS–multi–T_j OPPs. (a) Switching frequency. (b) Current TDD.

favorable balance between these two goals, as they can achieve near-optimal performance while meeting the thermal requirements for a range of operating points.

V. Conclusion

This article presented the computation of thermally constrained OPPs. By appropriately imposing a constraint on the junction temperature, the semiconductor devices can be operated at their thermal limits without violating them. As a result, the thermal capabilities of the converter can be fully utilized. Moreover, as demonstrated through numerical results, by relaxing artificial restrictions in the OPPs, such as the OPP symmetry and the polarity of the switch positions, the tradeoff between current TDD and junction temperature can be significantly improved, especially in the range of medium fundamental frequencies. This feature of the proposed OPPs can be leveraged to increase the rated output current without compromising the quality of the output current. Importantly, these benefits are enabled by the proposed OPP problem formulation, which brings substantial reductions in the required computation time. Finally, by accounting for the variation of the power factor in the optimization problem, safe operation can be ensured for a wide range of operating points when considering a varying load. The presented numerical results, obtained using two MV drive systems, demonstrated the favorable performance of the proposed OPPs.

References

[1] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[2] J. Kuprat, C. H. van der Broeck, M. Andresen, S. Kalker, M. Liserre, and R. W. D. Doncker, "Research on active thermal control: Actual status and future trends," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6494–6506, Dec. 2021.

[3] A. Ibrahim, M. Salem, M. Kamarol, M. T. Delgado, and M. K. M. Desa, "Review of active thermal control for power electronics: Potentials, limitations, and future trends," *IEEE Open J. Power Electron.*, vol. 5, pp. 414–435, 2024.

[4] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz, and R. W. De Doncker, "Methodology for active thermal cycle reduction of power electronic modules," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8213–8229, Aug. 2019.

[5] A. Wang, Y. Qi, and K. Ma, "Adaptive DC voltage control for optimal junction temperature redistribution under stall condition of electric machine drive inverter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4229–4234, Apr. 2023.

[6] J. Lemmens, P. Vanassche, and J. Driesen, "Optimal control of traction motor drives under electrothermal constraints," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 249–263, Jun. 2014.

[7] T. A. Polom, B. Wang, and R. D. Lorenz, "Control of junction temperature and its rate of change at thermal boundaries via precise loss manipulation," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4796–4806, Sep./Oct. 2017.

[8] J. Falck, G. Buticchi, and M. Liserre, "Thermal stress based model predictive control of electric drives," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1513–1522, Mar./Apr. 2018.

[9] M. Novak, V. Ferreira, M. Andresen, T. Dragicevic, F. Blaabjerg, and M. Liserre, "FS-MPC based thermal stress balancing and reliability analysis for NPC converters," *IEEE Open J. Power Electron.*, vol. 2, pp. 124–137, 2021.

[10] L. Wang, J. He, T. Han, and T. Zhao, "Finite control set model predictive control with secondary problem formulation for power loss and thermal stress reductions," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4028–4039, Jul./Aug. 2020.

[11] R. Han et al., "Modulated model predictive control for reliability improvement of extremely low frequency power amplifier via junction temperature swing reduction," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 302–313, Jan. 2022.

[12] C. Yang et al., "Electrothermal performance-based FCS-MPC for dynamic thermal balance control of traction converters," *IEEE Trans. Transp. Electrif.*, vol. 8, no. 1, pp. 277–287, Mar. 2022.

[13] J. Zhang, X. Du, C. Qian, Y. Ye, and J. Zhou, "Design of reference junction temperature swing of power module for thermal management," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 1132–1143, Jan. 2023.

[14] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765–776, Jan. 2018.

[15] J. Zhang, X. Du, C. Qian, R. Du, X. Hu, and H.-M. Tai, "Thermal management of IGBT module in the wind power converter based on the ROI," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8513–8523, Aug. 2022.

[16] A. Isidori, F. M. Rossi, F. Blaabjerg, and K. Ma, "Thermal loading and reliability of 10-MW multilevel wind power converter at different wind roughness classes," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 484–494, Jan./Feb. 2014.

[17] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Discontinuous-modulation-based active thermal control of power electronic modules in wind farms," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 301–310, Jan. 2019.

[18] E. Ugur, S. Dusmez, and B. Akin, "An investigation on diagnosis-based power switch lifetime extension strategies for three-phase inverters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 2064–2075, Mar./Apr. 2019.

[19] T.-M. Phan, N. Oikonomou, G. J. Riedel, and M. Pacas, "PWM for active thermal protection in three level neutral point clamped inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, Sep. 2014, pp. 3710–3716.

[20] T.-M. Phan, G. J. Riedel, N. Oikonomou, and M. Pacas, "Active thermal protection and lifetime extension in 3L-NPC-inverter in the low modulation range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 2269–2276.

[21] M.-H. Nguyen, S. Kwak, and S. Choi, "Model predictive control algorithm for prolonging lifetime of three-phase voltage source converters," *IEEE Access*, vol. 11, pp. 72781–72802, 2023.

[22] M.-H. Nguyen, S. Kwak, and S. Choi, "Modified discontinuous pulsewidth modulation approach with independent phase loss adjustment for voltage source converters," *IEEE Access*, vol. 11, pp. 115529–115555, 2023.

[23] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point-clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 835–845, Feb. 2014.

[24] K. Ma and F. Blaabjerg, "Modulation methods for three-level neutral-point-clamped inverter achieving stress redistribution under moderate modulation index," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 5–10, Jan. 2016.

[25] J. Zhou and P.-T. Cheng, "Modulation methods for 3L-NPC converter power loss management in STATCOM application," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4965–4973, Sep./Oct. 2019.
[26] J. Zhou, S.-C. Shie, and P.-T. Cheng, "A loss redistribution technique for the power devices in the NPC converter by PWM zero-sequence injection," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7049–7059, Jun. 2021.
[27] G. S. Buja, "Optimum output waveforms in PWM inverters," *IEEE Trans. Ind. Appl.*, vol. IA-16, no. 6, pp. 830–836, Nov. 1980.
[28] T. Geyer, P. Karamanakos, and I. Koukoula, "Optimized pulse patterns with bounded semiconductor losses," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3233–3243, Mar. 2024.
[29] A. Birth, T. Geyer, H. d. T. Mouton, and M. Dorfling, "Generalized three-level optimal pulse patterns with lower harmonic distortion," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5741–5752, Jun. 2020.
[30] I. Koukoula, P. Karamanakos, and T. Geyer, "Loss-constrained three-level optimized pulse patterns with robustness to power factor variations," *IEEE Trans. Ind. Appl.*, vol. 61, no. 4, pp. 6511–6523, Jul./Aug. 2025.
[31] T. Dorfling and T. Geyer, "Thermally constrained optimized pulse patterns for medium-voltage neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13160–13176, Oct. 2024.
[32] I. Koukoula, P. Karamanakos, and T. Geyer, "On bounding the junction temperature by means of optimal modulation with relaxed properties," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Oct. 2024, pp. 3877–3884.
[33] A. Pérez-Basante, S. Ceballos, G. Konstantinou, J. Pou, I. Kortabarria, and I. M. de Alegría, "A universal formulation for multilevel selective-harmonic-eliminated PWM with half-wave symmetry," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 943–957, Jan. 2019.
[34] I. Koukoula, P. Karamanakos, and T. Geyer, "Fast computation of optimized pulse patterns for multilevel converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Oct. 2024, pp. 4352–4354.
[35] "Asymmetric integrated gate-commutated thyristor 5SHY 55L4500," Hitachi Energy, Zürich, Switzerland, 2013. [Online]. Available: https://www.hitachienergy.com/products-and-solutions/semiconductors/integrated-gate-commutated-thyristors-igct/asymmetric-and-reverse-conducting
[36] "Fast recovery diode 5SDF 20L4520," Hitachi Energy, Zürich, Switzerland, 2017. [Online]. Available: https://www.hitachienergy.com/products-and-solutions/semiconductors/diodes

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