Three-Leg Operation of Back-to-Back Converters

Christos Leontaris, Gean Jacques Maia de Sousa, and Marcelo Lobo Heldwein, *Senior Member, IEEE*

***Abstract*—Bidirectional integrated motor drive systems require compact power converter designs that fit inside an electric machine housing. Therefore, high switching frequency is desirable, but it leads to increased heat generation, complicating the cooling strategy. Wide bandgap power semiconductors enable a reduction in switching losses, but this can be further improved by reducing the total number of switching transitions. This work introduces a voltage source back-to-back converter (V-BBC) that is operated in a holistic manner to reduce the total switching losses. The proposed concept is based on the synergetic control of the two converters, requiring only three out of six legs to switch at any given switching cycle. An 11-kW hardware prototype is presented, and its design is optimized. It achieved a power density of $\rho = 4.7\ \mathrm{kW/dm^3}$ and measured efficiencies above 98.2% at 100 kHz and above 98.5% at 50 kHz switching frequency. Peak efficiencies were $\eta = 98.68\%$ and $\eta = 98.87\%$ for 100 and 50 kHz, respectively, for equal input and output frequencies and voltages. Losses were compared to conventional V-BBC operation using state-of-the-art discontinuous modulation, showing significant improvement across the entire operating range.**

***Index Terms*—Synergetic control, three-phase ac–ac converter, variable speed drive (VSD) systems, voltage source back-to-back converter (V-BBC).**

I. Introduction

SYSTEMS driven by electric motors are responsible for more than 40% of all global energy consumption. This amount could be reduced by 30% by the end of the decade if multiple energy efficiency measures are used [1]. One important measure is the wide use of variable speed drive (VSD) systems. The integrated motor drive (IMD) concept further integrates the power electronic systems into an electric machine housing, enabling higher efficiency and overall higher power density, reducing also raw material usage. To achieve that, the power converter itself has to be very efficient and power dense [2]. An IMD system also eliminates the need for long cables to connect the machine and the inverter stage. This is significant, as these cables are heavy and expensive, and due to the switched PWM voltage at the inverter's output port, transmission line effects in long cables can deteriorate the machine insulation [3].

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The authors are with the Chair of High-Power Converter Systems, Technical University of Munich (TUM-HLU), 80333 Munich, Germany (e-mail: christos.leontaris@tum.de; gean.sousa@tum.de; marcelo.heldwein@tum.de).

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Many ac–ac topologies capable of interfacing a three-phase grid with a motor have been proposed in the literature. For example, in [4], the most common topology, a voltage source back-to-back converter (V-BBC), is analyzed and compared with other configurations targeting high power density ac–ac applications. This topology is preferred due to its simplicity and the low number of semiconductors required (12 MOSFETs). A 60° discontinuous pulse width modulation (DPWM) modulation is applied to both the rectifier and inverter stages, while the dc-link voltage is kept constant at 650 V. The study concludes that the V-BBC exhibits the lowest losses among the compared topologies, but suffers from higher weight due to the larger filter size. In addition, the current source back-to-back converter (C-BBC) has also been proposed as an alternative for grid-tied VSD applications, and a synergetic control of its current source rectifier and inverter has already been implemented [5]. In the C-BBC, the required filter volume is minimized, as only two magnetic components are employed. The voltage driving the machine is mostly sinusoidal, effectively reducing harmonic losses in the motor [6], [7]. However, for a 230-V rms grid, 12 bidirectional devices are required so that a typical SiC-based implementation leads to 24 MOSFETs, significantly increasing costs. Another compact ac–ac converter concept is the matrix converter (MC) [8]. It eliminates the need for energy storage components, extending system lifetime by avoiding dc-link capacitors, and achieves high efficiency. However, the main drawback of the MC is its lack of voltage step-up capability. Finally, a three-stage alternative has also been proposed. In [9], a three-stage ac–ac converter employing a synergetic control strategy is introduced. A two-level voltage source rectifier (VSR) connects to the grid, a current source inverter supplies sinusoidal voltages to the machine, and a buck-type dc–dc converter acts as an interface between the rectifier and inverter, facilitating synergetic operation among all stages.

In this work, an operation concept for a bidirectional power conversion system based on a V-BBC, as shown in Fig. 1, is introduced, which utilizes synergetic control to achieve very low switching losses. A VSR is connected to the grid, while a voltage source inverter (VSI) drives an ac load. Electromagnetic compatibility (EMC) filters are included exemplarily in both ac ports. The main idea behind the proposed modulation strategy is to minimize the number of switching transitions and ensure that the dc-link voltage is always kept at the minimum possible level, thereby reducing switching losses. This is achieved by observing the V-BBC as a single converter, where the minimum amount of legs that are required to switch at the switching frequency at any instant is only 3. Thus, semiconductors with low ON-state resistance, $R_{\mathrm{ds,on}}$, can be used, as conduction losses remain largely unaffected by the proposed modulation approach.

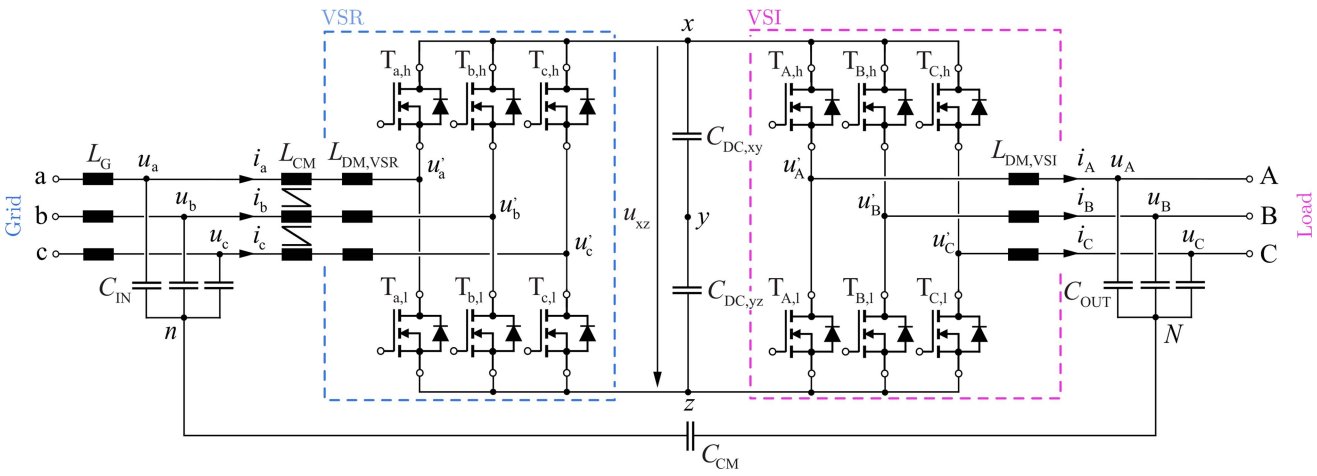

Fig. 1. Power circuit of the V-BBC. A VSR interfaces with the grid, while a VSI drives a load. A first stage DM/CM EMC filter is considered. A common mode (CM) capacitor C_{CM} acts as a short-circuit at high frequencies between the input and the output, helping reduce external CM current circulation.

The rest of this article is organized as follows. Section II presents the operation strategy that drives the converter system. A design procedure is explained in Section III, from which an 11-kW ac–ac system prototype is constructed and its experimental results are discussed in Section IV. Finally, Section V concludes this article.

II. Operation Principle

The proposed concept considers that the V-BBC in Fig. 1 is modulated through pulse width modulation (PWM) and each of its phase legs are driven with modulation signals d_j, with $j = \mathrm{a}, \mathrm{b}, \mathrm{c}$, and d_k, with $k = \mathrm{A}, \mathrm{B}$, and C. Fig. 2 depicts the main waveforms of the employed PWM strategies. Fig. 2(a) illustrates the negative 2/3 DPWM modulation with 120° clamping intervals at the negative dc-link rail [10], also known as discontinuous pulse width modulation (clamp-to-min) (DPWM-MIN) [11]. At any time interval, only two out of the three legs of a voltage source converter (VSC) are switching at the carrier frequency. This mode of operation ensures sinusoidal currents even though one leg is clamped since the three-phase currents sum to zero, i.e., controlling two-phase currents inherently determines the third. For this mode of operation, as with most PWM modulation using zero-axis signal injection, the minimum constant dc-link voltage required is equal to the maximum of the phase-to-phase voltages, $\sqrt{3} \cdot \hat{U}_{\mathrm{m}}$, where $\hat{U}_{\mathrm{m}}$ is the peak of the phase-to-neutral voltage. Also, for the negative 2/3 DPWM modulation, the zero-axis component, d_{CM}, added equally to all three modulation signals, presents no discontinuity. In contrast, in the positive and negative 2/3 DPWM modulations, the zero-axis component has discontinuities, leading to abrupt steps in the modulation signals and resulting in distortion of the current waveforms [11]. Therefore, negative 2/3 DPWM modulation is selected for the ac–ac converter application under consideration. The disadvantage, however, is an uneven distribution of losses in the semiconductors. Any discontinuous modulation strategy should, in principle, work.

Fig. 2(b) illustrates the 1/3 DPWM modulation. Only one out of the three phase legs is switched over any switching period [10], [12], [13], [14]. This modulation features a variable dc-link voltage that follows the envelope of the largest absolute phase-to-phase voltage. In this case, the number of switching transitions is further reduced, and the dc-link voltage is minimized while still ensuring sinusoidal currents, as long as the power injected into the dc-link by the other converter is constant. Consequently, this modulation strategy appears promising for reducing switching losses. The modulation strategy discussed in this work emphasizes using the 1/3 DPWM modulation as much as possible across the converter's entire operating range.

A set of sinusoidal three-phase grid voltages $u_{\mathrm{a,b,c}}$ is defined here as

$$u_j = \hat{U}_{\mathrm{m}} \sin(\omega_{\mathrm{m}} t - \theta_j), \text{ with } j = \mathrm{a}, \mathrm{b}, \mathrm{c}$$
$$\theta_{\mathrm{a}} = 0,\ \theta_{\mathrm{b}} = \tfrac{2\pi}{3},\ \theta_{\mathrm{c}} = -\tfrac{2\pi}{3} \tag{1}$$

where $\hat{U}_{\mathrm{m}} = \sqrt{2} \cdot 230\ \mathrm{V}$ is the amplitude of the grid phase voltage, and $\omega_{\mathrm{m}} = 2\pi f_{\mathrm{m}}$, $f_{\mathrm{m}} = 50$ Hz, is the grid frequency. In the same manner, a load side set of voltages $u_{\mathrm{A,B,C}}$ is defined as

$$u_k = \hat{U}_{\mathrm{o}} \sin(\omega_{\mathrm{o}} t - \phi - \theta_k), \text{ with } k = \mathrm{A}, \mathrm{B}, \mathrm{C}$$
$$\theta_{\mathrm{A}} = 0,\ \theta_{\mathrm{B}} = \tfrac{2\pi}{3},\ \theta_{\mathrm{C}} = -\tfrac{2\pi}{3} \tag{2}$$

where $\hat{U}_{\mathrm{o}}$ is the amplitude of the load phase voltage, $\omega_{\mathrm{o}} = 2\pi f_{\mathrm{o}}$, where f_{o} is the load fundamental frequency, which varies if the load is an electric machine under different operating points, and ϕ is an arbitrary phase angle between the grid and machine three-phase voltages.

The proposed scheme attains minimum switching losses in part by ensuring the minimum possible dc-link voltage u_{xz} under which the converter adequately operates. In order to define it, the phase-to-neutral voltages of the grid are initially sorted into maximum and minimum values, $u_{\mathrm{VSR,max}} = \max(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}})$ and $u_{\mathrm{VSR,min}} = \min(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}})$. The other phase is denoted as $u_{\mathrm{VSR,mid}}$. Similarly, for the phase-to-neutral load voltages: $u_{\mathrm{VSI,max}} = \max(u_{\mathrm{A}}, u_{\mathrm{B}}, u_{\mathrm{C}})$, $u_{\mathrm{VSI,min}} = \min(u_{\mathrm{A}}, u_{\mathrm{B}}, u_{\mathrm{C}})$, with the remaining phase denoted as $u_{\mathrm{VSI,mid}}$. The potential six-pulse shape dc-link waveforms are then used to define the

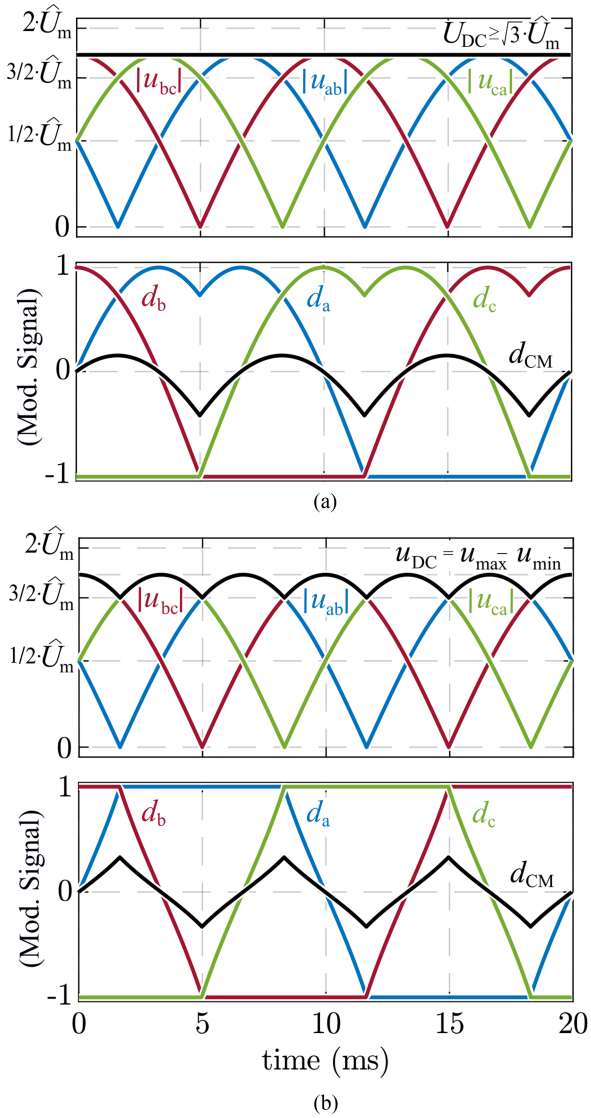

Fig. 2. Key characteristic waveforms for different PWM strategies. (a) Negative 2/3 DPWM modulation; only two out of three half-bridges are switching. The half-bridge that corresponds to the lowest phase voltage is clamped to the negative DC-link rail. (b) 1/3 DPWM modulation; only one half-bridge is switching. The DC-link voltage follows the envelope defined by the largest absolute phase-to-phase voltage.

dc-link voltage that should ideally be employed, i.e.,

$$u_{\mathrm{xz}} = \max(u_{\mathrm{VSR},13}, u_{\mathrm{VSI},13}) \tag{3}$$

with

$$\begin{aligned} u_{\mathrm{VSR},13} &= u_{\mathrm{VSR,max}} - u_{\mathrm{VSR,min}} \\ u_{\mathrm{VSI},13} &= u_{\mathrm{VSI,max}} - u_{\mathrm{VSI,min}} \end{aligned} \tag{4}$$

such that the converter, which interfaces the ac side having the highest instantaneous line voltage, operates with 1/3 DPWM modulation. The other converter operates with negative 2/3 DPWM modulation. The modulation signals for the converters need to take into account that the dc-link voltage is not constant. When the grid voltage is higher than the load voltage, the VSR operates with 1/3 DPWM modulation. Conversely, when the machine voltage is higher, the VSI operates with 1/3 DPWM modulation. In the transition region, where the grid and machine voltages are nearly identical in amplitude, i.e., when the $u_{\mathrm{VSR},13}$ and $u_{\mathrm{VSI},13}$ quantities intersect, the dc-link voltage switches from one quantity to the other, ensuring that it always follows the maximum. The VSR and VSI operations continuously alternate between 1/3 and negative 2/3 DPWM modulations under these circumstances.

The zero-axis component injection for both 1/3 and negative 2/3 DPWM modulations can be represented through a single equation [10], ensuring a smooth transition between these two modes of operation. This is defined as

$$d_{\mathrm{VSR-I,CM}} = \frac{u_{\mathrm{VSR-I,min}}}{u_{\mathrm{xz}}/2} - 1. \tag{5}$$

Adding this component to the modulation signals of both converters results in

$$\begin{aligned} d_{\mathrm{VSR-I,max}} &= (u_{\mathrm{VSR-I,max}})/(u_{\mathrm{xz}}/2) + d_{\mathrm{VSR-I,CM}} \\ d_{\mathrm{VSR-I,mid}} &= (u_{\mathrm{VSR-I,mid}})/(u_{\mathrm{xz}}/2) + d_{\mathrm{VSR-I,CM}} \\ d_{\mathrm{VSR-I,min}} &= (u_{\mathrm{VSR-I,min}})/(u_{\mathrm{xz}}/2) + d_{\mathrm{VSR-I,CM}} \end{aligned} \tag{6}$$

where $d_{\mathrm{VSR-I,max}}$, $d_{\mathrm{VSR-I,mid}}$, and $d_{\mathrm{VSR-I,min}}$ are the corresponding modulation signals to the converter leg connected to the maximum, middle, and minimum phase-to-neutral voltage, for the VSR and the VSI stages, respectively.

Fig. 3 presents simulation results showing the three different operation regions, i.e., VSR with 1/3 DPWM modulation, VSI with 1/3 DPWM modulation, and the transition region. When the grid voltage is higher than the load voltage, the dc-link voltage follows the six-pulse shape envelope of the grid. As a result, the switching voltage of the VSR is clamped for a total of 240° to either the positive or negative dc-link rail [see Fig. 3(b)], while the switching voltage of the VSI is clamped for 120° to the negative dc-link rail [see Fig. 3(c)]. The opposite pattern occurs when the load voltage is greater than the grid voltage. In the transition region, where $u_{\mathrm{VSR},13}$ and $u_{\mathrm{VSI},13}$ intersect, the dc-link voltage is set to the maximum of these values at each time instant. The converter with the highest ac-side voltage operates under 1/3 DPWM modulation, while the other operates with negative 2/3 DPWM modulation. This approach maximizes the use of 1/3 DPWM modulation, ensuring the minimum number of switching transitions and the lowest possible dc-link voltage. The grid currents are sinusoidal and, exemplarily, in phase with the grid voltage, i.e., approaching unity power factor. The currents supplied to the load are also sinusoidal, with amplitude and frequency depending on the operating point. In these simulations, a resistive load of 20 Ω is used with an output frequency f_{o} ramping up to 60 Hz. Fig. 3(d) presents the calculated zero-axis injection signals, $d_{\mathrm{VSR,CM}}$ and $d_{\mathrm{VSI,CM}}$, for both VSR and VSI. Fig. 3(e) and (f) illustrates the modulation signals for the VSR and VSI, respectively, while Fig. 3(g) and (h) shows the switching signals for the upper switch of phase a in the VSR and phase A in the VSI, respectively.

A potential control scheme based on the concept is illustrated in Fig. 4. A key requirement for proper operation is correctly shaping the dc-link voltage, u_{xz}, to follow the maximum value

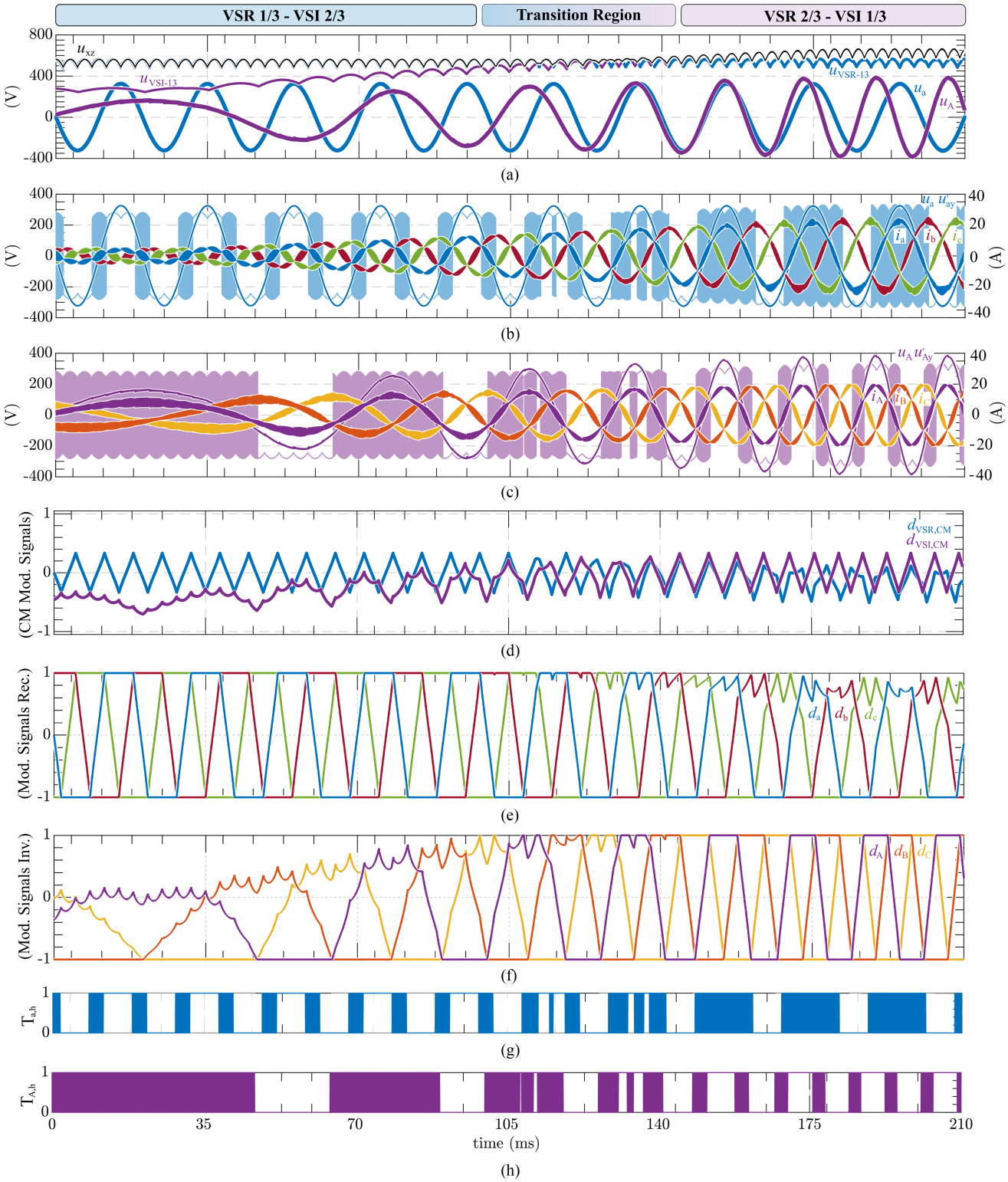

Fig. 3. Simulation waveforms for the proposed synergetic control of the V-BBC illustrate the three different operation modes. Initially, the amplitude of the load voltage u_{A} is lower than the amplitude of the grid voltage u_{a}. It gradually increases, fully surpassing the grid voltage at the end of the transition region. (a) Phase-to-neutral voltages on the grid and load sides, as well as the six-pulse shape signals $u_{\mathrm{VSR,13}}$ and $u_{\mathrm{VSI,13}}$, which define the DC-link voltage as it follows the envelope of their maxima. (b) Switching voltage of the VSR along with the grid currents, which are sinusoidal and in phase with the grid voltage, enabling high power factor. (c) Switching voltage of the VSI and load currents. (d) Zero-axis modulation signals for the VSR and the VS. (e) and (f) Modulation signals of the VSR and VSI, respectively. (g) and (h) PWM switching signals for the upper device of phase a of the VSR and phase A of the VSI, respectively. For this simulation, a resistive load of 20 Ω is considered. The load power is increased from 2 to 11 kW, while the output frequency f_{o} ramps up to 60 Hz. Simulation parameters are the same as for the final prototype, as presented in Table II.

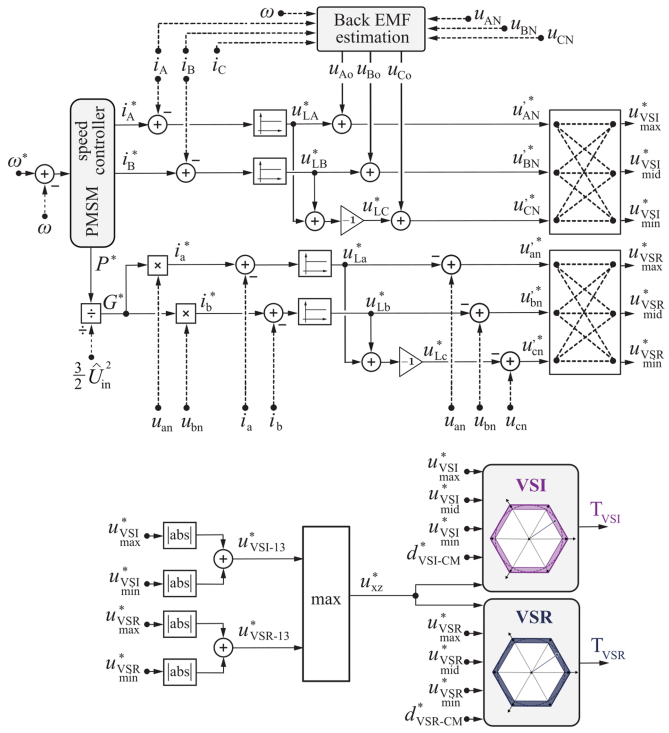

Fig. 4. Control block diagram for the V-BBC synergetic operation. A speed control motor drive application is considered, where the main input is the reference speed, ω^*. The speed controller determines the machine currents, $i^*_{\mathrm{A,B,C}}$ and the power reference P^*. The output currents are controlled through P-controllers, and the estimated back-EMF voltages are added to their outputs, which defines the differential voltages to be synthesized by the VSI. The power reference P^*, together with the amplitude of the grid voltage, defines the transconductance G^*. By multiplying this by the grid voltages, the references for the grid currents are obtained. These currents are almost in phase with the grid voltage and sinusoidal, resulting in power factor close to unity. P-controllers estimate the necessary LF voltages across the input boost inductors, while adding the measured grid voltages yields the average differential voltages to be synthesized by the VSR. Both VSR and VSI average voltages are sorted into maximum, middle, and minimum values. The $u^*_{\mathrm{VSR},13}$, $u^*_{\mathrm{VSI},13}$ references are generated, and the maximum of these defines the DC-link voltage reference, u^*_{xz}. Finally, the modulation signals are calculated within the respective modulators.

of the VSR and VSI six-pulse shape waveforms (3). Initially, the load angular speed reference, ω^*, is compared with the actual speed ω; a speed controller generates the machine reference currents, $i^*_{\mathrm{A,B,C}}$, and the power reference P^*. The power reference, along with grid voltage amplitude, is used to estimate the transconductance G^* of the VSR. The input current references are derived by multiplying this transconductance by the measured grid voltages. A P-controller compels the input currents to follow their sinusoidal references, achieving close to unity power factor. The reference average voltages at the VSR switching nodes, $u'^*_{\mathrm{an,bn,cn}}$, are computed. Similarly, a P-controller shapes the output currents, where the estimated load back-EMF voltages are added to their outputs, resulting in the average differential voltage to be synthesized by the VSI, $u'^*_{\mathrm{AN,BN,CN}}$. By sorting $u'^*_{\mathrm{an,bn,cn}}$ and $u'^*_{\mathrm{AN,BN,CN}}$ into maximum, middle, and minimum values, the $u^*_{\mathrm{VSR},13}$ and $u^*_{\mathrm{VSI},13}$ references are calculated. The maximum of these values determines the dc-link voltage reference, u^*_{xz}. This dc-link voltage reference, along with the switching node average voltage references and the CM components (5), defines the modulation signals based on (6).

TABLE I
MOTOR OPERATION REGION

	Description	Values
$P_{\mathrm{o,N}}$	Nominal power	11 kW
$\hat{I}_{\mathrm{o}}$	Peak current	18.8 A
$f_{\mathrm{o,N}}$	Nom. El. freq.	60 Hz
$[f_{\min},\ f_{\max}]$	El. freq . range	0–60 Hz
$U_{\mathrm{o,ph,RMS,N}}$	Nominal rms Ph. volt.	276 V
P.F.	Power factor	1.0

III. DESIGN PROCEDURE

To assess the performance of the proposed topology and modulation strategy, a design based on an optimization procedure is conducted. Special attention is given to estimating the switching and conduction losses of the semiconductors. In particular, a double-pulse test (DPT) setup is constructed to characterize the SiC devices in hand.

First, the machine's operating range is defined. The converter is designed for an 11-kW permanent magnet synchronous machine (PMSM) with a nominal electrical frequency of 60 Hz. The PMSM operates in constant current–torque mode at 18.8 A peak. As the motor's mechanical speed increases, the electrical output frequency increases until 60 Hz, and the power increases linearly with it ($P_{\mathrm{o}} \propto f$) reaching at the end of the nominal power of 11 kW. More details of the PMSM operating range are provided in Table I. A power factor of ≈ 1.0 for the machine is assumed.

A. Semiconductor Characterization

One semiconductor device is considered in this design [15]. This device, C3M0016120 K (1200 V, 16 mΩ), is characterized with the DPT setup, as presented in Fig. 5. A polynomial fitting is applied to the DPT measurement data [17] to enable extrapolation and use in estimating the switching converter losses. The conduction losses are estimated based on the ON-state resistance, determined from the datasheet value of $R_{\mathrm{ds,on}}$ at 100 °C and $u_{\mathrm{gs}} = 15$ V.

Fig. 6 shows the estimated semiconductor losses for the entire operation range. The black line indicates losses for the conventional modulation strategy with constant dc-link voltage, fixed at $\sqrt{3} \cdot \max(\hat{U}_{\mathrm{m}}, \hat{U}_{\mathrm{o}})$, using negative 2/3 DPWM modulation for both the rectifier and inverter. The losses are unaffected by any disposition between grid and machine voltage since the dc-link voltage is constant. It is important to note that this scenario assumes the best case for the state-of-the-art modulation since practical dc-link voltages are typically set with +15% margin above this minimum value [18]. In contrast, the yellow and blue lines represent the losses for the proposed modulation strategy. These losses are influenced by the relative phase between grid and machine voltages, as the dc-link is dynamically adjusted to follow the maximum six-pulse shape waveform of these voltages. This difference is more noticeable at 50 Hz operation,

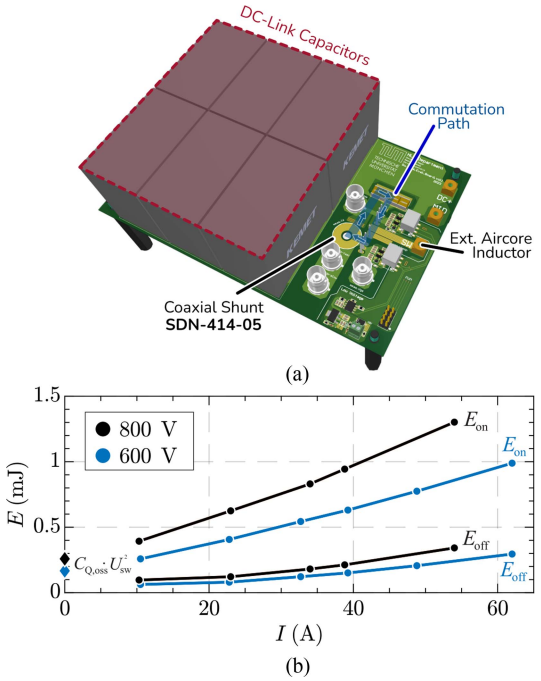

Fig. 5. DPT setup is used to characterize the C3M0016120 K (1200 V, 16 mΩ) device. (a) DPT hardware, with the commutation path highlighted and optimized to match the converter's prototype printed circuit board (PCB) layout. Current measurement is performed using a coaxial shunt, SDN-414-05 [16]. The external gate resistance is set to $R_{G,on/off} = 2\ \Omega$. (b) Experimental results, showing E_{on} and E_{off} energies for different current values, at 600 and 800 V DC link.

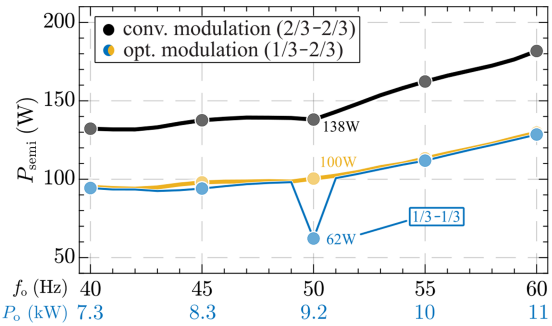

Fig. 6. Semiconductor losses across the entire operating range. Based on the DPT experimental data and simulation waveforms, estimation of the switching and conduction losses during the converter's operation. The semiconductor losses with conventional modulation are shown in black; in this case, the DC-link voltage remains constant at $\sqrt{3} \cdot \max(\hat{U}_m, \hat{U}_o)$, with negative 2/3 DPWM modulation applied to both the rectifier and inverter. The proposed modulation's estimated losses are shown in yellow and blue, representing the worst and best case scenarios, respectively. This difference reflects variations in the shape of the DC-link voltage due to any relative disposition of the grid and machine voltages, influencing the overall semiconductor losses. The selected switching frequency is $f_{sw} = 100$kHz for both VSR and VSI.

where both grid and machine voltages are 230 V rms. When the six-pulse waveforms of grid and machine are aligned and have the same amplitude, occurring when grid/machine voltages are phase-shifted by 0°, 60°, 120°, 180°, 240°, or 300°, both converters operate under 1/3 DPWM modulation, reducing total semiconductor losses to as low as 62 W.

TABLE II
PARAMETERS OF THE HARDWARE PROTOTYPE

	Description	Values
f_{sw}	Switching freq.	100 kHz
T_{VSR-I}	VSR-I semi.	C3M0016120K (1200 V, 16 mΩ)
$L_{DM,VSR-I}$	VSR-I DM ind.	140 µH (2 × KoolMu-60 E40/20, 22 turns)
L_{CM}	CM ind.	1.35 mH (2 × VAC 40/25/15, 3 × 6 turns)
L_G	DM ind.	6.8 µH (WE-7443640680B [21])
C_{IN}	VSR DM cap.	3.0 µF
$C_{DC,xy-yz}$	DC-link cap.	2 × 5.6 µF
C_{OUT}	VSI DM cap.	2.2 µF
C_{CM}	CM cap.	112 nF
ρ	Vol. power density	4.7 kW/dm^3
η	Max. meas. eff.	98.68% @ 100 kHz 98.87% @ 50 kHz

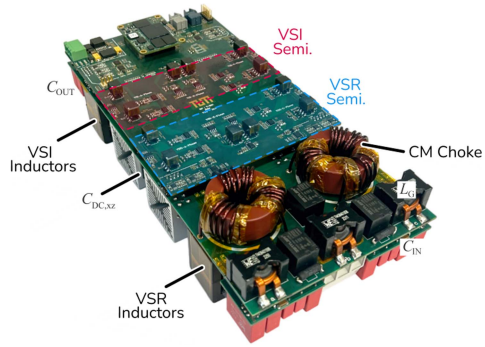

Fig. 7. Realized 11 kW hardware prototype with power density of 4.7 kW/dm^3 and dimensions of 280 × 132 × 63 mm^3.

B. Passive Components and Selected Design

To define the passive components, five distinct operating points of the system were selected: $f_o = 40$, 45, 50, 55, and 60 Hz with corresponding power levels of $P_o = 7.3$, 8.3, 9.2, 10, and 11 kW. At these operating points, the worst case capacitor charge conditions were identified, and the required capacitance was determined based on the allowable voltage ripple. For the differential mode (DM) capacitors C_{IN} and C_{OUT} at the ac side, the allowed worst case peak-to-peak voltage ripple is set to 1% of the grid peak phase voltage (325V). For the dc-link capacitors $C_{DC,xy-yz}$, the allowed peak-to-peak ripple is 2% of the grid peak phase-to-phase voltage (564V). For the CM capacitor C_{CM}, the voltage ripple limit is 10 V_{pk-pk}. For the magnetic design, including the DM inductors on both the grid and machine sides as well as the CM inductor, the inductance values were determined based on the allowable current ripple. The worst case voltage–time–area (V · s) was estimated, and the DM inductors were designed to allow a current ripple of 25% of the respective peak current, following the procedure of [19]. The CM inductance value was selected to limit the circulating high frequency (HF) common-mode current to below 0.5 A_{pk-pk} [20]. As mentioned, the SiC MOSFETmodel

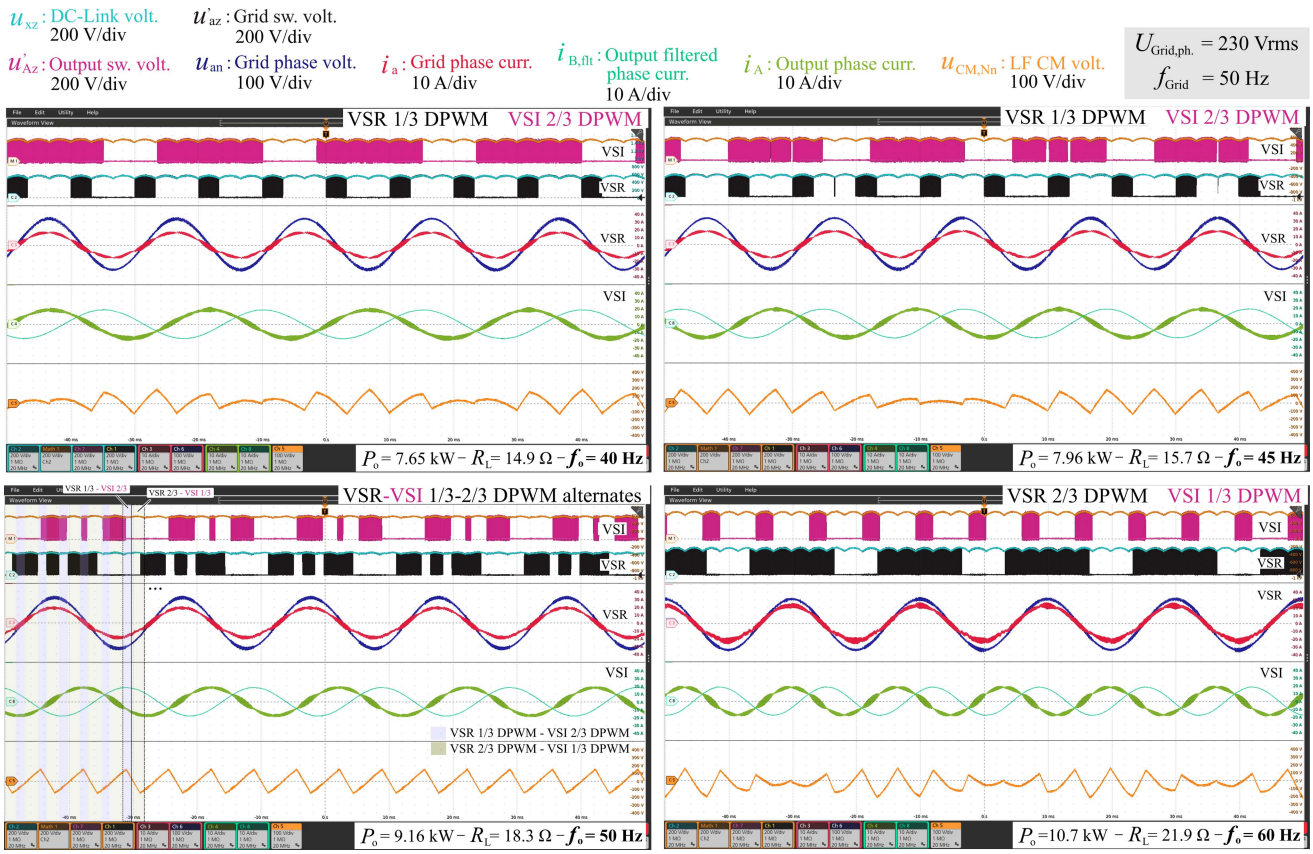

Fig. 8. Experimental waveforms of the converter with the proposed control scheme for four different operation points: 40, 45, 50, and 60 Hz output frequency. As the output frequency increases, the output power increases proportionally. For 40 and 45 Hz, the VSR operates with 1/3 DPWM modulation and the VSI with negative 2/3 DPWM modulation. The DC-link voltage follows the six-pulse waveform of the grid. At 50 Hz, the grid and machine voltages have the same amplitude and frequency, but the phase shift between them is arbitrary. Thus, the VSR and VSI change back and forth between 1/3 and negative 2/3 DPWM modulations, and the DC-link voltage follows the envelope of the maximum six-pulse shape waveform at each point in time. At 60 Hz, the VSI operates with 1/3 DPWM modulation, while the VSR uses negative 2/3 DPWM modulation. In all cases, the grid side operates with near unity power factor. The employed switching frequency is 100 kHz. The resistive load used in each case was chosen to approximate the machine operating point as closely as possible, based on available resistors.

C3M0016120K (1200 V, 16 mΩ) was chosen, and the switching frequency was fixed at $f_{sw} = 100$ kHz. After selecting the components that achieve the best tradeoff between power density and efficiency, the final power converter configuration is summarized in Table II.

IV. Experimental Results

The built 11 kW hardware prototype is presented in Fig. 7. It achieves a power density of $4.7\text{kW}/\text{dm}^3$ taking into account its boxed volume of $280 \times 132 \times 63$ mm^3.

A. Experimental Waveforms

Fig. 8 presents experimental waveforms from the hardware prototype at various operating points with the corresponding output frequency f_o, output power P_o, and resistive load R_L indicated for each case. The switching frequency is set to 100 kHz. For 40 and 45 Hz output frequencies, the grid voltage exceeds the output voltage and, thus, the dc-link voltage follows the six-pulse shape waveform related to the grid. The VSR operates under 1/3 DPWM modulation, while the VSI operates with negative 2/3 DPWM modulation. At the 45 Hz operating point, however, some transitions starts appearing between VSR–VSI 1/3–2/3 DPWM and VSR–VSI 2/3–1/3 DPWM modes. The amplitude of the grid current, i_a, is controlled based on the power to be transferred and remains in phase with the grid voltage ensuring near unity power factor. The output current, i_A, which drives the load, is also sinusoidal. After being filtered through the output DM capacitors, it appears as a predominantly sine wave. The low-frequency (LF) CM voltage $u_{CM,Nn}$, measured across the CM capacitor C_{CM}, is also presented. For different grid and machine frequencies, this CM voltage may become nonperiodic, if the ratio f_m/f_o is an irrational number. In addition, since negative 2/3 DPWM modulation is used, this CM voltage varies smoothly without abrupt changes. The high-frequency CM voltage is contained across the CM choke on the grid side. For a 50-Hz output frequency, the output voltage has the same amplitude as the grid voltage, so the dc-link voltage is determined by the maximum of the six-pulse waveforms of the grid and output voltages at each point in time. As a result, the converters alternate continuously between 1/3 and negative 2/3 DPWM modulations, minimizing switching transitions and maintaining the lowest possible dc-link voltage, resulting in the highest efficiency. Finally, for a 60-Hz output

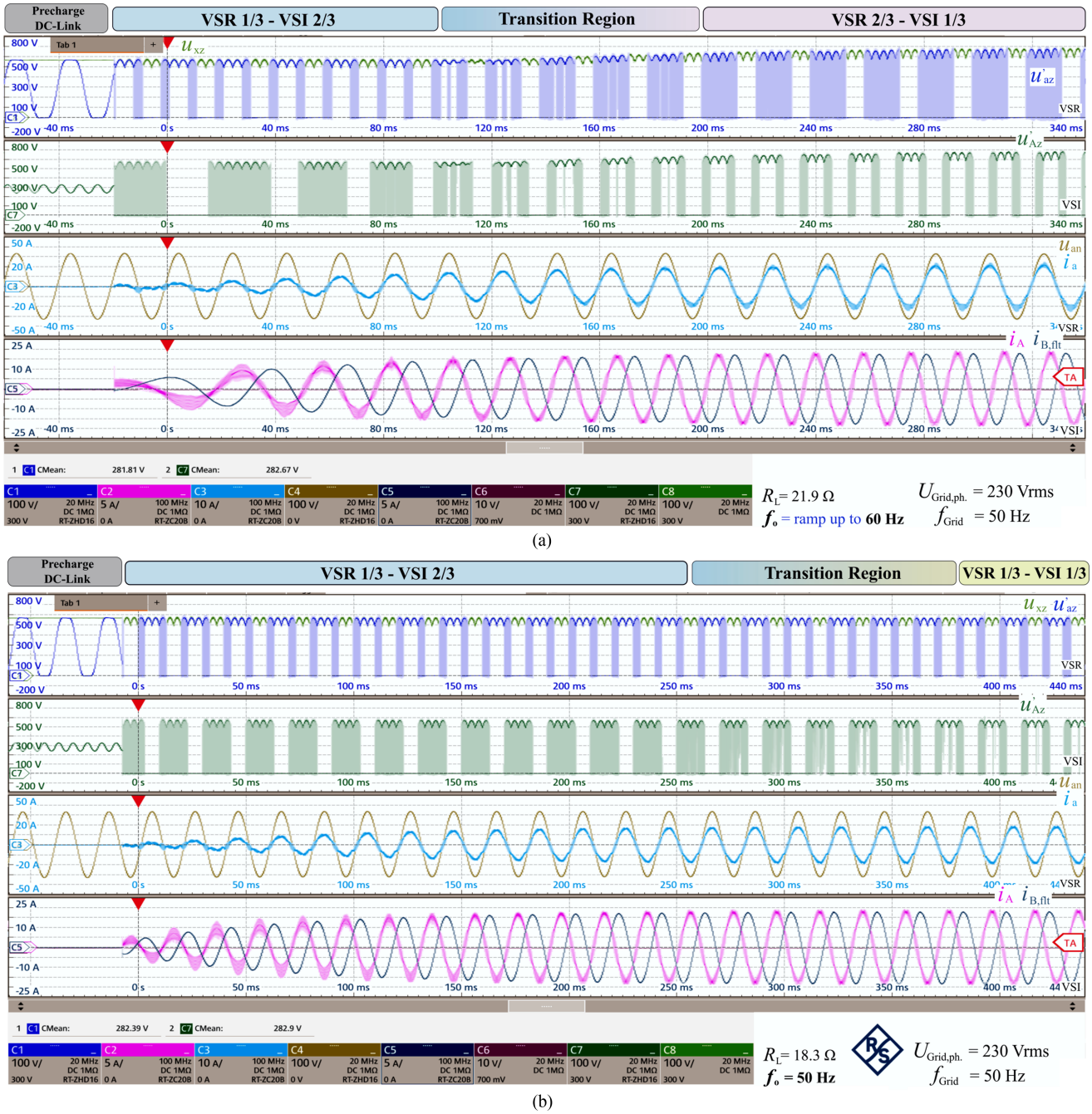

Fig. 9. Experimental waveforms of the converter with the proposed synergetic control for a full transition from start-up to a final operation point. (a) Transition, where the output current ramps up in both amplitude and frequency, reaching 60 Hz with a peak value of approximately 18.8 A, corresponding to the nominal 11 kW operation point. The V-BBC smoothly transitions through all operating modes. (b) Transition, where at the final operating point, the grid and machine phase voltages have equal amplitude and frequency with a 180° phase shift, resulting in both the VSR and VSI operating with 1/3–1/3 DPWM.

frequency, the output voltage exceeds the input voltage and, thus defines the dc-link voltage. The VSI operates under 1/3 DPWM modulation, and the VSR with negative 2/3 DPWM modulation.

Fig. 9 illustrates the complete transition of the V-BBC VSD system, from start-up to the final operating point. Fig. 9(a) shows an example of a machine drive application with a variable load current and frequency. After the dc-link precharge, the output current ramps up both in amplitude and frequency, reaching 60 Hz and a peak of approximately 18.8 A, which corresponds to the nominal 11 kW operating point. During the transient, the V-BBC operates through all its operating modes. Initially, while the output machine voltage is still low, the six-pulse shape dc-link voltage is defined by the grid side. The VSR operates with 1/3 DPWM, while the VSI operates with negative 2/3 DPWM. As the power and output voltage increase, the converter enters the transition region, where the VSR and VSI alternate continuously between 1/3 and 2/3 DPWM. This transition is

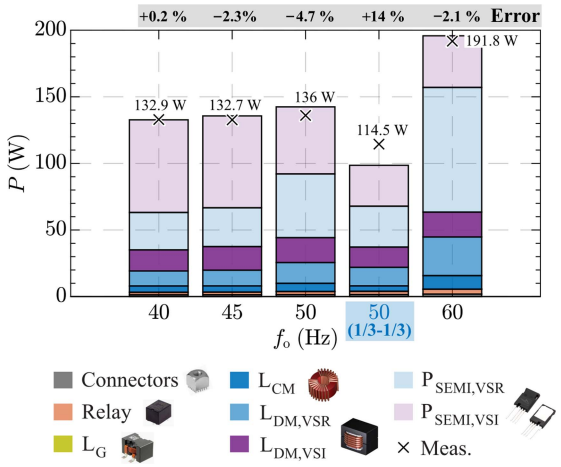

Fig. 10. Theoretical estimations of converter losses for four different operation points: 40, 45, 50, and 60 Hz output frequency. One converter operates with 1/3 DPWM modulation, while the other with negative 2/3 DPWM modulation. In addition, the special case, where both converters operate with 1/3 DPWM modulation, is included. The measurement results are shown with "×" alongside the theoretical estimations. The error between measured and calculated values is also presented. The switching frequency is 100 kHz.

smooth, since there is only a single duty cycle calculation (5) and (6) that applies regardless of the operating mode. Finally, once the output machine voltage exceeds the grid voltage, the dc-link voltage is defined by the output port, resulting in the VSR operating with negative 2/3 DPWM and the VSI with 1/3 DPWM. Fig. 9(b) highlights another case of system transition from start-up to the final operating point, where at the final point, both the grid and machine phase voltages have the same amplitude and frequency, and in this case a 180° phase shift. In this case, the output frequency was kept constant at 50 Hz (equal to the grid) during the whole transition. At the final operating point, both the VSR and VSI operate with 1/3–1/3 DPWM, meaning that only two out of the six legs of the total system are switching at any given point in time. To achieve this 1/3–1/3 DPWM operation, the output current peak value was manually adjusted so that the output phase voltage peak matches the grid phase voltage peak. In addition, the machine voltages have been synchronized to the grid voltages.

B. *Efficiency Measurements*

The achievable efficiency of the proposed synergetic control strategy is presented and compared with the efficiency that can be achieved with a conventional modulation strategy. Initially, in Fig. 10, measured losses are shown alongside theoretical estimations for the proposed synergetic control strategy. The operating points in the figure correspond to those shown in Fig. 8. In addition, losses are analyzed for the special case where, both, machine and grid voltages have identical amplitude, frequency, and phase shifts of either 0°, 60°, 120°, 180°, 240°, or 300°. For this comparison, a phase shift of 180° is selected. In these scenarios, where 1/3 DPWM modulation is employed in both converters, the total converter losses remain relatively constant irrelevant to the phase-shift condition. This is because the majority of the losses occur in the switches, and the switches experience similar losses under 1/3 DPWM modulation regardless of the phase shift. A difference can be observed in the magnetics, and especially in the CM choke core losses. For example, when the phase shift is 0°, the HF CM part of the voltage cancels out, resulting in reduced core losses, or, theoretically, zero core losses in the choke.

The losses from the connectors, relay, and small DM inductors [21] at the input side are relatively small. These losses were estimated by measuring the resistance of these components and calculating their conduction losses based on the rms current values. For the magnetic components, namely, $L_{\mathrm{DM,VSR}}$, $L_{\mathrm{DM,VSI}}$, and L_{CM}, both copper and core losses were analytically calculated. Improved generalized Steinmetz equations are used to estimate core losses, and Dowell equations for the winding losses. As the transferred power increases with higher output frequencies, magnetic losses increase, particularly on the VSR side where the current amplitude increases. Conversely, on the VSI side, the current amplitude remains constant due to the consideration of constant current mode machine operation. In the special case where 1/3 DPWM modulation is applied to both converters, the magnetic losses are minimized. The DM inductor losses are approximately the same for both VSR and VSI, and the CM choke losses are as small as 2 W for each of the two series-connected chokes.

Semiconductor switching losses dominate, resulting in higher overall losses when negative 2/3 DPWM modulation is employed. These losses are estimated based on the results presented in Section III. However, the parasitic capacitances of the switching node, $C_{\mathrm{PAR}} = C_{\mathrm{TIM}} + C_{\mathrm{IND}} + C_{\mathrm{PCB}}$, as measured in the hardware prototype, must also be considered when estimating switching losses. Here, $C_{\mathrm{TIM}} \approx 9$ pF, $C_{\mathrm{IND}} \approx 32$ pF, and $C_{\mathrm{PCB}} \approx 17$ pF, resulting in $C_{\mathrm{PAR}} \approx 58$ pF. The conduction losses are estimated using the ON-state resistance $R_{\mathrm{ds,on}}$ at 100°C and $u_{\mathrm{gs}} = 15$ V from the datasheet.

The difference between measured and predicted losses consistently remains below 5% (see Fig. 10), demonstrating the accuracy of the models used to estimate the total system losses. This also validates that the switching loss data obtained using the laboratory DPT setup align well with the experiments. A larger error in loss estimation of +14 % is observed in the case of 1/3 DPWM modulation for both converters. This discrepancy arises because, in practice, it is challenging to perfectly synchronize the six-pulse waveforms of the machine and grid sides at all times. As a result, unexpected switching transitions occur, as shown in Fig. 11.

Fig. 11 presents the efficiency and loss measurements for the proposed operation compared with conventional discontinuous modulation, where both converters operate with negative 2/3 DPWM modulation and a constant dc-link voltage. Results are shown for switching frequencies of both 100 and 50 kHz. The black/gray lines represent a carrier frequency of 100 kHz. For the conventional mode, at operation points 40, 45, and 50 Hz, the dc-link voltage is kept constant at 650 V, which includes a +15% margin above the minimum value of $\sqrt{3} \cdot \max(\hat{U}_{\mathrm{m}}, \hat{U}_{\mathrm{o}})$. For 60 Hz operation, the dc-link voltage is constant at 800 V (for 50 kHz switching frequency the dc-link voltage was 750

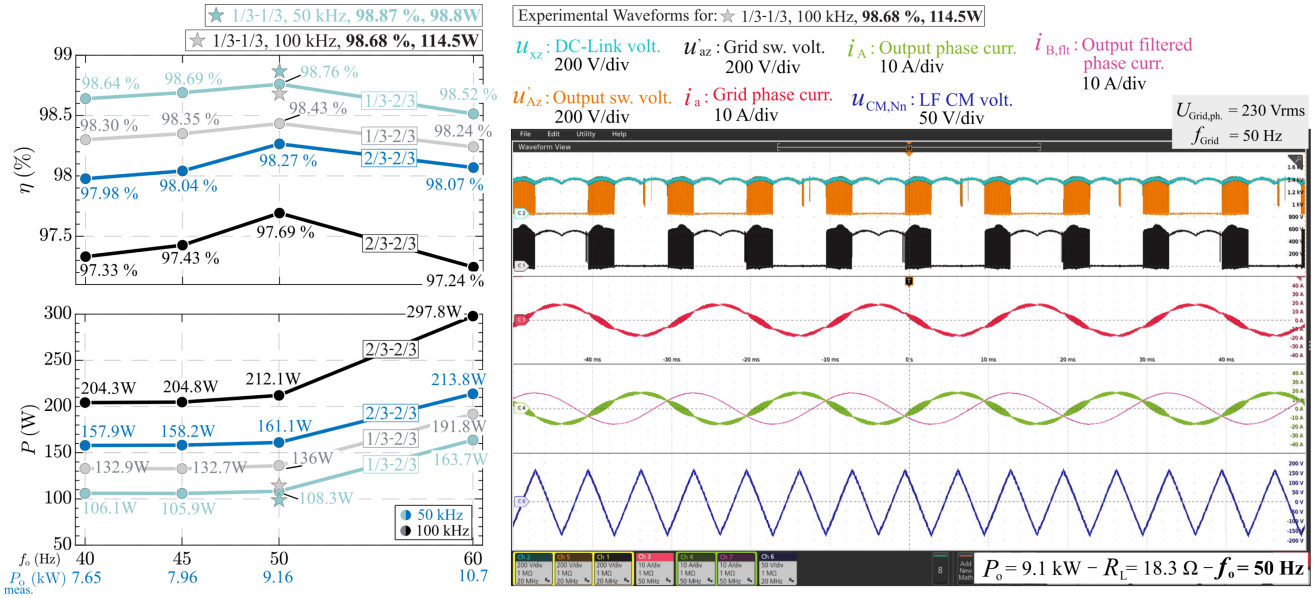

Fig. 11. Measured efficiency and loss curves, showing efficiency and losses versus output frequency f_o, representing different operating points. The black line represents the conventional modulation where both converters operate with negative 2/3 DPWM modulation at a 100 kHz switching frequency. The gray line corresponds to the proposed modulation, also at 100 kHz switching frequency. The blue and light blue lines show the conventional and proposed modulation, respectively, at a 50-kHz switching frequency. For the proposed modulation, the DC-link voltage follows the envelope of the maximum six-pulse waveforms, whereas in the conventional modulation, the DC-link voltage remains constant with a +15% margin above the minimum value of $\sqrt{3} \cdot \max(\hat{U}_m, \hat{U}_o)$, i.e., $U_{xz} \approx 650$ V for 40, 45, and 50 Hz, and $U_{xz} \approx 800$ V for 60 Hz. However, for the negative 2/3–2/3 DPWM modulation experiment at 60 Hz output frequency and 50 kHz switching frequency, the DC-link voltage was $U_{xz} \approx 750$ and not 800 V. In addition, the efficiency and losses for the special case of 1/3–1/3 DPWM modulation are highlighted with a star. An experimental waveform of the converter for this mode of operation, 100 kHz switching frequency, is also shown.

and not 800 V), which also includes a +15% margin. Across all these points, the proposed modulation nearly halves the losses compared to the conventional method. Efficiency peaks at 50 Hz operation for 100 kHz carrier frequency, reaching 98.43%, where maximum clamping of the switching cells of the VSR and VSI occurs, with both converters alternating between 1/3 and negative 2/3 DPWM modulation. In addition, for 100 kHz switching frequency, 1/3 DPWM modulation has also been implemented for both converters. These waveforms are shown in Fig. 11. Here, the grid and machine voltages have the same amplitude and frequency with a 180° phase shift. The LF CM voltage, shown in blue, is simply the superposition of the 1/3 DPWM CM voltage of both converters, i.e.,

$$u_{\mathrm{CM,LF}} = \frac{u_{\mathrm{VSR,max}} + u_{\mathrm{VSR,min}}}{2} - \frac{u_{\mathrm{VSI,max}} + u_{\mathrm{VSI,min}}}{2}. \quad (7)$$

Due to the 180° phase shift between the grid and machine voltages, the CM voltages align in phase and combine to produce a large, nearly triangular waveform, as depicted in the results. In this scenario, the efficiency reaches 98.68%, with total measured losses of only 114.5 W for the entire system. In addition, the same operating points were used with a lower carrier frequency of 50 kHz. The results are represented by the blue and light blue lines. At this switching frequency, the increased ripple in the DM currents enables regions of soft switching around each zero crossing of the currents. Soft-switching, combined with the lower switching frequency, leads to improved efficiency. This efficiency increase is particularly evident in the conventional modulation strategy, where both converters switch almost continuously. For the proposed modulation strategy, efficiency remains consistently above 98.50% across all operation region, peaking at 98.76% at 50 Hz output frequency operation. In the special case of 1/3 DPWM modulation applied to both converters, the system achieves an 98.87% efficiency, with total system losses reduced to just 98.8 W.

It should be noted that the deadtime has been set to a near optimum of $t_{\mathrm{deadtime}} = 100$ ns. In addition, the converter was originally optimized for a switching frequency of 100 kHz, which may not be the optimal choice. Halving the switching frequency to 50 kHz significantly increases efficiency while maintaining the same hardware and, thus, power density. Improving the design process in Section III by exploring a wider range of parameters, such as switching frequency, permissible current ripple, and different semiconductor devices, will possibly further increase the efficiency. However, the primary objective of this work is to showcase the proposed modulation scheme.

V. Conclusion

This work introduces a novel control–modulation concept for industrial bidirectional motor drive applications, where a rectifier is connected to the grid, ensuring near-unity power factor, and an inverter drives a load machine. The widely adopted V-BBC topology, featuring a two-level VSC on each side, is utilized. The proposed modulation strategy aims to reduce the switching transitions and ensures the minimum possible dc-link voltage, thereby enhancing efficiency. One converter operates at 1/3 DPWM modulation, while the other with negative 2/3 DPWM modulation with a variable dc-link voltage. During the transition region, the converters alternate seamlessly between

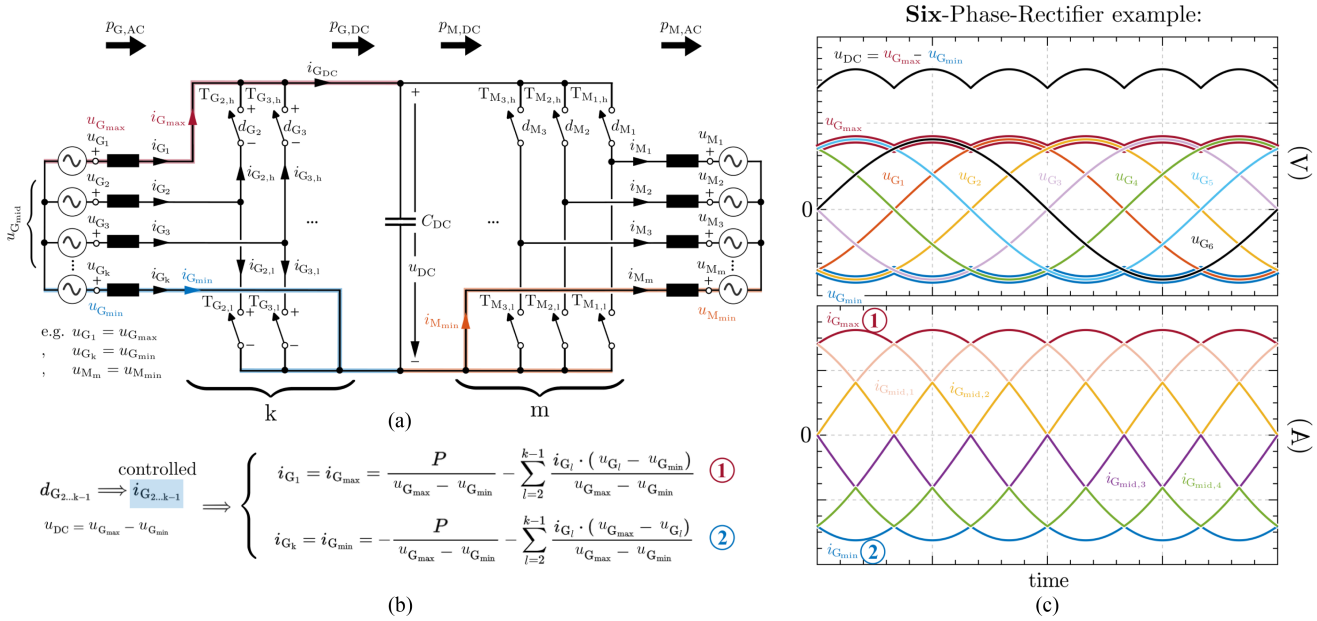

Fig. 12. Modeling of the V-BBC for k number of input phases and m number of output phases; mathematical equations for the proposed modulation scheme. (a) k-phase VSR operates with $(k-2)/k$ DPWM modulation, meaning that two phases are clamped to the positive or negative DC-link rail. The m-phase VSI operates with $(m-1)/m$ DPWM modulation, i.e., one phase is clamped. In total, only $k+m-3$ switching half-bridge legs are required to ensure constant power flow and sinusoidal currents in all input and output phases. (b) Mathematical equations for the input currents $i_{\mathrm{G_{max}}}$ and $i_{\mathrm{G_{min}}}$. These currents are not actively controlled, but it is shown that they naturally form parts of the sinusoidal input currents of the VSR. (c) Verifies the mathematical model using a six-phase rectifier. The upper part of the figure shows six-phase voltages that are phase-shifted by 60^{o}. The lower part shows the middle-phase currents, which follow the corresponding parts of the sinusoidal input currents. Similarly, and as derived from the equations in (b), the $i_{\mathrm{G_{max}}}$ and $i_{\mathrm{G_{min}}}$ currents are also components contributing to the formation of the sinusoidal input current waveforms.

1/3 and negative 2/3 DPWM modulation. A hardware prototype, featuring a power density of $\rho = 4.7\ \mathrm{kW/dm^3}$, was built to validate the proposed modulation scheme. Comparisons with a conventional modulation, where both converters operate with negative 2/3 DPWM modulation, highlight the advantages of the new approach. Across all operation points, efficiency remains above 98.2% at 100 kHz, and above 98.5% at 50 kHz carrier frequency, with peak efficiencies of 98.43% and 98.76% for 100 and 50 kHz, respectively. In the particular operation mode where both converters use 1/3 DPWM modulation, the measured efficiency reaches 98.68% and 98.87% for 100 and 50 kHz, respectively, translating to 99.34% and 99.43% efficiency per stage, respectively. Notably, in this mode, the rectifier and inverter experience identical losses. The proposed modulation achieves a significant reduction in total losses, reducing them by -35% compared to conventional modulation while maintaining the same hardware and power density. Further, optimization of the converter, particularly for lower switching frequencies and other power devices, could potentially push overall system efficiency beyond 99%.

Appendix A
Mathematical Derivation for Multiphase Systems

The operating principle of the synergistically controlled three-phase V-BBC converter is based on the idea that only three out of the six half-bridge legs are switching at any given time interval, while the other three are clamped to either the positive or negative dc-link rail. This concept can be extended for any number of input and output phases, denoted as k and m, respectively. The requirement is that there are always $k+m-3$ half-bridge legs switching.

Assuming the converter system presented in Fig. 12(a), with k grid phases and m machine phases. In addition, assume that the inverter operates with $(m-1)/m$ DPWM modulation, while the rectifier operates with $(k-2)/k$ DPWM modulation. On the inverter side, the phase with the minimum voltage is clamped to the negative dc-link rail. The analysis carried out in this section assumes the time interval where the phase m is clamped. The remaining phases $1,\ldots,m-1$, modulated with the modulation signals $d_{\mathrm{M}1,\ldots,m-1}$, control the corresponding currents $i_{\mathrm{M}1,\ldots,m-1}$ to be sinusoidal. In the case of a PMSM operating with unity power factor, these currents are in phase with the machine voltages $u_{\mathrm{M}1,\ldots,m-1}$. Since the sum of all phase currents must be zero, the current in the remaining phase is also sinusoidal. Multiplying the sinusoidal machine voltages and currents ideally results in a constant power on the machine, denoted as $p_{\mathrm{M,AC}}$. Neglecting any LF energy storage in the magnetic components and the dc-link capacitor, and ignoring losses in both the rectifier and inverter stages, the total power drawn from the grid is constant and equal to the output power

$$p_{\mathrm{G,AC}} = p_{\mathrm{G,DC}} = p_{\mathrm{M,DC}} = p_{\mathrm{M,AC}} = \sum_{l=1}^{m} u_{\mathrm{M}l} \cdot i_{\mathrm{M}l}. \quad (8)$$

The rectifier operates with $(k-2)/k$ DPWM modulation, meaning that two phases are clamped. Fig. 12(a) shows phase 1 and phase k clamped to the positive and negative dc-link rails,

respectively. This condition corresponds to the time interval where phase 1 has maximum voltage, $u_{\mathrm{G}1} = u_{\mathrm{G}\max}$, and phase k has minimum voltage, $u_{\mathrm{G}k} = u_{\mathrm{G}\min}$. The voltages of the remaining phases, $u_{\mathrm{G}2,\ldots,k-1}$, are between the maximum and minimum, and their corresponding half-bridges are switched according to the modulation signals $d_{\mathrm{G}2,\ldots,k-1}$.Therefore, the currents of these middle-voltage phases, $i_{\mathrm{G}2,\ldots,k-1}$, can be actively controlled. It is shown next that the remaining two currents, $i_{\mathrm{G}1} = i_{\mathrm{G}\max}$ and $i_{\mathrm{G}k} = i_{\mathrm{G}\min}$, assume the balanced sinusoidal shapes expected in the grid. Using Kirchhoff's voltage law on the loop that includes the sources, $u_{\mathrm{G}1} = u_{\mathrm{G}\max}$, $u_{\mathrm{G}l}$, and the voltage across the upper switch $u_{\mathrm{T}\mathrm{G}l,\mathrm{h}}$, where $l = 2, \ldots, k-1$, the voltage across the upper switching devices can be expressed as

$$u_{\mathrm{T}\mathrm{G}l,\mathrm{h}} = u_{\mathrm{G}\max} - u_{\mathrm{G}l},\ l = 2, \ldots, k-1 \tag{9}$$

as long as the voltage drops across the inductors can be neglected. The average value of $u_{\mathrm{T}\mathrm{G}l,\mathrm{h}}$ can also be expressed in terms of the respective modulation signal and the dc-link voltage as

$$u_{\mathrm{T}\mathrm{G}l,\mathrm{h}} = (1 - d_{\mathrm{G}l}) \cdot (u_{\mathrm{G}\max} - u_{\mathrm{G}\min}),\ l = 2, \ldots, k-1. \tag{10}$$

Combining (9) and (10), the modulation signals of the switching half-bridges of the rectifier can be expressed as

$$d_{\mathrm{G}l} = \frac{u_{\mathrm{G}l} - u_{\mathrm{G}\min}}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}},\ l = 2, \ldots, k-1. \tag{11}$$

The average current flowing through the upper switch, $\mathrm{T}_{\mathrm{G}l,\mathrm{h}}$, can also be expressed in terms of the modulation signals and the corresponding phase current, i.e.,

$$i_{\mathrm{T}\mathrm{G}l,\mathrm{h}} = \frac{i_{\mathrm{G}l} \cdot (u_{\mathrm{G}l} - u_{\mathrm{G}\min})}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}},\ l = 2, \ldots, k-1. \tag{12}$$

Finally, the current of the grid phase with the maximum voltage can be calculated using Kirchhoff's current law. Thus, $i_{\mathrm{G}1} = i_{\mathrm{G}\max} = i_{\mathrm{G}\mathrm{DC}} - \sum i_{\mathrm{T}\mathrm{G}l,\mathrm{h}}$, where $i_{\mathrm{G}\mathrm{DC}}$ can be calculated from the transferred constant power P and the dc-link voltage, i.e., $i_{\mathrm{G}\mathrm{DC}} = P/(u_{\mathrm{G}\max} - u_{\mathrm{G}\min})$. Substituting the above equations, the resulting current of the phase with the maximum voltage is

$$i_{\mathrm{G}\max} = \frac{P}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}} - \sum_{l=2}^{k-1} \frac{i_{\mathrm{G}l}(u_{\mathrm{G}l} - u_{\mathrm{G}\min})}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}}. \tag{13}$$

Following the same steps for the lower switch, the current in the phase with the minimum voltage, phase k, is,

$$i_{\mathrm{G}\min} = -\frac{P}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}} - \sum_{l=2}^{k-1} \frac{i_{\mathrm{G}l}(u_{\mathrm{G}\max} - u_{\mathrm{G}l})}{u_{\mathrm{G}\max} - u_{\mathrm{G}\min}}. \tag{14}$$

Fig. 12(c) shows an example of a six-phase grid, verifying the above equations. In the upper part of the figure, the six-phase grid voltages, phase-shifted by 60°, are shown. The dc-link voltage follows the envelope of the maximum minus the minimum grid-phase voltage at each point in time. In the lower part of the figure, the six-phase grid currents are displayed. The currents corresponding to the middle voltages can be actively controlled, and, for example, aligned in phase with their respective grid voltages in the case of a power factor correction (PFC) rectifier. The $i_{\mathrm{G}\max}$ and $i_{\mathrm{G}\min}$ currents cannot be actively controlled, but are derived from (13) and (14), respectively. These currents naturally form a set of balanced sinusoidal input currents of the VSR, thus verifying the operational principle of the proposed control–modulation strategy.

In the context of the proposed modulation scheme, a special case can occur. When the grid and machine voltages are similar in amplitude and frequency, and have a specific phase shift such that the envelopes of the maximum-minus-minimum phase voltages of both the grid and machine are aligned and equal in amplitude, then both converters can operate with $(k-2)/2$ and $(m-2)/2$ DPWM modulations, respectively. In this case, only $k+m-4$ switching half-bridge legs are required. This case can also be mathematically proven.

Fig. 13(a) illustrates again a system with a k-phase VSR and an m-phase VSI. Assuming that certain half-bridges are clamped to the positive and negative dc-link rails, as shown in the figure, and that the currents of the remaining switched half-bridge legs, $i_{\mathrm{G}l}$, $l = 2, \ldots, k-1$, and $i_{\mathrm{M}l}$, $l = 2, \ldots, m-1$, are actively controlled, it is shown that the currents $i_{\mathrm{G}\max}$, $i_{\mathrm{G}\min}$, $i_{\mathrm{M}\max}$, and $i_{\mathrm{M}\min}$ naturally form a set of balanced sinusoidal input and output current waveforms.

As before, Kirchhoff's voltage law is applied to the loop that includes the sources, $u_{\mathrm{G}\max}$ and $u_{\mathrm{G}l}$, and the voltage across the upper switch $u_{\mathrm{T}\mathrm{G}l,\mathrm{h}}$, where $l = 2, \ldots, k-1$. Similarly, Kirchhoff's voltage law is applied on the output side, in the loop that includes $u_{\mathrm{M}\max}$, $u_{\mathrm{M}l}$, and $u_{\mathrm{T}\mathrm{M}l,\mathrm{h}}$, where $l = 2, \ldots, m-1$. From these, the modulation signals $d_{\mathrm{G}l}$ and $d_{\mathrm{M}l}$ can be derived, which are identical to those given in (11). In addition, Kirchhoff's current law is applied at the positive dc-link rail, leading to the following expression:

$$i_{\mathrm{G}\max} + \sum_{l=2}^{k-1} d_{\mathrm{G}l} i_{\mathrm{G}l} = \sum_{l=2}^{m-1} d_{\mathrm{M}l} i_{\mathrm{M}l} + i_{\mathrm{M}\max}. \tag{15}$$

Kirchhoff's current law for the negative dc-link rail gives

$$i_{\mathrm{G}\min} + \sum_{l=2}^{k-1} (1 - d_{\mathrm{G}l}) i_{\mathrm{G}l} = \sum_{l=2}^{m-1} (1 - d_{\mathrm{M}l}) i_{\mathrm{M}l} + i_{\mathrm{M}\min}. \tag{16}$$

Assuming that the transferred power P is constant, as given in (8), the power expressed in terms of the output (machine) quantities is

$$P = i_{\mathrm{M}\max}(u_{\mathrm{M}\max} - u_{\mathrm{M}\min}) + \sum_{l=2}^{m-1} i_{\mathrm{M}l}(u_{\mathrm{M}l} - u_{\mathrm{M}\min}) \tag{17}$$

or

$$P = i_{\mathrm{M}\min}(u_{\mathrm{M}\min} - u_{\mathrm{M}\max}) + \sum_{l=2}^{m-1} i_{\mathrm{M}l}(u_{\mathrm{M}l} - u_{\mathrm{M}\max}). \tag{18}$$

By combining (15)–(18), with the modulation signals expressions from (11), analytical expressions for the currents $i_{\mathrm{G}\max}$, $i_{\mathrm{G}\min}$, $i_{\mathrm{M}\max}$, and $i_{\mathrm{M}\min}$ are derived. The dc-link voltage is now denoted as u_{DC}, which is equal to $u_{\mathrm{G}\max} - u_{\mathrm{G}\min}$ and also equal to $u_{\mathrm{M}\max} - u_{\mathrm{M}\min}$. Thus

$$i_{\mathrm{G}\max} = \sum_{l=2}^{m-1} \frac{i_{\mathrm{M}l}(u_{\mathrm{M}l} - u_{\mathrm{M}\min})}{u_{\mathrm{DC}}} - \sum_{l=2}^{k-1} \frac{i_{\mathrm{G}l}(u_{\mathrm{G}l} - u_{\mathrm{G}\min})}{u_{\mathrm{DC}}}$$

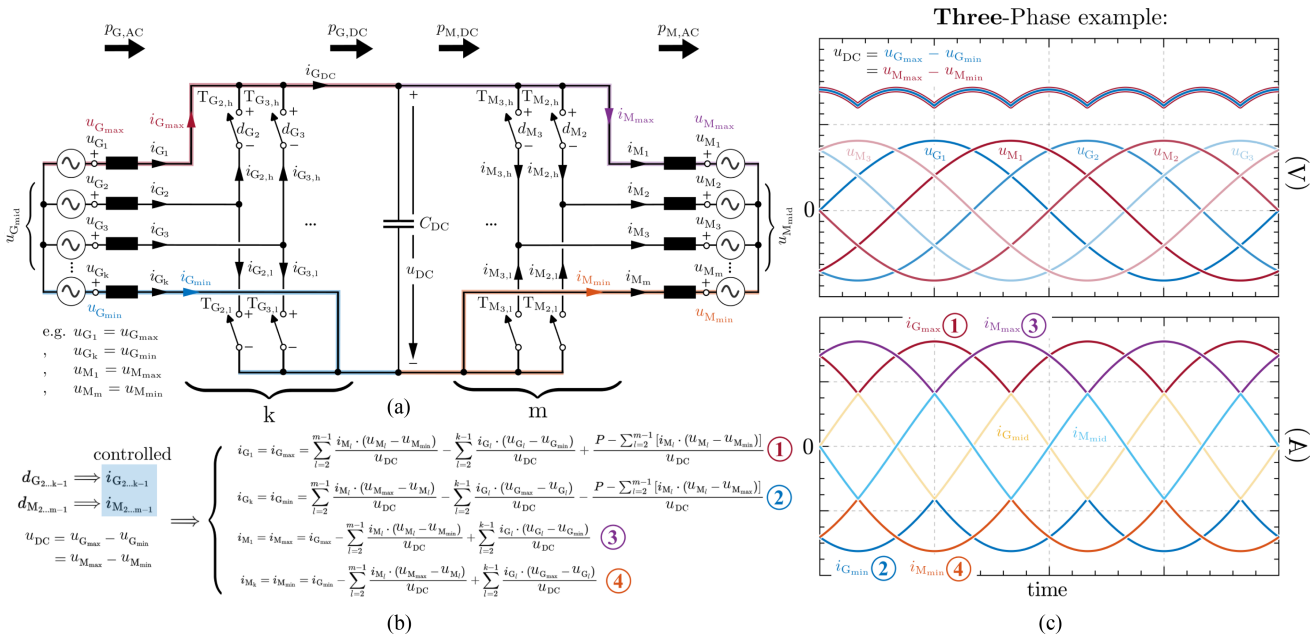

Fig. 13. Modeling of the V-BBC for k number of input phases and m number of output phases; mathematical equations for the special case where the maximum-minus-minimum voltage envelopes or input and output are identical. (a) k-phase VSR operates with $(k-2)/k$ DPWM modulation, meaning that two phases are clamped to the positive or negative DC-link rail. The m-phase VSI also operates with $(m-2)/m$ DPWM modulation, thus again two phases are clamped. In total, only $k+m-4$ switching half-bridge legs are required to ensure constant power flow and sinusoidal currents in all input and output phases. (b) Mathematical equations for the input and output currents $i_{\mathrm{G}\max}$, $i_{\mathrm{G}\min}$, $i_{\mathrm{M}\max}$, and $i_{\mathrm{M}\min}$. These currents are not actively controlled, but it is shown that they naturally form parts of the sinusoidal current waveforms. (c) Verifies the mathematical model using a three-phase system. The upper part of the figure shows the three-phase voltages of the grid and the machine. The lower part shows the middle-phase currents, which follow the corresponding parts of the sinusoidal input currents. Similarly, and as derived from the equations in (b), the $i_{\mathrm{G}\max}$, $i_{\mathrm{G}\min}$, $i_{\mathrm{M}\max}$, and $i_{\mathrm{M}\min}$ currents are also components contributing to the formation of the sinusoidal input/output current waveforms.

$$+\frac{P-\sum_{l=2}^{m-1} i_{\mathrm{M}l}(u_{\mathrm{M}l}-u_{\mathrm{M}\min})}{u_{\mathrm{DC}}} \tag{19}$$

$$i_{\mathrm{G}\min}=\sum_{l=2}^{m-1}\frac{i_{\mathrm{M}l}(u_{\mathrm{M}\max}-u_{\mathrm{M}i})}{u_{\mathrm{DC}}}-\sum_{l=2}^{k-1}\frac{i_{\mathrm{G}l}(u_{\mathrm{G}\max}-u_{\mathrm{G}l})}{u_{\mathrm{DC}}}$$
$$-\frac{P-\sum_{l=2}^{m-1} i_{\mathrm{M}l}\cdot(u_{\mathrm{M}l}-u_{\mathrm{M}\max})}{u_{\mathrm{DC}}} \tag{20}$$

$$i_{\mathrm{M}\max}=i_{\mathrm{G}\max}-\sum_{l=2}^{m-1}\frac{i_{\mathrm{M}l}(u_{\mathrm{M}l}-u_{\mathrm{M}\min})}{u_{\mathrm{DC}}}$$
$$+\sum_{l=2}^{k-1}\frac{i_{\mathrm{G}l}(u_{\mathrm{G}l}-u_{\mathrm{G}\min})}{u_{\mathrm{DC}}} \tag{21}$$

$$i_{\mathrm{M}\min}=i_{\mathrm{G}\min}-\sum_{l=2}^{m-1}\frac{i_{\mathrm{M}l}(u_{\mathrm{M}\max}-u_{\mathrm{M}l})}{u_{\mathrm{DC}}}$$
$$+\sum_{l=2}^{k-1}\frac{i_{\mathrm{G}l}(u_{\mathrm{G}\max}-u_{\mathrm{G}l})}{u_{\mathrm{DC}}}. \tag{22}$$

Based on these equations, the indirectly controlled currents can be found. It is shown, based on numerical calculations, that the currents are naturally forming parts of the respective sinusoidal input and output current waveforms. This confirms that all input and output currents are sinusoidal and that the transferred power remains constant. This is illustrated in the three-phase system example, as shown in Fig. 13(c). In the upper part of the figure, the three-phase voltages of the grid and the machine are shown. Although they are not in phase, their maximum-minus-minimum envelopes are identical, i.e., $u_{\mathrm{G}\max}-u_{\mathrm{G}\min}=u_{\mathrm{M}\max}-u_{\mathrm{M}\min}$, as highlighted in the figure. This makes 1/3–1/3 DPWM modulation possible; in other words, switching only two out of the six legs is sufficient to control the V-BBC system. In the lower part of the figure, the corresponding currents are shown. The middle-phase currents are actively controlled via the respective modulation signals, while the currents $i_{\mathrm{G}\max}$, $i_{\mathrm{G}\min}$, $i_{\mathrm{M}\max}$, and $i_{\mathrm{M}\min}$ naturally form parts of the sinusoidal current waveforms, thereby verifying the proposed operation principle.

Appendix B
IGBT-Based Converters in Higher Power Applications

The novel modulation scheme introduced in this work can also be extended to insulated gate bipolar transistor (IGBT)-based converters targeting power levels up to hundreds of kW and lower switching frequencies. In such cases, IGBT modules are preferred due to their lower cost and high current handling capabilities. As an example, the VSR and VSI three-phase half-bridges are replaced with the FS75R12W2T7 (1200 V and 75 A) sixpack IGBT module from Infineon [22] [see Fig. 14(a)], targeting a 50 kW motor drive application. The switching frequency is reduced to 10 kHz. At the nominal operation point, the

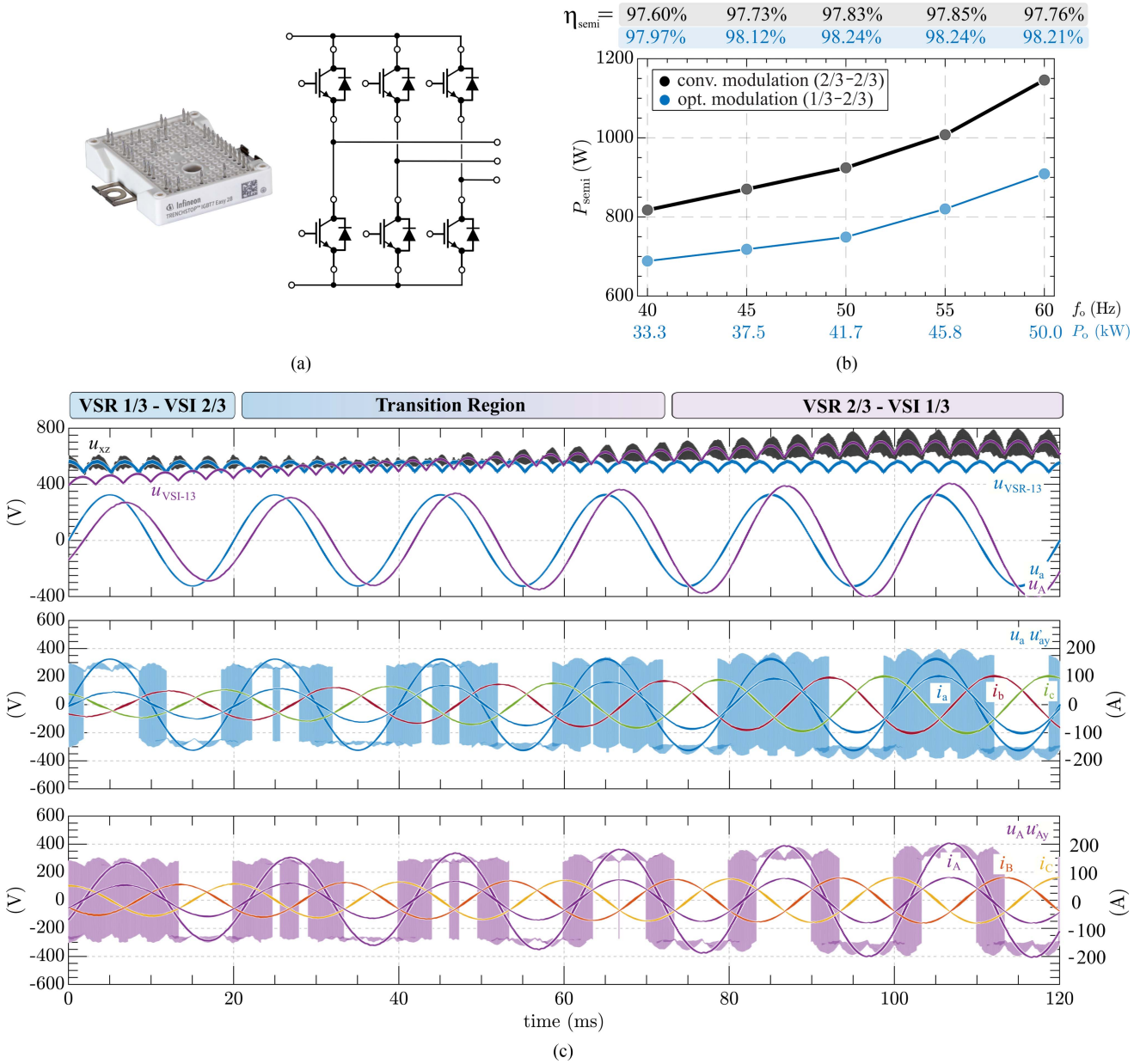

Fig. 14. Example of the novel modulation scheme applied to IGBT-based high-power applications. (a) VSR and VSI three-phase half-bridges are replaced with the FS75R12W2T7 (1200 V, 75 A) sixpack IGBT module from Infineon. (b) Comparison of losses and efficiency between the conventional modulation scheme and the proposed approach. The output current is kept constant at $\hat{I}_o = 85$ A, while the output frequency f_o varies from 40 to 60 Hz, with the output power increasing linearly up to 50 kW, emulating a constant current/torque motor operation. An average semiconductor efficiency improvement of +0.41% is observed. (c) Simulation results demonstrating the functionality of the proposed modulation scheme. In this scenario, the load is 5 Ω, the output electrical frequency is 50 Hz, the switching frequency is 10 kHz, and the output power increases from 20 to 50 kW. The grid has 230 V rms phase-to-neutral voltage and 50 Hz frequency. The simulation covers all operating regions; buck, transition, and boost modes. In the first plot, the phase-to-neutral voltages on the grid and machine sides are shown, along with the DC-link voltage, which tracks the envelope of the maximum phase-to-phase voltage from either the grid or the machine. The second and third plots display the switching node voltages and the corresponding grid-side and machine-side currents, respectively.

machine draws $P_{o,N} = 50$ kW, the electrical output frequency is $f_{o,N} = 60$ Hz, and the sinusoidal machine-side currents have an amplitude of $\hat{I}_o = 85$ A. The semiconductor losses and efficiency are estimated using a piecewise linear electrical circuit simulation (PLECS) [23] model of the module provided by the manufacturer. The analysis considers operation in constant current mode, while the output frequency f_o varies from 40 to 60 Hz, and the corresponding output power increases linearly from 33.3 to 50 kW. Fig. 14(b) compares the losses and efficiency of two modulation schemes. The conventional approach uses negative 2/3 DPWM for both converters and the constant dc-link voltage is set to the minimum possible value, $\sqrt{3} \cdot \max(\hat{U}_m, \hat{U}_o)$, where $\hat{U}_m$ and $\hat{U}_o$ are the peak phase-to-neutral voltages of the grid and machine, respectively. The novel modulation scheme, as already discussed, employs 1/3 DPWM as much as possible, and has a variable dc-link voltage that

is kept at the minimum allowable level. Notably, even in this high-power application with a relatively low switching frequency, the proposed modulation strategy—designed to reduce switching losses—significantly improves the overall system efficiency. More specifically, an average semiconductor efficiency increase of +0.41% is observed. At the nominal power, a reduction of 20.5% of the semiconductor losses is observed. In reality, a higher reduction is expected since the dc-link voltage is typically higher than $\sqrt{3} \cdot \max(\hat{U}_{\mathrm{m}}, \hat{U}_{\mathrm{o}})$.

Fig. 14(c) presents simulation results for the aforementioned application, demonstrating the functionality of the proposed modulation scheme. In this exemplary simulation case, the load is replaced by a constant 5 Ω resistance, the output electrical frequency is fixed at 50 Hz, the switching frequency is 10 kHz, and the output power increases from 20 to 50 kW. The grid operates at 50 Hz with 230 V rms phase-to-neutral voltage. The passive components are: $L_{\mathrm{DM,VSR-I}} = 1$ mH, $L_{\mathrm{CM}} = 8$ mH, $C_{\mathrm{IN}} = 8$ μF, $C_{\mathrm{OUT}} = 10$ μF, and $C_{\mathrm{DC,xy-yz}} = 20$ μF. Due to the relatively low switching frequency, the dc-link voltage u_{xz} has a noticeable ripple. Nevertheless, the output currents remain sinusoidal, and the converter operates smoothly across buck, boost, and transition modes.

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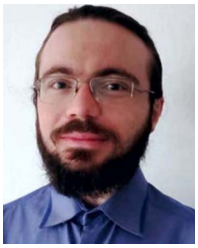
Christos Leontaris received the B.Sc. degree (Hons.) in electrical and computer engineering from the National Technical University of Athens, Athens, Greece, in 2018, and the M.Sc. degree (Hons.) in energy science and technology with a focus on specializing in power electronic systems from the Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 2021.

He is currently a Researcher with the Chair of High-Power Converter Systems, Technical University of Munich, Munich, Germany. In 2022, he was a Scientific Assistant with the Power Electronic Systems Laboratory, ETH Zürich, focusing on three-phase converters for onboard electric vehicle (EV) charging applications. He was a Magnetic Engineer with Resonant Link, Zürich, where he contributed to the development of highly efficient MSRS coils for wireless power transfer applications. His research interests include the field of three-phase EV chargers and ac–ac converters.



Gean Jacques Maia de Sousa received the B.S. degree in electrical engineering from the Federal University of Ceará, Fortaleza, Brazil, in 2010, and the M.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 2014 and 2022, respectively.

He is currently a Postdoctoral Researcher with the Chair of High-Power Converters, Technical University of Munich, Munich, Germany. His research interests include ac–dc and dc–dc converters, modeling and control for power electronics, and characterization of semiconductor devices.

Marcelo Lobo Heldwein (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH Zürich), Zurich, Switzerland, in 2007.

He is currently the Head of the Chair of High-Power Converter Systems, Technical University of Munich, Munich, Germany. From 1999 to 2003, he was with industry, including R&D activities with the Power Electronics Institute, Florianópolis, and Emerson Network Power, in Brazil and Sweden. From 2007 to 2009, he was a Postdoctoral Fellow with ETH Zürich and UFSC. From 2010 to 2022, he was a Professor with the Department of Electronics and Electrical Engineering, UFSC. His research interests include power electronics, advanced power distribution technologies, and electromagnetic compatibility.

Dr. Heldwein is a Member of the Brazilian Power Electronic Society (SOBRAEP) and a Member of the Advisory Board of PCIM Europe.