Switching Mechanism and Influence Analysis of Multimode Undamped Oscillation for GaN HEMTs in Half-Bridge Circuits

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***Abstract*—Gallium nitride high electron mobility transistors are widely used due to their advantages of fast switching speed and low ON-resistance. However, these characteristics also render the circuits highly susceptible to instability. Undamped oscillations are one of the instability problems, which can result in excessive power loss or even more serious device breakdown. Current research primarily focuses on the mechanism analysis and modeling of single undamped oscillation, without considering the coupling and switching between different undamped oscillations. The systematic theoretical study of multimode undamped oscillation mechanisms is lacking. In this article, the occurrence mechanism and switching law of multimode undamped oscillation are analyzed, which is the first time to reveal the basic mechanism between multiple undamped oscillations in the same process, and the influence of undamped oscillations in one process on the subsequent stage. First, the generation and persistence mechanism of different oscillations are analyzed. Then, the high-frequency equivalent models are developed to accurately analyze the influence of various parasitic parameters and external conditions on oscillation generation and the switching process between multimode oscillation. Finally, the accuracy of the proposed method is verified by simulation and experiment. The theory and models are established to analyze the generation and switching mechanism of undamped oscillations comprehensively. It can provide systematic guidance for the undamped oscillation study.**

***Index Terms*—Gallium nitride (GaN), high-electron-mobility transistors (HEMTs), undamped oscillation.**

NOMENCLATURE

Parameter	*Description*
$V_{\rm bus}$	DC input voltage.
$I_{\rm L}$	Load current.
$C_{\rm bus}$	Capacitance of decoupling capacitor.
$L_{\rm loop}$	Power loop inductance of the single pulse circuit.
$R_{\rm loop}$	Power loop resistance of the single pulse circuit.
$L_{\rm load}$	Inductance of load inductor.
$L_{\rm D1'in}$&$L_{\rm D2'in}$	Internal drain inductances of Q_1&Q_2.
$L_{\rm G1'in}$&$L_{\rm G2'in}$	Internal gate inductances of Q_1&Q_2.
$L_{\rm S1'in}$&$L_{\rm S2'in}$	Internal common source inductances of Q_1&Q_2.
$L_{\rm D1}$&$L_{\rm D2}$	Drain inductance of Q_1&Q_2.
$L_{\rm G1}$&$L_{\rm G2}$	Gate inductance of Q_1&Q_2.
$L_{\rm S1}$&$L_{\rm S2}$	Common source inductance of Q_1&Q_2.
$C_{\rm ds1}$&$C_{\rm ds2}$	Drain–source capacitance of Q_1&Q_2.
$C_{\rm gd1}$&$C_{\rm gd2}$	Gate–drain capacitance of Q_1&Q_2.
$C_{\rm gs1}$&$C_{\rm gs2}$	Gate–source capacitance of Q_1&Q_2.
$R_{\rm G1}$&$R_{\rm G2}$	Gate resistance of Q_1&Q_2.
$V_{\rm G}$	Driving voltage from driver IC.

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I. INTRODUCTION

HIGH efficiency, high power density, and high reliability are the key objectives in the development of power electronics. However, silicon (Si)-based devices have reached their performance thresholds due to material limitations [1], [2], [3]. In this context, wide bandgap (WBG) semiconductors, including gallium nitride (GaN) and silicon carbide (SiC), have gained significant attention and experience rapid advancements in recent years. In particular, GaN high electron mobility transistors (HEMTs) exhibit exceptional characteristics, including the high electric breakdown field, high electron mobility, and low ON-resistance [4], [5], [6], [7]. These characteristics of GaN devices provide a solid foundation to realize high frequency and high power density in emerging fields such as 5G technology, electric vehicles, and artificial intelligence [8], [9], [10], [11].

However, high switching speed makes circuits more susceptible to the influence of high-frequency parasitic parameters, while low ON-resistance reduces system damping. The negative factors will lead to serious instability problems in the circuit system, and the undamped oscillations are one of the instability problems [12], [13], [14], [15], [16], [17], [18], [19], [20]. Undamped oscillations can lead to instantaneous shoot-through

in the bridge-leg, excessive power loss, or even more serious device breakdown [21], [22], [23], [24]. Therefore, it is very necessary to analyze and suppress undamped oscillations in order to enhance the reliability of devices and circuit operation.

A lot of research works have been conducted on undamped oscillations, including false triggering oscillations (FTO) of the gate–source voltage and self-sustained oscillations (SSO) of the drain–source voltage. In studies [13] and [14], the generation mechanism of FTO is analyzed and the negative impedance model is developed, while the effect of various parasitic parameters on this phenomenon is studied. However, the common-source inductance (CSI) is neglected to simplify the model, which significantly affects gate–source voltage oscillation and cannot be overlooked. In studies [25] and [26], FTO is investigated and a passive suppression method with the addition of ferrite beads in power loop is introduced to suppress oscillation. However, the drive resistance is not considered, which has a significant effect on the FTO and may affect the accuracy of the model. In study [27], a loop conductance adaptive method is proposed to suppress switching oscillations in GaN-based circuits. This method explains the suppression mechanism from the perspective of oscillator theory. In study [15], based on the Barkhausen criterion, it is concluded that the ratio between the CSI and the gate–drain capacitance is a critical factor in effectively preventing FTO. However, the influence of the drive resistance is ignored for easier computation. Furthermore, in study [28], it is analyzed that FTO can also occur when the resonant frequency f_g of the parasitic inductance and the gate–source capacitance in the drive circuit is close to the resonant frequency f_d of the parasitic inductance and the drain–source capacitance in the power circuit. Although the Barkhausen criterion is a good way to explore undamped oscillations, it reflects less information about stability [29]. In study [30], FTO of SiC metal-oxide-semiconductor field-effect transistors (MOSFETS) is explored by the closed-loop transfer function, and it is identified that FTO can be triggered under two different testing conditions. In study [12], FTO occurring during the turn-OFF transients of cascode GaN HEMTs is investigated, and the influence of parasitic parameters on system stability is evaluated quantitatively. In study [20], the FTO mechanism of parallel GaN devices is revealed, and the effects of parasitic parameters on the FTO of parallel devices are analyzed and suppression methods are proposed. Based on the above analysis, it can be seen that FTO is prevalent in WBG devices. The existing studies mainly focus on the generation mechanism, parameter effects and suppression methods of a single FTO.

In addition to FTO, WBG devices may also generate other modes of undamped oscillations due to external conditions or inherent device characteristics. In study [17], the generation mechanism of SSO of the drain–source voltage is explored and the influence of parasitic parameters on system stability is analyzed. In study [31], a state-space model is used to analyze SSO. The state-space model is compared with the transfer function and their equivalence is demonstrated. In addition, undamped oscillations of p-GaN HEMT and Cascode GaN HEMT are investigated in different conditions, and the influence of circuit parameters on these oscillations are analyzed, the methods such as reducing the CSI remain effective in suppressing undamped oscillations [32], [33], [34], [35].

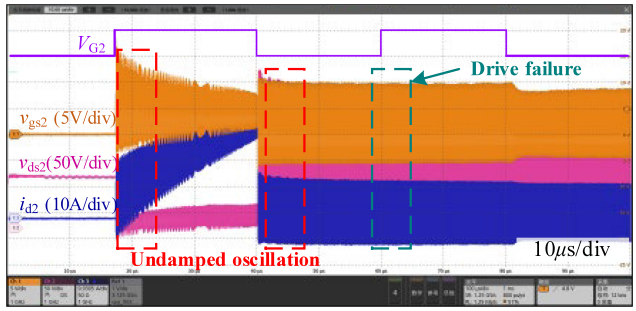

Fig. 1. Scene where multiple modes of undamped oscillations occur simultaneously.

The above analysis shows that the current studies mainly focus on single undamped oscillations, such as FTO for gate–source voltage and SSO for drain–source voltage. In practical engineering, the authors find that multiple undamped oscillations, such as FTO and SSO, occur at the same time, which is more complicated and harmful than a single oscillation, as shown in Fig. 1. The occurrence of multiple undamped oscillation results in more severe oscillations compared with the single oscillation, including larger voltage and current overshoots, and instantaneous shoot-through in the bridge-leg. However, the occurrence mechanism and switching law of multimode undamped oscillations are not clear at present.

In response to the above question, the switching mechanism and influence analysis of multimode undamped oscillation for GaN HEMTs are analyzed and proposed in this article. The main contributions of this work are as follows.

1) It is the first time to analyze the switching mechanism of two undamped oscillations at the same time and reveal the switching laws of different undamped oscillations at different time.
2) The multimode undamped oscillations are modeled, and the effects of external conditions and parasitic parameters on the generation and switching of different undamped oscillations are investigated.

The rest of this article is organized as follows. In Section II, the generation conditions and mechanisms of SSO and FTO are analyzed, and multimode undamped oscillation models are developed. Based on the established models, Section III investigates the influence of parasitic parameters on the generation and switching of different undamped oscillations. To validate the theoretical analysis, Section IV presents simulation and experimental results. Finally, Section V concludes this article.

II. Circuit Modeling and Stability Criteria

The GaN-based half-bridge circuit is used to investigate the system instability, as shown in Fig. 2, with key parameters summarized in Nomenclature. Both Q_1 and Q_2 are GaN HEMTs, where the top device Q_1 operates as a passive device, and the bottom device Q_2 operates as an active device, driven by a double-pulse signal. When the driving signal steps from high to low, Q_2 is turned off and the load current I_L will freewheel

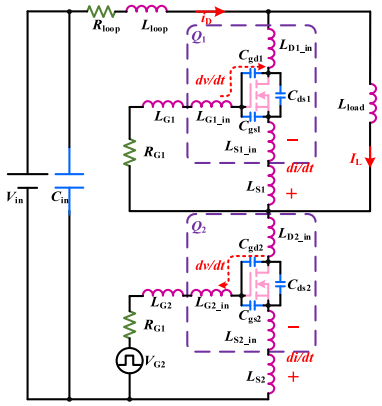

Fig. 2. Half-bridge circuit based on GaN HEMTs.

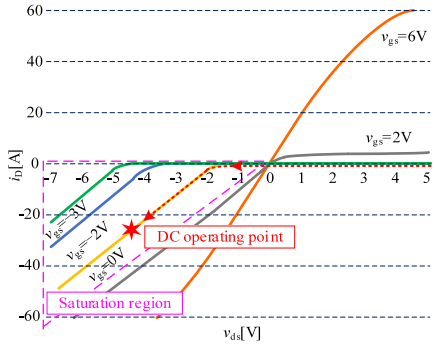

Fig. 3. Reverse conduction characteristics of GaN HEMTs.

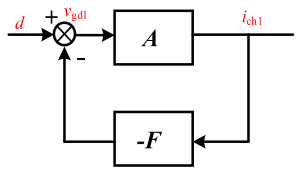

Fig. 4. Block diagram of the feedback system of SSO.

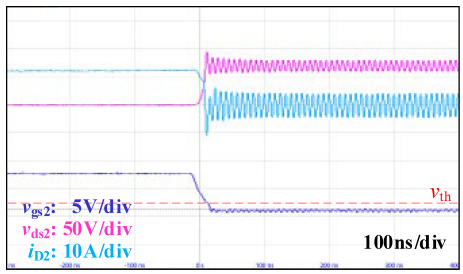

Fig. 5. Typical waveforms of SSO.

through Q_1. During the turn-OFF transient, the circuit may occur unexpected undamped oscillations due to the extremely high *dv/dt* and *di/dt*.

A. Generation Mechanism of Undamped Oscillations

The reverse conduction characteristics of GaN HEMTs are significantly different from those of Si or SiC MOSFETS. In SiC MOSFETS, the load current freewheels through the intrinsic body diode. In contrast, GaN HEMTs lack the body diode but can conduct reverse current due to their unique structure [4]. When gate–drain voltage or gate–source voltage gradually exceeds the threshold voltage, electrons are attracted to the AlGaN/GaN heterojunction interface, re-establishing the two-dimensional electron gas, and thereby enabling the GaN device to conduct current [7], [17], [36]. The channel current is controlled by the gate–source voltage when the drain–source voltage is positive, but it is controlled by the gate–drain voltage when the drain–source voltage is negative [37].

When Q_2 is turned OFF, the current charges the output capacitance of Q_1 reversely, causing the source–drain voltage of Q_1 to increase. Meanwhile, the gate–source voltage of Q_1 remains at a low level since there is no driving signal. The gate–drain voltage of Q_1 can be expressed as follows:

$$v_{\mathrm{gd1}} = v_{\mathrm{gs1}} + v_{\mathrm{sd1}} \approx v_{\mathrm{sd1}} \tag{1}$$

where v_{gd1}, v_{gs1}, and v_{sd1} are the gate–drain voltage, gate–source voltage, and source–drain voltage of Q_1, respectively.

The reverse conduction characteristics of Q_1 are shown in Fig. 3, gate–drain voltage and source–drain voltage of Q_1 satisfy the following:

$$\begin{cases} v_{\mathrm{gd1}} > V_{\mathrm{gd,th}} \\ v_{\mathrm{sd1}} > v_{\mathrm{gd1}} - V_{\mathrm{gd,th}} \end{cases} \tag{2}$$

where $V_{\mathrm{gd,th}}$ refers to the threshold voltage for reverse conduction of the device.

Therefore, Q_1 remains in the saturation region and the channel current is controlled by v_{gd1}, which can be expressed as follows:

$$i_{\mathrm{ch1}} = g_{\mathrm{m1}} \cdot v_{\mathrm{gd1}} \tag{3}$$

where g_{m1} represents the reverse transconductance of the GaN HEMTs, and i_{ch1} represents the reverse channel current of Q_1.

When the device works in the saturation region, a feedback system is established within the circuit. The forward path of this system is determined by the devices' transconductance, while the feedback loop is formed by the surrounding circuit elements. The self-sustained oscillation is caused by the inherent instability of the circuit system, and can be considered to occur in the absence of an external excitation source. A transient disturbance coupled to the gate drive signal is typically regarded as the input, which momentarily forces the device into the saturation region. Such disturbances may originate from factors like the reverse conduction characteristics of GaN, as well as *dv/dt* and *di/dt* effects. The corresponding feedback block diagram is shown in Fig. 4. If the feedback network becomes positive due to the reverse conduction characteristics and parasitic parameters, the disturbance will be continuously amplified by the positive feedback loop [17]. Q_2 will occur SSO of drain–source voltage while its gate–source voltage is normal. The typical waveforms are shown in Fig. 5.

In addition to SSO, other undamped oscillations may also occur during its turn-OFF period. At this time, Q_2 works in the

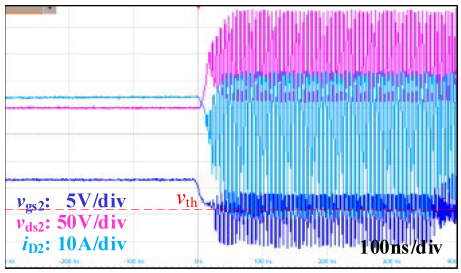

Fig. 6. Typical waveforms of FTO.

forward cutoff region. The gate–source voltage of Q_2 can be expressed as follows:

$$v_{\mathrm{gs2}} = -(L_{\mathrm{G2}} + L_{\mathrm{S2}}) \cdot \frac{di_{\mathrm{g2}}}{dt} - L_{\mathrm{S2}} \cdot \frac{di_{\mathrm{d}}}{dt} - i_{\mathrm{g2}} \cdot R_{\mathrm{G2}} \quad (4)$$

where v_{gs2}, i_{g2}, and i_{d} are gate–source voltage, gate current, and drain current of Q_2.

As shown in Fig. 2, the high *dv/dt* applied to the Miller capacitance generates a displacement current flowing into the gate node, which may result in an increase of v_{gs2}. Simultaneously, the di_{d}/dt on the CSI generates a negative voltage, potentially further increasing v_{gs2}. Once v_{gs2} exceeds the $V_{\mathrm{gs,\ th}}$, the channel of Q_2 is forcefully turned ON, which is called false turn-ON. At this point, Q_2 commutates from the cutoff region to the saturation region, because

$$\begin{cases} v_{\mathrm{gs2}} > V_{\mathrm{gs,th}} \\ v_{\mathrm{ds2}} > v_{\mathrm{gs2}} - V_{\mathrm{gs,th}} \end{cases}. \quad (5)$$

False turn-ON causes Q_2 to work in the saturation region, during which the channel current is controlled by v_{gs2}, indicating that a feedback system is established. In this case, if the feedback network exhibits positive feedback due to parasitic parameters, Q_2 will occur FTO of gate–source voltage. The typical waveforms are shown in Fig. 6.

Thus, although oscillation mechanisms of FTO and SSO are different, the necessary conditions for oscillation occurrence can be summarized into two key factors.

1) *Condition I:* The devices as oscillation source need to work in the saturation region to generate channel current, which leads to the establishment of the feedback network.
2) *Condition II:* The feedback network becomes positive feedback due to the influence of device characteristics and parasitic parameters.

B. Relationship Between Different Undamped Oscillations

The preceding analysis highlights the generation mechanism of single undamped oscillation, however, there is also relationship between different undamped oscillations.

Condition I is necessary regardless of whether the FTO occurs in Q_1 or Q_2. As previously discussed, the occurrence of false turn-ON is closely related to slew rates of voltage and current. Therefore, the magnitude of the bus voltage and load current, as well as the switching time, significantly influence the occurrence of FTO. For example, if Q_1 occurs FTO during the

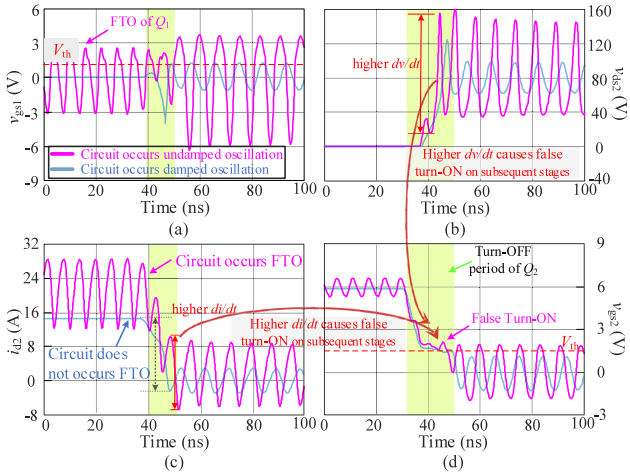

Fig. 7. Influence of undamped oscillations in the previous period on subsequent stage. (a) Waveforms of gate–source voltage in Q_1. (b) Waveforms of drain–source voltage in Q_2. (c) Waveforms of drain current in Q_2. (d) Waveforms of gate–source voltage in Q_2.

turn-ON period of Q_2, it will significantly increase the voltage and current slew rates in the subsequent switching transient. As shown in Fig. 7(a)–(d), the blue waveforms represent normal gate–source voltage of Q_1, drain current of Q_2, drain–source voltage of Q_2, and gate–source voltage of Q_2, respectively. In this case, the circuit does not satisfy Condition I, and therefore no sustained oscillation occurs in voltage or current. The red waveforms represent gate–source voltage of Q_1, drain current of Q_2, drain–source voltage of Q_2, and gate–source voltage of Q_2 when the FTO occurs in Q_1, respectively. It can be seen that the FTO of Q_1 will affect the oscillation of Q_2 at this time, making the drain–source voltage and drain current of Q_2 have a higher change rate, and that will affect the undamped oscillation on the subsequent stage, as shown in Fig. 7(b) and (c). Due to the higher *di/dt* and *dv/dt*, false turn-ON may occur, which will make the device enter the saturation region and satisfy Condition I, thus leading to the subsequent FTO, as shown in Fig. 7(d). In summary, the undamped oscillation in the previous stage influences *dv/dt* and *di/dt*, which directly affects the occurrence of oscillation in the following.

In addition, since both FTO and SSO may occur during the turn-OFF period of Q_2, interactions between Q_1 and Q_2 can arise, resulting in the following three possible situations.

1) Situation I: Q_2 occurs SSO of drain–source voltage, because Q_1 works in the saturation region to establish feedback path and feedback system becomes positive, as shown in Fig. 8(a).
2) Situation II: Q_2 occurs FTO of gate–source voltage, because false turn-ON of Q_2 causes the channel to reopen and transforms the feedback network into positive feedback, as shown in Fig. 8(c).
3) Situation III: Q_2 may occur both FTO and SSO. As mentioned earlier, when Q_2 is turned OFF, the load current is freewheeling through Q_1, which may result in SSO of the drain–source voltage of Q_2, while Q_2 is still in

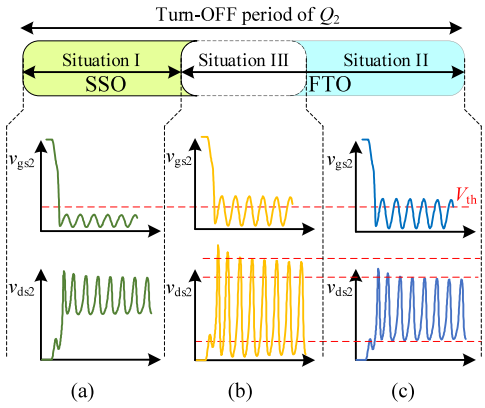

Fig. 8. Different situations of undamped oscillations. (a) Situation I. (b) Situation III. (c) Situation II.

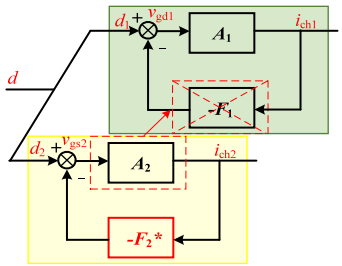

Fig. 9. Block diagram of the feedback system of FTO.

the turn-OFF state. At the same time, the FTO of the gate–source voltage may also occur during turn-OFF period of Q_2. Since the device is turned ON and OFF continuously during the occurrence of FTO, the SSO phenomenon may be masked by the FTO. In terms of the feedback path, when Q_2 occurs SSO, most of the energy is exchanged between the loop parasitic inductance and the output capacitance of Q_2. However, if Q_2 occurs FTO, the energy transfer path becomes unbalanced, thereby destabilizing the feedback loop of SSO, as shown in Fig. 9. Therefore, when both Q_1 and Q_2 satisfy the conditions for establishing the positive feedback system, the FTO of Q_2 tends to dominate the oscillation process. It is worth noting that, since the device is turned ON and OFF continuously, the SSO feedback system can momentarily re-establish during the OFF-state. Therefore, the oscillation amplitude of the drain–source voltage v_{ds2} at this time will be slightly larger than the amplitude when only a single FTO occurs, as shown in Fig. 8(b).

To further validate the underlying oscillation mechanism, the high-frequency equivalent models are developed in the following analysis.

C. Equivalent Circuit Setting and Stability Criterion

In this section, based on the analysis above, high-frequency equivalent models are established to analyze all oscillation mechanisms during the turn-OFF period of Q_2. To simplify the equivalent circuit as shown in Fig. 2, the following assumptions are made [18].

1) The bus capacitor C_{bus} is considered as short-circuited because its high-frequency impedance is sufficiently smaller than the other parameters. The load inductance L_{load} is considered as open-circuited, because its high-frequency impedance is sufficiently larger than the other parameters.
2) Since undamped oscillations occur during the turn-off period of Q_2, the V_{G} remains at a low level.
3) The existence of channel is a necessary condition for undamped oscillation to occur and is represented by a voltage-controlled current source.

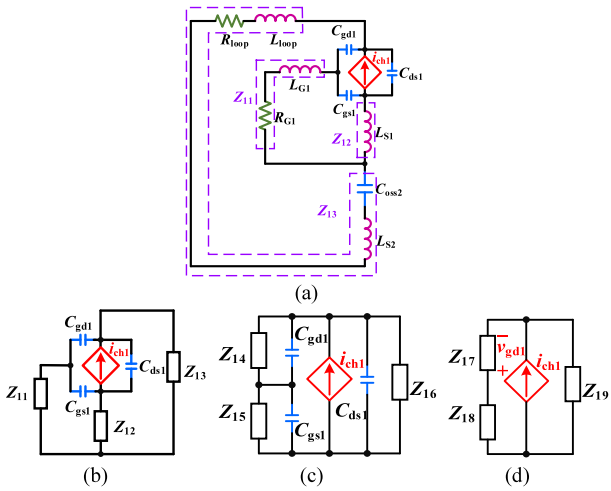

Fig. 10. Equivalent model of SSO. (a) Initial model of SSO. (b) Simplified model of SSO. (c) Further simplified model of SSO. (d) Final simplified model of SSO.

When Q_2 occurs SSO, high-frequency equivalent model is shown in Fig. 10(a). Q_1 is equivalently represented as a current source controlled by the gate–drain voltage. At this time, Q_2 can be equivalently represented by its output capacitance C_{oss2}.

To simplify the equivalent circuit, the star connection of Z_{11}, Z_{12}, and Z_{13} is transformed into a triangle connection using the following equation, as shown in Fig. 10(b) and (c)

$$\begin{cases} Z_{14} = \frac{Z_{11}Z_{12}+Z_{12}Z_{13}+Z_{11}Z_{13}}{Z_{12}} \\ Z_{15} = \frac{Z_{11}Z_{12}+Z_{12}Z_{13}+Z_{11}Z_{13}}{Z_{13}} \\ Z_{16} = \frac{Z_{11}Z_{12}+Z_{12}Z_{13}+Z_{11}Z_{13}}{Z_{11}} \end{cases} \tag{6}$$

where $Z_{11} = R_{\text{G1}}+sL_{\text{G1}}$, $Z_{12} = sL_{\text{S1}}$, $Z_{13} = R_{\text{loop}}+s(L_{\text{loop}}+L_{\text{S2}})+1/(sC_{\text{oss2}})$. After further simplification, Fig. 10(d) can be obtained. Z_{17}, Z_{18}, and Z_{19} are obtained using the following equations:

$$\begin{cases} Z_{17} = Z_{14}//(1/(sC_{\text{gd1}})) \\ Z_{18} = Z_{15}//(1/(sC_{\text{gs1}})) \\ Z_{19} = Z_{16}//(1/(sC_{\text{ds1}})) \end{cases}. \tag{7}$$

During the oscillation transient, the circuit can be regarded as a single-input single-output (SISO) feedback system, and SSO has been studied as a SISO system [17]. Fig. 4 illustrates the block

diagram of the feedback system, where A is the forward transfer function, F is the feedback transfer function, and d represents the disturbance.

From (3), the relationship between v_{gd1} and i_{ch1} has been derived, and A_1 can be calculated using the following equation:

$$A_1 = \frac{i_{\mathrm{ch1}}(s)}{v_{\mathrm{gd1}}(s)} = g_{\mathrm{m1}}. \tag{8}$$

The channel current is fed back to v_{gd1} through the circuit, and F_1 can be determined using the following equation:

$$F_1 = \frac{v_{\mathrm{gd1}}(s)}{i_{\mathrm{ch1}}(s)} = \frac{Z_{17}Z_{19}}{Z_{17}+Z_{18}+Z_{19}}. \tag{9}$$

Based on Fig. 4, the closed-loop transfer function of SSO can be expressed as follows:

$$\begin{aligned} T_1(s) &= \frac{A_1(s)}{1-A_1(s)F_1(s)} \\ &= \frac{g_{\mathrm{m1}}s(a_4s^4+a_3s^3+a_2s^2+a_1s^1+a_0)}{b_5s^5+b_4s^4+b_3s^3+b_2s^2+b_1s^1+b_0} \end{aligned} \tag{10}$$

where a_i ($i=0, 1, 2, 3, 4$) and b_j ($j=0, 1, 2, 3, 4, 5$) represent the coefficients of each term in the numerator and denominator of the closed-loop transfer function, respectively. The derivation shows that the closed-loop transfer function for analyzing the SSO is a fifth-order system.

When Q_2 occurs FTO, both Q_1 and Q_2 work in the saturation region. Gate disturbances in both devices can theoretically affect the stability of the circuit. At this stage, the circuit behaves as a multi-input feedback system, as illustrated by the feedback block diagram in Fig. 9. The formation of the channel in Q_2 interrupts the energy transfer path of SSO, thereby impairing its feedback mechanism. As a result, when both Q_1 and Q_2 are subjected to disturbances, the circuit occurs FTO dominated by Q_2. This phenomenon will be further demonstrated through modeling and experimental analysis.

The equivalent model of the FTO is shown in Fig. 11(a), in which Q_1 is represented by an equivalent impedance Z_{23}, the star connection of Z_{21}, Z_{22}, and Z_{23} is transformed into a triangle connection of Z_{24}, Z_{25}, and Z_{26}, as shown in Fig. 11(b) and (c), respectively. Subsequently, Z_{27}, Z_{28}, Z_{29} are obtained by further simplification, as shown in Fig. 11(d). Similarly, transfer function of the FTO can be derived as follows:

$$A_2 = \frac{i_{\mathrm{ch2}}(s)}{v_{\mathrm{gs2}}(s)} = g_{\mathrm{m2}} \tag{11}$$

$$F_2 = \frac{v_{\mathrm{gs2}}(s)}{i_{\mathrm{ch2}}(s)} = \frac{Z_{27}Z_{29}}{Z_{27}+Z_{28}+Z_{29}} \tag{12}$$

$$\begin{aligned} T_2(s) &= \frac{A_2(s)}{1-A_2(s)F_2(s)} \\ &= \frac{g_{\mathrm{m2}}(a_7s^7+a_6s^6+a_5s^5+a_4s^4+a_3s^3+a_2s^2+a_1s^1+a_0)}{b_7s^7+b_6s^6+b_5s^5+b_4s^4+b_3s^3+b_2s^2+b_1s^1+b_0} \end{aligned} \tag{13}$$

where a_i ($i=0, 1, 2, 3, 4, 5, 6, 7$) and b_j ($j=0, 1, 2, 3, 4, 5, 6, 7$) represent the coefficients of each term in the numerator and denominator of the closed-loop transfer function, respectively.

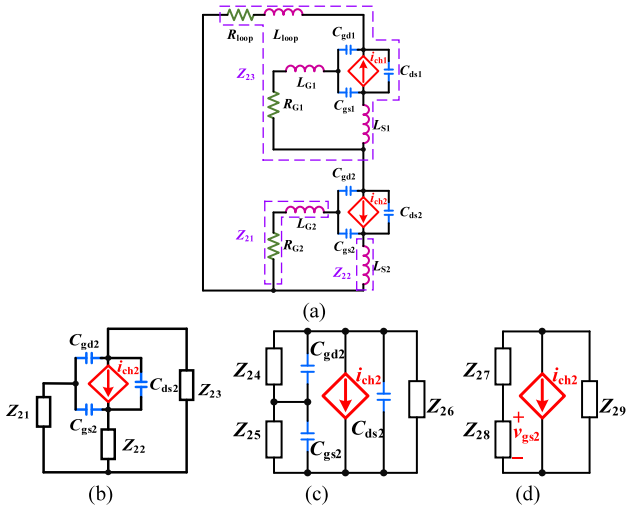

Fig. 11. Equivalent model of FTO. (a) Initial model of FTO. (b) Simplified model of FTO. (c) Further simplified model of FTO. (d) Final simplified model of FTO.

TABLE I
SPECIFICATIONS AND KEY CIRCUIT PARAMETER

Parameter	Value	Parameter	Value
g_{m1}	10S	R_{loop}	0.21 Ω
g_{m2}	55S	C_{oss1}	483 pF
L_{loop}	7.4 nH	C_{oss2}	161 pF
L_{G1}	4.47 nH	C_{iss1}	274 pF
L_{G2}	6.5 nH	C_{iss2}	240 pF
L_{S1}	0.7 nH	C_{rss1}	60 pF
L_{S2}	0.6 nH	C_{rss2}	1.72 pF

According to the Routh–Hurwitz stability criterion, the system is considered unstable if any pole of the transfer function lies in the right half of the s-plane. By incorporating circuit and device parameters into the derived transfer function, all poles can be calculated to assess the system's stability.

The parasitic inductances and high-frequency resistances are extracted using Ansys Q3D. After Q_2 is turned OFF, since the central tendency of the drain–source voltage of Q_2 is V_{bus}, the capacitances of Q_1 are obtained around $v_{\mathrm{ds}} = 0$ and the capacitance of Q_2 is approximately obtained at V_{bus}. The transconductance g_{m} is approximated by the slope of the transfer characteristics near the threshold voltage. Key parameters are summarized in Table I.

According to (10), the $T_1(s)$ of the SSO represents a fifth-order system comprising two pairs of conjugate poles and one real pole. The conjugate poles p_2, p_2*, and the real pole p_3 are located far from the imaginary axis, and thus have minimal impact on the system stability. Since p_1 and p_1* lie close to the imaginary axis and do not form dipoles with nearby zeros typically (a pole-zero pair is generally regarded as a dipole if their separation is at least one order of magnitude smaller than their own modulus

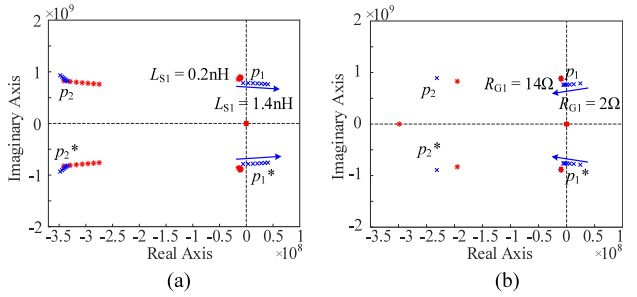

Fig. 12. Pole-zero trajectories of the SSO feedback system under the influence of Q_1's gate parameters. (a) Common-source inductance L_{S1} varies from 0.2 to 1.4 nH. (b) Gate resistance R_{G1} varies from 2 to 14 Ω.

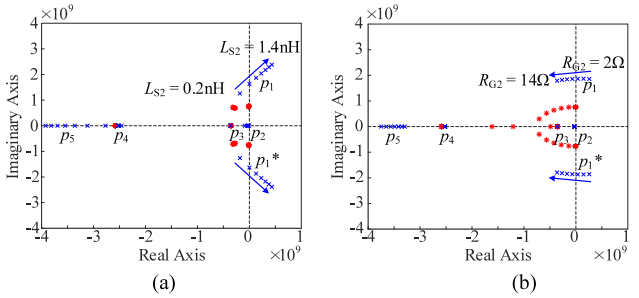

Fig. 13. Pole-zero trajectories of the FTO feedback system under the influence of Q_2's gate parameters. (a) Common-source inductance L_{S2} varies from 0.2 to 1.4 nH. (b) Gate resistance R_{G2} varies from 2 Ω to 14 Ω.

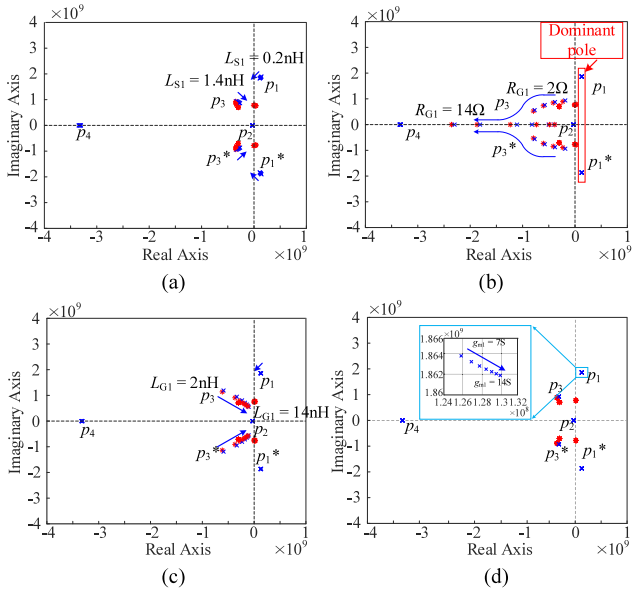

Fig. 14. Pole-zero trajectories of the FTO feedback system under the influence of Q_1's circuit parameters (a) the common-source inductance L_{S1} varies from 0.2 to 1.4 nH. (b) Gate resistance R_{G1} varies from 2 to 14 Ω. (c) The gate inductance L_{G1} varies from 2 to 14 nH. (d) Transconductance g_{m1} varies from 7S to 14 S.

[20], [38]), p_1 and p_1* are identified as the dominant poles of the SSO feedback system. Fig. 12(a) illustrates the trajectories of poles and zeros at V_{bus} = 100 V, with L_{S1} varying from 0.2 to 1.4 nH. The poles and zeros are marked in blue and red, respectively. When L_{S1} increases, the dominant poles gradually shift toward the right half of the s-plane, resulting in system instability, while the remaining poles stay in the left half-plane. Fig. 12(b) illustrates the trajectories of poles and zeros as R_{G1} increases from 2 to 14 Ω, while other parasitic parameters remain constant. The results show that increasing R_{G1} shifts the dominant poles toward the left half-plane, thereby enhancing system stability. Meanwhile, the other poles move further away from the imaginary axis.

According to (13), the $T_2(s)$ of the FTO is a seventh-order system. Among its poles, the conjugate poles p_3 and p_3* form dipoles with nearby zeros and therefore have negligible influence on system stability. The real pole p_2, located near the imaginary axis, exerts limited influence on the system due to its minimal variation. The conjugate poles p_1 and p_1* have the greatest impact on the system and are thus identified as the dominant poles. Fig. 13(a) validates the effect of L_{S2} on system stability. It is evident that increasing L_{S2} causes the system to become unstable. Fig. 13(b) demonstrates the influence of R_{G2} on system stability under the same conditions. The results indicate that increasing R_{G2} can enhance system stability.

When both Q_1 and Q_2 are capable of establishing feedback systems, the feedback system of FTO will dominate over that of SSO. However, since Q_1 remains in the saturation region, the gate parameters of Q_1 can still have an influence on the feedback system of FTO. As shown in Fig. 14(a), the common source inductance L_{S1} affects the stability of FTO feedback system. Increasing L_{S1} causes the dominant pole to shift slightly toward the left half-plane, due to changes in impedance along the feedback path. This behavior is consistent with the effect of varying L_{loop}. As shown in Fig. 14(b), the gate resistance R_{G1} affects the stability of FTO feedback system. As R_{G1} increases, conjugate pole pair p_3 and p_3*, which form dipoles, gradually shift toward the left half-plane and eventually transform into two real poles. In contrast, the dominant poles p_1 and p_1* remain nearly unchanged. Fig. 14(c) illustrates the impact of the gate inductance L_{G1} on system stability. As L_{G1} increases, the conjugate poles p_3 and p_3* shift toward the right, yet they remain in the left half-plane. The dominant poles p_1 and p_1* remain essentially unchanged. Fig. 14(d) shows the effect of Q_1's transconductance on the stability of the FTO feedback system. Increasing the g_{m1} causes a slight rightward shift of the poles, but the impact is minimal. These observations further confirm that the occurrence of FTO disrupts the feedback system of SSO and causes FTO to become the dominant oscillation.

III. Impact of Circuit and Device Parameters on Oscillation

Different modes of undamped oscillations fundamentally originate from the formation of distinct feedback systems, each involving specific core oscillatory devices and associated parasitic parameters. To clarify the switching mechanism of multi-mode undamped oscillations, this section investigates the influence of parasitic parameters on the switching process between these modes. The damping ratio ζ is employed as an indicator

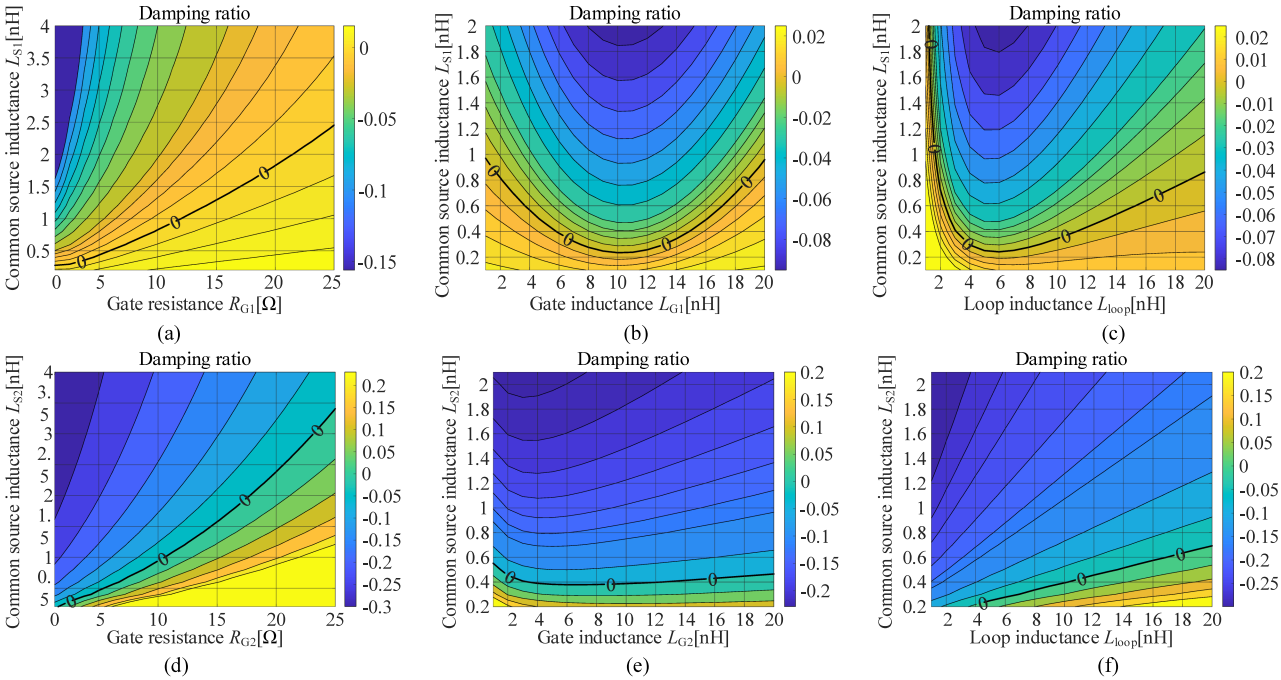

Fig. 15. Contour plot of parasitic parameters for undamped oscillations ((a)–(c) show the variation of the damping ratio of the SSO feedback system under Q_1's different parameters. (d)–(f) show the variation of the damping ratio of the FTO feedback system under Q_2's different parameters.). (a)R_{G1}–L_{S1}. (b)L_{G1}–L_{S1}. (c)L_{loop}–L_{S1}. (d)R_{G2}–L_{S2}. (e)L_{G2}–L_{S2}. (f)L_{loop}–L_{S2}.

to evaluate the system stability, and it is defined as follows:

$$\zeta = \frac{\sigma}{|p_1|} = \frac{\sigma}{\sqrt{\sigma^2 + \omega^2}} \tag{14}$$

where σ and ω is the real and imaginary parts of the dominant poles p_1 and p_1*, respectively. When $\zeta > 0$, the system is stable, and the oscillation exhibits a decaying trend. When $\zeta = 0$, the system has zero damping, resulting in sustained oscillations with constant amplitude. When $\zeta < 0$, the system exhibits negative damping, leading to divergent oscillations. However, due to the limitations of the circuit and device characteristics, divergent oscillations will eventually transition into sustained oscillations with constant amplitude. Based on the analysis of different oscillation mechanisms in Section II, this section further investigates the influence of various parasitic parameters on multimode oscillations.

Fig. 15 shows contour plots of the damping ratio ζ as a function of various parameters. Fig. 15(a)–(c) illustrate the variation of damping ratio when Q_2 occurs SSO, with experimental conditions of $V_{bus} = 100$ V and $I_L = 25$ A. Fig. 15(a) shows the variation of damping ratio between R_{G1} and L_{S1}. The system becomes increasingly unstable as L_{S1} increases and R_{G1} decreases. Fig. 15(b) illustrates that ζ initially decreases and then increases with the increase of L_{G1}. Fig. 15(c) shows that ζ decreases and then increases as L_{loop} increases. From this, it can be concluded that L_{S1} is negatively correlated with ζ, meaning that larger L_{S1} results in smaller ζ. R_{G1} is positively correlated with ζ, meaning that larger R_{G1} leads to larger ζ. Both excessively large or small values of L_{G1} and L_{loop} tend to enhance system stability, with the specific effects depending on V_{bus}. Fig. 15(d)–(f) show the contour plots of the system's damping ratio when Q_2 occurs FTO. Fig. 15(d) illustrates the variation of damping ratio between L_{S2} and R_{G2}. Increasing L_{S2} and decreasing R_{G2} make the system more unstable. Fig. 15(e) shows that ζ initially decreases and then increases with the increase of L_{G2}, however, the effect is minimal, particularly near the critical value, where variations in L_{G2} have negligible impact on ζ. Fig. 15(f) demonstrates that increasing L_{loop} can enhance the system stability.

Fig. 16(a) illustrates the variation of damping ratio for two undamped oscillations as the drain–source voltage changes. ζ_1 represents the damping ratio for SSO, and ζ_2 represents the damping ratio for FTO. The analysis indicates that as the drain–source voltage increases, the damping ratio of the SSO feedback system begins to decrease. When the voltage reaches approximately 40 V, ζ_1 becomes negative, indicating that the SSO feedback system becomes unstable, and Q_2 occurs SSO. As the drain–source voltage further increases to 80 V, ζ_2 also drops to zero, which will occur FTO. Fig. 16(b) and (c) illustrate the oscillation regions of the top and bottom devices under different gate resistances and common source inductances. It can be observed that the green region corresponds to $\zeta_1 < 0$, where SSO occurs, while the red region corresponds to $\zeta_2 < 0$, where FTO occurs. When both ζ_1 and ζ_2 are negative, the FTO of Q_2 tends to dominate the oscillation process.

IV. Simulation and Experimental Verification

A. Simulation Verification

In this section, the proposed model is validated using LTspice simulations. A half-bridge circuit is constructed based on the LTspice model provided by Infineon. Furthermore, the

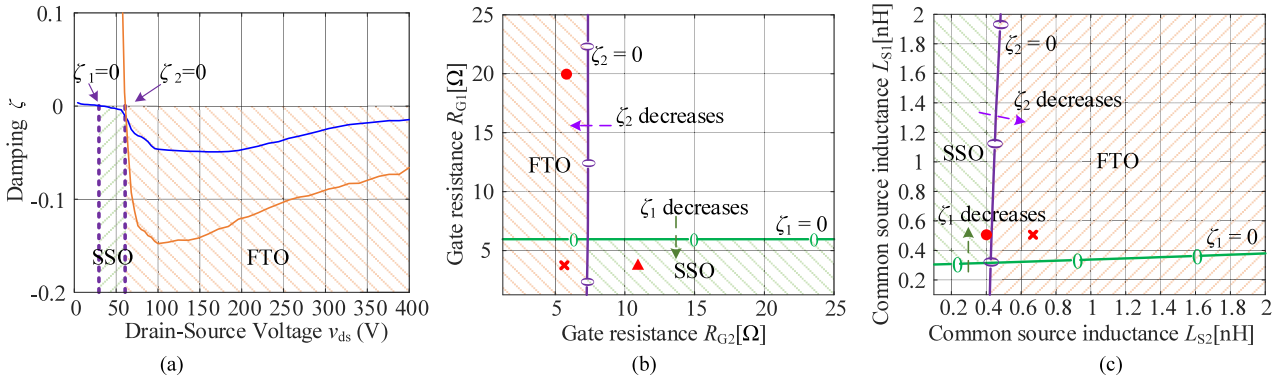

Fig. 16. Undamped oscillations region under different circuit parameters. (a) v_{ds}. (b) R_{G1} and R_{G2}. (c) L_{S1} and L_{S2}.

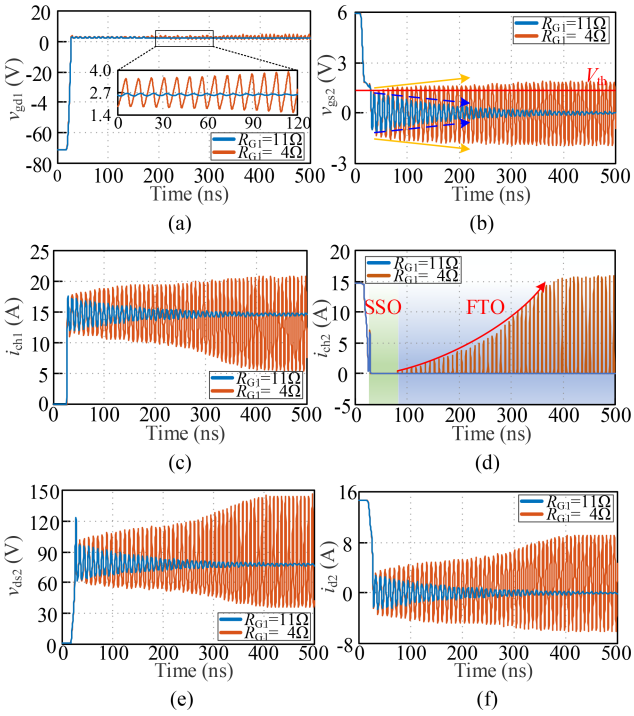

Fig. 17. Simulation waveforms under different R_{G1} at $R_{G2} = 6\ \Omega$. (a) v_{gd1}. (b) v_{gs2}. (c) i_{ch1}. (d) i_{ch2}. (e) v_{ds2}. (f) i_{d2}.

GS66508T model is modified to enable observation of the devices' channel current.

Fig. 17 shows simulation waveforms of v_{gd1}, v_{gs2}, i_{ch1}, i_{ch2}, v_{ds2}, and i_{d2} under different R_{G1}, respectively. When $R_{G1} = 11\ \Omega$, circuit is stable and occurs damped oscillation. However, when R_{G1} increases to $4\ \Omega$, Q_2 occurs SSO initially. It should be noted that due to the diverging tendency of SSO during the initial period, v_{gs2} also diverges and eventually exceeds V_{th}, as shown in Fig. 17(b). At this time, the oscillation mode transitions from SSO to FTO. Fig. 17(c) and (d) illustrate the channel currents of the top and bottom devices, confirming the switching process between two undamped oscillations. These results verify the conclusion in Section II-B that the FTO of Q_2 tends to dominate the oscillation process.

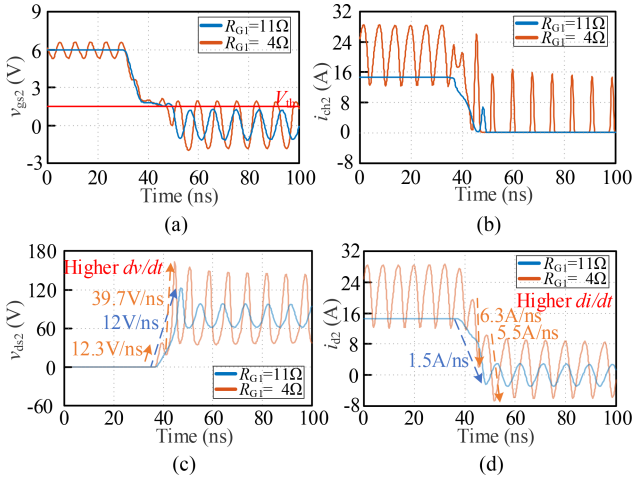

Fig. 18. Simulation waveforms under different R_{G1} at $L_{S1} = 1$ nH, $L_{S2} = 0.7$ nH, $R_{G2} = 6\ \Omega$. (a) v_{gs2}. (b) i_{ch2}. (c) v_{ds2}. (d) i_{d2}.

Fig. 18 verifies that undamped oscillations in the previous process influence *dv/dt* and *di/dt* in the subsequent switching transient. When R_{G1} is $11\ \Omega$, Q_2 does not occur FTO, resulting in converging waveforms. When R_{G1} increases to $4\ \Omega$, as analyzed earlier, since Q_1 occurs FTO during the turn-ON period of Q_2, which will cause higher *di/dt* and *dv/dt* in the subsequent switching transient, thus occurring FTO, as shown in Fig. 18(a) and (b). As shown in Fig. 18(c) and (d), when the system remains stable, *dv/dt* and *di/dt* are approximately 12 V/ns and 1.5 A/ns, respectively. Under the oscillatory state, *dv/dt* and *di/dt* reach peak values of 39.7 V/ns and 6.3 A/ns, respectively.

B. Experimental Verification

As shown in Fig. 19, it is the experimental platform of a GaN-based half-bridge circuit with an inductance load. The switching devices are 650 V e-mode GaN HEMT (GS66508T) produced by Infineon, and the driver chip is SI8271AB. A coaxial shunt resistor (SSDN-10) is used to measure the current, which has a high bandwidth (2000 MHz), a resistance of 0.1 Ω, and a parasitic inductance of 2 nH. Table II lists the other experiment parameters of this prototype.

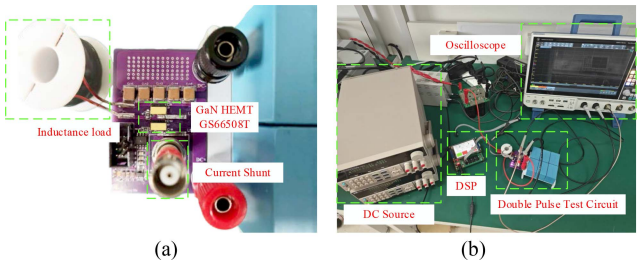

Fig. 19. Experimental platform. (a) Half-bridge circuit. (b) Top view of the experimental platform.

TABLE II
EXPERIMENT PARAMETERS

Parameter	Description	Value
V_{bus}	DC input voltage	100 V
I_{L}	Load current	25 A
V_{G}	Driver voltage	6 V
R_{G1}	Gate resistance of Q_1	3.2 Ω
R_{G2}	Gate resistance of Q_2	4.3 Ω

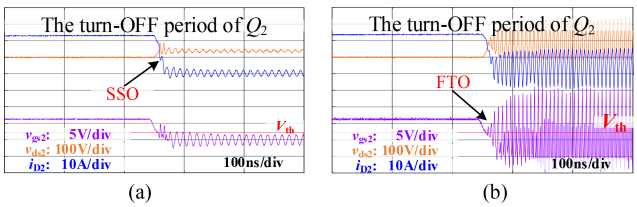

Fig. 20. Measured waveforms under different bus voltage ($I_{\text{L}} = 25$ A). (a) $V_{\text{bus}} = 40$ V. (b) $V_{\text{bus}} = 80$ V.

1) Bus Voltage: To verify the accuracy of the proposed model and the switching mechanism of multimode undamped oscillation, experiments are conducted under different bus voltages. Fig. 20 shows the voltage and current waveforms of Q_2. When the voltage is 40 V, Q_2 occurs SSO. As the voltage increases to 80V, the oscillation mode commutates from SSO to FTO. The experimental results show good agreement with the predictions shown in Fig. 16.

2) Load Current: The magnitude of the load current directly affects the Condition I, therefore, the occurrence of FTO is affected by load current. Fig. 21 illustrates undamped oscillations at different current levels. When I_{L} is 25 A, FTO occurs due to high *di/dt*, which satisfies Condition I. In contrast, the establishment of Condition I for SSO is independent of external parameters. Therefore, as long as Condition II of the SSO feedback system is satisfied, SSO will occur. As shown in Fig. 21(a), when the load current decreases to 2 A, SSO still occurs.

3) Gate Resistance: When R_{G2} increases, the gate impedance of Q_2 becomes larger, resulting in the FTO feedback system becoming negative. As a result, FTO is suppressed and Q_2 remains in the turn-OFF state. Under this condition, the SSO feedback system is established. If the SSO feedback system

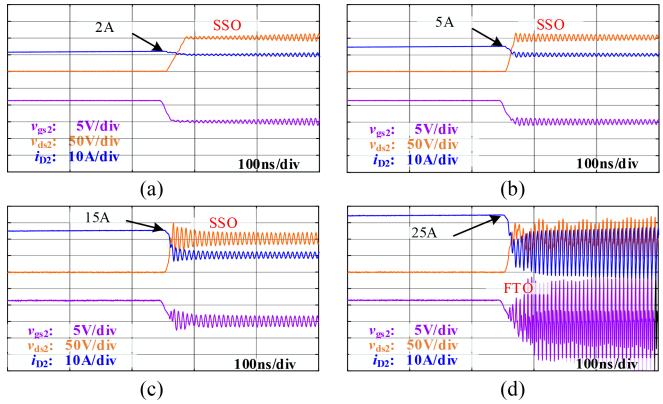

Fig. 21. Measured waveforms under different load current ($V_{\text{bus}} = 100$ V). (a) $I_{\text{L}} = 2$ A. (b) $I_{\text{L}} = 5$ A. (c) $I_{\text{L}} = 15$ A. (d) $I_{\text{L}} = 25$ A.

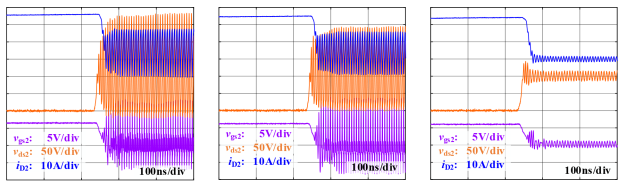

Fig. 22. Measured waveforms under different gate resistance at $L_{\text{S1}} = 0.5$ nH, $L_{\text{S2}} = 0.65$ nH ($V_{\text{bus}} = 100$ V, $I_{\text{L}} = 25$ A). (a) $R_{\text{G1}} = 2\ \Omega$, $R_{\text{G2}} = 4.3\ \Omega$. (b) $R_{\text{G1}} = 19\ \Omega$, $R_{\text{G2}} = 4.3\ \Omega$. (c) $R_{\text{G1}} = 2\ \Omega$, $R_{\text{G2}} = 11\ \Omega$.

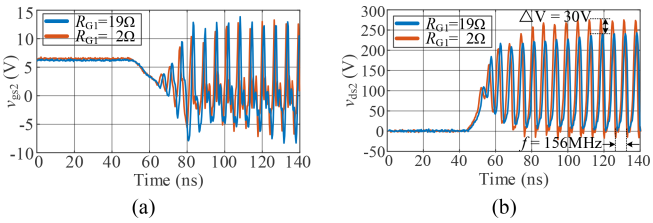

Fig. 23. Comparison of measured waveforms under different R_{G1}. (a) Gate–source voltage. (b) Drian–source voltage.

exhibits positive feedback, Q_2 will occur SSO, as shown in Fig. 22(a) and (c). Moreover, as previously analyzed, the SSO phenomenon is masked by the FTO, and the gate parameters of Q_1 have minimal impact on the system's dominant poles, as illustrated in Fig. 14(b). Therefore, as shown in Fig. 22(a) and (b), FTO occurs regardless of the variation in R_{G1}.

Fig. 23 further compares the effects of different R_{G1} values on the FTO. As shown in Fig. 23(a), the amplitude and resonant frequency of v_{gs2} are barely affected under different R_{G1}. As illustrated in Fig. 23(b), different R_{G1} only slightly influences the oscillation amplitude of v_{ds2}.

4) Common Source Inductance (CSI): The effect of CSI on the circuit system stability is relatively complex. If the CSI and the oscillation source are associated within the same devices, it will have a significant impact. On the other hand, if the CSI and the oscillation source are associated with different devices, the CSI can be considered as part of the loop inductance. As shown in Fig. 24(a), the parasitic parameters in the circuit satisfy all

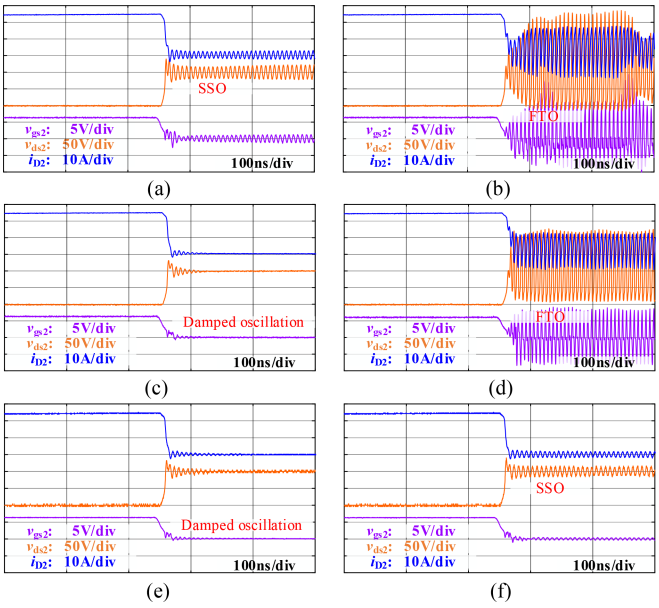

Fig. 24. Measured waveforms under different CSI ($V_{\rm bus}$ = 100 V, $I_{\rm L}$ = 25 A). (a) $R_{\rm G1}$ = 2 Ω, $L_{\rm S1}$ = 0.5 nH, $R_{\rm G2}$ = 3.7 Ω, $L_{\rm S2}$ = 0.4 nH. (b) $R_{\rm G1}$ = 2 Ω, $L_{\rm S1}$ = 0.5 nH, $R_{\rm G2}$ = 3.7 Ω, $L_{\rm S2}$ = 0.65 nH. (c) $R_{\rm G2}$ = 6.1 Ω, $L_{\rm S2}$ = 0.5 nH. (d) $R_{\rm G2}$ = 6.1 Ω, $L_{\rm S2}$ = 1 nH. (e) $R_{\rm G1}$ = 3.2 Ω, $L_{\rm S1}$ = 0.3 nH. (f) $R_{\rm G1}$ = 3.2 Ω, $L_{\rm S1}$ = 0.65 nH.

conditions for the SSO feedback system, while two conditions for the FTO feedback system are not simultaneously met. As a result, Q_2 occurs SSO. When $L_{\rm S2}$ increases, the oscillation amplitude of $v_{\rm gs2}$ becomes larger, eventually occurring false turn-ON, thereby satisfying Condition I of FTO. Meanwhile, the FTO feedback system becomes positive feedback. Consequently, the oscillation mode commutates from SSO to FTO, as illustrated in Fig. 24(b). When the circuit only satisfies the conditions for FTO but not for SSO, increasing $L_{\rm S2}$ causes the circuit to commutate from damped oscillation to FTO, as shown in Fig. 24(c) and (d). When the circuit system only satisfies the conditions for SSO but not for FTO, increasing $L_{\rm S1}$ causes the circuit to commutate from damped oscillation to SSO, as shown in Fig. 24(e) and (f).

5) Loop Inductance: Increasing the loop inductance can suppress SSO, as shown in Fig. 25(a) and (b), the circuit transitions from SSO to damped oscillations, while the voltage overshoot rises to 450 V. Similarly, increasing the loop inductance can also suppress FTO. As illustrated in Fig. 25(c) and (d), the circuit transitions from FTO to damped oscillations, and the drain–source voltage overshoot reaches 480 V. Although increasing the loop inductance can suppress undamped oscillations, excessive loop inductance results in larger voltage overshoot, which may cause device failure. Therefore, in practical layout design, the loop inductance should still be minimized as much as possible.

6) Influence of Current and Voltage Slew Rate on Subsequent Stages: Since the circuit also works in the saturation region during switching transients, the undamped oscillation from the previous stage will influence the voltage and current slew rates in the subsequent switching transient. As shown in Fig. 26(a), the circuit begins to commutate from FTO to SSO. Fig. 26(b)

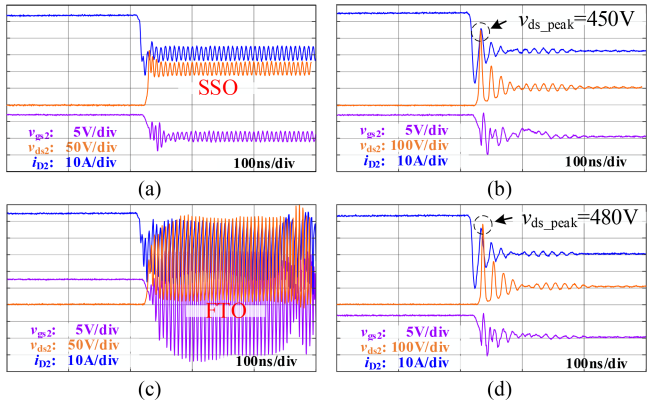

Fig. 25. Measured waveforms under different loop inductance ($V_{\rm bus}$ = 100 V, $I_{\rm L}$ = 25 A, $L_{\rm S1}$ = 0.4 nH, $L_{\rm S2}$ = 0.5 nH, $R_{\rm G1}$ = 2 Ω). (a) $L_{\rm loop}$ = 7.4 nH, $R_{\rm G2}$ = 4 Ω. (b) $L_{\rm loop}$ = 25.6 nH, $R_{\rm G2}$ = 4 Ω. (c) $L_{\rm loop}$ = 7.4 nH, $R_{\rm G2}$ = 3 Ω. (d) $L_{\rm loop}$ = 25.6 nH, $R_{\rm G2}$ = 3 Ω.

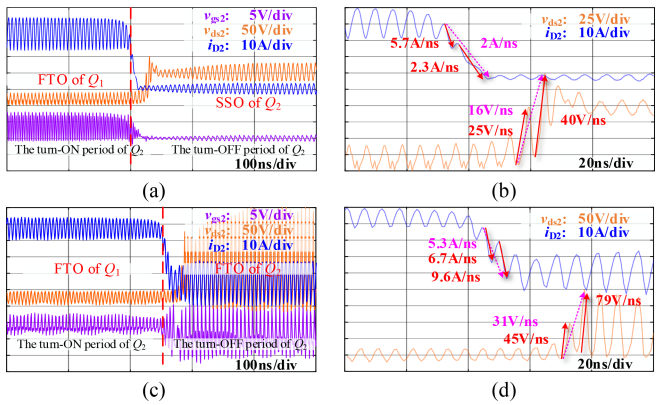

Fig. 26. Switching process of multi-mode undamped oscillations. (a) Switching from FTO during the turn-ON period of Q_2 to SSO during its turn-OFF period. (b) Waveform details corresponding to (a). (c) Switching from FTO during the turn-ON period of Q_2 to FTO during its turn-OFF period. (d) Waveform details corresponding to (c).

illustrates that the maximum *di/dt* and *dv/dt* can reach 5.7 A/ns and 40 V/ns, respectively, while average current and voltage slew rate are about 2 A/ns and 16 V/ns. Fig. 26(c) shows the circuit commutates from FTO to FTO, and Fig. 26(d) illustrates that the maximum *di/dt* and *dv/dt* can reach 9.6 A/ns and 79 V/ns respectively, while average current and voltage slew rate are about 5.3 A/ns and 31 V/ns. Therefore, the experiment results prove that FTO during the turn-ON period of Q_2 intensifies Condition I of FTO during turn-OFF period, because Condition I of FTO is sensitive to both *di/dt* and *dv/dt*.

C. Guidelines to Suppress FTO and SSO Simultaneously

Based on the above analysis, FTO and SSO can be suppressed from different perspectives. First, false turn-ON is a necessary condition for establishing the FTO feedback system. Therefore, a clamping circuit can be added across gate–source node to prevent the gate–source voltage from exceeding the threshold voltage, thereby suppressing FTO. As shown in Fig. 21, when Q_2 does not occur false turn-ON, FTO is effectively suppressed.

Second, the establishment of the SSO feedback system is solely influenced by the reverse conduction characteristics. Therefore, a diode can be connected in parallel between drain and source node of the passive device to suppress SSO [17]. In addition, as illustrated in Fig. 24, reducing the common source inductance and optimizing the gate resistance, as well as incorporating an RC snubber circuit can prevent the SSO feedback system from becoming positive feedback [1], [18].

V. Conclusion

This article proposes a comprehensive investigation on the multimode undamped oscillations. First, the necessary conditions for oscillations occurrence are identified. Then, the basic switching law between FTO and SSO within the same process, and the influence of FTO in the previous stage on the subsequent switching transient are revealed. These phenomena make the analysis of multiple undamped oscillations different from that of single oscillations. Subsequently, the high-frequency equivalent models are employed to evaluate the influence of various parasitic parameters on the generation and switching of undamped oscillations. The results indicate that when the conditions for both FTO and SSO are simultaneously satisfied, the oscillation is dominated by FTO. Finally, both simulation and experimental results validate the proposed generation mechanisms and switching laws. Based on the analyses in this article, the targeted solutions are proposed to suppress all undamped oscillations. For instance, a clamping circuit can be employed to clamp the gate–source voltage of Q_2 below its threshold voltage, thereby inhibiting the establishment of the FTO feedback system. In addition, optimizing parasitic inductance and gate resistance, or incorporating an RC snubber circuit, can prevent the SSO feedback loop from becoming unstable effectively. It provides the systematical guidance for further research on multimode undamped oscillations.

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