Letters

Resonant Double Pulse Test Setup

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***Abstract*—This letter proposes a novel resonant double-pulse test method for evaluating power semiconductor devices under realistic resonant converter operating conditions. The test setup enables precise evaluation of power losses and switching behavior as observed in practical resonant converters, specifically *LLC* converters, accounting for the influence of device-intrinsic parasitic capacitances, resonant tank parameters, dead time, and operating temperature. Rather than designing a complete resonant converter, which typically includes a high-frequency transformer, complete design spaces can be explored with less effort, and parameters can be optimized, thereby ensuring zero-voltage switching and improving overall efficiency. Finally, the proposed method is experimentally validated by evaluating the performance of a silicon-carbide device operating at 1 MHz, but the presented principles are general and applicable to any power semiconductor devices, regardless of their voltage and current ratings.**

***Index Terms*—Characterization, double-pulse test (DPT), *LLC* resonant converter, zero-voltage switching (ZVS).**

I. Introduction

RESONANT converters, particularly the *LLC* topology, have attracted considerable interest in recent years because of their ability to achieve high efficiency, reduce electromagnetic interference, and minimize switching losses. Research efforts have primarily focused on optimizing magnetic components and control strategies to improve overall system-level performance with respect to efficiency, power density, and transient response. However, evaluating the performance of semiconductor switching devices under realistic resonant operating conditions, prior to converter realization, has received relatively limited attention.

The conventional double-pulse test (DPT) is a standardized method used to characterize the switching behavior of semiconductor devices under hard-switching conditions. While effective in many applications, the DPT is inherently limited to linear current waveforms and therefore cannot faithfully replicate the sinusoidal or quasi-sinusoidal current profiles encountered in resonant converters, such as the *LLC* converter. To address this limitation, a modified test setup was proposed in [1], where the device under test (DUT) is subjected to either triangular or sinusoidal current excitation. However, that approach requires four active switches, and the mechanism for controlling the resonant current is not clearly defined, thereby limiting its practicality. Other studies [2], [3] introduced resonant test platforms, as shown in Fig. 1(a), aimed at characterizing integrated gate-commutated thyristor (IGCTs) operating at high frequencies. Nevertheless, these works primarily focus on IGCT performance and gate-driver design, and provide limited details regarding the test setup. Furthermore, in this circuit configuration, the placement of the magnetizing inductance L_m results in its voltage being clamped to the input, which is useful for precisely defining turn-OFFcurrent, but fails to reflect actual operating conditions of the *LLC* converter.

To address the aforementioned limitations, a novel resonant DPT (Res-DPT) circuit is proposed, as shown in Fig. 1(b). In this setup, the current through each switching device consists of two components: 1) a triangular magnetizing current associated with L_m and 2) a sinusoidal resonant current of the L_r–C_r

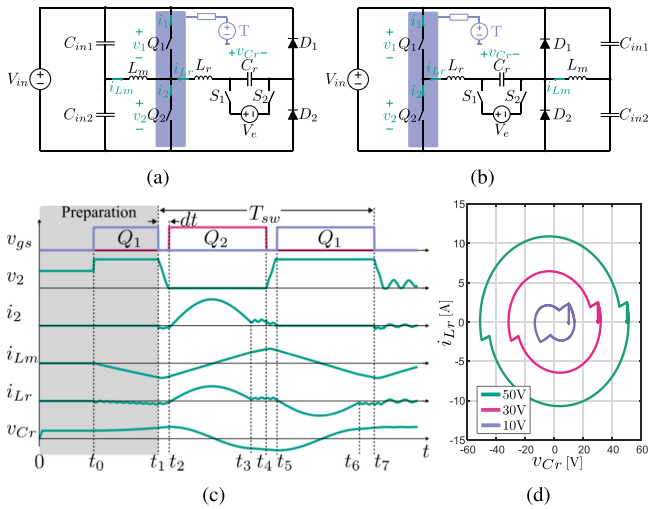

Fig. 1. DPT setup and representative operating waveform. (a) DPT circuit in [2] and [3]. (b) Circuit diagram of the proposed Res-DPT. The switching devices are mounted on a heating plate at a temperature T. (c) Typical operating waveforms of Res-DPT. (d) $v_{Cr} - i_{Lr}$ state-plane locus at different steady-state operating points (power).

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tank. In addition, the placement of the magnetizing inductor results in the current profile that closely reproduces the electrical stress encountered in *LLC* converters. (It should be noted that the proposed Res-DPT is valid for *LLC* converters with an approximately 50% duty cycle, operating below resonance or at exact resonance.)

II. Generalized Operating Principle of Res-DPT

The proposed Res-DPT provides a device-agnostic platform for reproducing resonant-converter stress at the device without building a full converter. The setup comprises two DUTs and two diodes providing freewheeling paths for the resonant current; the resonant inductor L_r, resonant capacitor C_r, and magnetizing inductance L_m are selected to match and mimic those of the target converter. The corresponding gate signals and representative device voltage and current waveforms are presented in Fig. 1(c). Throughout this work, the switching frequency satisfies $f_{\text{sw}} \leq f_r$, where f_r is the resonant frequency of the $L_r - C_r$ tank. The operation comprises two stages: 1) a preparation interval [shaded in Fig. 1(c)]; and 2) a testing interval.

A. *Preparation Interval:* $0 - t_1$

1) C_r is precharged by the charging circuit, comprising switches S_1 and S_2, and external power supply V_e, to the desired $v_{C_r}(t_1)$. This voltage appears when the resonant current is ZERO, and resonant current will be established in the subsequent swing. The v_{C_r} - i_{L_r} state-plane locus is illustrated in Fig. 1(d), allowing for easy identification of initial conditions for resonant capacitor voltage, matching the desired operating point (power) of the resonant converter.
2) Turn OFF S_1 and S_2 at t_0 to disconnect C_r from the external power supply, and turn Q_1 ON at t_0 to prebias L_m from the dc input. Adjust the on-time of Q_1 to a) set the desired turn-OFF current of Q_1 at t_1 and Q_2 at t_4, and b) eliminate the dc bias in i_{Lm} during the test.

B. *Testing Stage:* $t_1 - t_7$

Following the preparation interval, which provides needed initial conditions to achieve desired steady state operating point during testing, two pulses are applied, corresponding to nearly *50% duty cycle* operation of the resonant converter.

1) $t_1 - t_2$: At t_1, Q_1 is turned OFF with the desired turn-OFF current, allowing turn-OFF dynamics and energy to be characterized. After dead time dt, Q_2 turned ON at t_2. At this instant, the turn-ON performance of Q_2 can be studied. During dt, the output capacitance of both switching devices will be charged and discharged, respectively. By observing the gate-source and drain-source voltage waveforms at t_2, the zero-voltage switching (ZVS) condition of Q_2 can be examined, considering the device's output capacitance, magnetizing current defined by L_m, and the value of dead time. All these parameters can be adjusted as desired in testing.
2) $t_2 - t_3$: With Q_2 turned ON, C_r releases energy and resonates with L_r. The resonant current will freewheel through diode D_2. Due to the conduction of D_2, the voltage across the L_m is approximately clamped to half of the input, and the magnetizing current flows through the resonant tank and device Q_2. Analogous to *LLC* operation, when the secondary side rectifier conducts, the voltage of the L_m is clamped to the output voltage referred to the primary side, and the device current comprises resonant and magnetizing components.
3) $t_3 - t_4$: Since $f_{\text{sw}} < f_r$, the resonant current component reaches zero at t_3 and D_2 ceases conduction; consequently, the voltage across L_m is no longer clamped and L_m participates in the L_r–C_r resonance, mirroring the *LLC* operating condition in which all secondary rectifier diodes are off. By contrast, in the topologies of [2] and [3], the placement of L_m keeps it effectively clamped while Q_2 is on, reducing fidelity to *LLC*-representative conditions. By integrating the voltage and current of the Q_2 from t_2 to t_4, the conduction loss of the switching devices under realistic waveforms can be obtained.
4) $t_4 - t_5$: At t_4, Q_2 is turned OFF; after the dead time dt, Q_1 turned ON at t_5. These two instants permit turn-OFF and turn-ON characterization, respectively, and ZVS of Q_1 at t_5 can be verified from the gate-source and drain-source voltage waveforms.
5) $t_5 - t_7$: The operation is mirror symmetric to t_2–t_4, the resonant current reverses polarity, and the corresponding conduction loss of Q_1 can be evaluated approximately.

In summary, the proposed Res-DPT enables concurrent testing of two semiconductor devices, including power-loss measurement and switching-dynamics characterization under realistic waveforms representative of *LLC* converter operation.

III. Influence of Parasitic Elements

With the emergence of wide band gap devices, the operating frequency of the power electronics converter significantly increases to improve power density. For these high-frequency applications, achieving ZVS is essential to enhance converter efficiency and reduce electrical and thermal stress on power semiconductors. Rather than relying on datasheet-based methods, e.g., energy-based predictions [4], [5] and charge-based predictions [6], the proposed Res-DPT enables detailed examination of the ZVS condition while explicitly accounting for nonlinear device output capacitance and *LLC*-specific operating conditions, as well as easy addition of other parasitic capacitances.

Fig. 2 illustrates the current paths during the testing interval. Here, the DUTs are two silicon carbide (SiC) MOSFETs, and Schottky diodes provide the freewheeling paths. It can be seen that in addition to the primary $L_r - C_r$ resonance, two types of transition oscillations arise: 1) during the dead-time intervals ($t_1 - t_2, t_4 - t_5$), and 2) during the resonance current discontinuous intervals ($t_3 - t_4, t_6 - t_7$). In what follows, the intervals $t_3 - t_4$ and $t_4 - t_5$ are analyzed as representative cases.

At t_3, since the circuit operates at below-resonance mode ($f_{\text{sw}} < f_r$), no current flows through the diode D_2; consequently,

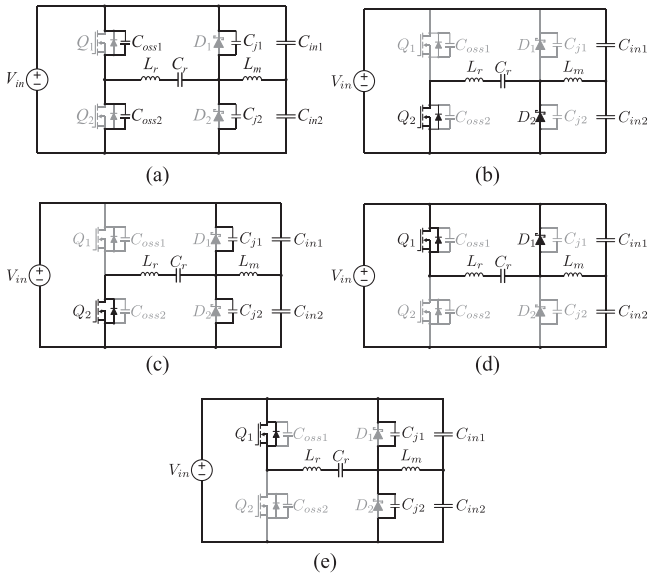

Fig. 2. Current paths during the indicated intervals; gray elements are non-conducting. (a) $t_1 - t_2$ and $t_4 - t_5$. (b) $t_2 - t_3$. (c) $t_3 - t_4$. (d) $t_5 - t_6$. (e) $t_6 - t_7$.

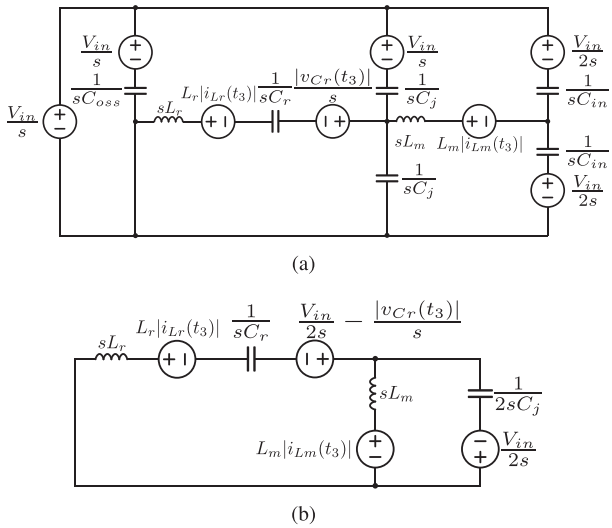

Fig. 3. Circuit diagrams for the interval $t_3 - t_4$. (a) s-domain equivalent circuit. (b) Simplified equivalent circuit.

L_m and C_j (the junction capacitance of the freewheeling diode) participate in the resonance with L_r and C_r. The s-domain equivalent circuit of the proposed Res-DPT during this interval is depicted in Fig. 3(a) and equivalently in Fig. 3(b). The input capacitance C_{in} is neglected because $C_{\text{in}} \gg C_j$. In addition to the magnetizing current i_{Lm}, a high-frequency resonant component appears in the tank current, which affects the subsequent turn-OFF current of Q_2 at t_4. Fig. 4(a) illustrates s-domain circuit models of the Res-DPT during the dead time, with the equivalent circuit depicted in Fig. 4(b). During this interval, both devices output capacitance C_{oss} and the diode junction capacitance C_j are charged and discharged, thereby affecting the charging and discharge rates and, hence, the transition speed of the switching device.

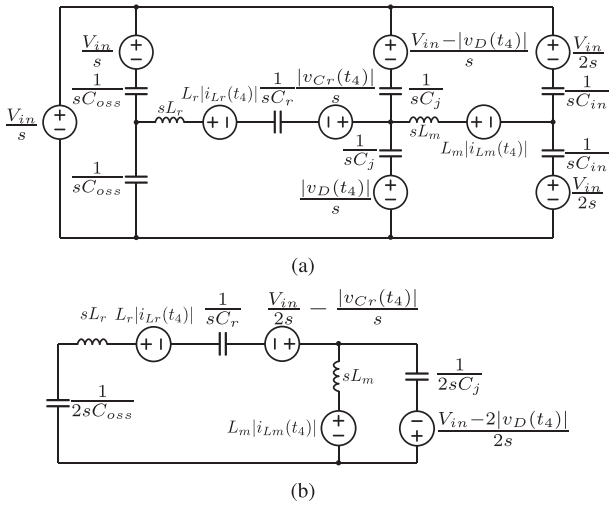

Fig. 4. Circuit diagrams for the dead-time interval $t_4 - t_5$. (a) s-domain equivalent circuit. (b) Simplified equivalent circuit.

TABLE I
PARAMETERS OF RES-DPT SETUP AND LLC CONVERTER

Parameter	Value	Parameter	Value
V_{in}	400 V	f_{sw}	1 MHz
L_r	0.6 µH	C_r	30 nF
L_m	8.2 µH, **15 µH**, 20 µH	$\hat{V}_{Cr}$	16 V to **52.5 V**
$C_{oss1(2)}$	161 pF	$C_{j1(2)}$	20 pF
n	50 / 3	$C_{e1(2)}$	5.5 nF
V_o	12 V	R_o	0.12 Ω

L_m and $\hat{V}_{Cr}$ values employed in the simulations are highlighted in boldface.

In a practical *LLC* converter, the transformer parasitic capacitance and the secondary rectifier junction capacitances will affect the achievement of ZVS for the primary side switching devices because they participate in the resonance during both the dead-time intervals and the current-discontinuous portion of the cycle. Therefore, accurate prediction of ZVS in practice must include all of these capacitances. From the equivalent circuits shown in Figs. 3(b) and 4(b), the proposed Res-DPT is topologically equivalent to an *LLC* converter. By placing extra capacitors in parallel with the diode to emulate the effect of the secondary rectifier junction capacitance and transformer parasitic capacitance, the Res-DPT enables prior evaluation of the primary-side switching characteristics, and the resonant-tank components and dead time can then be optimized to achieve ZVS.

Fig. 5 compares the Res-DPT with an *LLC* converter in simulation. Table I lists the simulation parameters, L_m and V_{cr} values employed in the simulations are highlighted in boldface. The close agreement between the two sets of waveforms confirms that the Res-DPT closely reproduces the resonant operating conditions of an *LLC* converter.

IV. EXPERIMENT VALIDATION AND DISCUSSION

To demonstrate the effectiveness of the proposed Res-DPT, a test setup for an SiC device was implemented (Fig. 6). The setup parameters are listed in Table I, and the main components and

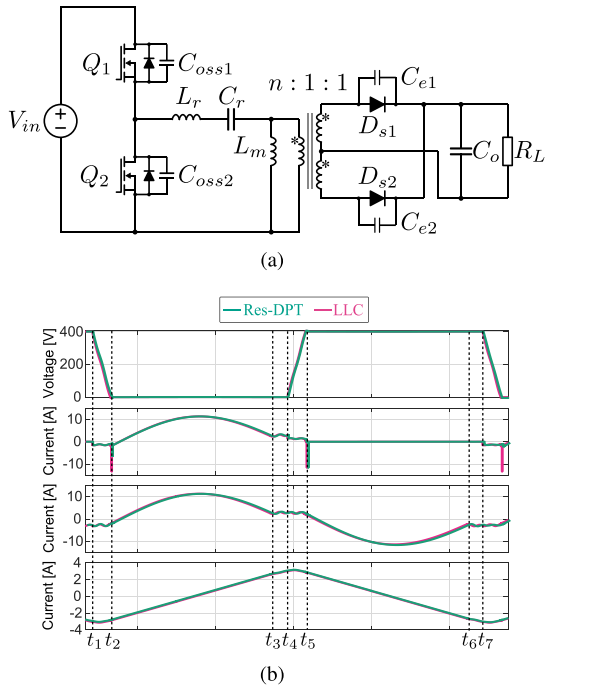

Fig. 5. Simulation validation of the Res-DPT. (a) Reference *LLC* resonant converter. (b) Simulation waveforms of the Res-DPT and *LLC* converter during the testing interval.

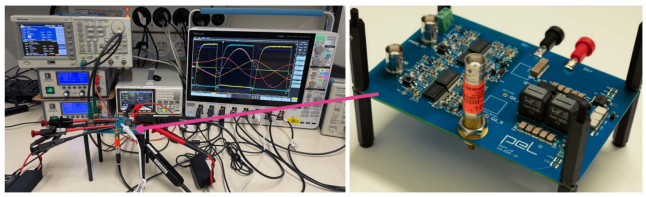

Fig. 6. Res-DPT setup for testing SiC MOSFETs.

TABLE II
COMPONENTS AND MEASUREMENT EQUIPMENT OF RES-DPT SETUP

Item	Part No.	Description
Q_1 and Q_2	IMLT65R033M2H	650V SiC Mosfet
D_1 and D_2	C3D02065E-TR	650V Schottky diode
Gate driver	UCC21759	10 A Source/Sink
Digital oscilloscope	MSO58B	1 GHz, 12 Bits
Current measuring resistor	SSDN-414-10	0.1 Ω 2 GHz
Differential voltage probe	DP705	±700 V 500 MHz
Voltage probe	701939	600 V 500 MHz
Current probe	TCP305A	50 A, 50 MHz
Function generator	AFG3022C	250 MS/s
Heating Component	56760-500	Thermoelectric Peltier

measurement equipment are summarized in Table II. For electrical measurements, a current-sense resistor and a low-capacitance passive voltage probe were used to measure the current through and the drain-to-source voltage of the low-side device, while two differential probes captured the gate-drive signals. To regulate temperature, the devices were mounted on a thermoelectric Peltier module using thermal interface material. A thermocouple attached to the Peltier module monitored the plate temperature; to approximate a junction temperature of 125 °C, the Peltier

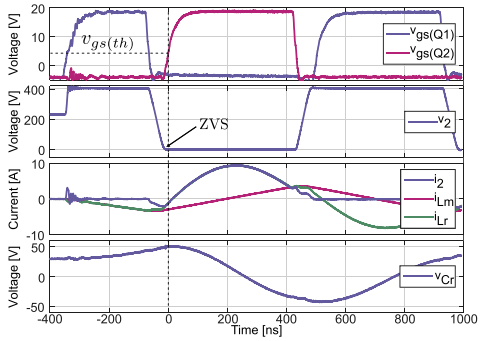

Fig. 7. Experimental waveform of the Res-DPT setup (dt =70 ns).

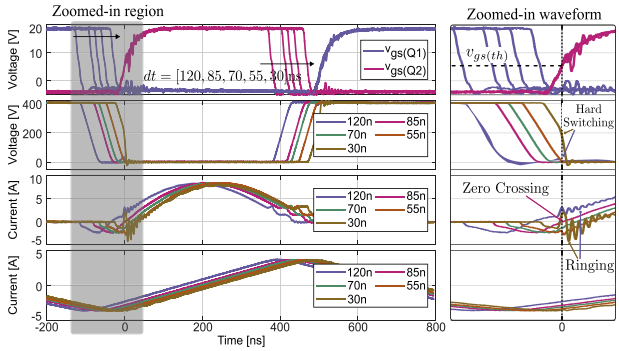

Fig. 8. Effect of the dead time on switching performance. The straight arrow indicates decreasing dead time. From top to bottom: $v_{gs(Q1)}$ and $v_{gs(Q2)}$; v_2; i_2; and i_{Lm}.

setpoint was controlled to 135 °C. Unless otherwise noted, all results reported as follows were obtained at this temperature.

A. Experimental Results

Fig. 7 presents experimental waveforms with the dead time set to 70 ns; these results verify that the Res-DPT reproduces *LLC*-like waveforms at the device terminals, and—with the chosen resonant-tank parameters and dead time, ZVS is achieved. Extending this, Fig. 8 sweeps the dead time with the magnetizing inductance held at 15 μH: ZVS is maintained for 55 to 85 ns, whereas for dead times below 55 ns, the devices' output capacitances cannot fully discharge (brown trace), leading to hard switching, ringing, and increased loss; and for dead times above 85 ns, the device current reverses before the gate signal, the output capacitance recharges (purple trace), and hard switching results. With the resonant-tank parameters fixed, varying L_m changes magnetizing current amplitude and shifts the ZVS window; Fig. 9 maps the dead-time ranges that achieve ZVS, and presents i_{Lm} amplitude at the turn-OFF instant (t_1 and t_4).

Measurement results demonstrate that the Res-DPT allows device-level evaluation for *LLC* applications without building a full converter. Furthermore, it provides a practical bench-top means to optimize the resonant tank parameters, especially L_m, and specify the dead time to secure ZVS. When loss information is needed, switching energy and conduction losses can be obtained by integrating the measured voltage–current product

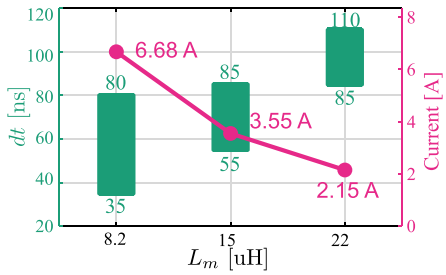

Fig. 9. ZVS boundary versus dead time at different L_m.

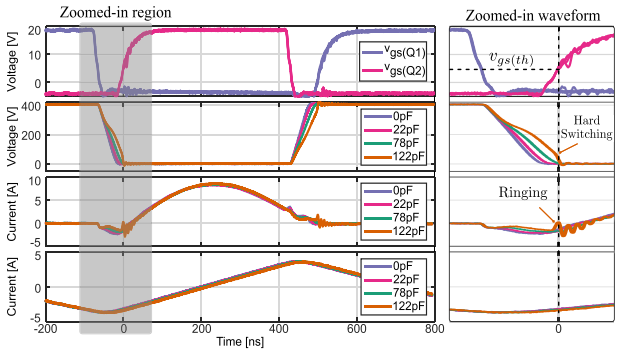

Fig. 10. Effect of the auxiliary diode-parallel capacitance on the switching behavior.

over the corresponding transition and conduction intervals, respectively.

B. Discussion

Fig. 10 shows waveforms for different parallel capacitances to the diodes at a fixed dead time of 70 ns. The added capacitance participates in the resonance during both the current-discontinuous interval and the dead time, thereby shifting the ZVS boundary. In this setup, when the added capacitance exceeds 78 pF, ZVS is no longer achieved.

As discussed, this auxiliary capacitance provides a means to emulate the secondary-rectifier junction capacitance and the transformer parasitic capacitance during measurement. However, the fidelity of this emulation is limited by the accuracy of the estimated transformer and diode-junction capacitances.

V. Conclusion

In this letter, a novel Res-DPT setup is proposed. The setup reproduces current and voltage waveforms representative of resonant operation (e.g., an *LLC* converter operating below resonance or at exact resonance), enabling rapid and accurate device-level evaluation of switching losses and dynamics. The resulting measurements inform device selection and guide optimization of resonant-tank parameters, particularly L_m, and the dead time dt to achieve ZVS. To substantiate the approach, the methodology was validated on an SiC platform through simulations and hardware experiments. Although validated only on a SiC platform, the method is general and applicable to a broad range of power semiconductor devices for evaluating their performance under resonant operating conditions.

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