Multiharmonic Frequency-Domain Model With MOSFET Junction Capacitance for Digital Synchronous Rectification in 300-kHz SiC Bidirectional *CLLC* Converters

Haoran Li, *Member, IEEE*, Xin Wang, Cungang Hu, *Senior Member, IEEE*, Xirui Zhu,
Xi Tang, *Member, IEEE*, Zhiliang Zhang, *Senior Member, IEEE*, and Wenping Cao, *Senior Member, IEEE*

***Abstract*—Hardware detections or complex time-domain models are generally adopted in conventional *CLLC* synchronous rectification (SR). However, they are vulnerable to high *dv/dt* generated by SiC power devices, or encounter challenges in achieving high-precision SR because of the fitting method limitations. High-precision SR is crucial as the forward voltage of SiC MOSFETs body diode can be five times higher than Si MOSFETs, which will cause high conduction loss. A digital SR algorithm based on frequency-domain model is proposed for SiC-based bidirectional *CLLC* converter. Considering multiple harmonics and SR MOSFETs junction capacitance, the secondary current phase and the SR on-time are calculated by the proposed model to determine the SR turn-ON and turn-OFF instants. It provides high-precision and reliable SR driving signals without extra hardware detections and is immune to high-frequency noise. To validate the proposed SR, a prototype of 6.6-kW 300-kHz SiC bidirectional *CLLC* charger was built. The forward *CLLC* efficiency is up to 98.28% at 6.6 kW and the reverse *CLLC* efficiency is 98.16% at 3.3 kW. Compared to the time-domain SR method, the efficiency increments are 0.28% and 0.18% in the forward and reverse modes, respectively.**

***Index Terms*—*CLLC* converter, frequency-domain model, multiharmonics, SiC power devices, synchronous rectification (SR).**

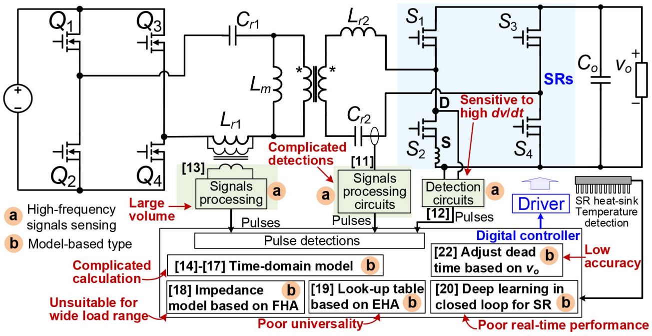

Fig. 1. Existing *CLLC* SR strategies.

I. INTRODUCTION

BIDIRECTIONAL operations are widely required in many applications, such as electrical vehicle charger, energy storage, and energy recycling dc electronic load. *LLC* resonant converter can achieve wide ZVS range and high efficiency, but it is hardly used in the bidirectional operations. [1], [2], [3] Since the reverse *LLC* converter becomes *LC* resonant converter, the output voltage cannot be regulated with pulse frequency modulation (PFM) [4]. Fortunately, the *CLLC* converter is suitable for bidirectional operation because of the symmetric structure and wide ZVS range [5].

Compared to conventional Si MOSFETs, SiC MOSFETs own lower parasitic capacitance, faster switching speed, and lower ON-state resistance, which can be used in the *CLLC* converters to achieve high efficiency and high-power density. In the bidirectional operations, synchronous rectification (SR) control is important for the conduction loss reduction [6], [7].

The forward voltage of SiC MOSFETs body diode V_{sd} can be up to five times higher than Si MOSFETs. For example, 600 -V 20 -mΩ Si MOSFETS (IPDQ60R020CFD7) from Infineon is only 0.9 V, while V_{sd} of 650 -V 20 -mΩ SiC MOSFETs body diode (IMW65R020M2H) from Infineon is 4.3 V. Moreover, wide load range in the *CLLC* converter will cause large variation of SR on-time, so that the accuracy of SR gate signals is important to achieve high efficiency [8], [9]. If the SR on-time is too long, it will cause reverse current and high circulating loss. If it is too low, the rectifier current will flow through the body diode of SR MOSFET. Thus, it is crucial to make full use of high precision SR with SiC power devices.

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Haoran Li, Xin Wang, Cungang Hu, Xi Tang, and Wenping Cao are with the School of Electrical Engineering and Automation, Anhui Province Engineering Research Center for Advanced Power Electronics and Energy Conversion, Anhui University, Hefei 230601, China (e-mail: haoranli@ahu.edu.cn; xinwang@stu.ahu.edu.cn; hcg@ahu.edu.cn; xitang@ahu.edu.cn; wpcao@ahu.edu.cn).

Xirui Zhu is with Aerospace System Engineering, Shanghai 201100, China (e-mail: xiruizhu@nuaa.edu.cn).

Zhiliang Zhang is with the Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zlzhang@nuaa.edu.cn).

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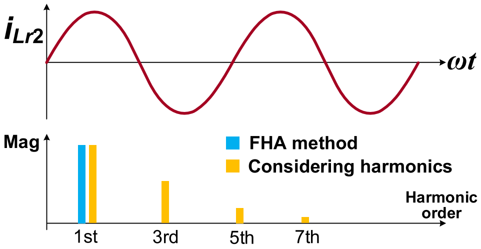
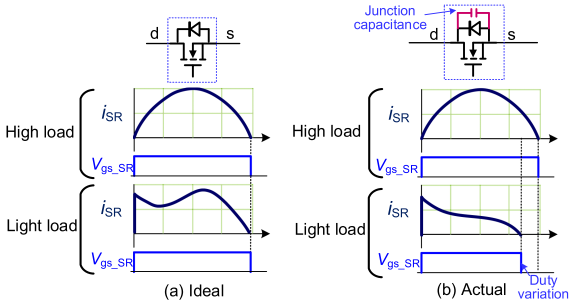
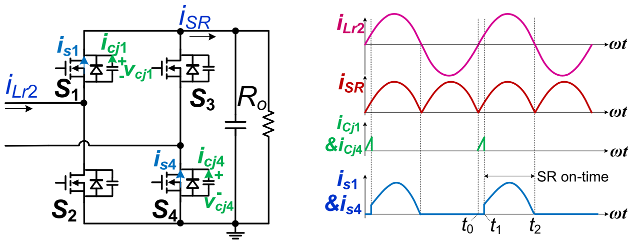


Fig. 2. FFT analysis for secondary transformer current.



(a) Ideal (b) Actual

Fig. 3. Waveforms of SR driving signals. (a) Ideal. (b) Actual.



(a) (b)

Fig. 4. Rectifier circuit and waveforms. (a) Rectifier circuit. (b) Waveforms.

The *CLLC* SR methods can be generally divided into two types: high-frequency voltage/current sensing methods and model-based calculation methods.

A. High-Frequency Voltage/Current Sensing Methods

As shown in Fig. 1, the SR method is implemented by sensing the high-frequency resonant voltage/current or the drain-source voltage of SR MOSFETs. In [10], the resonant current is sensed by a current transformer sensor. With rectifier circuit, the sampled resonant current can be converted into a dc current signal, which will be sent to the input of a comparator. By comparing with a fixed value, pulses will be generated and sent to the DSP to regulate the SRs.

In [11], the high-frequency resonant currents on the primary and secondary sides are sensed by using Rogowski coil sensors. The sensor-generated pulses are subsequently transmitted to the DSP for SRs control. However, the extra sensors inevitably increase the *CLLC* converter volume and complexity.

A SR method is proposed consisting of drain-source voltage sensing circuit and a customized valley-conduction-detection circuit [12]. It employs a combination of blocking and absorptive diodes to detect the SR body diode conduction. Through real-time monitoring of the rectifier switches operational states, the SR driving signals can be derived directly. By sensing the resonant inductor voltage, an SR control is presented in [13]. The resonant current polarity is determined by integrating the inductor voltage through a voltage sensing coil and integrator circuit. This polarity detection enables the DSP to produce SR driving signals.

The hardware detections inevitably induce complexity and extra PCB space to the *CLLC*. Furthermore, the utilization of SiC power devices generates high *dv*/*dt*, which will cause false operation of detection circuits through parasitic inductance.

B. Model-Based Calculation Methods

In the time domain, a *CLLC* SR using switching delay is presented in [14] considering the hard turn-ON issue of SR MOSFETs. However, it employs a search-based method to determine the switching delay, which results in excessive computation and limits the viability for high-frequency applications. In [15], a real-time computation *CLLC* SR is proposed and the analytic models are constructed to calculate the SR conduction time. But it adopts approximation method to achieve the SR on-time, which hurts the SR accuracy.

A superposition principle-based method for the *CLLC* converters is proposed under the above-resonant frequency-mode in [16] by using simplified time-domain analysis. An expression of the voltage gain, resonant currents, and voltages is obtained to calculate the SR time. To derive the SR angle fitting formulas, a time-domain *CLLC* converter model is developed in [17]. While the computational demands are reduced, it compromises the SR accuracy.

In the frequency domain, an impedance model-based SR scheme is proposed in the resonant converter [18]. The equivalent impedance models are built to calculate the SR on-time. It uses fundamental harmonic approximation (FHA) and neglects high-order harmonics, so that it is unsuitable for wide load range applications. An extended harmonics approximation method is used in [19] to achieve the *CLLC* SR. A look-up table is adopted to address the algorithmic complexity. But the SR implementation shows limited universality due to the parameter dependency and the equivalent output capacitance of SR MOSFETs is also neglected causing low accuracy.

A SR strategy using deep-learning techniques was proposed in [20] to determine the SR MOSFET regulation principle. But using a thermocouple to sample the loss data is time-intensive causing poor real-time performance. With a neural-network model, a strategy is studied to provide initial SR control signals [21]. But the data used to train the neural network are also derived from the *CLLC* time-domain model, which is inconvenient compared to the SR directly from analytic model.

In [22], an SR method is proposed to dynamically adjust the deadtime based on the variations of output voltage, thereby modulating the SR on-time accordingly. However, it fails to include the output current variations causing low accuracy.

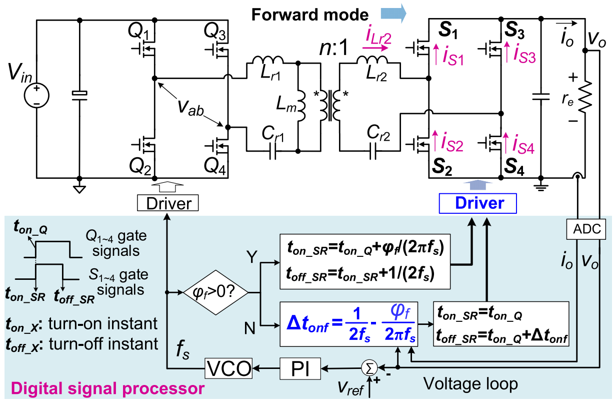


Fig. 5. Proposed *CLLC* SR using frequency-domain model in forward mode.

The contribution is to present a digital SR algorithm for SiC *CLLC* using multiharmonic frequency-domain model. The secondary current phase and SR on-time are derived accurately to calculate the SR switching instants with high efficiency.

The rest of this article is organized as follows. Section II gives the SR challenge and Section III proposes the SR control. Section IV analyzes the proposed model and Section V introduces the transient. Section VI gives the design and tolerances analysis. Section VII shows the experiments. Finally, Section VIII concludes this article.

II. CHALLENGES FOR HIGH-PRECISION *CLLC* SR ALGORITHM IN SIC-BASED APPLICATIONS

A. *Effects of Multiple Harmonics Consideration in High-Precision SRs Regulation*

Fig. 2 illustrates the FFT analysis of transformer current on the secondary side. The ac current can be decomposed into fundamental harmonic and multiple harmonics, which will be rectified through the rectification bridge. Conventional FHA method only considers the fundamental harmonics causing low accuracy, so that the high-order harmonics should also be considered. In order to achieve high-precision SR control, multiple harmonics are incorporated in the mathematical model. Therefore, it poses serious challenge to build high-precision model for *CLLC* SRs regulation.

B. *Effects of mosfets Junction Capacitance*

Fig. 3 shows the SR conduction time varies with the switching frequency or output loads. When the output loads change in the actual applications, the junction capacitance of SR MOSFETs will affect the variations of SR conduction time. In order to regulate the SRs with high precision, the junction capacitance of SR MOSFETs should be considered.

Fig. 4 demonstrates the *CLLC* rectifier circuit and waveforms. The MOSFETs junction capacitance will affect the SR conduction time and the states are analyzed as follows.

State 1 [t_0, t_1]: In this stage, the rectifier current i_{s1} and i_{s4} flow through the junction capacitance of S_1 and S_4 to release the charge. Then the drain-source voltage V_{cj1} and V_{cj4} will be decreased rapidly. (t_1–t_0) is the discharging time of SR junction capacitance, which is related to the output load.

State 2 [t_1, t_2]: When the drain-source voltage is approaching zero, S_1 and S_4 should be turned on to help i_{s1} and i_{s4} flow through the MOSFETs channel. Otherwise, i_{s1} and i_{s4} will flow

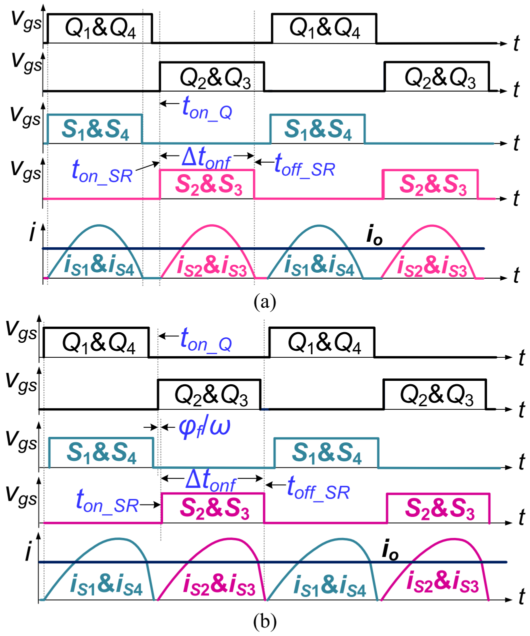


Fig. 6. *CLLC* waveforms in forward mode. (a) Below the resonance. (b) Above the resonance.

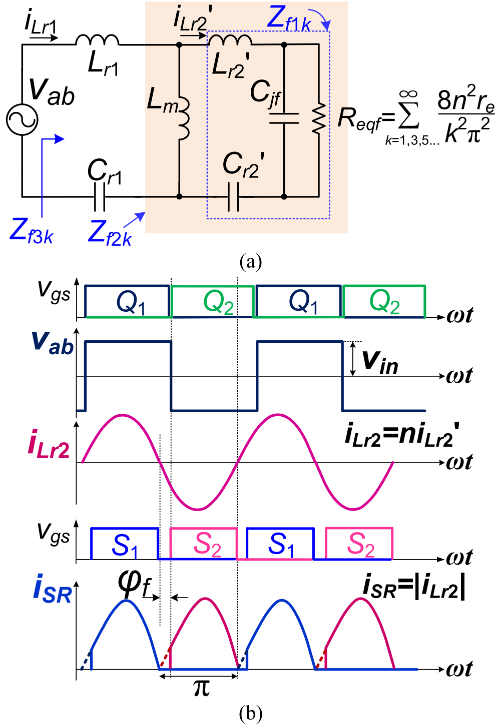


Fig. 7. *CLLC* equivalent circuit and waveforms in forward mode. (a) Equivalent circuit. (b) Waveforms.

into the body diode of SR MOSFETs, which will result in high conduction loss.

The charge of MOSFETs junction capacitance and the output load decide the discharging time (t_1–t_0). (t_2–t_1) is the SR on-time, which will be highly affected by the discharging time. Thus, the SR MOSFETs junction capacitance has to be considered in the SR on-time model, so that the on-time can be controlled precisely.

III. PROPOSED DIGITAL *CLLC* SR SCHEME USING MULTIHARMONIC FREQUENCY-DOMAIN MODEL

The proposed *CLLC* SR scheme using multiharmonic frequency-domain model considering the MOSFET junction capacitor in the forward mode is illustrated in Fig. 5 and the waveforms are shown in Fig. 6. SiC MOSFETs are used to take the advantage of high-voltage/high-frequency characteristics. The forward voltage of SiC MOSFETs body diode can be up to five times higher than Si, which will result in higher conduction loss. Thus, it is crucial to make full use of SR control when using the SiC MOSFETs.

The secondary current phase φ_f denotes the secondary transformer current i_{Lr2} with respect to the middle point voltage of bridge v_{ab}. The key point is to calculate φ_f and determine the SR on-time $\Delta t_{\mathrm{ON}f}$ from the proposed model, which incorporates the multiple harmonics and SR junction capacitance. From Figs. 5 and 6, when the phase of i_{Lr2} is ahead of v_{ab} (φ_f>0), the SR turn-OFF instant t_{OFF_SR} is based on the calculated SR on-time with identical turn-ON instants for the primary and secondary driving signals. As the phase of i_{Lr2} lags behind v_{ab} (φ_f<0), the SR turn-ON instants t_{ON_SR} equal the primary turn-ON instants t_{ON_Q} plus the phase delay time φ_f.

Compared to the SR methods from Infineon [10] and Texas Instruments (TI) [11], the proposed SR control can be achieved without adding hardware detections in the 300-kHz 6.6-kW applications. Additionally, the SR control in [19] neglects the MOSFETs junction capacitance, so that the SR on-time variations will not be considered that will result in lower accuracy and higher conduction loss.

Thanks to the *CLLC* symmetric structure design, the proposed SR in the reverse mode is same to the proposed control in the forward mode. By using the proposed frequency-domain model considering the multiple harmonics and MOSFETs junction capacitance, the proposed control can be regulated effectively in the reverse mode.

IV. FREQUENCY-DOMAIN MODELING FOR PROPOSED SR

By using the proposed model considering the harmonics and junction capacitance, the SR phase delay time and ON-time are calculated with high precision. Furthermore, the comparisons between the proposed model and simulations are analyzed.

A. Modeling for Proposed SRs

In the forward mode, the *CLLC* equivalent circuit and waveforms are shown in Fig. 7 and the symmetry structure is designed. v_{ab} is the middle point voltage of the bridge that is equal to v_{in}. i_{Lr1} is the primary resonant current and C_{jf} is the equivalent output capacitor of SR MOSFETs. The equivalent junction capacitances of SR MOSFETs are considered as constant value, which equals $2C_{\mathrm{oss}}/n^2$. $L_{r2}{}^{'}$ and $C_{r2}{}^{'}$ denote L_{r2} and C_{r2} reflected from the secondary side to the primary side.

In the proposed model, the fundamental harmonic and extended harmonics are considered and the power devices, resonant *LC* pairs and transformer are ideal. The leakage inductance is emerged with the resonant inductance and the dead time is also neglected in the analysis. $L_{r2}{}^{'}$, $C_{r2}{}^{'}$ are equal to L_{r2}/n^2 and n^2C_{r2} and n is the transformer ratio.

The secondary current in the time domain is

$$i'_{Lr2}(t) = \sum_{k=1,3,5,7\ldots}^{\infty} \sqrt{2}I_{Lr2k}\sin(k\omega t + \varphi_{fk}). \tag{1}$$

I_{Lr2k} is the rms value for secondary current of kth harmonics. In Fig. 7, $i^{'}_{Lr2}$ will have a zero crossing when ωt is equal to φ. It is deduced as

$$i'_{Lr2}(t) = \sum_{k=1,3,5,7\ldots}^{\infty} \sqrt{2}I_{Lr2k}\sin(k\varphi + \varphi_{fk}) = 0. \tag{2}$$

The secondary current phase φ_f can be calculated and its sign is opposite to φ. The key point is to calculate φ considering multiple harmonics. The impedance Z_{f1k} is

$$Z_{f1k} = g_{1k} + \mathrm{j}h_{1k}. \tag{3}$$

g_{1k} and h_{1k} are

$$g_{1k}{=}R_{eqf}/(R_{eqf}{}^2C_{jf}{}^2k^2\omega^2 + 1) \tag{4}$$

$$h_{1k}{=}k\omega L'_{r2} - \frac{R^2_{eqf}C_{jf}k\omega}{R^2_{eqf}C^2_{jf}k^2\omega^2 + 1} - \frac{1}{k\omega C'_{r2}} \tag{5}$$

where ω is the switching frequency in angle. The output equivalent resistance is defined as

$$R_{eqf}{=}\sum_{k=1,3,5\ldots}^{\infty}\frac{8n^2r_e}{k^2\pi^2}. \tag{6}$$

r_e is the output load and k is kth harmonic. Therefore, the impedance angle of Z_{f1k} is

$$\varphi_{f1k} = \arctan(g_{1k}/h_{1k}). \tag{7}$$

Considering the magnetizing inductance L_m, Z_{f2k} is

$$Z_{f2k} = Z_{f1k}//(\mathrm{j}k\omega L_m) = \frac{g_{2k} + \mathrm{j}h_{2k}}{p_{2k} + \mathrm{j}q_{2k}} \tag{8}$$

where g_{2k}, h_{2k}, p_{2k}, and q_{2k} are

$$g_{2k} = (C_{jf}f_n^2 - C'_{r2} - C_{jf})R_{eqf}L_mk^2\omega^2 \tag{9}$$

$$h_{2k} = (1 - k^2f_n^2)k\omega L_m \tag{10}$$

$$p_{2k} = 1 - (1+\lambda)k^2f_n^2 \tag{11}$$

$$q_{2k} = [-(1+\lambda)C_{jf}k^2f_n^2 + C'_{r2} + C_{jf}]R_{eqf}k\omega. \tag{12}$$

f_n is ω/ω_r and ω_r is the resonant frequency. θ_{f2k} is

$$\varphi_{f2k} = \arctan\frac{-g_{2k}q_{2k} + h_{2k}p_{2k}}{g_{2k}p_{2k} + h_{2k}q_{2k}}. \tag{13}$$

TABLE I
FFT ANALYSIS COMPARISONS OF SECONDARY TRANSFORMER CURRENT

Forward mode: v_o = 360 V, P_o = 6.6 kW						
Output load	f_s = 270 kHz			f_s = 330 kHz		
Harmonics	1	3	5	1	3	5
Simulations (A)	20.7	1.55	0.65	18.37	1.28	0.72
Proposed (A)	20.3	1.46	0.63	18.25	1.23	0.70
Tolerances (A)	0.4	0.09	0.02	0.12	0.1	0.02
Reverse mode: v_o = 500 V, f_s = 340 kHz						
Output load	P_o = 1.65 kW			P_o = 3.3 kW		
Harmonics	1	3	5	1	3	5
Simulations (A)	3.54	0.5	0.28	7.11	0.82	0.45
Proposed (A)	3.41	0.48	0.21	6.89	0.75	0.4
Tolerances (A)	0.13	0.02	0.07	0.22	0.07	0.05

The output impedance Z_{f3k} is derived as

$$Z_{f3k} = \frac{1}{\mathrm{j}k\omega C_{r1}} + \mathrm{j}k\omega L_{r1} + Z_{f2k} = \frac{g_{3k} + \mathrm{j}h_{3k}}{p_{3k} + \mathrm{j}q_{3k}} \tag{14}$$

where g_{3k}, h_{3k}, p_{3k}, and q_{3k} in (14) are

$$g_{3k} = (2\lambda + 1)k^4 f_n^4 - (2\lambda + 2)k^2 f_n^2 + 1 \tag{15}$$

$$\begin{aligned} h_{3k} = {} & k\omega R_{eqf} C_{jf}(1 - k^2 f_n^2)\left[1 + m^{-1} - f_n^2(\lambda + 1)\right] \\ & -\lambda k^3 \omega R_{eqf} C_{jf} f_n^2 (m^{-1} + 1 - k^2 f_n^2) \end{aligned} \tag{16}$$

$$p_{3k} = \left[(\lambda + 1)C_{jf} f_n^2 k^2 - (C_{r1} + C_{jf})\right] R_{eqf} C_{r1} k^2 \omega^2 \tag{17}$$

$$q_{3k} = -(\lambda + 1)k^3 \omega C_{r1} f_n^2 + k\omega C_{r1}. \tag{18}$$

The impedance angle of Z_{f3k} is

$$\varphi_{f3k} = \arctan \frac{-g_{3k} q_{3k} + h_{3k} p_{3k}}{g_{3k} p_{3k} + h_{3k} q_{3k}}. \tag{19}$$

The transformer current on the secondary side is

$$\begin{aligned} i'_{Lr2}\angle\varphi_{fk} = {} & \frac{2\sqrt{2}v_{\text{in}}}{k\pi}\angle 0 \cdot \frac{|Z_{f2k}|\angle\varphi_{f2k}}{|Z_{f3k}|\angle\varphi_{f3k} \cdot |Z_{f1k}|\angle\varphi_{f1k}} \\ = {} & I_{Lr2k}\angle(\varphi_{f2k} - \varphi_{f3k} - \varphi_{f1k}). \end{aligned} \tag{20}$$

As φ is lower than zero and φ_f is higher than zero, the SR on-time can be deduced as

$$\Delta t_{\text{on}f} = 0.5 f_s^{-1} - \varphi_f / \omega. \tag{21}$$

When φ is higher than zero and φ_f is lower than zero, the SR on-time is same to the primary side, which has the phase delay of φ_f / ω at turn-ON instant.

B. Comparisons Between Proposed Model and Simulations

Table I gives the comparisons of FFT analysis for the transformer current in the secondary side. The resonant frequency is 300 kHz. As the switching frequency is lower or higher than the resonant frequency, the secondary transformer current can be decomposed into the fundamental harmonic, third harmonic and fifth harmonic. Based on Table I, the proposed model is able to analyze the secondary-side current of transformer and help to achieve the SR function.

Fig. 8 gives the SR conduction time comparisons at 280 and 340 kHz. The *CLLC* resonant frequency is 300 kHz. Based on Fig. 8, the tolerance is as low as 0.66% and 0.27% when

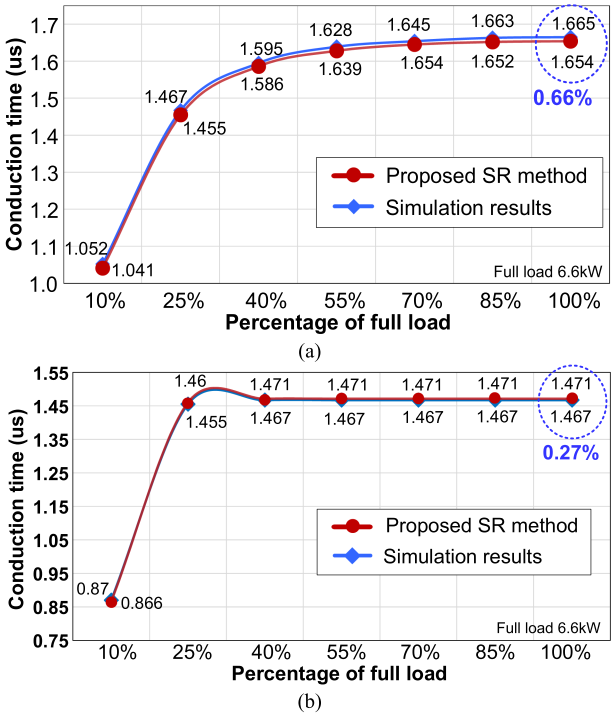


Fig. 8. SR on-time comparisons in forward mode. (a) $v_o = 400$ V, $f_s = 280$ kHz. (b) $v_o = 350$ V, $f_s = 340$ kHz.

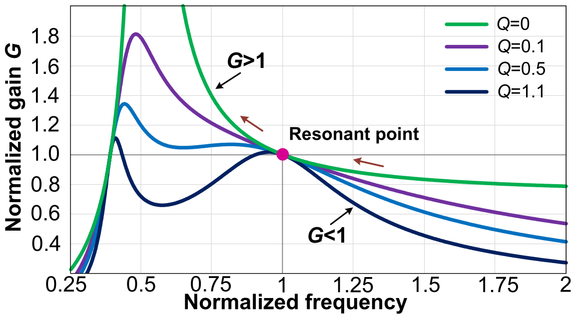


Fig. 9. *CLLC* voltage gain curve.

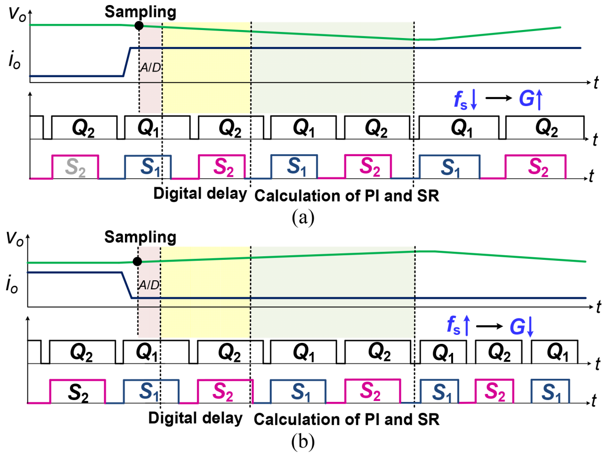


Fig. 10. *CLLC* driving signals when loads change. (a) Loads step up. (b) Loads step down.

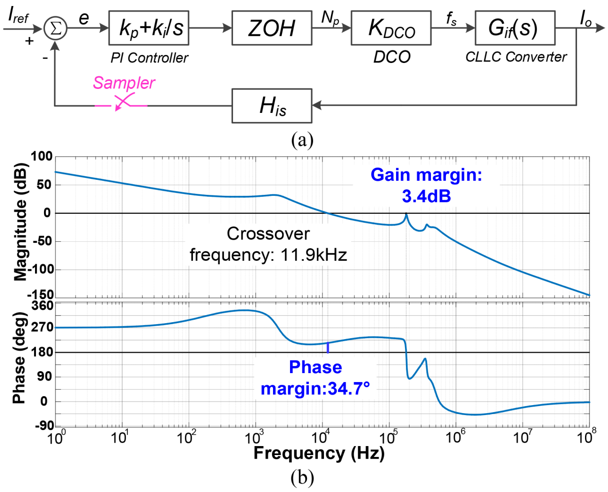


Fig. 11. *CLLC* control. (a) Control loop of output current. (b) Bode diagram: $f_s = 280$ kHz, $V_o = 460$ V, $P_o = 6.6$ kW.

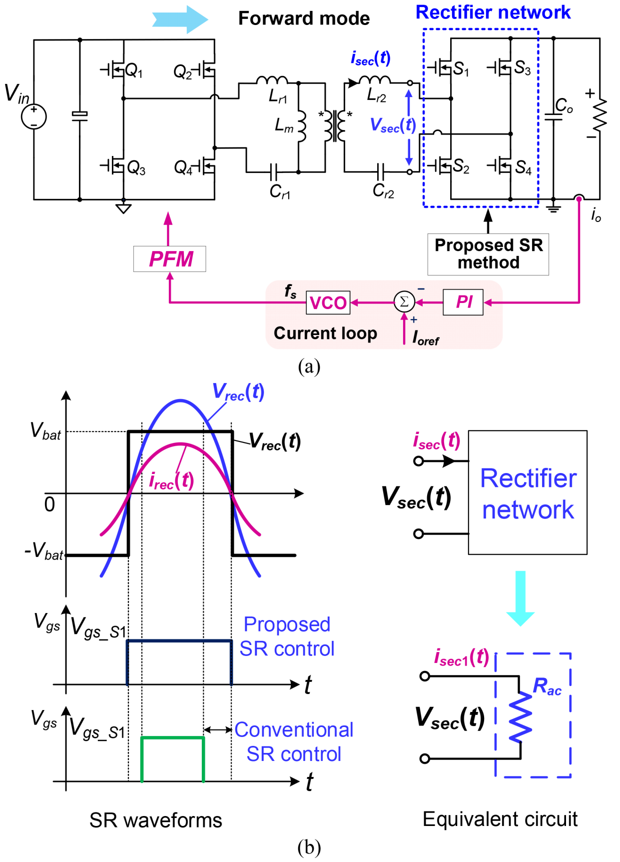


Fig. 12. SR waveforms and equivalent circuit of rectifier network. (a) Forward *CLLC* control. (b) SR waveforms and rectifier equivalent circuit.

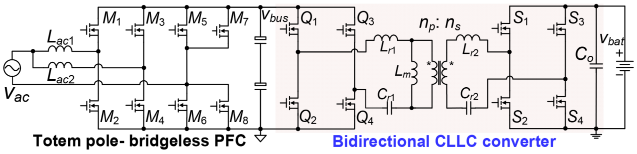


Fig. 13. Topology of SiC bidirectional *CLLC* charger.

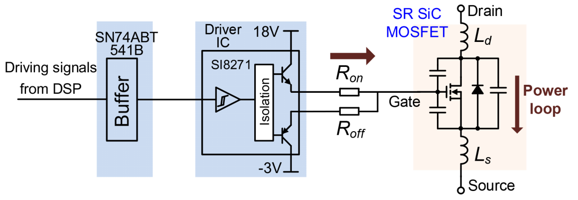


Fig. 14. *CLLC* driving circuit for SiC MOSFET.

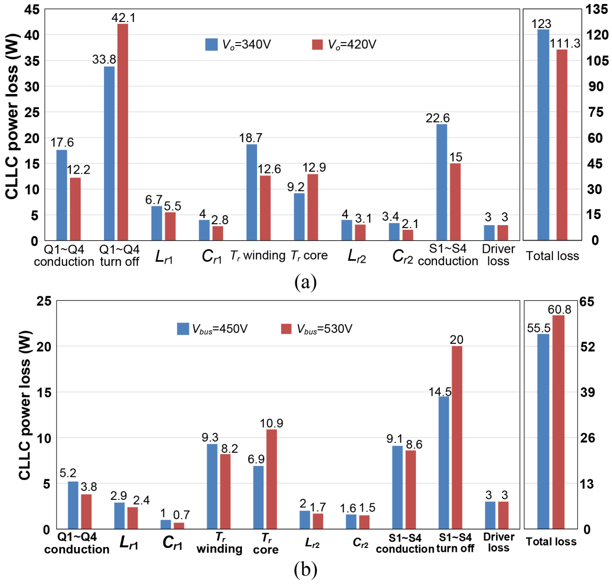


Fig. 15. Power loss analysis: $f_s = 300$ kHz. (a) Forward mode: $P_o = 6.6$ kW. (b) Reverse mode: $P_o = 3.3$ kW.

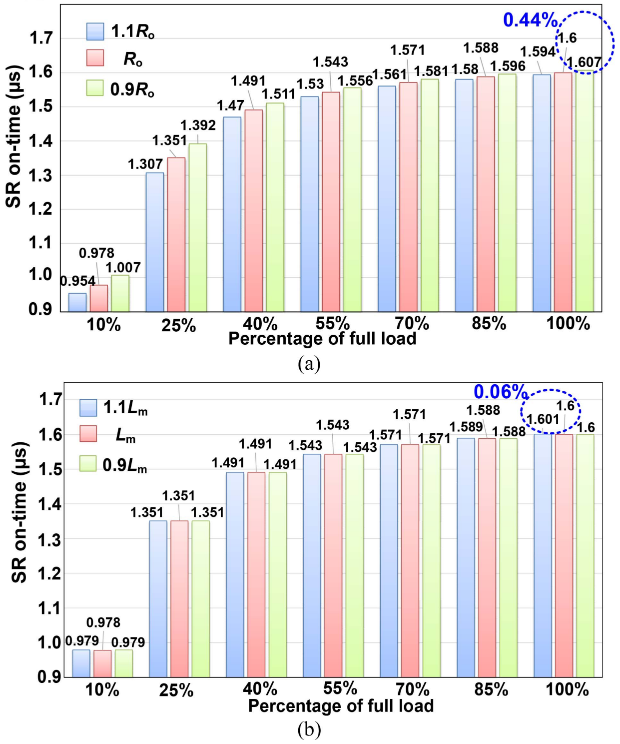


Fig. 16. Parameter tolerances in forward mode: $v_o = 400$ V, $f_s = 300$ kHz. (a) Output load. (b) Magnetizing inductance.

the switching frequency is higher or lower than the resonant frequency at full load. Thus, when considering the harmonics, the proposed method can achieve high precision to implement the SR performance.

V. ANALYSIS OF TRANSIENTS AND CONTROL SYSTEM

In the dynamic response, SR safety should be considered primarily. As for the proposed SR, it can work effectively in the dynamic response. Moreover, the *CLLC* control stability analysis is also given to validate the proposed control.

A. *Transients Analysis for Proposed SR*

Fig. 9 shows the *CLLC* voltage gain curve. G denotes the *CLLC* normalized gain and Q is the quality factor. PFM is generally adopted to regulate the *CLLC* output voltage or current [23], [24]. When the output load changes, the switching frequency f_s will vary to maintain the output voltage or current.

Fig. 10 illustrates the driving signals when the transient happens. From Fig. 10(a), as the loads step up, the SR on-time cannot be calculated timely due to the ADC processing delay and digital delay. But the SR on-time is limited by the last SR on-time calculation. In Fig. 10(b), as the transient happens, the SR on-time is maintained from the last SR calculation, which has been limited to avoid the shoot through.

B. *Stability Analysis for* CLLC *Control*

Fig. 11 shows the *CLLC* control loop of output current and the bode diagram. H_{is} is unity and K_{DCO} is the gain of digital oscillation which is 1800. k_p and k_i are 1.2 and 0.012 in the PI controller, respectively. Based on Fig. 11, the gain margin and phase margin for the *CLLC* control system are 3.4 dB and 34.7°, so that it is stable as the switching frequency changes.

The *CLLC* control in the charging mode and the SR equivalent circuit and waveforms are shown as Fig. 12. $V_{\text{sec}}(t)$ and $i_{\text{sec}}(t)$ are the transformer voltage and current on the secondary side. $V_{\text{sec}1}(t)$ and $i_{\text{sec}1}(t)$ are the fundamental harmonics of $V_{\text{sec}}(t)$ and $i_{\text{sec}}(t)$. From Fig. 12, the rectifier network is equivalent to a resistive load and the proposed SR control does not affect the model of the *CLLC* converter. Consequently, the SR control will have no effect on the *CLLC* control parameters design and the system stability. Moreover, the *CLLC* output current and voltage does not contain the double frequency ripple due to the *CLLC* control design. Hence, the input double frequency ripple voltage will have no effect on the calculation step.

VI. *CLLC* PARAMETERS DESIGN AND TOLERANCE EFFECTS ANALYSIS

The *CLLC* parameters design is introduced including the transformer ratio, resonant tank parameters, and power devices selections. The *CLLC* power loss by using the proposed SR is analyzed. The parameters tolerances are evaluated carefully, which are too low to affect the SR implementations.

TABLE II
PARAMETERS FOR BIDIRECTIONAL SiC *CLLC* CONVERTER

Parameters	Symbol	Values
Charging/discharging power	P_{o1}/ P_{o2}	6.6 kW/3.3 kW
DC-link voltage	v_{bus}	380 V−700 V
Transformer ratio	n_p: n_s	10:7
Primary resonant inductor/ capacitor	L_{r1}/ C_{r1}	8.7 μH/32 nF
Secondary resonant inductor/ capacitor	L_{r2}/ C_{r2}	4.3 μH/63 nF
Magnetizing inductor	L_m	36.9 μH
Output battery voltage	v_{bat}	200 V−500 V
CLLC switching frequency range	f_{s_CLLC}	260 kHz−390 kHz
CLLC resonant frequency	f_r	300 kHz
Primary SiC MOSFETs	Q_1−Q_4	IMW120R030M1H
Secondary SiC MOSFETs	S_1−S_4	IMW65R020M2H

A. *Parameters Design for* CLLC *Converter*

Fig. 13 illustrates the *CLLC*-based charger topology, which consists of totem-pole bridgeless PFC (TP-BPFC) and *CLLC* converter. The rated charging power is 6.6 kW, so that interleaved inductors for the PFC are adopted.

1) Transformer Turns Ratio Determination: The CLLC output voltage is 200–500 V and the bus voltage is 380–700 V to track the battery voltage. Thus, the transformer ratio can be optimized as 10:7. The resonant frequency is 300 kHz and EE70 was selected as the transformer core from Dongyang magnetics enterprise group company. In the output voltage range of 200–270 V, the switching frequency of *CLLC* converter increases to achieve lower voltage gain.

2) CLLC *Voltage Gains Requirements:* The varying bus voltage is used to reduce the *CLLC* voltage regulation, so that the maximum and minimum voltage gains are deduced as 1.02 and 0.74.

3) Resonant Tank Parameters: With 300-kHz resonant frequency and 6.6-kW output, the resonant tank parameters can be calculated from

$$\pi^2\sqrt{(L_{r1}/C_{r1})}\Big/(8n^2R_{\text{eq}}) = Q \qquad (22)$$

where Q is the quality factor. From (22), L_{r1} is 8.7 μH, C_{r1} is 32 nF and L_m is 36.9 μH. As L_{r1} is equal to L_{r2}/n^2 and C_{r1} is equal to n^2C_{r2}, so that L_{r2} is 4.3 μH and C_{r2} is 66 nF.

4) SiC mosfets Selections: In the primary side, IMW120R030M1H from Infineon is selected with 1200 -V withstand voltage to handle the 700 -V bus voltage. In the secondary side, since the maximum battery voltage is 500 V, IMW65R020M2H from Infineon is adopted with 650 -V withstand voltage. The detailed *CLLC* parameters are shown in Table II.

5) SiC mosfets Driving Circuit Design: The *CLLC* SiC driving circuits is shown in Fig. 14. To achieve the isolation driving circuits of SiC MOSFETs, the driver IC SI8271 from Silicon Labs and isolation power supplies QA01C-18 from MORNSUN are adopted. The input of auxiliary power supplies is 15 V and the isolation output voltage is +18 V/−3 V. Thus, the *CLLC* SiC MOSFETs can be regulated well to achieve low conduction loss and high efficiency.

Fig. 15 shows the *CLLC* power loss distribution. The losses evaluated for each of the components are based on the theoretical calculation. In Fig. 15(a), the total loss in the forward mode is

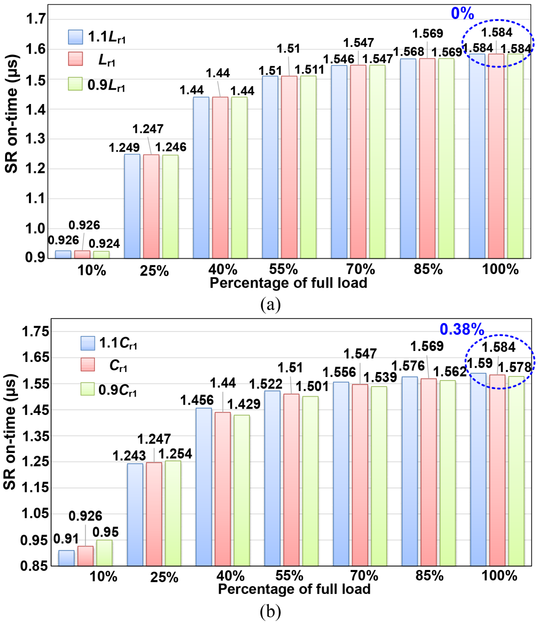


Fig. 17. Parameter tolerances in reverse mode: $v_{\mathrm{bus}} = 450$ V, $f_s = 300$ kHz. (a) Primary resonant inductor. (b) Primary resonant capacitor.

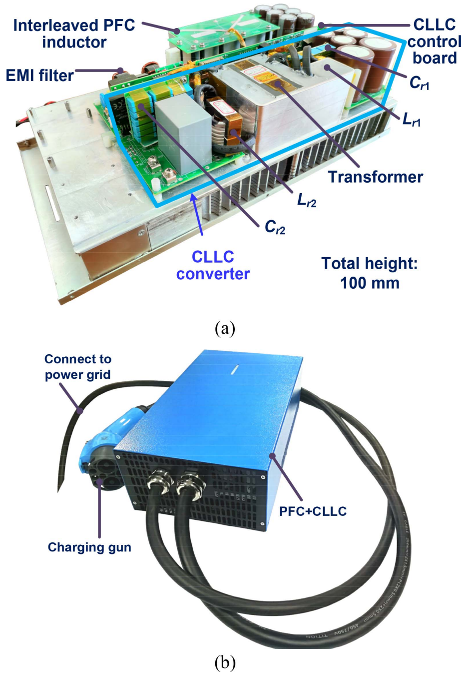


Fig. 18. 6.6-kW 300-kHz SiC-based bidirectional *CLLC* charger. (a) Charger PCB prototype. (b) *CLLC* charger with casing and charging gun.

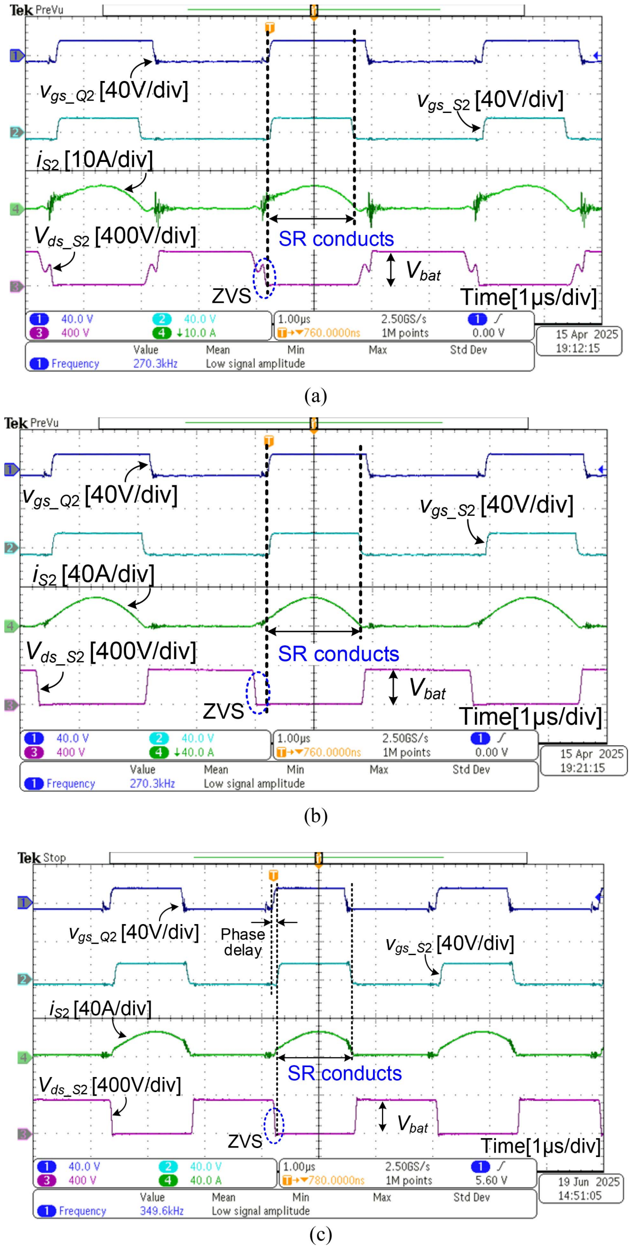


Fig. 19. SR waveforms in forward mode: $v_{\mathrm{bat}} = 360$ V. (a) 20% of full load: $f_s = 270$ kHz. (b) Full load: $f_s = 270$ kHz. (c) Full load: $f_s = 350$ kHz.

only 111.3 W at 420 V output and the efficiency is up to 98.3%. Moreover, the total power loss in the reverse mode is 55.5 W at 450 V and the efficiency is 98.4%, which verifies the *CLLC* design and proposed SR control.

B. Tolerances Effect Analysis for CLLC *Converter*

Fig. 16 illustrates the parameters tolerances analysis in the forward mode. Based on Fig. 16(a), the SR on-time at full load is 1.6 μs, while the SR on-time is 1.607 μs when the output load has 10% tolerance. It can be seen that the tolerance is only 0.44% for the output load. Moreover, when the magnetizing inductance L_m has 10% tolerance, the SR on-time tolerance is as low as 0.06%. Therefore, the *CLLC* parameters tolerance will not affect the proposed SR implementations and the proposed SR control is robust.

Fig. 17 shows the tolerances analysis of primary resonant inductor L_{r1} and primary resonant capacitor C_{r1} in the reverse mode. Based on Fig. 17, the tolerances for L_{r1} and C_{r1} are as low as zero and 0.38% at full load, respectively. Therefore, the proposed SR accuracy will be maintained when the *CLLC* resonant parameters have 10% tolerances.

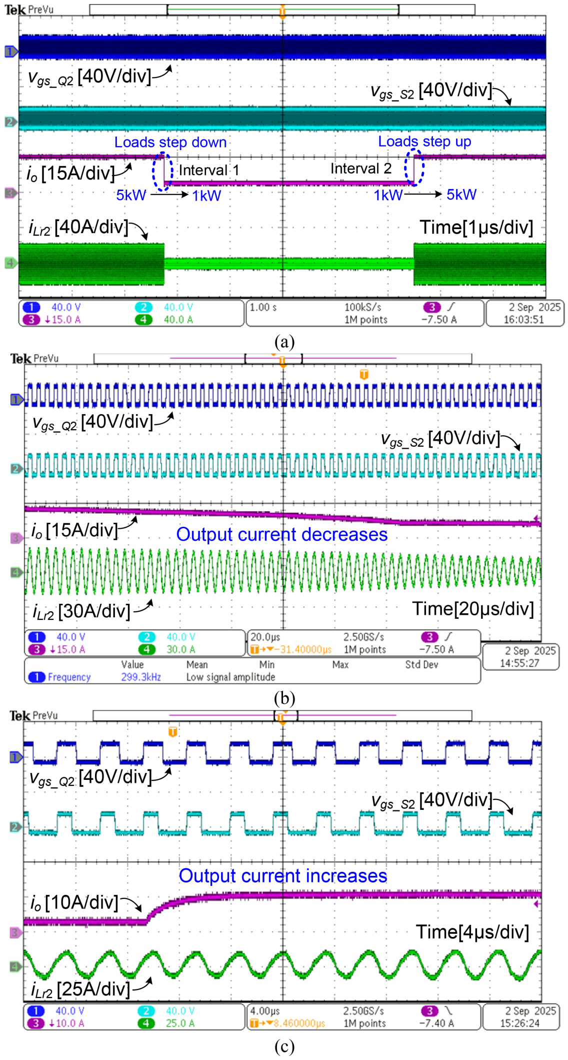


Fig. 20. *CLLC* dynamic change in forward mode: $v_{\text{bat}} = 340$ V. (a) Loads change. (b) Interval 1 is zoomed in. (c) Interval 2 is zoomed in.

VII. EXPERIMENTAL VERIFICATIONS AND ANALYSIS

A. Experimental Prototype of CLLC *Converter*

The proposed SR control is verified by a SiC-based *CLLC* charger and the prototype is shown as Fig. 18. The TP-BPFC is the front-end stage and the *CLLC* converter is the second stage, which can be seen as Fig. 13. Two interleaved inductors are used in the PFC stage to handle high power and reduce the total harmonics distortion of input ac current. In the mode transition from charging mode to discharging mode, the mode is preset before it starts to work and the transition is achieved by turning OFF the charger. The computation time of the proposed algorithm is approximate 4.6 μs. Furthermore, the controller used to implement this solution is TMS320F280049C from TI.

In the charging mode, the rated power is 6.6 kW and the discharging power is 3.3 kW. The output dc voltage is from 200 to 500 V. The SiC power devices are all from Infineon to achieve high efficiency and the *CLLC* specifications are given in Table II.

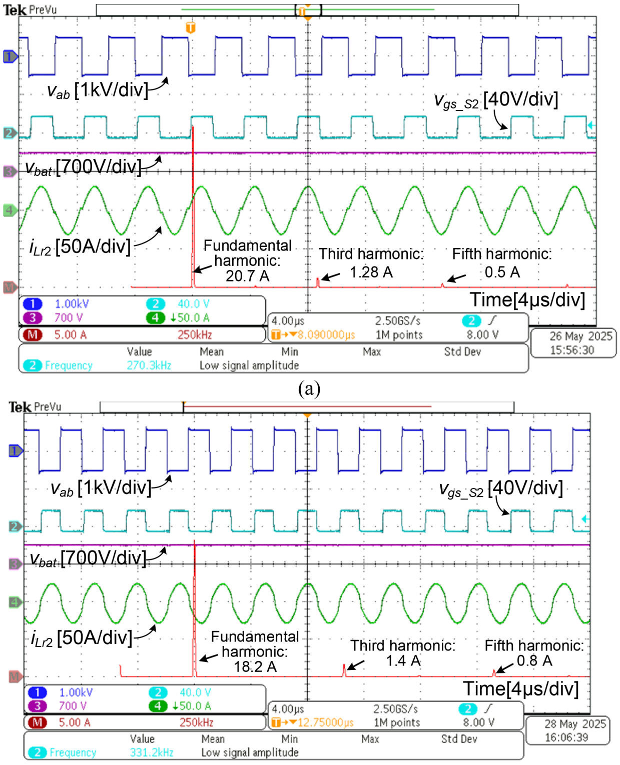


Fig. 21. FFT analysis of secondary current in forward mode: $v_{\text{bat}} = 360$ V, $P_o = 6.6$ kW. (a) $f_s = 270$ kHz. (b) $f_s = 330$ kHz.

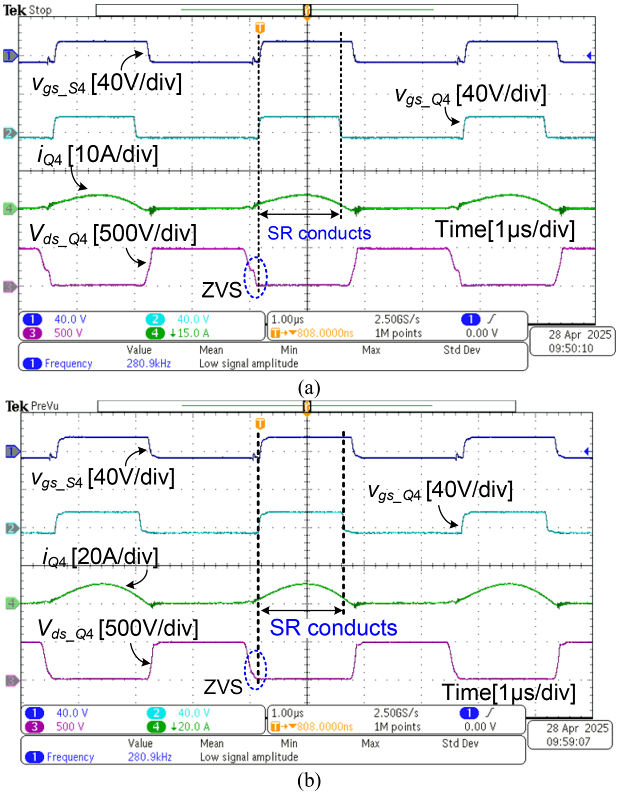
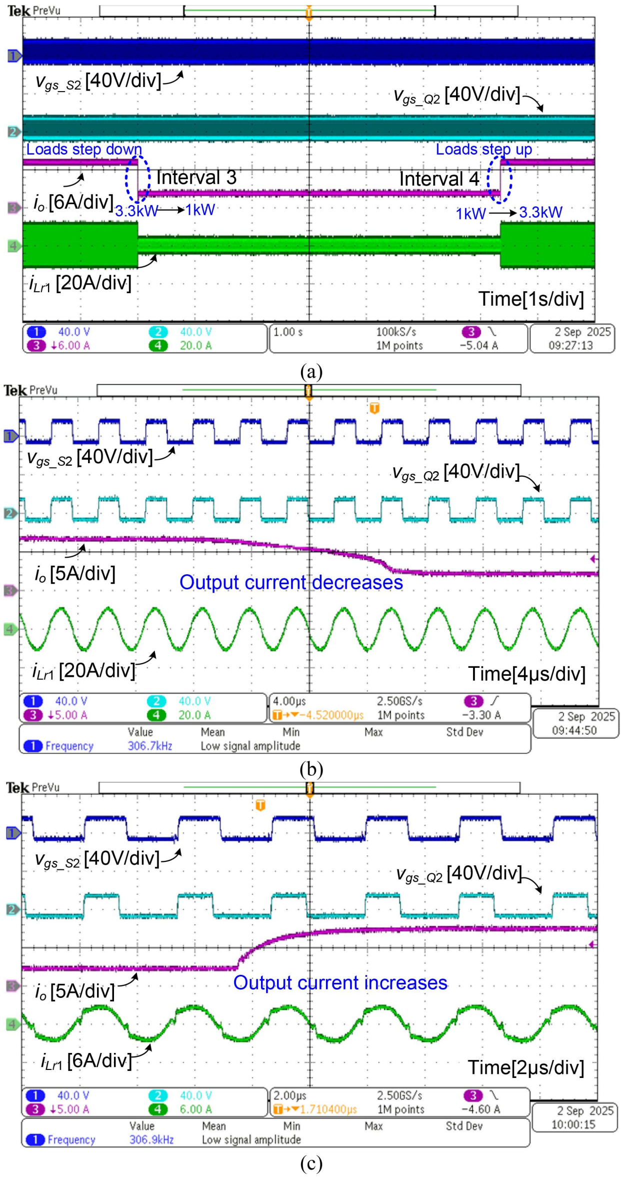


Fig. 22. Reverse SR waveforms: $v_{\text{bus}} = 500$ V, $f_s = 280$ kHz. (a) 50% of full load: $P_o = 1.65$ kW. (b) Full load: $P_o = 3.3$ kW.



(a)

(b)

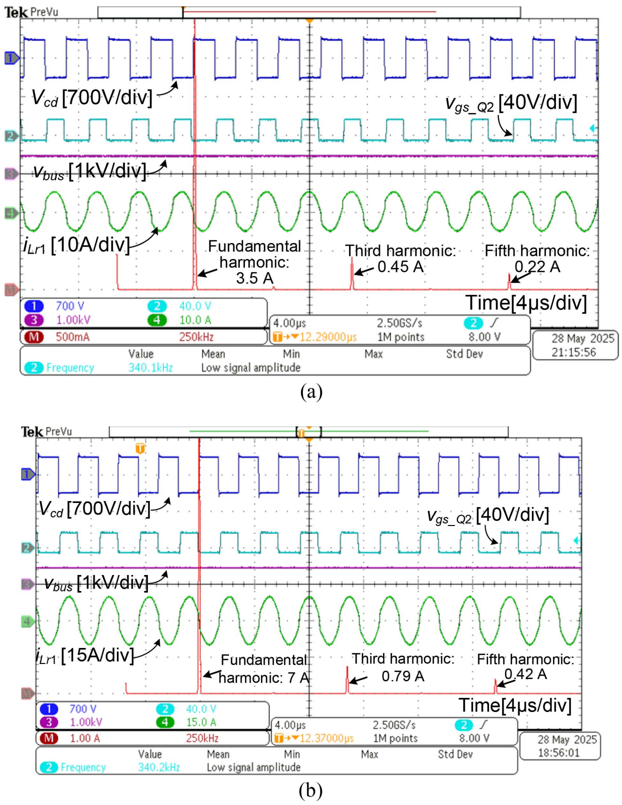
(c)

Fig. 23. Reverse *CLLC* dynamic response: $v_{bus} = 450$ V. (a) Loads change. (b) Interval 3 is zoomed in. (c) Interval 4 is zoomed in.

B. Proposed CLLC *SR Algorithm in Forward Mode*

Fig. 19 shows the *CLLC* SR waveforms in the forward mode. Observed From Fig. 19(a) and (b), as the load is from 20% of full load (1.32 kW) to the full load (6.6 kW) at 270 kHz, the SR on-time is tuned precisely to regulate S_1–S_4. The SR conduction loss can be reduced largely to achieve ZVS and high efficiency. Furthermore, when the switching frequency is 350 kHz at full load 6.6 kW based on Fig. 19(c), the proposed SR achieves good performance.

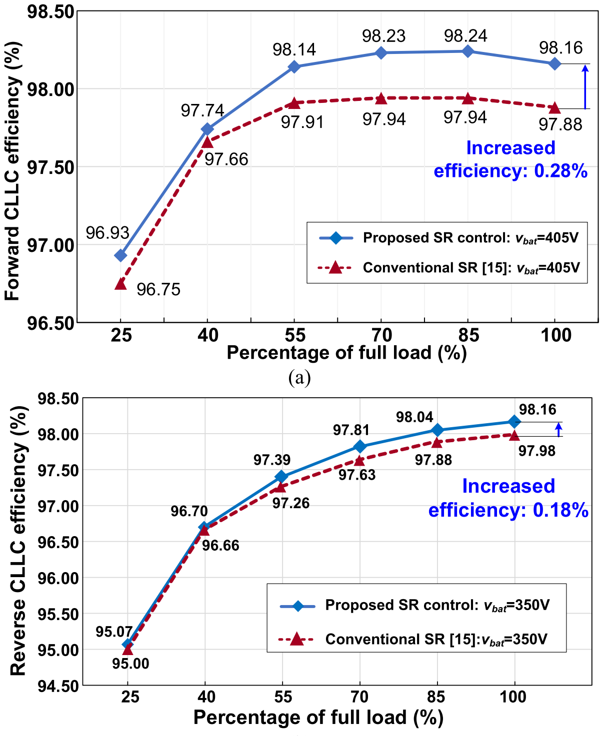
The *CLLC* dynamic change is illustrated in Fig. 20. The interval 1 and interval 2 are zoomed in as Fig. 20(b) and (c). As the loads step up from 1 to 5 kW, the *CLLC* switching frequency varies from 309 to 291 kHz and the SRs are also regulated. When the loads change, the proposed SR is robust in the dynamic behavior.



(a)

(b)

Fig. 24. FFT analysis of transformer current in reverse mode: $v_{\text{bus}} = 500$ V, $f_s = 340$ kHz. (a) 50% of full load: $P_o = 1.65$ kW. (b) Full load: $P_o = 3.3$ kW.



(a)

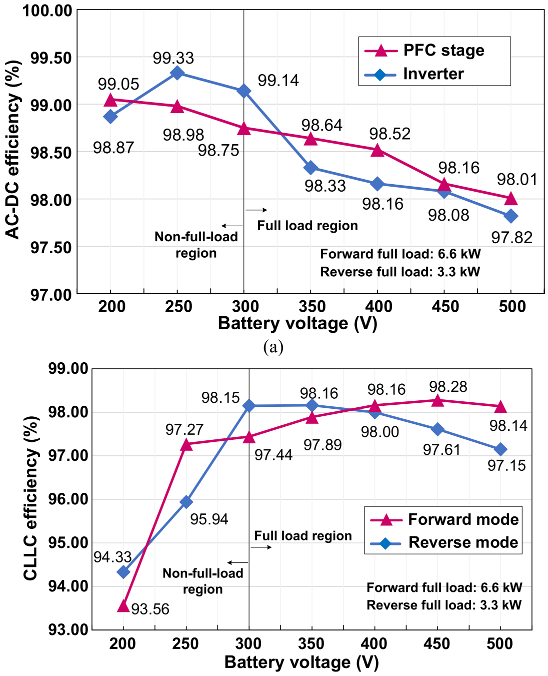
(b)

Fig. 25. *CLLC* efficiency comparisons: $f_s = 300$ kHz. (a) Forward mode: $v_{\text{bat}} = 405$ V. (b) Reverse mode: $v_{\text{bat}} = 350$ V.

TABLE III
COMPARISONS OF *CLLC* SR METHODS

Ref	Detailed	Extra components	Sensors number	Operation voltage	Resonant frequency	Peak forward efficiency	Peak reverse efficiency
[10]	Resonant tank current sensing	Current sensors	6	800 V	73 kHz	97.25%@7.5 kW	97%@6.6 kW
[11]		Rogowski coil	6	600 V	500 kHz	97.53%@6.6 kW	97.63%@6.6 kW
[13]	V_{Lr} sensing	Voltage sensing coil	5	260 V	110 kHz	96.5%@3 kW	-
[15]	Time-domain model	None	3	700 V	300 kHz	97.56%@6.6 kW	97.75%@3.1 kW
[16]	Superposition principle	None	4	480 V	100 kHz	96.92%@1.5 kW	96%@1.5 kW
[17]	Time-domain model	None	4	400 V	50 kHz	96.68%@2 kW	-
[19]	EHA method	None	4	400 V	100 kHz	97.2%@ 3.3 kW	-
[20]	Deep-learning-aided	Thermocouple	6	400 V	50 kHz	95%@2.4 kW	-
[21]	Neural-network-assisted	None	4	400 V	160 kHz	95.73%@800 W	-
Proposed	Frequency-domain model	None	3	**700 V**	**300 kHz**	**98.28%@6.6 kW**	**98.16%@3.3 kW**

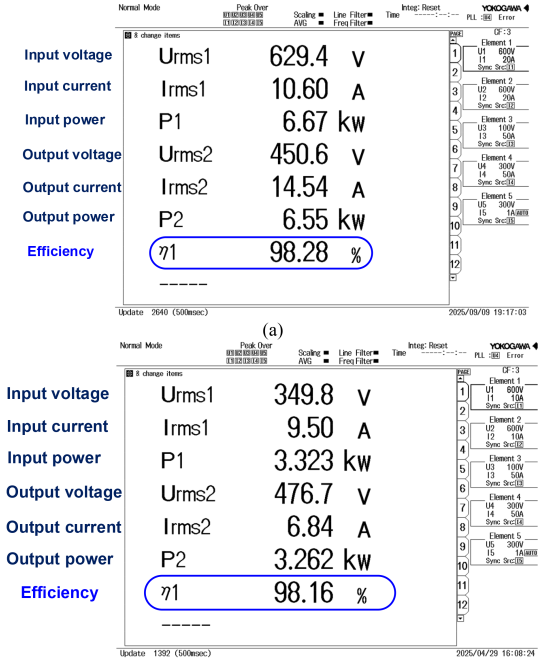
The significance of bold values is to emphasize the index of proposed method.



(a)

(b)

Fig. 26. PFC and *CLLC* efficiency. (a) PFC efficiency. (b) *CLLC* efficiency.



Input voltage Urms1 629.4 V
Input current Irms1 10.60 A
Input power P1 6.67 kW
Output voltage Urms2 450.6 V
Output current Irms2 14.54 A
Output power P2 6.55 kW
Efficiency η1 98.28 %

U1 600V I1 20A Sync Src: I1
U2 600V I2 20A Sync Src: I2
U3 100V I3 50A Sync Src: I3
U4 300V I4 50A Sync Src: I4
U5 300V I5 1A AUTO Sync Src: I5

Update 2640 (500msec) 2025/09/09 19:17:03

(a)

Input voltage Urms1 349.8 V
Input current Irms1 9.50 A
Input power P1 3.323 kW
Output voltage Urms2 476.7 V
Output current Irms2 6.84 A
Output power P2 3.262 kW
Efficiency η1 98.16 %

U1 600V I1 10A Sync Src: I1
U2 600V I2 10A Sync Src: I2
U3 100V I3 50A Sync Src: I3
U4 300V I4 50A Sync Src: I4
U5 300V I5 1A AUTO Sync Src: I5

Update 1392 (500msec) 2025/04/29 16:08:24

(b)

Fig. 27. *CLLC* power analyzer image: $f_s = 300$ kHz. (a) $v_{\text{bat}} = 450$ V, $P_o = 6.6$ kW. (b) $v_{\text{bat}} = 350$ V, $P_o = 3.3$ kW.

Fig. 21 shows the FFT analysis of secondary-side current in the transformer at 270 and 330 kHz. Based on Fig. 21, the secondary-side current mainly consists of fundamental harmonic, third harmonic, and fifth harmonic. Furthermore, compared to the values of multiple harmonics in Table I, the proposed model is accurate to analyze the secondary-side current and the SR performance can be achieved correspondingly.

C. *Proposed* CLLC *SR Algorithm in Reverse Mode*

Fig. 22 illustrates the SR waveforms in the reverse mode. When the output loads are 50% of full load (1.65 kW) and full load (3.3 kW) at 280 kHz, the SR on-time can be regulated precisely based on the proposed model. Fig. 23 shows the *CLLC* transients at 450 output voltage. The interval 3 and interval 4 are zoomed in as Fig. 23(b) and (c).

Based on Fig. 23, as the loads vary from 3.3 to 1 kW, the switching frequency is from 299 to 315 kHz to maintain the output bus voltage. In conclusion, as the loads step down or up, the proposed SR can be effective.

The FFT analysis for the secondary current in the reverse mode is illustrated as Fig. 24. Observed from Fig. 24, when the output loads are 1.65 and 3.3 kW at 500 V output, the current values of fundamental harmonic, third harmonic, and fifth harmonic are also close to the calculated values in Table I. Thus, the proposed model can be verified to achieve the SR performance.

D. *Efficiency Measurement and Comparisons*

Fig. 25 shows the comparisons of *CLLC* efficiency with the same hardware devices. Based on Fig. 25, the efficiency improvements are up to 0.28% and 0.18% in the forward and reverse modes compared to the conventional SR method, respectively. Figs. 26 and 27 illustrate the PFC and *CLLC* efficiency. Fig. 27 are the *CLLC* efficiency images from the power analyzer of YOKOGAWA WT1800. The rated power in the forward and reverse modes are 6.6 and 3.3 kW.

Based on Fig. 26, the ac–dc efficiency is up to 98.75% at 6.6 kW in the forward mode and 99.14% at 3.3 kW in the reverse mode. Moreover, from Fig. 27, the *CLLC* efficiency is 98.28% and 98.16% at full load in the forward and reverse modes, which shows the effectiveness of proposed SR.

Table III shows the comparisons of *CLLC* SR methods. Compared to the SR schemes from Infineon [10] and TI [11], the efficiency of proposed SR algorithm is higher in the forward and reverse modes. Additionally, the proposed SR does not need extra hardware components. Compared to the model-based calculation SR methods, the proposed SR also demonstrates higher efficiency in the high-frequency/ high-voltage applications.

VIII. CONCLUSION

This article proposed a digital SR algorithm based on the multiharmonic frequency-domain model for the SiC bidirectional *CLLC* converter. The proposed model considers the multiple harmonics and junction capacitance of SR MOSFETs, which are capable of deriving the secondary current phase and SR on-time precisely. As the secondary current phase is ahead of the input square wave voltage, the SR turn-OFF instants are based on the calculated SR on-time with identical turn-ON instants for the primary and secondary driving signals. When the secondary current phase lags, the SR driving signals equal the primary driving signals considering the phase delay time at the turn-ON moment.

Compared to the conventional SRs of TI and Infineon using high-frequency signals detections, the proposed SR achieves higher efficiency without extra hardware components. Additionally, the conventional SR using EHA method neglects the effects of SR junction capacitance and SR on-time variations, which inevitably causes lower accuracy and higher conduction loss than the proposed SR algorithm.

By using the proposed control, the *CLLC* efficiency is as high as 98.28% at 6.6 kW in the forward mode and 98.16% at 3.3 kW in the reverse mode. Compared to the conventional time-domain SR method, the efficiency increments are up to 0.28% and 0.18% at full load by using the proposed SR scheme in the forward and reverse modes, respectively.

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Haoran Li (Member, IEEE) received the B.Sc. degree from the Anhui University, Hefei, China, in 2013, the M.Sc. degree from the Shanghai University of Electric Power, Shanghai, China, in 2016, and the Ph.D. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2021, all in electrical engineering.

He is currently a Faculty Member with the School of Electrical Engineering and Automation, Anhui University. His research interests include high-frequency SiC/GaN applications and digital control for bidirectional dc–dc converters.

Xin Wang received the B.S. degree in biological engineering from the North University of China, Taiyuan, China, in 2023. He is currently working toward the M.Sc. degree in electrical engineering with the School of Electrical Engineering and Automation, Anhui University, Hefei, China.

His research interests include high-frequency SiC applications and digital control techniques for the bidirectional dc–dc resonant converters.

Cungang Hu (Senior Member, IEEE) received the B.S. degree in electrical engineering and automation from the Electronic Engineering Institute, China, in 2001, the M.S. degree in detection technique and automatic device form the Hefei University of Technology (HFUT), Hefei, China, in 2004, and the Ph.D. degree in power electronics and electric drives from the HFUT, in 2008.

From 2004 to 2013, he was with the HFUT. Since 2013, he has been a Professor with the Anhui University, Hefei, China. His research interests include multilevel converter technology and power quality.

Dr. Hu is the Technical Program Committee Chairman of the 11th and 14th IEEE Conference on Industrial Electronics and Applications, the General Chairman 12th IEEE Conference on Industrial Electronics and Applications.

Xirui Zhu received the B.S. degree in electronic information engineering from the Nanjing University of Information Science and Technology, Nanjing, China, in 2013, the M.S. degree in electronic information engineering from the City University of Hong Kong, Hong Kong, in 2015, and the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2021.

He is currently a Research Engineer with the Shanghai Institute of Aerospace Systems Engineering, Shanghai, China. His research interests include avionics and wireless power transmission.

Xi Tang (Member, IEEE) received the B.S. degree in physics from the Nanjing University, Nanjing, China, in 2011, the M.S. degree in electronic and computer engineering from the Cornell University, Ithaca, NY, USA, in 2012, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hongkong, in 2017.

He is currently a Professor with the Institute of Physical Science and Information Technology, Anhui University, Hefei, China. His research interests include design of GaN and SiC electronic devices, optoelectronic devices and circuits.

Zhiliang Zhang (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2002 and 2005, respectively, and the Ph.D. degree in electrical engineering from the Queen's University, Kingston, ON, Canada, in 2009.

He is currently a Professor with the Aero-Power Sci-Tech Center, NUAA. His research interests include high-frequency power conversion with wide bandgap devices.

Dr. Zhang has been serving as an Associate Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS OF POWER ELECTRONICS, since 2018.

Wenping Cao (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from the Beijing Jiaotong University, Beijing, China, in 1991, and the Ph.D. degree in electrical machines and drives from the University of Nottingham, Nottingham, U.K., in 2004.

He is currently a Distinguished Professor with the Anhui University, Hefei, China. He has served as an Associated Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, IEEE INDUSTRY APPLICATIONS MAGAZINE, and *IET Power Electronics*. His research interests include fault analysis and condition monitoring of electrical machines, and power electronics.