Four-Level TCM-Operated Inverter With Full Soft-Switching Capability Using a Hybrid Si+SiC Configuration

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***Abstract*—Triangular current mode (TCM) modulation is a promising technique for achieving zero-voltage switching (ZVS) in dc–ac power inverters, which already inherently offers a high output voltage quality without a sine-wave filter. Despite slightly higher conduction losses than hard-switched inverters using conventional pulsewidth modulation (PWM), TCM-operated inverters achieve outstanding efficiency by significantly reducing switching losses, especially under low-load conditions. However, TCM faces the challenge of a wide variation in switching frequency throughout the fundamental cycle, which is often managed by suspending TCM operation near zero-crossings to prevent exceeding frequency limits. This article introduces a novel multilevel TCM inverter topology featuring two cascaded stages and an asymmetrically subdivided dc-link. For optimized cost and performance, the two stages employ a hybrid configuration using silicon carbide (SiC) MOSFETs in the high-frequency stage and Si IGBTs in the low-frequency stage. This design reduces the voltage stress on all power semiconductors and ensures full soft-switching capability even near voltage zero-crossings without excessive switching frequency fluctuations. The effectiveness of the presented topology is maximized when paired with a control algorithm that ensures continuous soft-switching across all devices and manages the necessary voltage control for the subdivided dc-link. A single-phase 2 kW hardware demonstrator with a 1.5 kV dc-link was designed and implemented to validate this concept, incorporating the proposed control algorithm. The demonstrator achieves a peak efficiency of more than 98.6% at nominal load, demonstrating the effectiveness of the full soft-switching capability provided by the new topology.**

***Index Terms*—Charge balancing, four-level asymmetric dc-link, multilevel inverter, novel topology, silicon carbide (SiC), soft-switching, triangular current mode (TCM), voltage control, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

POWER electronic voltage-source inverters (VSIs) have undergone continuous improvements over the past decades to meet the ever-increasing demands across various applications. High efficiency, a compact and lightweight design, low electromagnetic interference (EMI), high reliability, high durability, high robustness, and low costs are among the most important objectives of every converter design [1], [2]. With the current design trend of increasing switching frequencies enabled by wide band-gap (WBG) devices, high power density and low costs can be achieved by downsizing or even eliminating passive components [3], [4]. However, higher switching frequencies also yield higher switching losses in power semiconductor devices. This increases the cooling effort, limiting both the achievable efficiency of the inverter and the power density [4]. To overcome these boundaries, solutions are required to achieve low losses despite high switching frequencies. One way to accomplish this is through the principle of soft-switching operation, which employs either zero-voltage switching (ZVS) or zero-current switching (ZCS) in the power semiconductors. Soft-switching is a key technique for reducing switching losses, enabling high switching frequencies of up to hundreds of kilohertz, while also allowing for softer voltage transients that decrease EMI [2], [5], [6], [7].

The ability to achieve soft-switching in power electronic inverters can be realized through hardware-based or software-based techniques. Hardware-based approaches involve the addition of auxiliary circuits and can be classified into load-resonant systems, systems with resonant dc-link, and resonant transition systems [2], [7]. In contrast, software-based techniques employ peak current mode control, characterized by a low filter inductor value and a large inductor current ripple. By reversing the direction of inductor current flow in each switching cycle, these techniques enable ZVS turn-ON during each current commutation [8], [9], [10]. Compared to hardware-based solutions, the implementation of soft-switching using a peak current control technique achieves excellent reliability, lower control complexity, and lower costs, as no additional auxiliary components are required [2], [11]. Due to the characteristic shape of the inductor current, this modulation method is widely known as *triangular current mode* (TCM) and is sometimes also referred to as *boundary conduction mode* or *critical conduction mode*. Although TCM modulation results in an increase in rms current, leading to higher conduction losses ($\approx$ 30% higher according to [12]) compared to hard-switched inverters using conventional PWM schemes, this drawback can be more than compensated by the significant reduction in switching losses [8].

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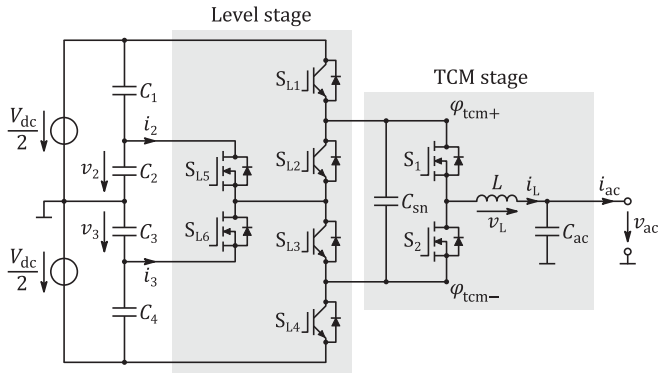


Fig. 1. Circuit diagram of the proposed soft-switching multilevel TCM inverter in a single-phase configuration, comprising a level stage and a TCM stage supplied by an asymmetrically subdivided 4-level DC-link.

Consequently, TCM modulation is a promising candidate, especially for low-power applications that employ very high switching frequencies to maximize power density. Extensive research has already been conducted on its use in rectifiers [12], [13], [14], [15], [16], but also in inverters [8], [9], [17], [18] or bidirectional converters [19], [20].

Inherent to the TCM operating principle is a wide, load-dependent variation of the switching frequency. Specifically, a 2-level topology supplying a resistive load exhibits very high switching frequencies at the output voltage zero-crossings. To limit the switching frequency variation, the current envelope can be partially widened [11], [13], [18], [21], or alternatively, TCM operation can be suspended near zero-crossings by changing to ZCS with discontinuous conduction mode (DCM) [19], [20], [22]. Another approach is to employ multilevel topologies, in which TCM modulation can also be applied. Previous research has explored its use in ANPC [23] and T-type NPC [10], [24], [25], [26] structure. In particular, [26] demonstrated that a 3-level topology reduces the variation in switching frequency and thus decreases the required filter volume. However, the 3-level ANPC and T-Type inverter still face the problem that TCM operation is not feasible near the voltage zero-crossings due to the lack of sufficient voltage across the inductor to build up the triangular inductor current, resulting in unacceptably low switching frequencies. In addition, the high-side and low-side transistors must block the full dc-link voltage V_{dc} in the T-Type, which imposes constraints on component selection and limits the attainable dc-link voltage. To combat these limitations and maintain soft-switching in the area of voltage zero-crossings without excessive switching frequencies, this article presents a 4-level topology with an asymmetric dc-link. The suggested TCM-operated inverter in single-phase configuration is shown in Fig. 1.

The inverter is technically extended based on the Active-Neutral-Point-Clamped (ANPC) topology. It comprises an asymmetric subdivided 4-level dc-link (with $v_2 \approx v_3 \ll V_{dc}/2$), a level stage, and a TCM stage. The dc-link provides two overlapping voltage ranges that feed the TCM stage via the level stage. The principle of overlapping voltage ranges that feed a downstream inverter stage was first introduced in [27] and has now been applied to this topology. Due to this characteristic, a minimum voltage is supplied to the inductor even near voltage zero-crossings. This allows an alternating inductor current of sufficient magnitude to build up within a specific time frame, thereby maintaining a minimum permissible switching frequency. Consequently, the overlapping voltage ranges enable unrestricted TCM operation with full soft-switching capability throughout the entire fundamental cycle.

Another key benefit of the proposed topology is its ability to employ a hybrid configuration of Si and SiC devices, which reduces costs while improving performance. In this configuration, SiC MOSFETs operate at high switching frequencies to generate the sinusoidal output, while the Si IGBTs act as voltage level selectors by switching at the fundamental frequency. This concept is well known in hard-switched ANPC topologies [28], [29], [30], [31], [32] and can be applied here as well. As suggested in [28], [32], [33], [34], the TCM stage is decoupled from the level stage using a snubber capacitor C_{sn} to shorten the commutation loops and mitigate the forward recovery effects caused by the hybrid configuration. In addition, by implementing precise timing and actively charging/discharging C_{sn} during the transition between two states, the level-stage transistors can also be soft-switched using ZVS and ZCS. Moreover, the switches S_1, S_2, and S_{L1} to S_{L4} only need to block slightly more than half of the dc-link voltage, which reduces the voltage stress on all components and allows the use of lower-voltage devices even at higher dc-link voltages.

To prevent a potential drift at the inner dc-link levels, it is crucial to balance the dc-link capacitors during each fundamental cycle. Voltage balancing is realized by two low-voltage 250 V Si MOSFETs. Based on the voltage deviation, these MOSFETs are controlled to direct the current through either C_2 or C_3, thereby maintaining the voltage balance of the dc-link capacitors.

The concepts presented have been implemented, and their functioning has been experimentally verified using a 2 kW inverter prototype with a 1.5 kV dc-link. The main advantages of the novel topology are as follows.

1) Continuous soft-switching under TCM operation without excessive switching frequency fluctuations.
2) Soft-switching across all semiconductor devices, including those in the level stage.
3) Cost and performance optimization using a Si+SiC hybrid configuration.
4) Lower voltage stress on all semiconductor devices.

The rest of this article is organized as follows. After introducing and classifying the proposed inverter topology within the current state-of-the-art in Section I, Section II describes the operation principle of the topology applying TCM modulation. Building on this, Section III analyzes the switching frequency in the TCM stage and introduces a dc-link voltage control scheme. Section IV then deals with the realization of soft-switching in the level stage. Section V addresses the experimental realization of the proposed circuit and provides detailed insights into its implementation. The experimental results are then presented and discussed in Section VI. Finally, Section VIII concludes this article.

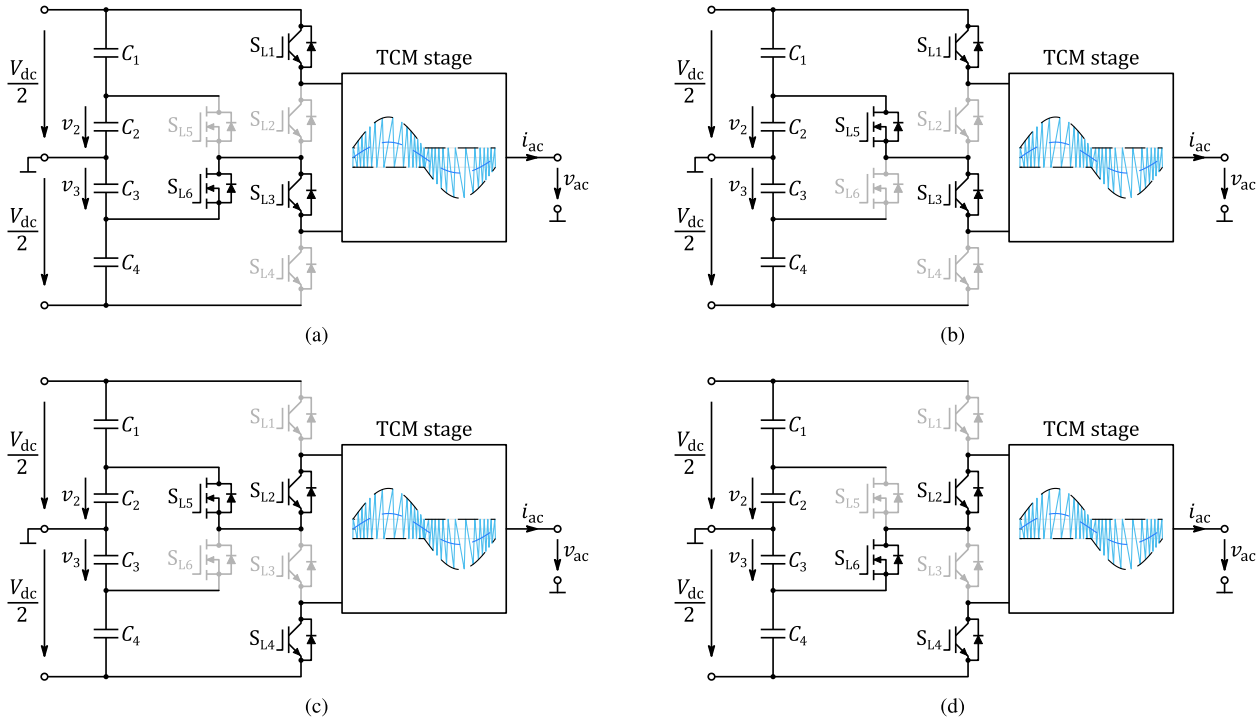


Fig. 2. Four valid switching states of the level stage: (a) and (b) correspond to switching states Ⓐ and Ⓑ used during the positive half-wave of the output voltage v_{ac}. (c) and (d) correspond to switching states Ⓒ and Ⓓ used during the negative half-wave of v_{ac}.

II. Operation Principle of the Topology

The dc-link capacitors subdivide the dc-link of the topology into four asymmetrical parts, which provide the overlapping voltage ranges $[-v_3,\ V_{dc}/2]$ and $[-V_{dc}/2,\ v_2]$. The overlap section $[-v_3,\ v_2]$ ensures the necessary voltage across the inductor L of the TCM stage to build up an alternating inductor current, thereby achieving full ZVS even in the area of zero-crossings of the output voltage. The inner dc-link voltages v_2 and v_3 must always satisfy the following criteria:

$$v_2 \geq V_{res} \wedge v_3 \geq V_{res} \tag{1}$$

where V_{res} is the reserve voltage, indicating the required minimum voltage across the inductor. Any number of phases can be connected to the dc-link. However, this article intends to explain and validate the operation principle based on the topology in a single-phase inverter structure. The findings and the principle discussed can easily be transferred to a three-phase setup.

A. Level Stage

The level stage consists of six switches S_{L1} to S_{L6} and works as a level selector. This stage has four valid switching states, as depicted in Fig. 2(a)–(d).

Three switches are always conducting at the same time, with the simultaneous turn-ON of S_{L1} and S_{L4} prohibited due to the voltage stress within the TCM stage. The switching states Ⓐ and Ⓒ correspond to normal operation, whereby the TCM stage is supplied with the two overlapping voltage ranges [see Fig. 3(a)]. However, to control the dc-link voltages with the output current i_{ac} during operation, the switching states Ⓑ and Ⓓ must be additionally used. As indicated in Fig. 3(a), $S_{L1\sim L4}$ must alternate only once per fundamental cycle to synthesize the positive [Ⓐ and Ⓑ] and negative [Ⓒ and Ⓐ] voltage half-waves. The voltage criterion defined in Table I specifies when each switching state can be applied during the fundamental cycle.

TABLE I
Voltage Criterion for DC-Link Voltage Control Through Capacitor Charge Balancing

Switching state	Voltage criterion	Operation
Ⓐ	$-v_3 + V_{res} \leq v_{ac} < V_{dc}/2$	Normal
Ⓑ	$v_2 + V_{res} \leq v_{ac} < V_{dc}/2$	Balancing
Ⓒ	$-V_{dc}/2 < v_{ac} \leq v_2 - V_{res}$	Normal
Ⓓ	$-V_{dc}/2 < v_{ac} \leq -v_3 - V_{res}$	Balancing

Since $S_{L1\sim L4}$ switch at the fundamental frequency, resulting in very low switching losses, low-cost IGBTs with a blocking voltage slightly higher than $[V_{dc}/2 + v_{2,3}]$ can be used. The change from normal to balancing operation occurs twice within a fundamental cycle, resulting in a switching frequency of $2f_{ac}$ for S_{L5} and S_{L6}. These transistors only need to block a voltage of $[v_2 + v_3]$, making cost-effective low-voltage Si MOSFETs with a low $R_{ds,on}$ preferable for this purpose.

B. TCM Stage

The fundamental principles, timing, and analytical description of TCM operation have already been thoroughly covered in the past literature, for example [11], [35]. For this reason, only

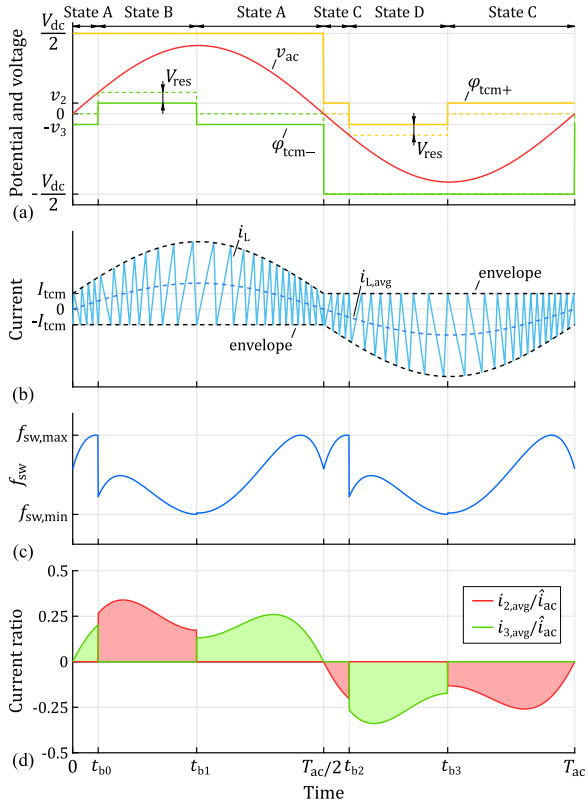


Fig. 3. Calculated key waveforms of the topology over a fundamental cycle T_{ac}. (a) Inverter output voltage v_{ac} and node potentials φ_{tcm+} and φ_{tcm-} of the TCM stage. (b) Characteristic triangular inductor current i_L and its specified current envelope with a FRC I_{tcm} synthesizes the sinusoidal short-term average value $i_{L,avg}$. Note that the resonant transition is short compared to the linear current rises/falls and is therefore neglected. (c) Switching frequency f_{sw} of the TCM switches S_1 and S_2. (d) Relative short-term average currents through the inner DC-link capacitors C_2 and C_3.

the fundamental and most important relationships are recalled to enable a cohesive article.

The TCM stage comprises a conventional 2-level half-bridge topology, incorporating an inductor L, an output capacitor C_{ac}, and a snubber capacitor C_{sn}. SiC MOSFETs with a blocking voltage of at least $[V_{dc}/2 + v_{2,3}]$ are employed for the half-bridge switches S_1 and S_2, operated with TCM modulation as detailed in [36], [37]. The output capacitances C_{oss} of the switches and the inductor L form a resonant circuit, in which the inductor current i_L is controlled to reverse the direction once during each switching cycle. The alternating current flow charges/discharges the MOSFET's C_{oss} and passes through the body diode before each switching transition, thus enabling the ZVS turn-ON for S_1 and S_2. The reverse inductor current I_{tcm} is an additional design parameter and must be selected adequately to drive the drain-source voltage of the transistor to 0 V, ensuring complete ZVS [10], [20].

The implementation of TCM control requires setting the upper and lower boundaries of the inductor current i_L, referred to as the envelope of a nonlinear current hysteresis. The short-term average value of this triangular current synthesizes the desired sinusoidal output current $i_{ac} \approx i_{L,avg}$. The durations of the inductor current build-up and build-down phases are defined by the current envelope and the inductor voltage v_L. The inductor voltage is calculated by subtracting v_{ac} from the node potentials φ_{tcm+} and φ_{tcm-}. This results in a wide switching frequency variation for S_1 and S_2 over the fundamental cycle. The f_{sw}-variation leads to a broad spectral distribution of the total switching noise energy, which is beneficial for meeting EMI regulatory standards [10], [21]. However, it is essential to ensure that the switching frequency range does not exceed certain application-specific or regulatory boundaries. Efforts to limit the frequency variation while maintaining ZVS have led to the development of various current control techniques [13], [20]. Three fundamental schemes have emerged from the basic operation principle. They are each defined by their current envelope curves and classified into fixed reverse current (FRC), constant hysteresis current mode (CHCM), and variable hysteresis current mode (VHCM). Among these, FRC modulation achieves the highest efficiency, but also the highest distortion, while CHCM offers the lowest distortion accompanied by the lowest efficiency [8], [9]. Given the high achievable efficiencies and simpler current control, standard TCM modulation with FRC was selected for this study. Fig. 3(b) illustrates the characteristic TCM current waveforms along with their envelope over a fundamental cycle.

Using the overlapping voltage ranges $[-v_3, V_{dc}/2]$ and $[-V_{dc}/2, v_2]$ maintains TCM operation near the voltage zero-crossings during transitions between states Ⓐ and Ⓒ. The same overlap also limits the switching frequency by appropriately choosing V_{res}. The corresponding switching frequency f_{sw} profile of the TCM stage is shown in Fig. 3(c). Its upper and lower limits are determined by the operating point and the selected design parameters, see also Section III-A.

C. Avoidance of Forward Recovery in Si+SiC Configurations

Previous literature [34], [38], [39] has investigated hybrid topologies that combine fast-switching SiC MOSFETs with slow-switching Si IGBTs, identifying the forward recovery effect of bipolar switching devices as a major challenge. The carrier density of the IGBT's drift region is insufficient to sustain the current with a high $\mathrm{d}i/\mathrm{d}t$ caused by the rapid switching of the SiC devices, resulting in a temporary lower effective conductivity of the already turned-ON Si IGBTs. The elevated resistance leads to a temporary additional voltage drop across the IGBTs, causing significant induced losses and simultaneously increasing the voltage stress on SiC MOSFETs [34], [38], [39]. To mitigate the adverse effects of high $\mathrm{d}i/\mathrm{d}t$ on IGBTs, a snubber capacitor, as described in [28], [32], [33], [34], can be used to decouple the TCM stage from the level stage. For this purpose, a snubber capacitor C_{sn} with a small capacity is placed on the dc-side of the TCM stage, as shown in Fig. 1. This simple measure minimizes the adverse effects of forward recovery while reducing the commutation loop inductance of the switching cells. With C_{sn} in place, its voltage must be adjusted during state transitions to also achieve soft-switching in the level stage. More details are provided in Section IV.

III. Mathematical Analysis

For the following analysis of inverter operation and dc-link voltage control, several common assumptions and simplifications are made as follows.

1) The passive components are assumed to be ideal, and all power semiconductors are regarded as ideal switches (output capacitance, voltage drop, and switching times are neglected).
2) The commutation duration is assumed to be negligibly short, resulting in an ideal triangular inductor current.
3) The ripple of the dc-link voltage over a fundamental cycle is considered negligible due to a sufficiently large dc-link capacitance.
4) The inner and outer dc-link capacitances are equal ($C_1 = C_4$ and $C_2 = C_3$) and perfectly balanced.
5) The inverter's output voltage v_{ac} and current i_{ac} are considered to be a perfect sine wave.
6) The entire inverter system operates in a steady state.

The output voltage v_{ac} and output current i_{ac} of the inverter can generally be described as follows:

$$v_{\mathrm{ac}}(t) = \underbrace{M\frac{V_{\mathrm{dc}}}{2}}_{\widehat{v}_{\mathrm{ac}}} \sin(\omega t), \text{with } M \in [0,1) \tag{2}$$

$$i_{\mathrm{L,avg}} \approx i_{\mathrm{ac}}(t) = \widehat{i}_{\mathrm{ac}} \sin(\omega t - \varphi) \tag{3}$$

with M as the modulation index, ω as the fundamental angular frequency, $\widehat{i}_{\mathrm{ac}}$ as the current amplitude, and φ as the phase shift angle of the load. In the case of a balanced dc-link, the voltages v_2 and v_3 are equal and can both be replaced by v_{n}. Along with this, we simplify the analysis by assuming that the reserve voltage also equals v_{n} following:

$$v_2 = v_3 = v_{\mathrm{n}} = n\frac{V_{\mathrm{dc}}}{2} = V_{\mathrm{res}} \tag{4}$$

with n as the voltage ratio between the inner and outer dc-link capacitors.

A. Switching Frequency in the TCM Stage

A defining property of the proposed topology is its markedly reduced variation in switching frequency over the fundamental cycle. Based on the assumptions outlined above, the resulting switching frequency can be expressed as

$$f_{\mathrm{sw}}(\omega t) = \frac{V_{\mathrm{dc}}\left[1 - M\left|\sin(\omega t)\right|\right]\left[M\left|\sin(\omega t)\right| \pm n\right]}{4L(1 \pm n)\left[\hat{i}_{\mathrm{ac}}\left|\sin(\omega t - \varphi)\right| + I_{\mathrm{tcm}}\right]} \tag{5}$$

where the "+" sign applies during normal operation [states Ⓐ and Ⓒ] and the "−" sign during balancing operation [states Ⓑ and Ⓓ]. The switching frequency heavily depends on the electrical angle ωt. The maximum is

$$f_{\mathrm{sw,max}} = \frac{V_{\mathrm{dc}}(1+n)}{16LI_{\mathrm{tcm}}} \tag{6}$$

and occurs at

$$|v_{\mathrm{ac}}| = \frac{V_{\mathrm{dc}}}{4}(1-n) \text{ with } i_{\mathrm{ac}} = 0. \tag{7}$$

With $n = 1$ for a 2-level TCM inverter, $f_{\mathrm{sw,max}}$ is roughly twice as high as in the proposed topology and occurs at the output voltage zero-crossings for purely resistive loads ($\varphi = 0°$).

TABLE II
CURRENTS THROUGH THE INNER DC-LINK CAPACITORS C_2 AND C_3 AVERAGED OVER A SWITCHING CYCLE

State	Short-term average dc-link capacitor current	
Ⓐ	$i_{2,\mathrm{avg}} = 0$	$i_{3,\mathrm{avg}} = i_{\mathrm{L,avg}}\frac{V_{\mathrm{dc}}/2 - v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_3}$
Ⓑ	$i_{2,\mathrm{avg}} = i_{\mathrm{L,avg}}\frac{V_{\mathrm{dc}}/2 - v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 - v_2}$	$i_{3,\mathrm{avg}} = 0$
Ⓒ	$i_{2,\mathrm{avg}} = i_{\mathrm{L,avg}}\frac{V_{\mathrm{dc}}/2 + v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_2}$	$i_{3,\mathrm{avg}} = 0$
Ⓓ	$i_{2,\mathrm{avg}} = 0$	$i_{3,\mathrm{avg}} = i_{\mathrm{L,avg}}\frac{V_{\mathrm{dc}}/2 + v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 - v_3}$

By contrast, the switching frequency at the voltage zero-crossings in the proposed topology is

$$f_{\mathrm{sw,0}}(\omega t = 0) = \frac{nV_{\mathrm{dc}}}{4L(1+n)\left(\hat{i}_{\mathrm{ac}}\sin|\varphi| + I_{\mathrm{tcm}}\right)} \tag{8}$$

and it reaches its minimum for purely reactive loads ($\varphi = \pm 90°$).

B. DC-Link Voltage Control

A suitable dc-link voltage control is crucial for the stable and efficient operation of inverters with a split dc-link configuration. To control the voltages of the individual dc-link capacitors during operation, their charges are balanced by additionally utilizing the states Ⓑ and Ⓓ [see Fig. 3]. Achieving this balance requires meeting several essential criteria. These criteria depend on the modulation index, the phase shift angle of the load, and the voltage ratio between the outer and inner dc-link capacitors. The balancing method was first described in [40] and is implemented in a simplified version in this work.

In practical operation, the switching frequency of the TCM stage is chosen to be much higher than the fundamental frequency ($f_{\mathrm{sw}} \gg f_{\mathrm{ac}} = 1/T_{\mathrm{ac}}$). Consequently, the inductor current i_{L} and the capacitor currents i_2 and i_3 can be considered constant during a switching cycle and are referred to as $i_{\mathrm{L,avg}}$, $i_{2,\mathrm{avg}}$ and $i_{3,\mathrm{avg}}$. $i_{\mathrm{L,avg}}$ can thus be equated with the output current i_{ac}. The short-time average currents $i_{2,\mathrm{avg}}$ and $i_{3,\mathrm{avg}}$ can be calculated based on the duty cycles applied to the TCM switches S_1 and S_2. Table II summarizes the results for the four switching states.

Fig. 3(d) illustrates the simulated short-term average dc-link currents over one fundamental cycle. In a fully balanced operation, the areas of the same color in the figure add up to zero.

1) Required Criteria for Voltage Balancing: In addition to compliance with the voltage criterion outlined in Table I, the current criterion must also be fulfilled to apply the balancing states during operation. The mean values of the capacitor currents over a fundamental cycle I_2 and I_3 will be first considered without active voltage balancing. These currents can be obtained through integration and with the help of (2) and (3) as follows:

$$I_2 = \frac{1}{T_{\mathrm{ac}}}\int_{T_{\mathrm{ac}}/2}^{T_{\mathrm{ac}}} i_{2,\mathrm{avg}}(t)\mathrm{d}t = \frac{\widehat{i}_{\mathrm{L,avg}}\cos(\varphi)(\pi M - 4)}{4\pi\left(2\frac{v_2}{V_{\mathrm{dc}}} + 1\right)} \tag{9}$$

$$I_3 = \frac{1}{T_{\mathrm{ac}}}\int_{0}^{T_{\mathrm{ac}}/2} i_{3,\mathrm{avg}}(t)\mathrm{d}t = \frac{\widehat{i}_{\mathrm{L,avg}}\cos(\varphi)(4 - \pi M)}{4\pi\left(2\frac{v_3}{V_{\mathrm{dc}}} + 1\right)}. \tag{10}$$

TABLE III
CURRENT CRITERION FOR DC-LINK VOLTAGE CONTROL THROUGH CAPACITOR CHARGE BALANCING

	Current without balancing	Current criterion for balancing	State to be used
$\cos(\varphi) > 0$	$I_2 < 0$	$i_{\mathrm{L,avg}} > 0$	Ⓑ
	$I_3 > 0$	$i_{\mathrm{L,avg}} < 0$	Ⓓ
$\cos(\varphi) < 0$	$I_2 > 0$	$i_{\mathrm{L,avg}} < 0$	Ⓑ
	$I_3 < 0$	$i_{\mathrm{L,avg}} > 0$	Ⓓ

Equations (9) and (10) demonstrate that the sum of the two currents averaged over T_{ac} can theoretically only be zero without balancing during pure reactive ($\varphi = \pm 90°$) power operation. Under all other load conditions, nonzero currents I_2 and I_3 cause the inner levels of the dc-link to drift, requiring appropriate dc-link voltage control. By accurately setting the time durations $[t_{\mathrm{b0}}, t_{\mathrm{b1}}]$ and $[t_{\mathrm{b2}}, t_{\mathrm{b3}}]$ of the switching states Ⓑ and Ⓓ [compare Fig. 3], the capacitor currents I_2 and I_3 can be compensated to zero, according to (11) and (12) shown at the bottom of this page. Table III provides an overview of the current criterion required for voltage balancing across different load scenarios. Fig. 4 displays the essential waveforms for different load situations.

Here, T_{b} denotes the time required to balance the dc-link capacitor voltages using the states Ⓑ and Ⓓ, with $T_{\mathrm{b,max}}$ indicating the maximum available balancing time. Assuming a uniform voltage distribution at the dc-link, the duration of state Ⓑ equals the duration of state Ⓓ, and half symmetry of the waveforms is achieved as described by the following:

$$t_{\mathrm{b2}} = t_{\mathrm{b0}} + T_{\mathrm{ac}}/2 \text{ and } t_{\mathrm{b1}} - t_{\mathrm{b0}} = t_{\mathrm{b3}} - t_{\mathrm{b2}} = T_{\mathrm{b}}. \tag{13}$$

Along with (4), the capacitor currents are now denoted by I_{n}

$$I_{\mathrm{n}} = -I_2 = I_3. \tag{14}$$

The start of the balancing operation for load scenarios, as shown in Fig. 4(a) and (c), is constrained by the voltage criterion. The starting angle, at which the voltage criterion is satisfied, is denoted by α_0 and can be calculated as follows:

$$\alpha_0 = \arcsin\left(\frac{2V_{\mathrm{res}}}{\widehat{v}_{\mathrm{ac}}}\right) = \arcsin\left(\frac{2n}{M}\right) \text{ with } t_{\mathrm{b0}} = \frac{\alpha_0}{\omega}. \tag{15}$$

However, for phase shift angles $\varphi \in [\alpha_0, \pi/2]$ and $\varphi \in [-\pi + \alpha_0, -\pi/2]$, as shown in Fig. 4(b), the beginning of the balancing operation is constrained by the current criterion. Therefore, balancing is only feasible from $t \geq t_{\mathrm{b0}} = \varphi/\omega$ and $t \geq t_{\mathrm{b2}} = (\varphi + \pi)/\omega$, respectively.

2) Feasibility Limits for Voltage Balancing: Various calculations were conducted based on previous simplifications and equations to determine the feasibility limits of voltage balancing and, consequently, the applicability of the proposed topology. The results of this analysis are presented in Fig. 5.

Voltage balancing is independent of the output current but relies significantly on the output voltage. A minimum modulation index M_{min} can be derived from the voltage criterion, below which the available balancing time $T_{\mathrm{b,max}}$ is insufficient for complete charge equalization. Fig. 5(a) shows the average dc-link current and the utilization of the available balancing time over the modulation index and phase shift angle. Balancing is theoretically only possible above $M = 2n$ with $T_{\mathrm{b,max}} > 0$. Stable operation with full balance ($I_{\mathrm{n}} = 0$) can only be accomplished above M_{min} with $T_{\mathrm{b}} \leq T_{\mathrm{b,max}}$. Without or with incomplete balancing ($I_{\mathrm{n}} \neq 0$), the positive and negative areas in Fig. 3(d) would not cancel each other out, causing the dc-link potentials to drift in one direction. Consequently, the implementation precludes operation below M_{min}.

Fig. 5(b) shows the required balancing time versus the total available balancing time as functions of the modulation index and phase shift angle. As the modulation index increases, the angle α_0 required to meet the voltage criterion decreases, resulting in a greater available margin of the balancing time. The calculations also indicate that balancing is theoretically unnecessary for purely reactive loads.

As seen from Fig. 5(c), the chosen voltage ratio determines the minimum possible modulation index. For the implemented design ($n = 50\,\mathrm{V}\,/\,750\,\mathrm{V} \approx 0.067$), the theoretical minimum modulation index is $M_{\mathrm{min}} \approx 0.15$. It can be observed from the equations provided in Table II that the current through the inner dc-link capacitors increases as the modulation index decreases. Consequently, M_{min} is not only limited by the current and voltage criterion, but also by the allowable voltage fluctuations across C_2 and C_3, which must be carefully considered during the design process. Within the limits analyzed above, the controller selects the sequence of switching states, and a PI controller adjusts the duration of the balancing states T_{b} based on the voltage imbalance of the dc-link. The state transitions are determined by (13) and (15).

IV. REALIZING SOFT-SWITCHING IN THE LEVEL STAGE

When switching between different states, the voltage across the snubber capacitor ($v_{\mathrm{C,sn}} = \varphi_{\mathrm{tcm+}} - \varphi_{\mathrm{tcm-}}$) can deviate considerably from the voltage supplied by the dc-link segment to be connected. The voltage discrepancy would cause the level

$$0 = I_2 = \underbrace{\int_{t_{\mathrm{b0}}}^{t_{\mathrm{b1}}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 - v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 - v_2}\right) \mathrm{d}t}_{\text{switching state Ⓑ}} + \underbrace{\int_{\frac{T_{\mathrm{ac}}}{2}}^{t_{\mathrm{b2}}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 + v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_2}\right) \mathrm{d}t}_{\text{switching state Ⓒ}} + \underbrace{\int_{t_{\mathrm{b3}}}^{T_{\mathrm{ac}}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 + v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_2}\right) \mathrm{d}t}_{\text{switching state Ⓒ}}. \tag{11}$$

$$0 = I_3 = \underbrace{\int_{0}^{t_{\mathrm{b0}}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 - v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_3}\right) \mathrm{d}t}_{\text{switching state Ⓐ}} + \underbrace{\int_{t_{\mathrm{b1}}}^{\frac{T_{\mathrm{ac}}}{2}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 - v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 + v_3}\right) \mathrm{d}t}_{\text{switching state Ⓐ}} + \underbrace{\int_{t_{\mathrm{b2}}}^{t_{\mathrm{b3}}} i_{\mathrm{L,avg}}\left(\frac{V_{\mathrm{dc}}/2 + v_{\mathrm{ac}}}{V_{\mathrm{dc}}/2 - v_3}\right) \mathrm{d}t}_{\text{switching state Ⓓ}}. \tag{12}$$

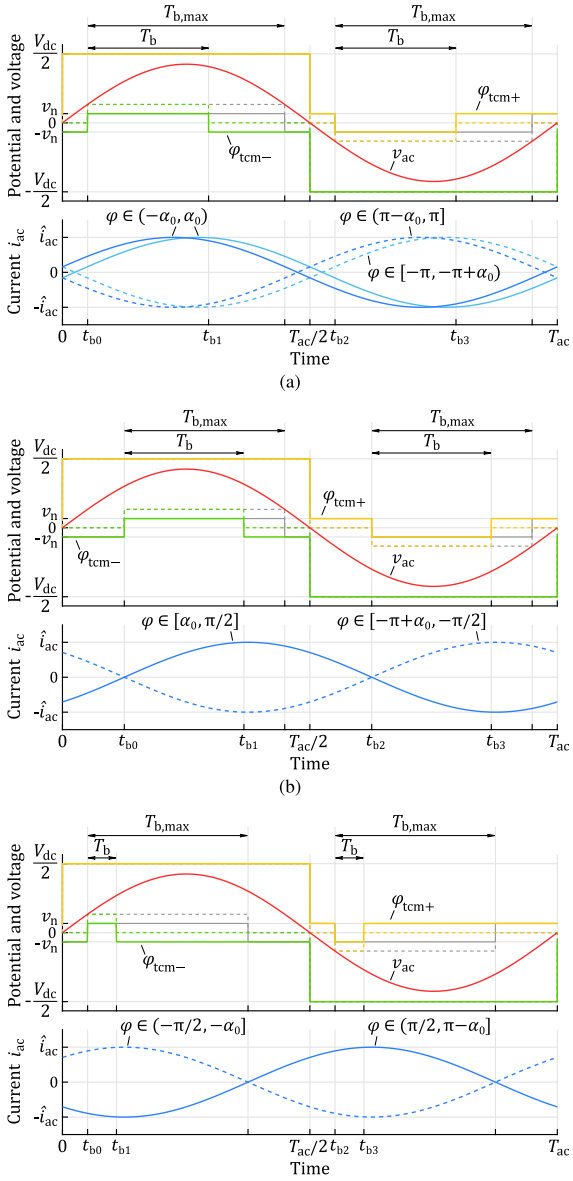


Fig. 4. Current, voltage, and potential waveforms over one fundamental cycle T_{ac} for different load scenarios. (a) $\varphi \in (-\alpha_0, \alpha_0)$ or $\varphi \in (\pi - \alpha_0, \pi]$. (b) $\varphi \in [\alpha_0, \pi/2]$ or $\varphi \in [-\pi + \alpha_0, -\pi/2]$. (c) $\varphi \in (-\pi/2, -\alpha_0]$ or $\varphi \in (\pi/2, \pi - \alpha_0]$.

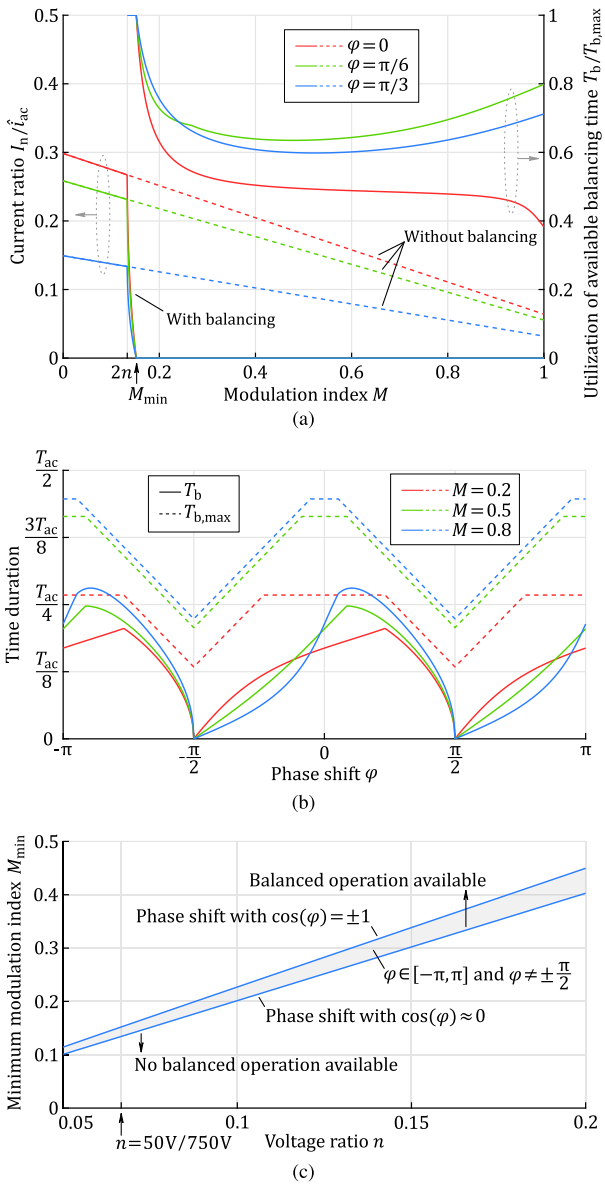


Fig. 5. Feasibility limits for voltage balancing as functions of the (a) modulation index M, (b) phase shift angle φ, and (c) voltage ratio n.

stage transistors to turn-ON at nonzero voltage, leading to hard-switched behavior with high transient currents, which in turn increases switching losses and EMI [41]. To prevent this and enable full soft-switching even in the level stage, the voltage across C_{sn} must be actively adjusted during state changes to match the voltage supplied by the dc-link after the transition. For this purpose, C_{sn} is charged or discharged by the high-frequency alternating inductor current i_L within a TCM switching cycle $1/f_{sw}$. The transition from normal to balancing operation is particularly critical, as C_{sn} needs to change its voltage by $2v_n$. Achieving a smooth transition between different switching states requires a precise timing of the switching operations. Therefore, the switching signals of the transistors are synchronized using a dedicated logic circuit, which will be described in Section V-A. The concept of soft-switching in the level stage during a transition from state Ⓐ to Ⓑ is schematically displayed in Fig. 6.

During these transitions, the switching states of the transistors S_{L1} to S_{L4} remain unchanged, while the transistors S_{L5} and S_{L6} are both turned-OFF between t_1 and t_3, thereby allowing C_{sn} to be charged or discharged by i_L. In state Ⓐ, C_{sn} is charged to $[V_{dc}/2 + v_n]$ by the dc-link. But the capacitor voltage in state Ⓑ is equal to $[V_{dc}/2 - v_n]$. As a consequence, C_{sn} must be discharged by $2v_n$ during the state transition so that S_{L5} can be turned-ON at zero voltage at t_3. The charge drawn from C_{sn} is denoted as Q. Note that the voltage across L also decreases in magnitude during the transition state Ⓘ, which slows the rise of i_L. In addition to ZVS, ZCS is realized at t_1 and t_3 by switching the level stage transistors only at the zero-crossings of i_L. When

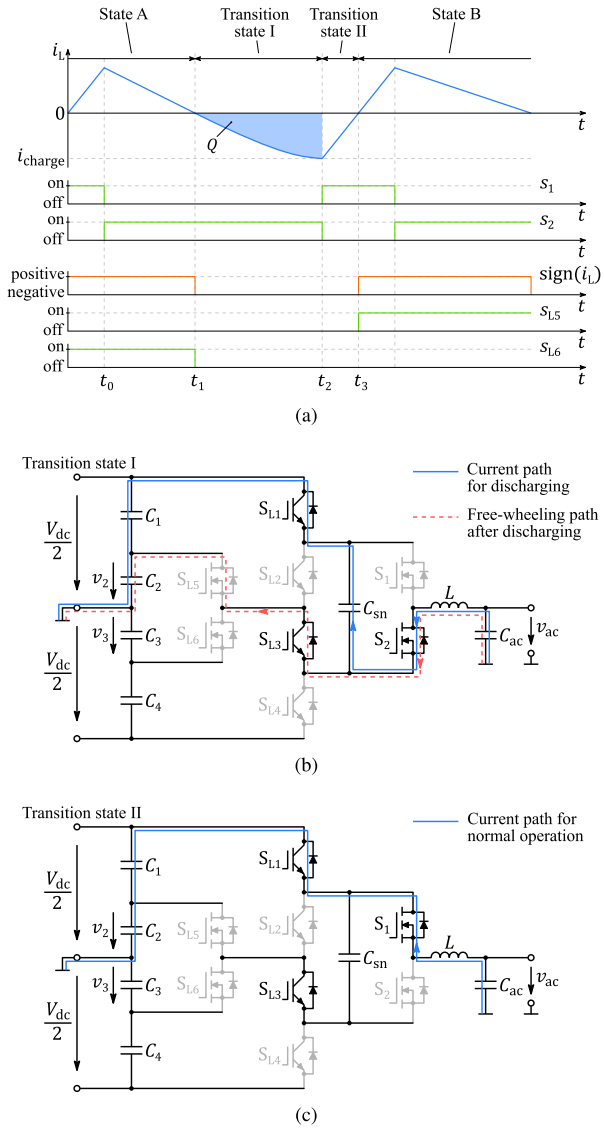


Fig. 6. Voltage adjustment of C_{sn} with switching signal synchronization during the transition Ⓐ → Ⓑ. The same principle applies to transitions from Ⓑ → Ⓐ or Ⓒ → Ⓓ and vice versa. (a) Switching signals during state transition. (b) and (c) Current paths during transition states Ⓘ and Ⓘ.

the magnitude of i_L reaches the charge current level i_{charge}, which is used to adjust $v_{C,sn}$, the system changes the transition state from Ⓘ to Ⓘ at time instant t_2.

Energy balancing techniques can be used to estimate the minimum charge current $i_{charge,min}$ needed to achieve a complete voltage adjustment from the source to the target state. During the transition from Ⓐ to Ⓑ, the energy released from C_{sn} can be estimated as follows:

$$\ominus\Delta E_{sn} = \frac{1}{2}C_{sn}\left[\left(\frac{V_{dc}}{2}+v_3\right)^2-\left(\frac{V_{dc}}{2}-v_2\right)^2\right]. \quad (16)$$

The increased energy in the dc-link capacitors C_1 and C_2 is given by

$$\oplus\Delta E_{dc} = C_{sn}\left(v_2+v_3\right)\frac{V_{dc}}{2} \quad (17)$$

TABLE IV
MINIMUM CHARGE CURRENT REQUIRED TO ENSURE COMPLETE VOLTAGE ADJUSTMENT DURING DIFFERENT STATE CHANGES

State transition	$i_{charge,min} =$
Ⓐ → Ⓑ	$-\sqrt{\frac{C_{sn}}{L}(v_2+v_3)(v_3-v_2+2v_{ac})}$
Ⓑ → Ⓐ	$\sqrt{\frac{C_{sn}}{L}(v_2+v_3)(v_3-v_2+2v_{ac})}$
Ⓒ → Ⓓ	$\sqrt{\frac{C_{sn}}{L}(v_2+v_3)(v_2-v_3-2v_{ac})}$
Ⓓ → Ⓒ	$-\sqrt{\frac{C_{sn}}{L}(v_2+v_3)(v_2-v_3-2v_{ac})}$
Ⓐ → Ⓒ (charging of C_{sn})	$\sqrt{\frac{C_{sn}}{L}(v_2-v_3)(v_3-v_2+2v_{ac}+V_{dc})}$
Ⓐ → Ⓒ (discharging of C_{sn})	$\sqrt{\frac{C_{sn}}{L}(v_3-v_2)(v_2+v_3-2v_{ac})}$
Ⓒ → Ⓐ (charging of C_{sn})	$-\sqrt{\frac{C_{sn}}{L}(v_3-v_2)(v_2-v_3-2v_{ac}+V_{dc})}$
Ⓒ → Ⓐ (discharging of C_{sn})	$-\sqrt{\frac{C_{sn}}{L}(v_2-v_3)(v_2+v_3+2v_{ac})}$

whereas the decreased energy in the output capacitor C_{ac} can be expressed as

$$\ominus\Delta E_{ac} = C_{sn}\left(v_2+v_3\right)v_{ac} \quad (18)$$

and the increased energy in the TCM inductor L, assuming a starting value of $i_L = 0$ (ZCS), can be estimated using

$$\oplus\Delta E_L = \frac{1}{2}L\cdot {i_{charge,min}}^2. \quad (19)$$

In consideration of the energy balance

$$\Delta E_L + \Delta E_{dc} = \Delta E_{ac} + \Delta E_{sn} \quad (20)$$

the required $i_{charge,min}$ to achieve full soft-switching in the level stage can be determined. The results are summarized in Table IV for all possible state transitions.

The above calculation neglects the output capacitance of the transistors S_{L5} and S_{L6}. To achieve complete voltage adjustment, the set value of the inductor current envelope must always exceed $i_{charge,min}$ to ensure full ZVS in the level stage. In some cases, $i_{charge,min}$ dictates the value of the current envelope rather than the TCM strategy. If this is the case, the controller must also adjust the current envelope in the reverse direction during operation to synthesize the desired $i_{L,avg}$. As soon as C_{sn} is discharged to $[V_{dc}/2 - v_2]$, the current automatically commutates to the body diode of S_{L5}, since S_{L3} is permanently turned-ON during transition state Ⓘ and Ⓘ. The diode's conduction condition is fulfilled somewhere between t_1 and t_2 when $\varphi_{tcm-} \approx v_2$. Fig. 6(b) and (c) illustrates the current paths during both transition states.

In the second case shown in Fig. 7, a state transition from Ⓐ to Ⓒ at the zero-crossing of the phase output voltage is considered.

The two dc-link voltages v_2 and v_3 are usually slightly different during operation, necessitating a small voltage adjustment. In this example, the need for a slight discharge of C_{sn} is considered. At t_1, the IGBTs S_{L1} and S_{L3} are turned OFF at zero current during the falling edge of the current sign. Subsequently, the inductor current discharges C_{sn} to $[V_{dc}/2 + v_2]$ in transition state Ⓘ and charges/discharges the output capacitances of the IGBTs

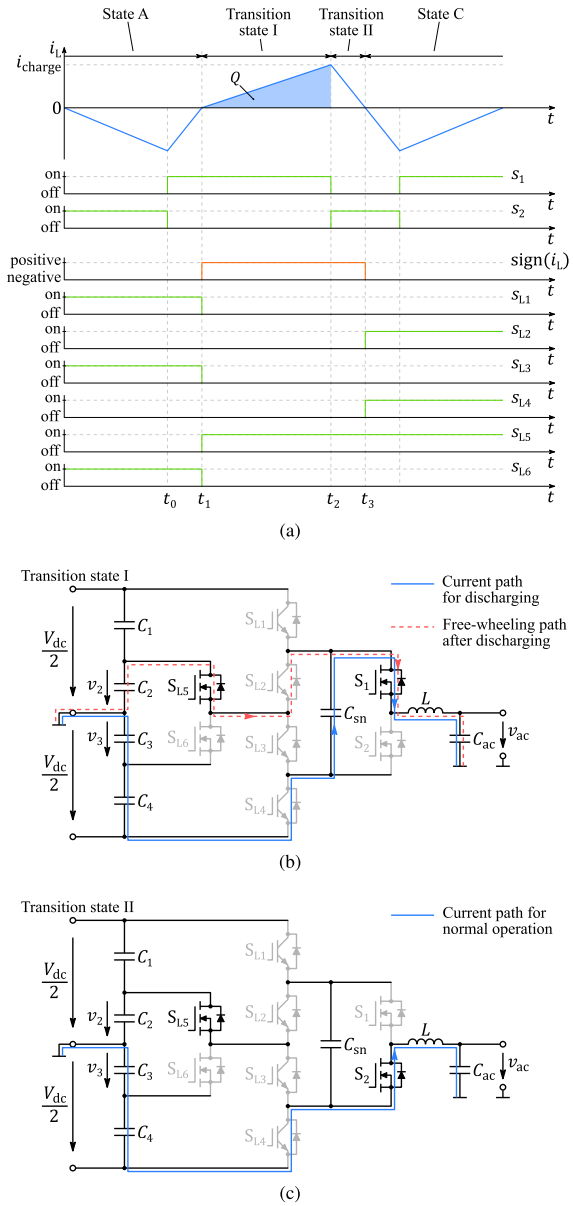


Fig. 7. Voltage adjustment of C_{sn} with switching signal synchronization during the transition Ⓐ → Ⓒ. The same principle applies to a transition from Ⓒ → Ⓐ. (a) Switching signals during state transition. (b) and (c) Current paths during transition states Ⓘ and Ⓘⓘ.

accordingly. Again, the IGBTs S_{L2} and S_{L4} turn-ON with the falling edge of the current sign at zero voltage and zero current at t_3. In the case, where charging of C_{sn} is necessary, the procedure follows the same signal synchronization, with charging occurring during transition state Ⓘⓘ. The same principle applies to the reverse switching actions. The detailed implementation with switching signal synchronization is covered in Section V-A.

V. Practical Realization of the Proposed Topology

To verify the proposed concepts, a single-phase 2 kW inverter prototype operating with TCM modulation and powered by a 1.5 kV 4-level dc-link was designed and built. A photograph of the assembled prototype is presented in Fig. 8.

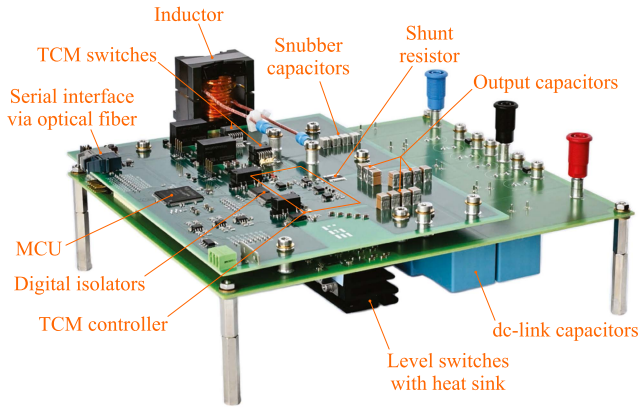


Fig. 8. Experimental prototype of the single-phase 4-level TCM inverter.

It consists of several key components arranged on two stacked PCBs and an inductor designed with a ferrite core. The upper PCB includes a microcontroller unit (MCU) with a measurement processing unit for inverter control, TCM switches equipped with gate drivers, output and snubber capacitors, and a shunt resistor for inductor current measurement. The lower PCB contains the level stage switches with their gate drivers and heat sink, along with the dc-link capacitors and voltage measurement circuitry. Data communication is carried out over a serial link using optical fiber. Thanks to the advantages of soft-switching, the inverter requires no active cooling and is cooled by natural convection.

A. Hardware Design and Control Algorithm Implementation

The control unit's schematic and the hardware setup for gate signal generation with synchronization capability are shown in Fig. 9.

The control system consists of a hybrid circuit that uses both analog and digital components. The TCM controller shown in Fig. 9(a), implemented using discrete logic devices, is integrated into a separate circuit at the output potential and operates at a high variable frequency. The MCU samples at a lower constant frequency of 30 kHz to control the current envelope generator, the dead-time generator, and the level stage controller. Digital isolators separate the TCM controller and the MCU. Since the logic circuit of the TCM controller is at the output potential, a precise wideband analog signal isolator is no longer necessary. Consequently, the signals between the grounded MCU/synchronization circuit and the TCM controller at the output potential are exclusively digital.

Controlling the proposed inverter requires measuring the output voltage v_{ac} as well as the dc-link voltages v_2, v_3, and V_{dc}. Furthermore, measuring the inductor current i_L and detecting its zero-crossing is essential for the correct operation with TCM modulation and for achieving a precise switching timing of the level stage transistors. Therefore, i_L is measured using a shunt resistor, amplified, and its current sign is determined. The measurement method provides a low-cost solution with very high accuracy and high bandwidth. Compared to the current

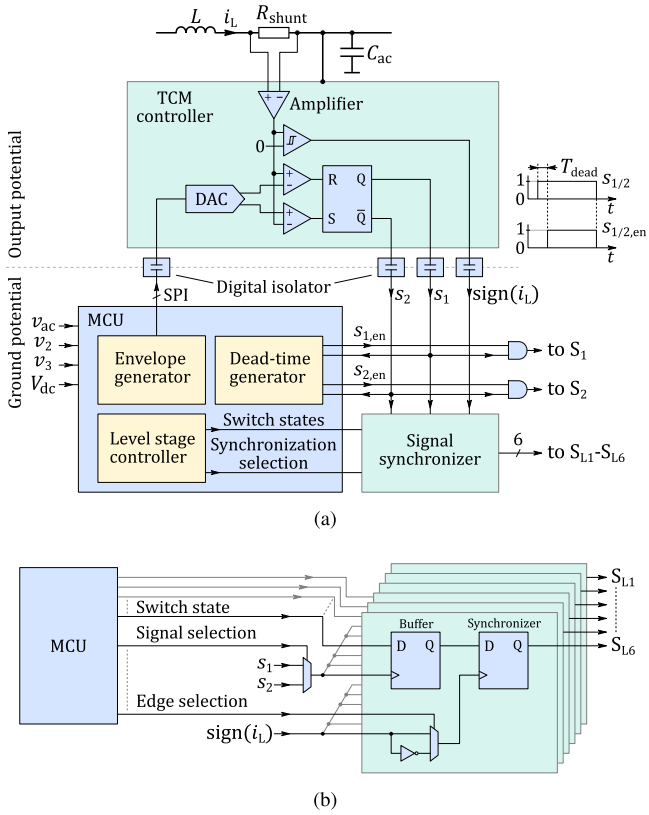


Fig. 9. (a) Schematic of the basic control unit consisting of a TCM controller floating at the output potential and a ground-referenced MCU. (b) Generation of the gate signals for the level stage switches $S_{L1\sim L6}$ with synchronization unit.

measurement method presented in [17], this approach is simplified and does not require galvanic isolation of the analog signal, making it ideally suited for the proposed TCM-operated topology.

Based on the voltages and currents sampled, the MCU generates the required current envelope, as depicted in Fig. 3(b), with a sampling frequency of 30 kHz during operation. The current envelope values are then transmitted through the serial peripheral interface (SPI) to the digital-to-analog converter (DAC), which converts them back into an analog signal. Using the current envelope and the measured inductor current, the TCM controller generates the control signals s_1 and s_2 for the TCM transistors at a high operating frequency. To achieve full ZVS, the rising edges of the control signals are delayed by the required dead-time, and the adapted switching signals are subsequently forwarded to the gate driver units.

The control signals are synchronized in two stages using a simple logic circuit to ensure optimal timing of the synchronization unit, as depicted in Fig. 9(b). Examples of the synchronous control concept employed to achieve ZVS and ZCS in the level stage during different state transitions are illustrated in Figs. 6 and 7. At time instant t_0, the recalculated switching states of the level stage transistors are stored in the buffer using the rising edge of s_1 or s_2. The switching signals are then synchronized for execution at t_1 and t_3 with the zero-crossing of i_L, using either the rising or falling edge of the current sign for synchronization.

The signal and edge selection of the two-stage synchronization process are summarized in Table V for all state transitions.

B. Component and Parameter Selection

Selecting appropriate components and parameters is crucial for the correct operation of the proposed 4-level TCM inverter. The optimal design depends on the specific application and its design objectives, such as the minimum and maximum switching frequency. The following discussion highlights the key considerations for the assembled prototype. An overview of the design is provided in Table VI.

Semiconductor devices: Given the asymmetrical dc-link, a hybrid configuration with different semiconductor technologies and voltage ratings is optimal for cost and performance. According to [42], minimizing residual ZVS losses in soft-switched operation requires power devices with a very low internal gate resistance $R_{g,int}$ and a low input capacitance C_{iss}. Based on this, the design employs four 1200 V / 75 mΩ SiC MOSFETs *Sanan AMS1200075P* (two devices paralleled per switch) to form the 2-level TCM half-bridge. As shown by [34], Infineon's High Speed 3 IGBTs demonstrate particularly favorable forward recovery characteristics. Therefore, the level stage includes four 1200 V Si IGBTs *Infineon IKY50N120CH3* with co-packaged freewheeling diodes and two 250 V / 20 mΩ Si MOSFETs *Infineon IPB64N25S3-20*.

Inductance L: The choice of the inductance decisively determines the switching frequency of the TCM transistors. To enable high switching frequencies with short rise and fall times of the current, a small inductance of 40 µH is entirely sufficient, thereby contributing to a compact and lightweight design. It is important to highlight that L also influences the selection of the design parameters n and I_{tcm}, as well as the value of $i_{charge,min}$. Therefore, the optimal design may require an iterative approach, starting with the choice of L.

Snubber capacitance C_{sn}: To effectively decouple the TCM stage from the level stage and mitigate the forward recovery effects, a snubber capacitor is installed between the two stages. C_{sn} serves to reduce the high current slopes through the IGBTs and absorbs the current surges. Class 1 ceramic capacitors or film capacitors are preferred for this purpose due to their ability to handle high current gradients without significant piezoelectric effect, as well as their low ESR for minimal heat generation and high stability [34]. The snubber capacitor should be chosen as large as possible to enhance the decoupling effect and minimize forward recovery effects. However, as indicated in Table IV, $i_{charge,min}$ is determined by the ratio C_{sn}/L and thus increases with larger capacitance values. Therefore, a tradeoff must be made when selecting C_{sn}. According to [34], even a relatively small capacitance on the order of tens of nF is sufficient to achieve the desired effect. In this design, C0G MLCCs with a total capacitance of 56 nF were chosen to balance these considerations.

Reverse inductor current I_{tcm}: This design parameter defines the FRC set point within the hysteresis control, enabling an alternating current flow through the inductor during each switching cycle. Achieving full ZVS requires a sufficiently high reverse

TABLE V
TWO-STEP SWITCHING SIGNAL SYNCHRONIZATION OF THE TRANSISTORS S_{L1} TO S_{L6} IN THE LEVEL STAGE

State transition	Signal for buffer update (update with rising edge at t_0)	Edge selection of sign (i_L) for execution						C_{sn}
		S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{L5}	S_{L6}	
Ⓐ → Ⓒ	s_1	↑	↓	↑	↓	↑	↑	charging / discharging
Ⓒ → Ⓐ	s_2	↑	↓	↑	↓	↓	↓	charging / discharging
Ⓐ → Ⓑ	s_2	–	–	–	–	↑	↓	discharging
Ⓑ → Ⓐ	s_1	–	–	–	–	↑	↓	charging
Ⓒ → Ⓓ	s_1	–	–	–	–	↑	↓	discharging
Ⓓ → Ⓒ	s_2	–	–	–	–	↑	↓	charging

[↑ : rising edge of sign (i_L), ↓ : falling edge of sign (i_L), – : remain unchanged]

TABLE VI
MAIN DESIGN PARAMETERS AND COMPONENTS OF THE PROTOTYPE

	Parameter / Component	Value
Inverter	dc-link voltage V_{dc}	1.5 kV
	Inner dc-link voltage $v_2 \approx v_3 \approx v_n$	50 V
	Voltage ratio n	1/15
	Outer dc-link capacitance C_1, C_4	20 µF
	Inner dc-link capacitance C_2, C_3	1054 µF
	Transistor S_1, S_2	AMS1200075P
	Transistor $S_{L1} \sim S_{L4}$	IKY50N120CH3
	Transistor S_{L5}, S_{L6}	IPB64N25S3-20
	Inductance L	40 µH
	Snubber capacitance C_{sn}	56 nF (C0G MLCCs)
	Output capacitance C_{ac}	2 µF
	TCM reverse current I_{tcm}	3.5 A
	Shunt resistor R_{shunt}	10 mΩ
	Dead-time of TCM switches T_{dead}	50 ∼ 400 ns
MCU	Type	XMC 4800
	Clock frequency	144 MHz

current, which is determined by the inductance L and the output capacitance C_{oss} of the transistors S_1 and S_2 [12], [43]. At the start of each commutation process, the energy stored in L must exceed the energy required to fully charge and discharge the output capacitances. During the output voltage zero-crossing, the energy necessary to charge C_{oss} reaches its maximum, thereby estimating the minimal required I_{tcm} under the simplification that $V_{dc}/2 \gg v_n$ as follows:

$$\frac{1}{2}LI_{tcm}{}^2 > 4E_{oss} = 4\left[\int_0^{800\,\mathrm{V}} v_{ds}C_{oss}\left(v_{ds}\right)\mathrm{d}v_{ds}\right]. \quad (21)$$

According to (21), with a stored energy in C_{oss} of $E_{oss} = 30\,\mu\mathrm{J}$ at $V_{ds} = 800\,\mathrm{V}$ [44], the minimal I_{tcm} is approximately 2.5 A. To maintain a margin and avoid unnecessary additional conduction losses, a reverse inductor current of 3.5 A was set in the controller.

Voltage ratio n: The voltage ratio n and the inner dc-link voltage v_n are key design parameters in the 4-level topology. The lower limit of v_n is set by the minimum acceptable switching frequency and the maximum tolerable output-voltage ripple. Considering the load phase-angle range, the design parameters I_{tcm}, L, and a specified minimum switching frequency at the voltage zero-crossing, the minimum required voltage ratio n_{min} is derived from (8). From (6), it is evident that n has only a minor effect on $f_{sw,max}$ as long as $n \ll 1$. The upper bound is constrained by the device voltage ratings and the required charge current during state transitions when using a hybrid Si+SiC configuration. Since the voltage across C_{sn} must be actively adjusted by $2v_n$ at each transition, n should be selected so that the charge current remains within the allowable limit. Using (20), an upper limit with a given permissible $I_{charge,min}$ during state transitions can be estimated as

$$n_{max} = \frac{I_{charge,min}}{V_{dc}}\sqrt{\frac{L}{2C_{sn}}}. \quad (22)$$

A value of $v_n = 50\,\mathrm{V}$ (with $n = 1/15$) was chosen to balance these considerations and ensure safe operation with 1200 V power devices.

DC-link capacitance $C_{1\sim4}$: To keep the voltage fluctuation within acceptable limits during a fundamental cycle, a capacitance of sufficient size must be installed in the dc-link. From both an energy-related safety perspective and a cost perspective, it is preferable to design the inner low-voltage capacitors C_2 and C_3 with a large capacitance.

Dead-time T_{dead}: The required dead-time of the TCM switches depends on the instantaneous value of i_L. The controller sets it so that C_{oss} of both TCM switches are fully charged and discharged to achieve complete ZVS during each switching transition. Therefore, the dead-time varies between 50 and 400 ns throughout the fundamental cycle.

The control algorithm is fully implemented in an *Infineon XMC4800-F144K2048 AA* general-purpose MCU.

VI. EXPERIMENTAL RESULTS

Unless otherwise specified, the inverter design discussed above was experimentally verified at the operating point presented in Table VII. A *Keysight MXR608A* oscilloscope with *DP0001A* and *N2790A* differential voltage probes and *N2783B* current probes were used to acquire all relevant time signals simultaneously.

A. Results Over Fundamental Cycles

Fig. 10 presents the inverter's key waveforms and the time-dependent switching frequency of the TCM switches over two and a half fundamental cycles.

TABLE VII
EXPERIMENTAL OPERATING POINT PARAMETERS

Parameter / Component	Value
Fundamental frequency f_{ac}	50 Hz ($\widehat{=} T_{ac} = 20$ ms)
Phase output voltage $V_{ac,rms}$	478 V ($\widehat{=} M = 0.9$)
Phase output current $I_{ac,rms}$	4.3 A
Output active power P_{ac}	2 kW
Load resistor R_{load}	110 Ω
Phase shift angle φ	$\approx 0°$

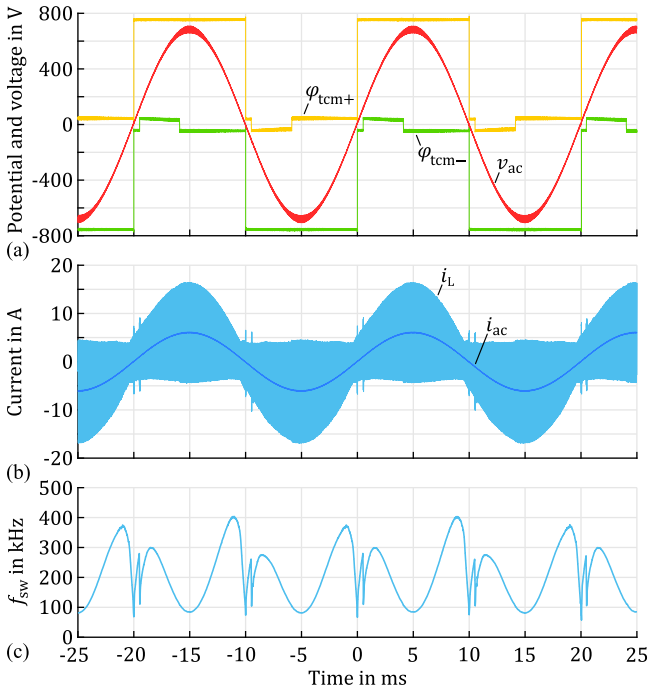


Fig. 10. Experimental results at nominal load over two and a half fundamental cycles. (a) Inverter output voltage and node potentials of the TCM stage. (b) Triangular inductor current and output current. (c) Instantaneous switching frequency of the TCM switches, with $f_{sw,min} = 60$ kHz and $f_{sw,max} = 400$ kHz.

Due to the high switching frequencies, the inverter achieves quasi-sinusoidal output waveforms solely through the filtering action of the inherent LC components in the TCM stage. TCM operation is maintained throughout the entire fundamental cycle. Symmetrical potential waveforms indicate a balanced dc-link with a uniform use of the states Ⓑ and Ⓓ, demonstrating the effectiveness of the applied balancing method. The parasitic oscillation between L and C_{oss} of S_1 and S_2 after the TCM switch turns OFF causes slight deviations between the measured inductor current envelope and the simulated waveform in Fig. 3(b) with FRC. This discrepancy can be attributed to the varying resonance amplitudes throughout the fundamental cycle. Boundary compensation techniques, such as those mentioned in [25], would further improve the envelope shape. In addition, individual current peaks in i_L are noticeable in the area of state transitions. At these specific time instants, the controller sets i_L based on the required value of $i_{charge,min}$ as outlined in Table IV, rather than following the specified current envelope of the TCM operation. The inductor voltage and load current

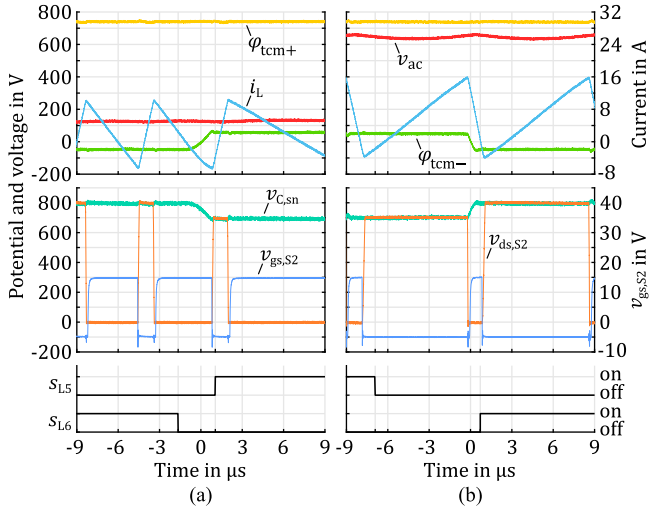


Fig. 11. Voltage adjustment of C_{sn} with switching signal synchronization during the transition (a) Ⓐ → Ⓑ and (b) Ⓑ → Ⓐ.

primarily determine the instantaneous switching frequency of the TCM switches. For the present design and operating point, the minimum and maximum switching frequencies were roughly 60 and 400 kHz, respectively, corresponding to a frequency ratio of 6.7 ($f_{sw,max}/f_{sw,min}$). The switching frequency obtained from the measurement results aligns well with the waveform in Fig. 3(c) using (5). However, due to the mentioned current peaks at state transitions, f_{sw} is observed to dip below the analytical prediction. This should be considered when selecting n in the design process.

B. Results During Switching State Transitions

To verify the soft-switching operation within the level stage, different switching transitions were acquired to assess the correct functioning of the switching signal synchronization and the voltage adjustment of the snubber capacitor. Fig. 11 shows the measured curves for the switching transitions between states Ⓐ and Ⓑ.

A closer look at the potential waveforms φ_{tcm+} and φ_{tcm-} reveals a minimal, negligible forward recovery effect in response to switching within the TCM stage. The output voltage ripple is larger in Fig. 11(b) due to the lower instantaneous switching frequency and the higher output current. However, the ripple remains within the desired range thanks to the selection of a sufficiently large output capacitance C_{ac}. The control signals forwarded to the gate driver units are displayed at the bottom. In practical implementation, the entire signal synchronization is slightly shifted to compensate for component-induced delays within the signal path. Thus, the switching signals of the transistors S_{L5} and S_{L6} change their value prematurely, with a current hysteresis of ± 2 A. The charge/discharge duration of C_{sn} depends on the instantaneous inductor current i_L. Once the voltage $v_{C,sn}$ across C_{sn} has fully adjusted to the voltage of the target state, the respective transistor turns ON at zero voltage.

The switching transitions in the area of a voltage zero-crossing from state Ⓐ to Ⓒ and vice versa are shown in Fig. 12. As

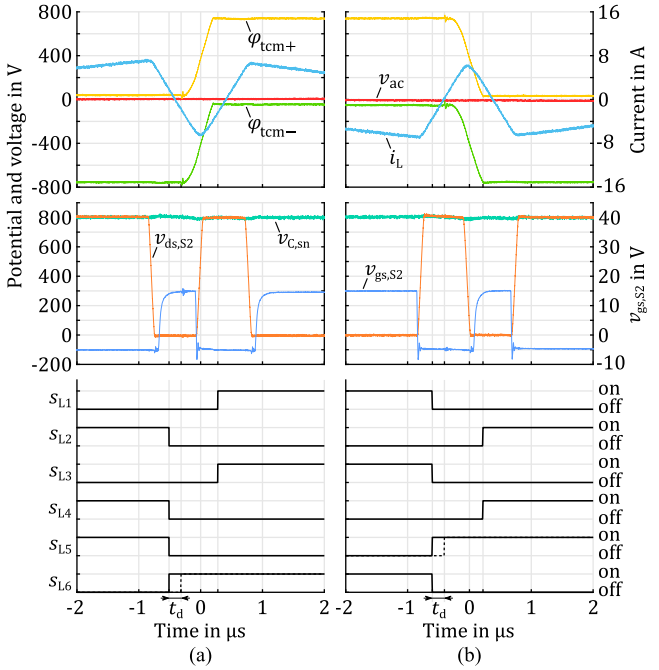


Fig. 12. Voltage adjustment of C_{sn} with switching signal synchronization during the transition (a) Ⓒ → Ⓐ and (b) Ⓐ → Ⓒ.

S_{L5} and S_{L6} are synchronized to the same current sign reversal when transitioning between the states Ⓐ and Ⓒ, both transistors would switch simultaneously according to the procedure described in Section V-A. To prevent a possible short circuit, a dead-time of about 100 ns is incorporated into the practical implementation. The value t_d indicated in the time diagram represents the sum of the dead-time set in the gate driver plus the response delay of the gate circuit, totaling roughly 195 ns.

C. Efficiency

Further investigation included efficiency measurements using the precise power analyzer *Yokogawa WT5000*. The measured efficiency excludes the power losses of the gate driver, voltage and current measurement circuits, and the control circuitry, which are minor and amount to only a few watts. To ensure realistic efficiency results, measurements at each operating point were conducted under steady-state conditions for more than 5 min. Fig. 13 shows the inverter's efficiency versus the modulation index for two resistive loads ($\varphi \approx 0$).

The lowest output power measured at $M = 0.3$ was 100 W. Lower modulation indices down to $M \approx 0.15$ are achievable, but they require an extended control scheme to maintain voltage balance among the dc-link capacitors. The results indicate that efficiency increases with higher output power, achieving a full-load efficiency of more than 98.6% at $M = 0.9$ and $P_{ac} \approx 2$ kW, despite the use of a hybrid topology consisting of Si IGBTs and low-voltage Si MOSFETs. Since the novel TCM-operated inverter inherently achieves high output voltage quality, it eliminates the need for additional sine-wave filtering. Consequently, efficiency reductions due to downstream filtering, often required by conventional PWM-operated inverters, are not expected.

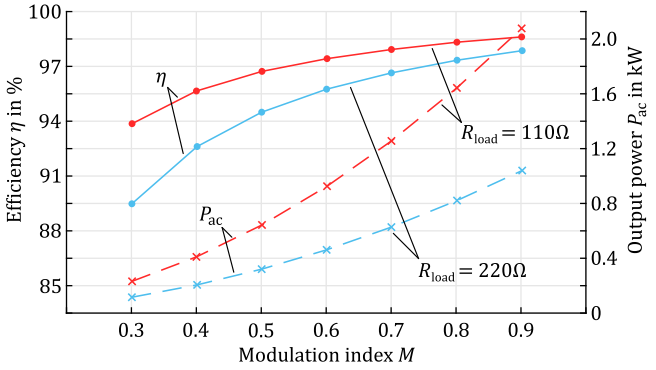


Fig. 13. Measured efficiency as a function of the modulation index. The measured modulation indices range from 0.3 to 0.9, corresponding to rms output voltages between 160 and 478 V.

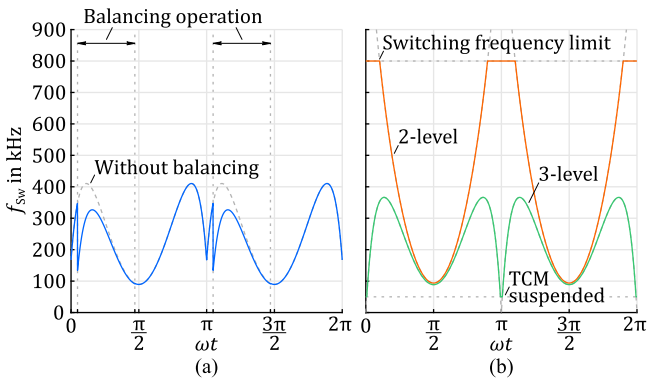


Fig. 14. Switching frequency profile over one fundamental cycle using TCM operation in different topologies: (a) proposed 4-level topology and (b) conventional 2- and 3-level topologies.

Several approaches are available to further improve efficiency. One involves combining TCM with discontinuous modulation (DPWM) schemes, as demonstrated in [45]. Conversely, in [19], [20], [22], [46], the inverter control alternates between TCM at high load currents and DCM at low load currents within each fundamental cycle. Furthermore, the combination of TCM at low load currents and continuous conduction mode (CCM) at high load currents has been examined in [47]. All these operational strategies, including the various current envelope schemes mentioned in Section II-B, are also applicable to the proposed topology. If cost is not a primary concern, unipolar devices can replace Si IGBTs in the level stage as an additional measure to reduce power losses, especially the forward recovery losses associated with the hybrid configuration discussed in Section II-C.

VII. Comparison With Other Topologies

To evaluate the presented topology based on its characteristics, it will be qualitatively compared in the following with the TCM-operated 2-level and 3-level variants as well as with the hard-switched 3-level ANPC in CCM operation. Fig. 14 displays the switching frequency profile over one fundamental cycle for different voltage levels, all evaluated at the same operating point and with the same design parameters listed in Tables VI and VII.

TABLE VIII
COMPARISON OF DIFFERENT TOPOLOGIES APPLYING TCM AND CCM MODULATION

Topology		TCM			CCM
		2-Level [8], [13], [20], [21], [35], [46], [48]	3-Level T-Type NPC [10], [24], [25], [26]	4-Level [proposed topology]	3-Level ANPC [29], [30], [31], [32]
Number of switches per phase		$2^{(\mathrm{I})}$	$2^{(\mathrm{I})}+2^{(\mathrm{II})}$	$6^{(\mathrm{II})}+2^{(\mathrm{III})}$	$6^{(\mathrm{II})}$
Voltage stress of	SG I	V_{dc}	V_{dc}	–	–
	SG II	–	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}+V_{\mathrm{n}}$	$\frac{V_{\mathrm{dc}}}{2}$
	SG III	–	–	$2V_{\mathrm{n}}$	–
Average number of current-carrying power devices over T_{ac} in	SG I	1	$f(M)=0\ldots\frac{2}{\pi}$	–	–
	SG II	–	$2\left[1-f(M)\right]$	2	2
	SG III	–	–	$f(M)=\frac{\pi-2}{\pi(1+n)}\ldots\frac{1}{1+n}$	–
Frequency ratio $f_{\mathrm{sw,max}}/f_{\mathrm{sw,min}}$		highest without enlarged envelope	high	moderate	1
Output voltage harmonic distortion		low	lowest	lowest	high (sine-wave filter might be needed)
System and control complexity		moderate	moderate +	high	moderate
Soft-switching		continuous only with enlarged envelope	interrupted or 2-level operation around voltage zero-crossing	always continuous	not possible

SG: Switch group
Excellent Good Acceptable Unfavorable / trade-off Not evaluated

Based on the simplified analysis, continuous TCM operation is feasible for the proposed topology within an f_{sw}-range of 90 to 450 kHz. In the 2-level case, the switching frequency diverges at integer multiples of π (voltage zero-crossings) when using a FRC envelope. Widening the current envelope around zero-crossings can reduce the maximum switching frequency, but this incurs the penalty of increased rms current and higher conduction losses. In the 3-level case, the voltage across the inductor at the voltage zero-crossing is insufficient to build up a sign-reversing TCM current. Therefore, the transistors must either switch hard or the output voltage must be clamped in that region. For the specific case of the T-type NPC topology, TCM can only be realized through unipolar modulation[1] in the region of voltage zero-crossings. Table VIII summarizes and compares the main characteristics of the different topologies and operating principles.

In the proposed topology, either two or three switches conduct the inductor current at any given time. The average number of current-carrying devices depends on the modulation index and, consequently, on the output voltage. This differs from a conventional 2-level inverter, where only one switch conducts the current, and from a 3-level T-type NPC inverter, which requires one or two switches. However, this topology reduces the voltage stress on the semiconductor devices to roughly half, enabling operation at double V_{dc} using the same components. Consequently, the output current is halved for the same P_{ac} and M. Therefore, current conduction through multiple devices does not necessarily constitute a notable disadvantage.

[1]Switching is performed exclusively between the positive and negative dc-link rails, with the zero-voltage state suspended.

The output voltage harmonic distortion is lowest in both the proposed topology and the 3-level T-type inverter because they provide more than two output voltage levels, allow higher switching frequencies compared to CCM operation thanks to soft-switching, and already include the sine-wave filter by design. The main tradeoff lies in system and control complexity, which is greatest in the proposed topology due to the more complex charge balancing of the 4-level dc-link and the continuous adjustment of the voltage across C_{sn} during operation.

VIII. CONCLUSION

This article introduces a novel TCM-operated inverter topology with an asymmetrically subdivided 4-level dc-link that integrates Si and SiC power semiconductor devices. The design successfully achieves full soft-switching capability for all transistors and across all transitions without requiring additional resonant components. This is accomplished by overlapping voltage ranges, which provide the necessary voltage to build up an alternating triangular inductor current, even at output voltage zero-crossings. The hybrid configuration combines the fast switching capabilities of SiC MOSFETs with cost-effective Si IGBTs and low-voltage Si MOSFETs, achieving a peak efficiency of more than 98.6% at nominal load. Experimental results validate the design's capability in maintaining soft-switching and demonstrate the effectiveness of the dc-link voltage control method. Due to its advantageous characteristics, the proposed multilevel TCM inverter is capable of covering low-power applications in the medium-voltage range, where high requirements for power density, EMI, and voltage quality must be met. Future work might focus on refining design parameters and further optimizing the topology for specific applications.

REFERENCES

[1] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," *IEEE Trans. Ind. Appl.*, vol. 34, no. 4, pp. 847–860, Jul./Aug. 1998.

[2] S. A. Q. Mohammed and J.-W. Jung, "A state-of-the-art review on soft-switching techniques for DC–DC, DC–AC, AC–DC, and AC–AC power converters," *IEEE Trans. Ind. Informat.*, vol. 17, no. 10, pp. 6569–6582, Oct. 2021.

[3] Y. Liu et al., "LCL filter design of a 50-kW 60-kHz SiC inverter with size and thermal considerations for aerospace applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8321–8333, Oct. 2017.

[4] Y. Wang, O. Lucia, Z. Zhang, S. Gao, Y. Guan, and D. Xu, "A review of high frequency power converters and related technologies," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 247–260, 2020.

[5] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Trans. Ind. Applicat.*, vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.

[6] T. Lehmeier, A. Amler, Y. Zhou, and M. März, "Three-phase ARCP inverter using soft-switching with a single shared inductor," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2505–2521, Feb. 2024.

[7] H. Lu, Q. Wang, J. Chai, and Y. Li, "Review of three-phase soft switching inverters and challenges for motor drives," *Trans. Electr. Mach. Syst.*, vol. 8, no. 2, pp. 177–190, Jun. 2024.

[8] S. M. Tayebi and I. Batarseh, "Analysis and optimization of variable-frequency soft-switching peak current mode control techniques for microinverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1644–1653, Feb. 2018.

[9] A. Amirahmadi et al., "Hybrid ZVS BCM current controlled three-phase microinverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2124–2134, Apr. 2014.

[10] S. Miric, P. S. Niklaus, J. Huber, C. Stäger, M. Haider, and J. W. Kolar, "Analysis and experimental verification of the EMI signature of three-phase three-level TCM soft-switching converter systems," *IEEE Access*, vol. 11, pp. 57391–57400, 2023.

[11] A. Amirahmadi, L. Chen, U. Somani, H. Hu, N. Kutkut, and I. Bartarseh, "High efficiency dual-mode current modulation method for low-power DC/AC inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2638–2642, Jun. 2014.

[12] M. Haider et al., "Analytical calculation of the residual ZVS losses of TCM-Operated single-phase PFC rectifiers," *IEEE Open J. Power Electron.*, vol. 2, pp. 250–264, 2021.

[13] M. Haider et al., "Novel ZVS S-TCM modulation of three-phase AC/DC converters," *IEEE Open J. Power Electron.*, vol. 1, pp. 529–543, 2020.

[14] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[15] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kV SiC-based medium-voltage ZVS bidirectional single-phase PFC AC/DC stage," *IEEE Trans. Power Electron.*, vol. 7, no. 2, pp. 779–797, Jun. 2019.

[16] Z. Liu, B. Li, F. C. Lee, and Q. Li, "High-efficiency high-density critical mode rectifier/inverter for WBG-device-based on-board charger," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9114–9123, Nov. 2017.

[17] B. Fan, Q. Wang, R. Burgos, A. Ismail, and D. Boroyevich, "Adaptive hysteresis current based ZVS modulation and voltage gain compensation for high-frequency three-phase converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1143–1156, Jan. 2021.

[18] T. Liu, C. Chen, K. Xu, Y. Zhang, and Y. Kang, "GaN-Based megahertz single-phase inverter with a hybrid TCM control method for high efficiency and high-power density," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6797–6813, Jun. 2021.

[19] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in 3 MHz GaN totem-pole PFC rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.

[20] N. Haryani, S. J. Ohn, and R. Burgos, "ZVS turn-on triangular current mode (TCM) control for three-phase two-level converters with reactive power control," *IEEE Open J. Power Electron.*, vol. 4, pp. 923–933, 2023.

[21] T. Liu, Y. Zhang, Z. Wang, C. Chen, and Y. Kang, "Output DM EMI noise prediction for MHz TCM-Based single phase inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14499–14513, Dec. 2022.

[22] J. Deng, J. Chen, W. Han, and Z. Xin, "Light load efficiency improvement for three-phase inverter employing valley switching under mixed TCM/DCM operation," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7675–7684, Jun. 2024.

[23] G. Zhang, Y. Wu, R. Qiang, P. Venugopal, J. Xu, and T. B. Soeiro, "Doubled-frequency triangular current mode modulation with sinusoidal frequency profile for a three-level ANPC converter," *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 14923–14936, Oct. 2025.

[24] D. Leuenberger and J. Biela, "Comparison of a soft switched TCM T-type inverter to hard switched inverters for a 3 phase PV grid interface," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, IEEE, 2012, pp. LS1d.1-1–LS1d.1-8.

[25] Z. Zhang, J. Zhang, S. Shao, and J. Zhang, "A high-efficiency single-phase T-type BCM microinverter," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 984–995, Jan. 2019.

[26] T. Langbauer, S. Miric, M. Haider, J. Huber, and J. W. Kolar, "Comparative evaluation of ARCP and three-level TCM soft-switching bridge-legs for high-frequency SiC converter systems," in *Proc. Int. Power Electron. Conf. ECCE Asia*, IEEE, 2022, pp. 1734–1741.

[27] Y. Zhou, "Multi-level soft switching inverter driving system and voltage window switching method thereof," China Patent CN111697861A, Jun. 22, 2020.

[28] Y. Zhang et al., "A SiC and Si hybrid five-level unidirectional rectifier for medium voltage applications," *IEEE Trans. Ind. Applicat.*, vol. 69, no. 8, pp. 7537–7548, Aug. 2022.

[29] L. Zhang et al., "Evaluation of different Si/SiC hybrid three-level active NPC inverters for high power density," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8224–8236, Aug. 2020.

[30] Q.-X. Guan et al., "An extremely high efficient three-level active neutral-point-clamped converter comprising SiC and Si hybrid power stages," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341–8352, Oct. 2018.

[31] C. Li et al., "Space vector modulation for SiC and Si hybrid ANPC converter in medium-voltage high-speed drive system," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3390–3401, Apr. 2020.

[32] D. Zhang, J. He, and S. Madhusoodhanan, "Three-level two-stage decoupled active NPC converter with Si IGBT and SiC MOSFET," *IEEE Trans. Ind. Applicat.*, vol. 54, no. 6, pp. 6169–6178, Nov./Dec. 2018.

[33] C. Li et al., "An SiC MOSFET and Si diode hybrid three-phase high-power three-level rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6076–6087, Jul. 2019.

[34] Y. Zhou, T. Lehmeier, A. Amler, and M. März, "Forward recovery and its mitigation in hybrid Si/SiC-based DC–AC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, IEEE, 2025, pp. 1767–1773.

[35] Q. Zhang, H. Hu, D. Zhang, X. Fang, Z. J. Shen, and I. Bartarseh, "A controlled-type ZVS technique without auxiliary components for the low power DC/AC inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3287–3296, Jul. 2013.

[36] J. Biela, D. Hassler, J. Minibock, and J. W. Kolar, "Optimal design of a 5 kW/dm^3 / 98.3% efficient TCM resonant transition single-phase PFC rectifier," in *Proc. Int. Power Electron. Conf. ECCE Asia*, IEEE, 2010, pp. 1709–1716.

[37] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in *Proc. Int. Power Electron. Conf. ECCE Asia*, IEEE, 2010, pp. 1725–1732.

[38] C. L. Kahraman, S. Lakshmeesha, S. Rosado, and T. Wijekoon, "Impact of forward recovery effects in different Si-IGBT technologies used in hybrid Si-IGBT, SiC-MOSFET based ANPC topology," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, IEEE, 2022, pp. 1364–1370.

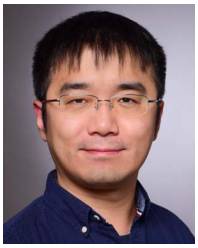
[39] S. Lakshmeesha, C. L. Kahraman, S. Rosado, and T. Wijekoon, "Switching behavior of a hybrid Si-IGBT and SiC MOSFET based ANPC topology," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, IEEE, 2021, pp. 293–298.

[40] Y. Zhou, "Multi-level soft switching inverter circuit and method for balancing terminal voltage of intermediate level of multi-level soft switching inverter circuit," China Patent CN114362574 A, Dec. 8, 2021.

[41] Z. Guo and H. Li, "Three-level gate driving method for inrush current suppression in a hybrid Si SiC based transformer-less medium voltage PV inverter," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl.*, IEEE, 2019, pp. 1–5.

[42] T. Lehmeier, Y. Zhou, M. März, and A. P. Pai, "Influence of SiC MOSFET device parameters on zero-voltage switching losses," in *Proc. Int. Exhib. Conf. Power Electron. Intell. Motion Renewable Energy Energy Manage. Europe*, 2025, pp. 1928–1934.

[43] M. Kasper, R. Burkat, F. Deboy, and J. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[44] Sanan Semiconductor, "1200V 75mΩ Silicon Carbide power MOSFET: AMS1200075P preliminary datasheet," Rev. 0.0.2, Jul. 2024, pp. 1–15.
[45] Y. Feng, Y. Guan, H. Ben, Y. Wang, S. Yang, and D. Xu, "Smoothed TCM-DPWM and input current ripple reduction for three-phase DC–AC ZVS inverters," *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 16283–16293, Dec. 2024.
[46] G. Son, Z. Huang, Q. Li, and F. C. Lee, "Analysis and control of critical conduction mode high-frequency single-phase transformerless PV inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13188–13199, Nov. 2021.
[47] Y. Jiang, Y. Shen, L. Shillaber, and T. Long, "Design of a SiC-based switched CCM/TCM inverter for high-speed machine drive with low PWM-Induced current ripple," in *Proc. IEEE Energy Convers. Congr. Expo.*, IEEE, 2020, pp. 5784–5789.
[48] G. Zhang, Y. Wu, J. Xu, and T. B. Soeiro, "iTCM-Operated three-phase three-wire voltage-source converter system featuring capacitor-split virtual ground connection," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9415–9429, Aug. 2024.



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