Enhancing Light-Power Efficiency and Achieving Wide-Range ZVS in MMC-Based DC Transformers by Varying AC-Link Voltage and Frequency

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***Abstract*—The modular multilevel converter-based dc transformers (MMC-DCT) are becoming essential parts of medium voltage dc applications. The implementation of zero-voltage switching (ZVS) is necessary for MMC-DCT to achieve higher switching frequencies, thereby improving power density and realizing lightweight. However, with conventional phase shift control, the ZVS range is very narrow. To solve this issue, a variable ac-link voltages and frequency control strategy is proposed, which is achieved by adjusting the number of constantly inserted or bypassed submodules (SMs) within a switching cycle. Meanwhile, the capacitor voltage-balancing algorithm is introduced. With this strategy, the ZVS range is extended over a wide power range. Moreover, since the switching loss of SMs and core loss of transformer are reduced, the efficiency of MMC-DCT is significantly improved at light power. Finally, the feasibility and effectiveness of the proposed control strategy is validated by experimental results.**

***Index Terms*—DC transformer (DCT), dual-active-bridge (DAB), modular multilevel converter (MMC), zero-voltage switching (ZVS).**

NOMENCLATURE

V_H	Voltage of the high-voltage side (HVS).
V_L	Voltage of the low-voltage side (LVS).
i_H	HVS current.
i_L	LVS current.
N_1	Number of LVS SMs per arm.
N_2	Number of HVS SMs per arm.
$x \in \{a, b, c, d\}$	Phase x, x can be a, b, c, or d.
$y \in \{u, l\}$	Upper arm and lower arm.
$z \in \{1, 2, 3 \ldots\}$	zth SM in an arm.
L_x	Self-inductance of the coupled inductor.
M_x	Mutual inductance of the coupled inductor.
T_1	Medium-frequency ac-link transformer.
$1:n$	Turns ratio between the primary and secondary sides.
L_T	Transformer leakage inductor.
L_r	Series connected inductor.
v_{ab}	Primary ac-link voltage.
v_{cd}	Secondary ac-link voltage.
v_{xy}	Upper/lower arm voltage of phase x.
i_{xy}	Upper/lower arm current of phase x.
i_p	Transformer primary current.
i_s	Transformer secondary current.
f_s	Switching frequency.
T_s	Switching cycle, $T_s = \frac{1}{f_s}$.
f_b	Switching frequency base.
V_b	Voltage base $V_b = V_L$.
P_b	Power base $P_b = \frac{V_b^2}{8L_k f_b}$.
P	Normalized transferred power.
f	Normalized switching frequency, $f = \frac{f_s}{f_b}$.
φ	Normalized PS between the ac-link voltages v_{ab} and v_{cd}.
θ	Normalized PS between the adjacent bypassed or inserted SMs.
k_1	Normalized amplitude of v_{ab}.
k_2	Normalized amplitude of v_{cd}.
θ_1	Normalized duration of v_{ab} falling or rising transition, $\theta_1 = k_1 N_1 \theta$.
θ_2	Normalized duration of v_{cd} falling or rising transition, $\theta_2 = k_2 N_2 \theta$.
M	Voltage gain $M = \frac{V_H}{nV_L}$.
I_{zvsp}	Current required to implement ZVS of primary side.
I_{zvss}	Current required to implement ZVS of secondary side.
v_{xyz}	Capacitor voltage of SM$_{xyz}$.
S_1	Upper switch of SM.
S_2	Lower switch of SM.
C	SM capacitor.
C_L	LVS dc-link capacitor.
C_H	HVS dc-link capacitor.
P_{rate}	Rated power.
sign()	Sign function.
floor()	Round toward negative infinity.

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I. INTRODUCTION

OWING to their higher efficiency, lower investment costs and elimination of reactive power compensation equipment, the medium voltage dc (MVDC) systems have received

increasing attention in many fields, such as dc collection of wind and photovoltaic farms [1], [2], urban future dc distribution networks [3], [4], and modern electric ships [5], [6].

In MVDC systems, the isolated bidirectional dc–dc converters, also known as dc transformers (DCT), are key equipments that interface different MVDC feeders. Dual-active-bridge (DAB) dc–dc converters are a promising choice due to the following excellent attributes: galvanic isolation, unified bidirectional power flow control, and inherent zero-voltage switching (ZVS) nature [7]. However, conventional two-level DAB converters cannot meet the voltage and current requirements of MVDC applications. Replacing the single switch with the series-connected power semiconductor devices is a feasible solution [8]. However, the extremely high dv/dt may threaten the insulation of transformers or inductors and also lead to serious electromagnetic interference (EMI) issues. In addition, it is a challenge to realize static and dynamic voltage balancing between the series-connected power switches. Cascaded modular DAB converters in input-series output-series manner are another effective method [9]. With proper input and output voltages sharing techniques, the MV terminal voltage can be evenly distributed to all the cells and thereby reducing the voltage stress on the devices. However, the insulation voltage more than the input and output port voltages is required for the high-frequency transformer in each cells, which increases costs and limits power density. In recent years, the modular multilevel converters (MMCs) have been successfully adopted in MV applications due to their flexible modularity and scalability, high efficiency, and enhanced reliability [10]. Hence, a topology combining MMC converter and DAB converter (called MMC-DCT) is proposed, in which the two MMCs are connected front-to-front with a centralized medium-frequency transformer [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. Various modulation methodologies are proposed for MMC-DCT, which can be roughly classified into sine-wave modulation (SIM) [11] and square-wave modulation (SQM) [14], [21], [22] according to the shape of the ac-link voltages. Due to the lower dc voltage utilization and power transmission capability of SIM compared to SQM, and the inability to guarantee ZVS with SIM, SQM is more suitable for MMC-DCT [16]. However, the ultra-high dv/dt stress on the transformer is produced by the ac-link voltages employing SQM, resulting in potential insulation breakdown. Therefore, trapezoidal-wave modulation (TRM) is proposed by sequentially bypassing/inserting submodules (SMs) at falling/rising edges of the ac-link voltages [12], [13], [15], [18], [19], [20]. With such modulation, dv/dt stress is significantly reduced, and the ac-link voltages can be approximately equivalent to a trapezoidal waveform.

In order to improve the power density of MMC-DCT, higher frequency has become a trend as it can reduce the size and weight of the transformers, inductors, and SM capacitors, especially in offshore wind power collection and delivery platforms [1], [23]. Therefore, it is necessary to implement ZVS to reduce switching loss and increase conversion efficiency. In [18], the modulation strategy based on phase shifted carrier is introduced to increase the equivalent switching frequency, thereby achieving lower passive component size. However, the SMs are frequently inserted and bypassed within half of the ac-link cycle, and ZVS is lost. In [12] and [13], actually, ZVS can only be satisfied in a relatively narrow region under heavy load. One reason is that, compared to traditional DAB converters, the range of ZVS is reduced by using TRM, and another reason is that the inherent circulating current in the arm current of MMC affects the achievement of ZVS. In [15], by inserting or bypassing constant SMs, the high- and low-level values of the ac-link voltages is controllable, providing a possible way to realize ZVS. Neverthless, ZVS operation range is still limited. In addition, the achievement of ZVS can eliminate severe reverse-recovery problem caused by the body diode of the switching devices, thereby avoiding serious EMI of SMs. Overall, a detailed analysis of the ZVS range should be conducted, taking into account the influence of TRM, and extended with an effective control strategy.

The capacitor voltage-balancing algorithm is essential for the normal operation of MMC-DCT. In [14], [21], and [22], automatic voltage-balancing of the SMs within one arm is realized by periodically swapping the predefined switching patterns, but ZVS is hard to be maintained. In [24], based on the sorted SM charge differences and voltages, the gate signals of SMs are reassigned to achieve balancing control. In [25], two novel algorithms are given to mitigate the low-frequency voltage ripple and avoid additional switching actions. Most of the existing balancing algorithms are proposed for the MMC-DCT with constant ac-link voltage amplitudes, where all SMs of an arm are inserted or bypassed during each switching cycle. For variable ac-link voltage amplitudes, although the capacitor voltage-balancing algorithm is discussed in [15], this algorithm is not applicable because the SMs with the lowest voltages will never participate in dynamic voltage balancing, and lacks experimental verification. Some literatures propose the MMC-based *LLC* and *LC* resonant converters for MVDC to low-voltage dc (LVDC) applications [26], [27], [28], [29], [30]. To adapt a wide voltage gain range, the amplitude of the ac-link voltage varies according to the MV side voltage, and is controlled by changing the number of SMs constantly inserted and bypassed in a switching cycle. However, with the proposed voltage-balancing methods, additional switch actions are introduced when the SMs are reassigned with new gate signals, resulting in potential ZVS loss.

The major contribution of this article is to propose a variable ac-link voltages and frequency (VAVF) control strategy for MMC-DCT. By adjusting the constantly inserted or bypassed SMs within a switching cycle, ZVS is guaranteed over a wide power range. In addition, with the proposed capacitor voltage-balancing algorithm, all SMs in one arm are dynamically charged and discharged and well balanced. Furthermore, since the ac-link voltages decrease as power decrease, the core loss of transformer is reduced as well. Due to the reduction in the number of dynamically inserted or bypassed SMs, the equivalent switching frequency of SMs can be reduced, thereby decreasing switching loss. Therefore, the efficiency is significantly improved at light power operation. The rest of this article is organized as follows. In Section II, the converter topology is introduced, and then five operating modes and ZVS range are analyzed. In Section III, the implementation of closed-loop control strategy along with capacitor voltage-balancing algorithm

TABLE I
NORMALIZED TRANSFERRED POWER AND PRIMARY-SIDE TRANSFORMER CURRENTS OF THE CONVERTER

Symbol	Modes 1 or 5	Modes 2 or 4	mode 3	
	$\varphi \in \left[\frac{\theta_1+\theta_2}{2}, 0.25\right] \cup \left[-0.25, -\frac{\theta_1+\theta_2}{2}\right]$	$\varphi \in \left(\frac{\lvert\theta_1-\theta_2\rvert}{2}, \frac{\theta_1+\theta_2}{2}\right) \cup \left(-\frac{\theta_1+\theta_2}{2}, -\frac{\lvert\theta_1-\theta_2\rvert}{2}\right)$	$\varphi \in \left[-\frac{\lvert\theta_1-\theta_2\rvert}{2}, \frac{\lvert\theta_1-\theta_2\rvert}{2}\right]$	
			$\theta_1 \le \theta_2$	$\theta_1 > \theta_2$
$i_p(\alpha)$	$\frac{2}{f}\left[(1-4\lvert\varphi\rvert-2\theta_1)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(1-4\lvert\varphi\rvert-2\theta_1)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(-\frac{4\varphi^2+4\theta_1\varphi+\theta_1^2}{\theta_2}+1-\theta_2)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(-4\varphi-2\theta_1+1)k_2M+(2\theta_1-1)k_1\right]$
$i_p(\beta)$	$\frac{2}{f}\left[(1-4\lvert\varphi\rvert+2\theta_1)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(-\frac{4\varphi^2-4\theta_1\lvert\varphi\rvert+\theta_1^2}{\theta_2}+1-\theta_2)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(-\frac{4\varphi^2-4\theta_1\varphi+\theta_1^2}{\theta_2}+1-\theta_2)k_2M+(2\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(4\varphi-2\theta_1+1)k_2M+(2\theta_1-1)k_1\right]$
$i_p(\gamma)$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+(4\lvert\varphi\rvert-2\theta_2-1)k_1\right]$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+\frac{k_1}{\theta_1}(4\varphi^2-4\theta_2\lvert\varphi\rvert+\theta_2^2)+(\theta_1-1)k_1\right]$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+(-4\varphi+2\theta_2-1)k_1\right]$	$\frac{2}{f}\left[(\frac{4\varphi^2-4\theta_2\varphi+\theta_2^2}{\theta_1}-1+\theta_1)k_1+(1-2\theta_2)k_2M\right]$
$i_p(\delta)$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+(4\lvert\varphi\rvert+2\theta_2-1)k_1\right]$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+(4\lvert\varphi\rvert+2\theta_2-1)k_1\right]$	$\frac{2}{f}\left[(1-2\theta_2)k_2M+(4\varphi+2\theta_2-1)k_1\right]$	$\frac{2}{f}\left[(\frac{4\varphi^2+4\theta_2\varphi+\theta_2^2}{\theta_1}-1+\theta_1)k_1+(1-2\theta_2)k_2M\right]$
P	$\frac{4k_1k_2M}{f}[2\varphi-4\lvert\varphi\rvert\varphi-\mathrm{sign}(\varphi)(\frac{\theta_1^2+\theta_2^2}{3})]$	$\frac{k_1k_2M}{f}[\frac{8}{3\theta_1\theta_2}\lvert\varphi\rvert\varphi^3-\frac{16\theta_1+16\theta_2}{3\theta_1\theta_2}\varphi^3+(\frac{4\theta_1^2+4\theta_2^2}{\theta_1\theta_2}-8)\lvert\varphi\rvert\varphi$ $+(-\frac{4\theta_1^3+4\theta_2^3}{3\theta_1\theta_2}+8-4\theta_1-4\theta_2)\varphi$ $+sign(\varphi)(\frac{\theta_2^4-4\theta_1\theta_2^3-4\theta_1^3\theta_2+\theta_1^4}{6\theta_1\theta_2}+\theta_1\theta_2)]$	$\frac{8k_1k_2\varphi M}{3\theta_2 f}(-4\varphi^2-3\theta_2^2+3\theta_2-\theta_1^2)$	$\frac{8k_1k_2\varphi M}{3\theta_1 f}(-4\varphi^2-3\theta_1^2+3\theta_1-\theta_2^2)$

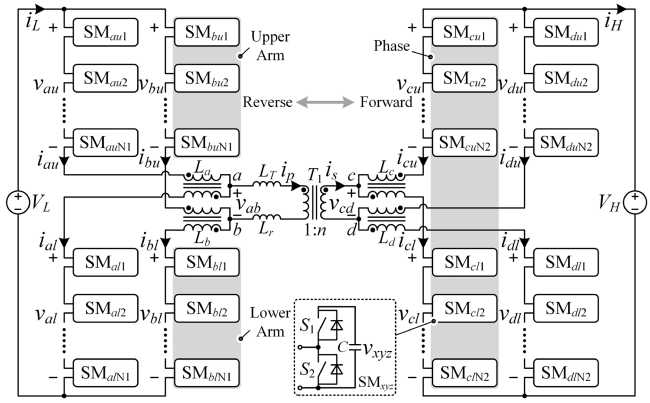


Fig. 1. Topology of the MMC-DCT.

TABLE II
ZVS CONSTRAINTS

Primary side	$i_{zvs1} = \frac{1}{2}[\max(i_p(\alpha), i_p(\beta)) + P] < -I_{zvsp}$
	$i_{zvs2} = \frac{1}{2}[-\max(i_p(\alpha), i_p(\beta)) + P] > I_{zvsp}$
Secondary side	$i_{zvs3} = \frac{1}{2n}[-\min(i_p(\gamma), i_p(\delta)) - \frac{P}{M}] < -I_{zvss}$
	$i_{zvs4} = \frac{1}{2n}[\min(i_p(\gamma), i_p(\delta)) - \frac{P}{M}] > I_{zvss}$

is presented. After that, the experimental results are provided in Section IV to validate the theoretical analysis. In Section V, discussion and comparison of different converter topologies and strategies are presented. Finally, Section VI concludes this article.

II. BASIC STRUCTURE AND OPERATING PRINCIPLE

A. Converter Topology

As shown in Fig. 1, the MMC-DCT consists of four phases, where each phase is composed of one coupled inductor as well as two arms named the upper arm and the lower arm, respectively. The total equivalent ac-link inductor L_k referred to the primary side can be calculated by

$$L_k = L_T + L_r + \frac{1}{2}(L_a - M_a + L_b - M_b) + \frac{1}{2n^2}(L_c - M_c + L_d - M_d). \quad (1)$$

B. Operating Modes

Depending on the temporal sequence of the falling and rising edges of v_{ab} and v_{cd}, five operating modes can be distinguished for bidirectional power flow, as illustrated in Fig. 2. The boundaries between these modes are specified in Table I, and the expressions for P and i_p are also summarized in Table I. Modes 1 and 2 operate under forward power flow (i.e., from LVS to HVS), whereas modes 4 and 5 are used under reverse power flow (i.e., from HVS to LVS). Mode 5 serves as a transitional mode between forward and reverse power flow. In addition, modes 1 (i.e., $\varphi \in [\frac{\theta_1+\theta_2}{2}, 0.25]$) and 5 (i.e., $\varphi \in [-0.25, -\frac{\theta_1+\theta_2}{2}]$) correspond to heavy-load operating conditions, whereas modes 2 (i.e., $\varphi \in (\frac{|\theta_1-\theta_2|}{2}, \frac{\theta_1+\theta_2}{2})$) and 4 (i.e., $\varphi \in (-\frac{\theta_1+\theta_2}{2}, -\frac{|\theta_1-\theta_2|}{2})$) are associated with light-load operational states. It should be noted that k_1 and k_2 are variable in all modes.

Similar to the DAB converters, the transmitted power of the MMC-DCT can be controlled by the phase shift (PS) φ between the ac-link voltages v_{ab} and v_{cd}. However, due to the different inserted or bypassed sequence of the SMs in one arm, the ac-link voltages of the MMC-DCT approximate trapezoidal waveforms instead of square waveforms, which complicate the analysis of ZVS and affects the ZVS range. In addition, benefiting from the variable amplitude (i.e., k_1 and k_2) of the ac-link voltages, MMC-DCT has two more control degrees of freedom compared to DAB converters, which can be utilized to further optimize the converter.

C. ZVS Range

ZVS constraints are listed in Table II. $i_{\mathrm{zvs1-4}}$ are the currents at ZVS boundaries, which are shown in Fig. 3, for bidirectional power flow. Taking phase a (c) upper arm SMs as an example, i_{zvs1} (i_{zvs3}) represents the ZVS boundary when they are bypassed (i.e., S_1 turns OFF, S_2 turns ON), and i_{zvs2} (i_{zvs4}) represents the ZVS boundary when they are inserted (i.e., S_2 turns OFF, S_1 turns ON). As can be seen in Fig. 3, for the forward power direction, it is difficult for the phase $a(c)$ upper arm SMs to

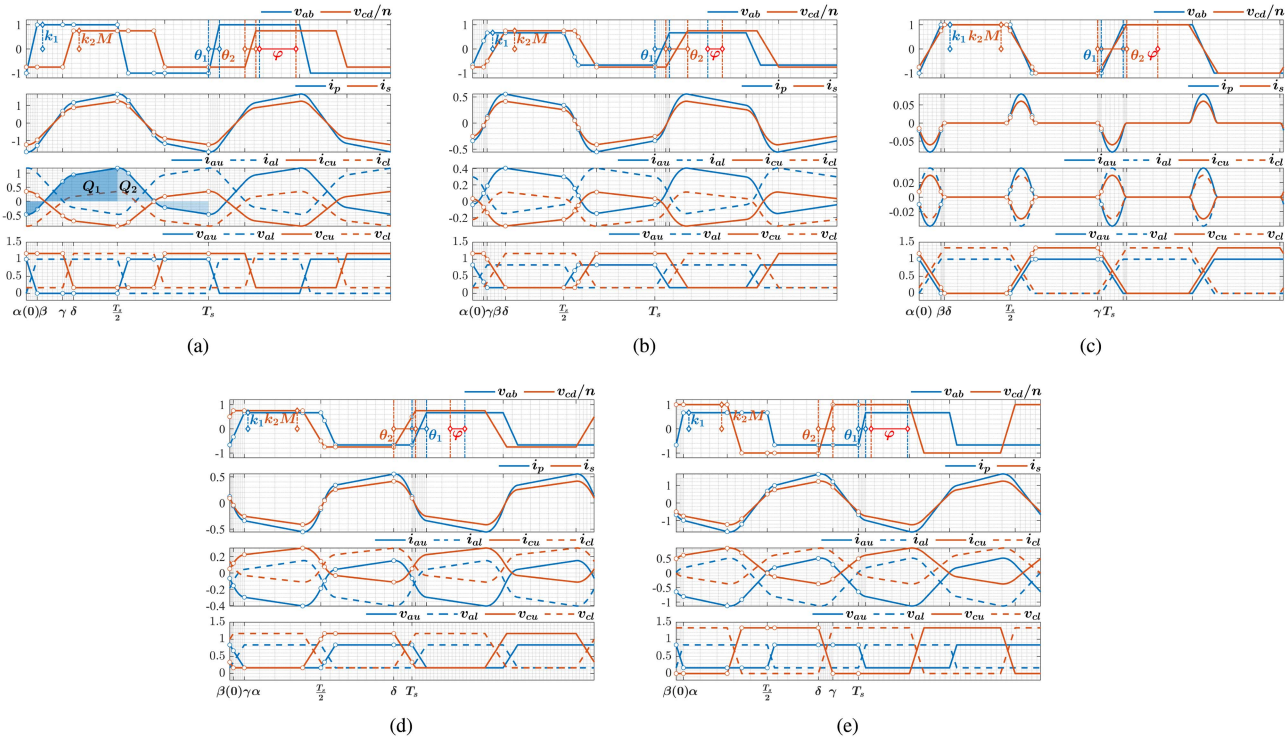


Fig. 2. Ideal voltage and current waveforms for different modes, $N_1 = 6$ and $N_2 = 8$. (a) Mode 1: $\varphi = 0.2$, $k_1 = 1$, $k_2 = 3/4$, $f = 1$, and $\theta = 0.01$. (b) Mode 2: $\varphi = 0.08$, $k_1 = 2/3$, $k_2 = 3/4$, $f = 1$, and $\theta = 0.02$. (c) Mode 3: $\varphi = 0$, $k_1 = 1$, $k_2 = 1$, $f = 1$, and $\theta = 0.02$. (d) Mode 4: $\varphi = -0.08$, $k_1 = 2/3$, $k_2 = 3/4$, $f = 1$, and $\theta = 0.02$. (e) Mode 5: $\varphi = -0.2$, $k_1 = 2/3$, $k_2 = 1$, $f = 1$, and $\theta = 0.01$.

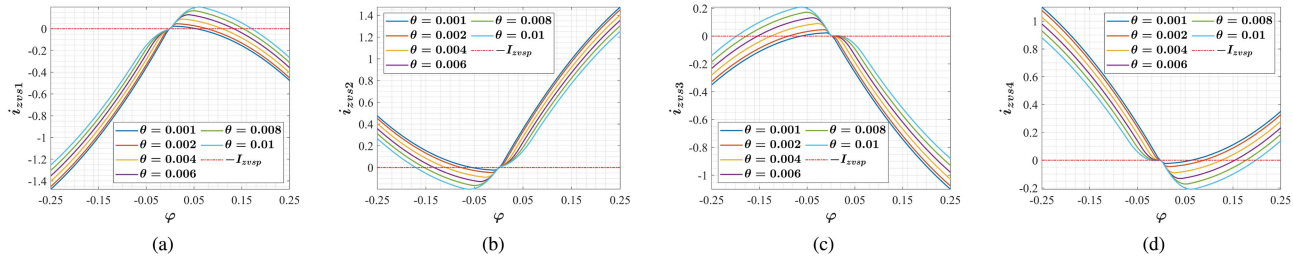


Fig. 3. Currents at ZVS boundaries with different θ, $k_1 = 1$, $k_2 = 1$, $f = 1$, $M = 1$, $N_1 = 6$, and $N_2 = 8$. (a) i_{zvs1}. (b) i_{zvs2}. (c) i_{zvs3}. (d) i_{zvs4}.

realized ZVS when they are bypassed (inserted). For the reverse power direction, it is difficult for the phase $a(c)$ upper arm SMs to realized ZVS when they are inserted (bypassed). The reason is the presence of dc circulating component in the arm current.

The ZVS range at different powers is illustrated in Fig. 4. In Fig. 4(a), it can be seen that the ZVS range is narrowed with increased θ. ZVS cannot be achieved within 93.7% power range for $\theta = 0.01$, as well as 44.1% power range for $\theta = 0.001$. Since θ_1 and θ_2 are increased with the increase of SM quantity, ZVS range is very limited. In addition, it should be mentioned that I_{zvsp} and I_{zvss} are assumed to be 0 in the analysis. However, their values are required to be greater than 0 to sufficiently charge or discharge the parasitic capacitor of the power semiconductor devices in practice, which means that the ZVS range will be narrower. As shown in Fig. 4(b), if I_{zvsp} and I_{zvss} are 0.15, then ZVS is lost within 89.5% power range even for $\theta = 0.001$. Consequently, it is worth to propose feasible control strategy to extend the ZVS range of the MMC-DCT, thereby reducing switching loss.

III. Closed-Loop Control Strategy

A. Optimized Control Variables

For a certain power, the transformer currents are increased as the ac-link voltages are decreased, while the dc circulating component in the arm current remains unchanged. Therefore, the amplitude of the ac-link voltages (i.e., k_1 and k_2) can be regulated to broaden ZVS region. However, the improvement of ZVS range is limited because k_1 and k_2 are discontinuous (i.e., $k_1 \in \{1, \frac{N_1-2}{N_1}, \frac{N_1-2}{N_1}, \ldots\}$ and $k_2 \in \{1, \frac{N_2-2}{N_2}, \frac{N_2-2}{N_2}, \ldots\}$). Hence, the switching frequency f is also selected as a control variable. The flowchart illustrating the procedure for obtaining the optimized control variables is presented in Fig. 5. The control variables of all modes are $x_c = (k_1, k_2, \varphi, f)$. First of all, the

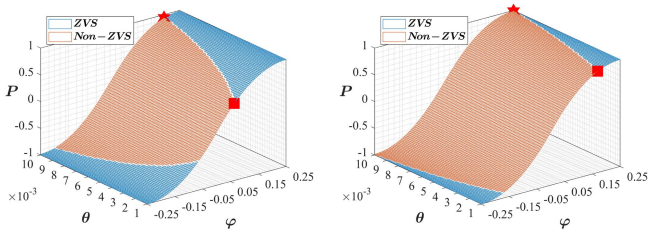


Fig. 4. ZVS range at different powers, $k_1 = 1$, $k_2 = 1$, $f = 1$, $N_1 = 6$, $N_2 = 8$, and $M = 1$. (a) ★: (0.194,0.01,0.937), ■: (0.0631,0.001,0.441), $I_{\text{zvsp}} = 0$, and $I_{\text{zvss}} = 0$. (b) ★: (0.25,0.01,0.987), ■: (0.139,0.001,0.895), $I_{\text{zvsp}} = 0.15$, and $I_{\text{zvss}} = 0.15$.

transmitted power reference P^* and other relevant parameters are initialized. Secondary, since k_1 and k_2 are discrete variables, they serve as the top-level nested loops to cover all possible combinations. Due to the increase in transformer currents to achieve ZVS, the square of the primary rms current (i.e., I^2_{prms}) is designed as the cost function to reduce conduction loss (i.e., $f(x_c) = I^2_{\text{prms}}$), which is expressed as (2) shown at the bottom of this page. For each mode, an optimizer (i.e., "fmincon" function in MATLAB) is employed to find the minimum of the cost function subject to the following constraints.

1) Nonlinear equality $ceq(x_c) = 0$*:* $P(x_c) - P^* = 0$, where the expressions for P^* are provided in the last row of Table I.

2) Nonlinear inequalities $c(x_c) \le 0$*:* ZVS constraints, as detailed in Tables I and II.

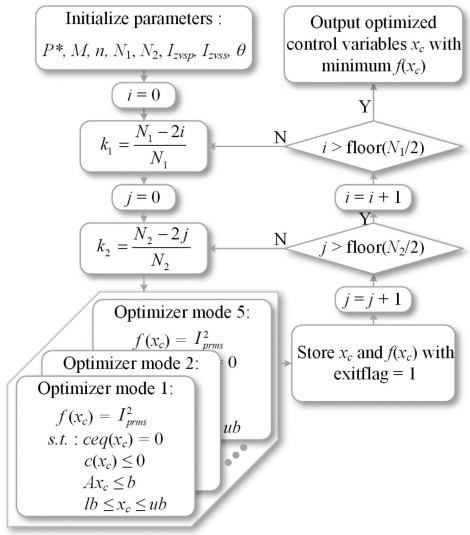


Fig. 5. Flowchart for obtaining optimized control variables.

3) Linear inequalities $Ax \le b$*:* mode boundaries, given in the first row of Table I.

4) The upper and lower limits of variables $lb \le x_c \le ub$*:* $f_{\min} \le f \le f_{\max}$, where $f_{\min} = 0.6$ and $f_{\max} = 1.25$.

For each mode-specific optimizer, the feasible solution x_c and its cost function value $f(x_c)$ that satisfy the constraints functions (i.e., exitflag $= 1$) are stored. Finally, the optimized control variables x_c with minimum $f(x_c)$ are selected and output as the final solution for the target power P^*. Based on the procedure

$$
\begin{aligned}
I^2_{\text{prms}} &= \frac{1}{T}\int_0^T i_p^2 dt \\
&= \begin{cases}
\frac{4}{15f^2}\left\{\begin{matrix}(16\theta_2^3 - 20\theta_2^2 + 5)k_2^2M^2 + \\ 10[24\varphi^2 - 32\varphi^2|\varphi| - 8(\theta_1^2+\theta_2^2)|\varphi| + 2(\theta_1^2+\theta_2^2) - 1]k_1k_2M \\ +(16\theta_1^3 - 20\theta_1^2 + 5)k_1^2\end{matrix}\right\}, \varphi \in \left[\frac{\theta_1+\theta_2}{2}, 0.25\right] \cup \left[-0.25, -\frac{\theta_1+\theta_2}{2}\right] \\
\frac{4}{15\theta_1\theta_2 f^2}\left\{\begin{matrix}(16\theta_2^3 - 20\theta_2^2 + 5)k_2^2M^2\theta_1\theta_2 + \\ \left[\begin{matrix}32\varphi^4|\varphi| - 80(\theta_1+\theta_2)\varphi^4 \\ +80(\theta_1^2+\theta_2^2-2\theta_1\theta_2)\varphi^2|\varphi| \\ +40\left(6\theta_1\theta_2 - 3\theta_1^2\theta_2 - \theta_2^3 - 3\theta_1\theta_2^2 - \theta_1^3\right)\varphi^2 \\ +10\left(\theta_2^4 - 4\theta_1\theta_2^3 + 6\theta_1^2\theta_2^2 - 4\theta_1^3\theta_2 + \theta_1^4\right)|\varphi| \\ +10(2-\theta_1)\theta_1\theta_2^3 - (\theta_2+5\theta_1)\theta_2^4 - 10\theta_1^3\theta_2^2 \\ +5(4\theta_1^3 - \theta_1^4 - 2\theta_1)\theta_2 - \theta_1^5\end{matrix}\right]k_1k_2M \\ +(16\theta_1^3 - 20\theta_1^2 + 5)k_1^2\theta_1\theta_2\end{matrix}\right\}, \varphi \in \left(\frac{|\theta_1-\theta_2|}{2}, \frac{\theta_1+\theta_2}{2}\right) \cup \left(-\frac{\theta_1+\theta_2}{2}, -\frac{|\theta_1-\theta_2|}{2}\right) \\
\frac{4}{15\theta_2 f^2}\left\{\begin{matrix}(16\theta_2^3 - 20\theta_2^2 + 5)k_2^2M^2\theta_2 + \\ \left[\begin{matrix}80(3\theta_2 - 3\theta_2^2 - \theta_1^2)\varphi^2 - 160\varphi^4 \\ +10(2\theta_2 - \theta_2^2 - 2\theta_1^2)\theta_2^2 - 2\theta_1^4 + 10(2\theta_1^2 - 1)\theta_2\end{matrix}\right]k_1k_2M \\ +(16\theta_1^3 - 20\theta_1^2 + 5)k_1^2\theta_2\end{matrix}\right\}, \varphi \in \left[-\frac{|\theta_1-\theta_2|}{2}, \frac{|\theta_1-\theta_2|}{2}\right] \text{ and } \theta_1 \le \theta_2 \\
\frac{4}{15\theta_1 f^2}\left\{\begin{matrix}(16\theta_2^3 - 20\theta_2^2 + 5)k_2^2M^2\theta_1 + \\ \left[\begin{matrix}80(3\theta_1 - 3\theta_1^2 - \theta_2^2)\varphi^2 - 160\varphi^4 \\ +20(\theta_1 - \theta_1^2)\theta_2^2 - 2\theta_2^4 + 10(2\theta_1^2 - \theta_1^3 - 1)\theta_1\end{matrix}\right]k_1k_2M \\ +(16\theta_1^3 - 20\theta_1^2 + 5)k_1^2\theta_1\end{matrix}\right\}, \varphi \in \left[-\frac{|\theta_1-\theta_2|}{2}, \frac{|\theta_1-\theta_2|}{2}\right] \text{ and } \theta_1 > \theta_2.
\end{cases}
\end{aligned}
\tag{2}
$$

TABLE III
SYSTEM PARAMETERS IN EXPERIMENTS

Symbol	Value	Symbol	Value
V_L	300 V	V_H	400 V
L_a	$58.2\mu H$	M_a	$39.3\mu H$
L_c	$57.9\mu H$	M_c	$39.4\mu H$
L_T	$16.6\mu H$	$1:n$	3 : 4
L_r	$226.7\mu H$	f_b	10 kHz
P_{rate}	1 kW	N_1	6
N_2	8	C	$260\mu F$
C_L	$375\mu F$	C_H	$325\mu F$

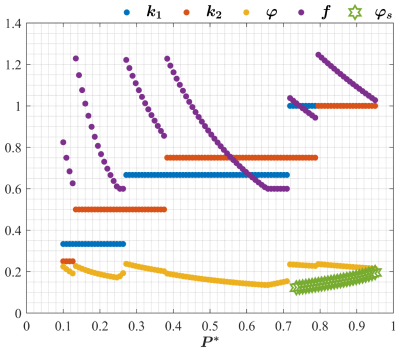


Fig. 6. Optimized control variables k_1, k_2, f, and φ.

shown in Fig. 5 and the system parameters in Table III, the optimized control variables are shown in Fig. 6, where I_{zvsp} and I_{zvss} are set to be 0.15, and θT_s is set to be 0.5 μs. It can be observed that the amplitude of the ac-link voltage decreases with the decrease of power, and ZVS cannot be maintained within only 10% of the power range. In addition, since ZVS is difficult to guarantee for modes 2–4, MMC-DCT operates in mode 1 for forward power flow, and vice versa in mode 5.

B. Capacitor Voltage-Balancing Algorithm for Varying AC-Link Voltage

The capacitor voltage-balancing algorithm for each arm in the LVS can be derived in a similar way. Therefore, taking mode 1 as an example, as shown in Fig. 2(a), the total charge of the upper arm SMs in phase a can be calculated by (3) and (4) for $t=(0,\frac{T_s}{2})$ and $t=(\frac{T_s}{2},T_s)$, respectively

$$\begin{aligned} Q_1 = &-\frac{1}{f^2}\Big[2k_2M(k_1+1)(2\varphi^2-\varphi)+k_2M\theta_1(4\varphi-1)\\ &+\frac{1}{3}(k_1+1)k_2M\theta_2^2+\frac{1}{3}(k_1+3)k_2M\theta_1^2+k_1\theta_1\\ &-\frac{4}{3}k_1\theta_1^2\Big] \end{aligned} \tag{3}$$

$$\begin{aligned} Q_2 = &-\frac{1}{f^2}\Big[2k_2M(k_1-1)(2\varphi^2-\varphi)-k_2M\theta_1(4\varphi-1)\\ &+\frac{1}{3}(k_1-1)k_2M\theta_2^2+\frac{1}{3}(k_1-3)k_2M\theta_1^2-k_1\theta_1\\ &+\frac{4}{3}k_1\theta_1^2\Big] \end{aligned} \tag{4}$$

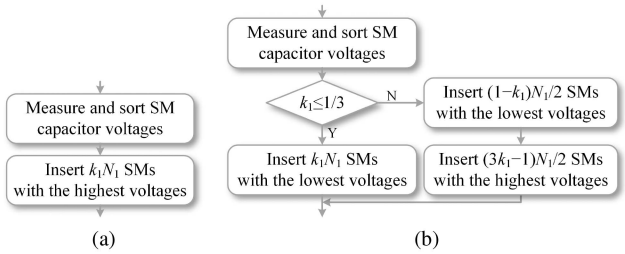


Fig. 7. Flowchart of the capacitor voltage-balancing algorithm at $t=\frac{T_s}{2}$. (a) conventional [15]. (b) modified.

where Q_1 and Q_2 are normalized by the $Q_b=\frac{V_L}{8L_kf_b^2}$. According to the optimized control variables, $Q_1>0$, and $Q_2<0$. As a result, the SMs in inserted state are charged during $(0,\frac{T_s}{2})$ and discharged during $(\frac{T_s}{2},T_s)$. In order to balance the capacitor voltages, at $t=0$, the k_1N_1 SMs with the highest voltages among the $\frac{(k_1+1)N_1}{2}$ SMs, which are in inserted state, should be bypassed [15]. Since $i_{ap}(0)<0$, the order of being bypassed is that those with the lowest voltages among the k_1N_1 SMs are bypassed first. Similarly, at $t=\frac{T_s}{2}$, the k_1N_1 SMs with highest voltages among the $\frac{(k_1+1)N_1}{2}$ SMs, which are in bypassed state, should be inserted, and those with the lowest voltages among the k_1N_1 SMs are inserted first, as shown in Fig. 7(a). However, according to the previous analysis, $\frac{(1-k_1)N_1}{2}$ SMs with the lowest voltages will never be inserted, so the capacitor voltages cannot be balanced between the N_1 SMs. The charge for $t=(0,T_s)$ can be obtained by

$$\begin{aligned} Q=Q_1+Q_2&=-\frac{2k_1k_2M}{f^2}\left[4\varphi^2-2\varphi+\frac{1}{3}\left(\theta_1^2+\theta_2^2\right)\right]\\ &=\frac{I_L}{2f}. \end{aligned} \tag{5}$$

Since $I_L>0$ and $Q>0$, the inserted SMs are charged for the entire switching cycle, which means that the SMs with the lowest voltage should be inserted for charging to participate in voltage balancing. Hence, the flowchart of the modified capacitor voltage-balancing algorithm is shown in Fig. 7(b).

Step 1: Measure and sort SM capacitor voltages in an arm.

Step 2: At $t=\frac{T_s}{2}$, k_1N_1 SMs need to be inserted, and $\frac{(1-k_1)N_1}{2}$ SMs are charged in the next switching cycle. If $k_1N_1\le\frac{(1-k_1)N_1}{2}$, then the k_1N_1 SMs with the lowest voltages should be inserted. Otherwise, the $\frac{(1-k_1)N_1}{2}$ SMs with the lowest voltages should be inserted first, followed by the $\frac{(3k_1-1)N_1}{2}$ SMs with the highest voltages.

For the HVS SMs, the capacitor voltage-balancing algorithm is the same as that proposed in [15] because all SMs in an arm have the opportunity to be inserted, and they can be well balanced. In addition, due to the symmetrical characteristics of DAB, the situation of reverse power flow (i.e., mode 5) is not further elaborated.

The optimization process, detailed in Section III-A, is designed to be performed offline once for a given converter design, and the offline optimization for the entire operating range is

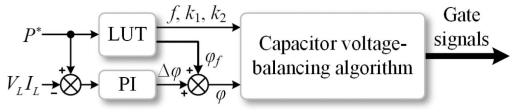


Fig. 8. Closed-loop implementation of the proposed control strategy.

completed in approximately a few minutes on a standard PC. The resulting optimal sets of control variables (φ, f, k_1, and k_2) for different power levels are stored in a lookup table (LUT) within the digital controller's memory. The LUT is structured as a 1×100 array for each control variable (φ, f, k_1, and k_2), corresponding to 100 uniformly spaced power reference points spanning the full operating range from 0.1 to 0.95 per unit (p.u.) The lower limit (0.1 p.u.) is set to exclude extremely light-load conditions where the proposed modulation strategy is not necessary. The upper limit (0.95 p.u.) is chosen to maintain a conservative safety margin below the converter's absolute maximum power rating (1.0 p.u.), ensuring reliable operation under all conditions. The total memory footprint of the LUT is minimal, making it suitable for implementation in embedded systems. During real-time operation, the controller simply accesses the precomputed values according to the desired power reference P^* from this LUT, and a computationally lightweight 1-D previous neighbor interpolation (the interpolated value at a query point is the value at the previous sample grid point) is applied in real time. This approach ensures that the computational burden on the real-time controller is negligible, requiring only a few microseconds per execution cycle. The closed-loop implementation of the proposed control strategy is shown in Fig. 8. The control variables are directly obtained from the LUT. A proportional–integral controller is adopted to regulated the LVS power, and the output of it $\Delta\varphi$ plus φ_f is the PS angle φ of the ac-link voltages. Finally, the bypassed or inserted sequence of SMs is determined by the capacitor voltage-balancing algorithm, and then the gate signals can be allocated.

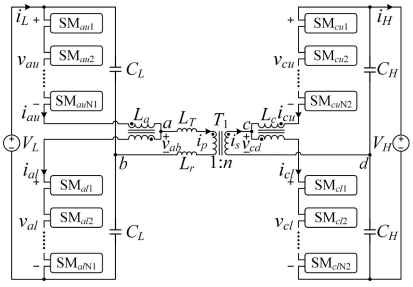
IV. Experimental Results

A. Prototype

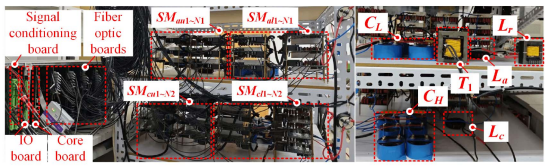
A lab-scale prototype is established to verify the performance of the proposed control strategy, and the schematic of it is illustrated in Fig. 9. In the experiment, both the primary and secondary sides of MMC-DCT are composed of single-phase MMC, and its characteristics are equivalent to those of two-phase MMC. The system parameters are summarized in Table III. The control algorithms are implemented by a TMS320F28379 DSP and an EP4CE22F17 FPGA, which are integrated on the core board. The controller of each SM is an EP4CE6E22 FPGA, which receives gate signals from the fiber optic boards, and send back the monitored capacitor voltages and real-time states.

B. Operating Waveforms and ZVS Conditions

Fig. 10 shows the experimental results with the proposed VAVF control. As can be observed, the amplitudes of the ac-link



(a)



(b)

Fig. 9. (a) Schematic of the laboratory prototype. (b) Photograph of the laboratory prototype.

voltages decrease as the transmitted power decreases. θ is set as 500 ns. In Fig. 10(a), $P = 1$ p.u., since $k_1 = 1$ and $k_2 = 1$, and v_{al} and v_{cl} are trapezoidal waveforms with six and eight steps, respectively. Within one switching cycle, all SMs in the same arm are completely bypassed or inserted. For $P = 0.8$ p.u., in Fig. 10(b), $k_1 = 1$, $k_2 = 3/4$, and $f = 1.025$, and v_{al} and v_{cl} are trapezoidal waveforms with six steps. During the rising transition of v_{cl}, six SMs of HVS lower arm should be inserted among the seven SMs in bypassed state, and during the falling transition of v_{cl}, six SMs should be bypassed among the seven SMs in inserted state. For $P = 0.12$ p.u., in Fig. 10(f), $k_1 = 1/3$, $k_2 = 1/4$, and $f = 0.750$, and v_{al} and v_{cl} are trapezoidal waveforms with two steps. The maximum values of v_{al} and v_{cl} are 200 V and 250 V, and their minimum values are 100 V and 150 V, respectively. The amplitude and frequency of the ac-link voltages in the experiment agree well with the theoretical analysis and Fig. 6.

The upper arm and lower arm SM capacitor voltages of primary and secondary sides are illustrated in Fig. 11(a) and (b). It can be concluded that the SM capacitor voltages are stabilized at the rated value of 50 V and well balanced at different transmitted power.

Figs. 12 and 13 show the ZVS conditions with VAVF control. v_{ds1} (v_{ds2}) and v_{gs1} (v_{gs2}) are the voltage across S_1 (S_2) and gate driving voltages, respectively. In Fig. 12(a), i_{al} is positive during the rising transition of v_{al}. ZVS of the first and last inserted SMs is realized because the drain–source voltage is decreased to zero before the gate driving voltage is higher than the threshold voltage. In Fig. 12(b), i_{cl} is negative during the falling transition of v_{cl}. ZVS of the first and last bypassed SMs is achieved. In Fig. 13, compared with conventional PS control, the ac-link voltages is reduced, thereby increasing ac-link currents. As a results, although the transmitted power is small (0.12 p.u.), ZVS can still be guaranteed. In addition, the experimental results employing conventional PS control are given in Fig. 14. In

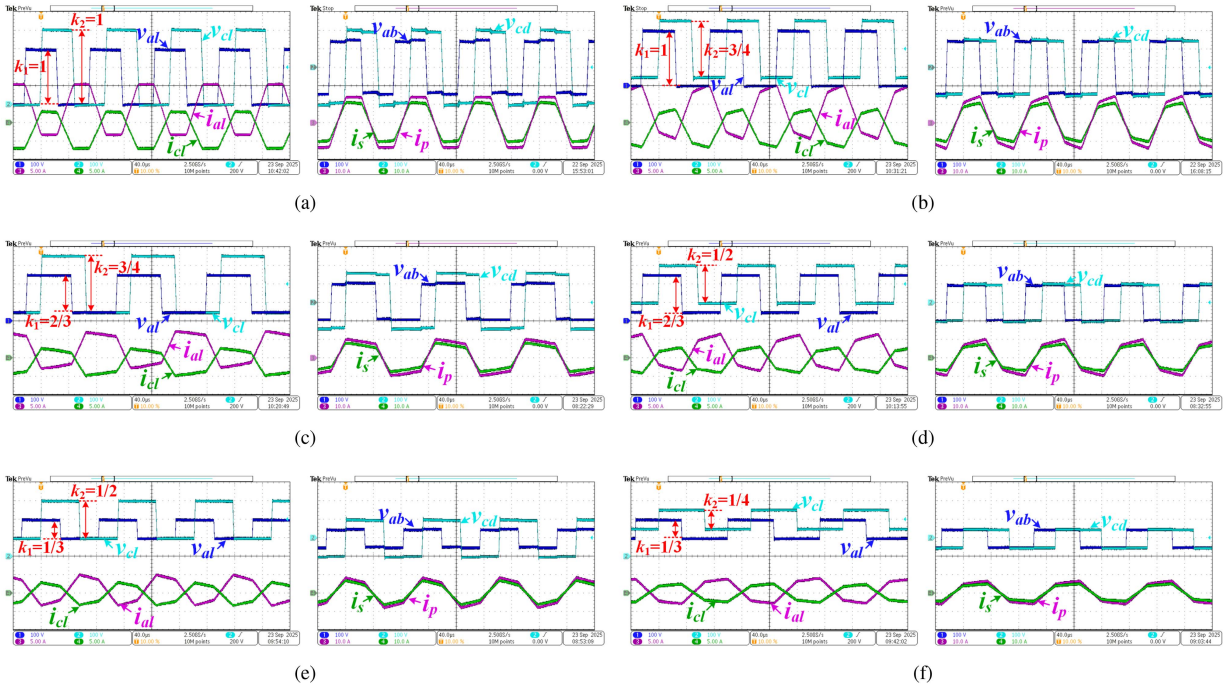


Fig. 10. Experimental results with VAVF control at different transmitted powers, lower arm voltages v_{xl}, lower arm currents i_{xl}, ac-link voltages v_{ab} and v_{cd}, and ac-link currents i_p and i_s. (a) 1 p.u., $k_1 = 1$, $k_2 = 1$, and $f = 1.071$. (b) 0.8 p.u., $k_1 = 1$, $k_2 = 3/4$, and $f = 1.025$. (c) 0.6 p.u., $k_1 = 2/3$, $k_2 = 3/4$, and $f = 0.771$. (d) 0.4 p.u., $k_1 = 2/3$, $k_2 = 1/2$, and $f = 0.879$. (e) 0.2 p.u., $k_1 = 1/3$, $k_2 = 1/2$, and $f = 0.899$. (f) 0.12 p.u., $k_1 = 1/3$, $k_2 = 1/4$, and $f = 0.750$.

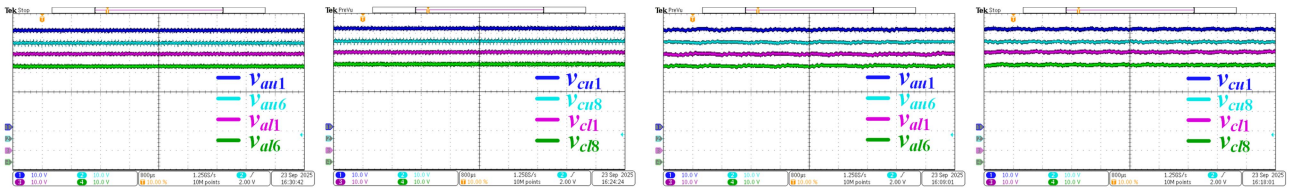


Fig. 11. SM capacitor voltages waveforms of phase a v_{ayz} and phase c v_{cyz} at different transmitted powers. (a) 1 p.u. (b) 0.12 p.u.

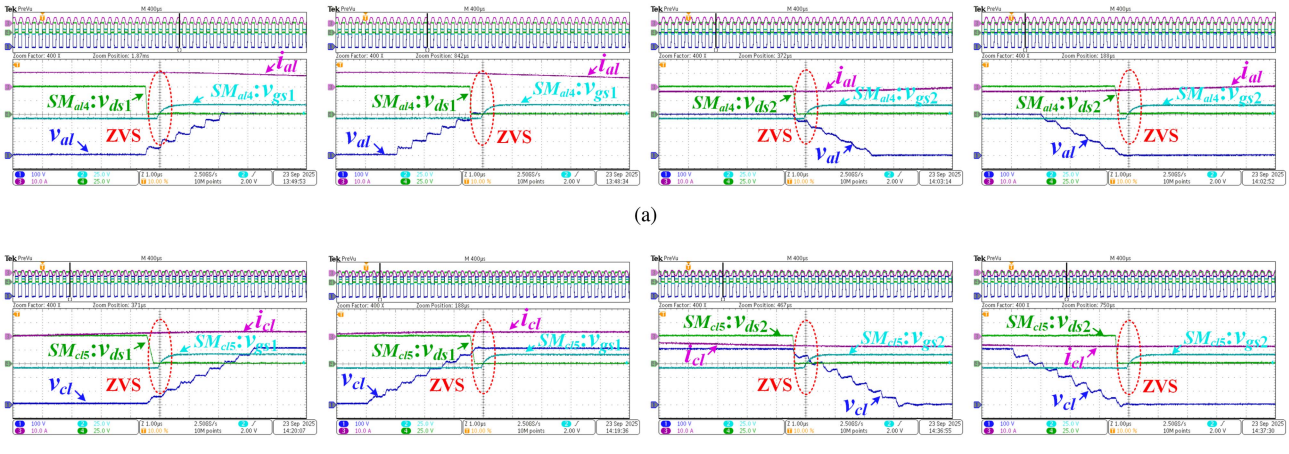


Fig. 12. ZVS conditions with VAVF control at 1 p.u. power, lower arm voltages v_{xl}, lower arm currents i_{xl}, drain–source voltages of S_1 (v_{ds1}) and S_2 (v_{ds2}), gate driving voltages of S_1 (v_{gs1}) and S_2 (v_{gs2}). (a) LVS. (b) HVS.

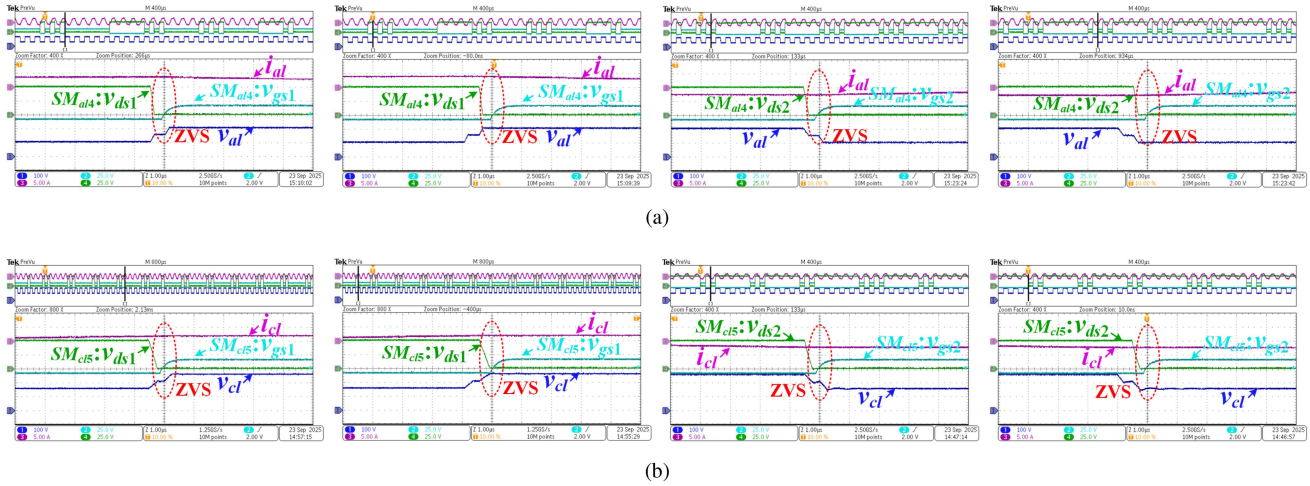


Fig. 13. ZVS conditions with VAVF control at 0.12 p.u. power, lower arm voltages v_{xl}, lower arm currents i_{xl}, drain–source voltages of S_1 (v_{ds1}) and S_2 (v_{ds2}), gate driving voltages of S_1 (v_{gs1}) and S_2 (v_{gs2}). (a) LVS. (b) HVS.

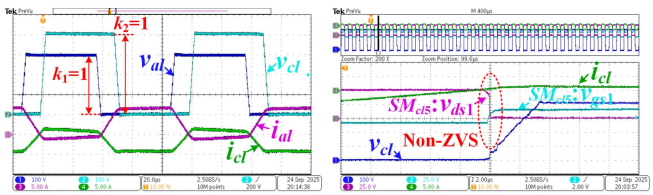


Fig. 14. Typical experimental operating waveforms and ZVS conditions with conventional PS control at 0.8 p.u. power, lower arm voltages v_{xl}, lower arm currents i_{xl}, drain–source voltage (v_{ds1}) and gate driving voltage (v_{gs1}) of S_1.

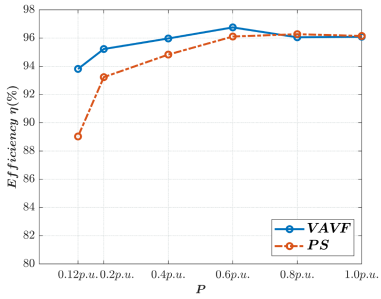


Fig. 15. Conversion efficiency of VAVF and PS control.

comparison with Fig. 10(b), the current i_{cl} is insufficient to fully charge and discharge the junction capacitance of the switches, resulting in a loss of ZVS. Overall, the experimental results demonstrate that ZVS can be achieved with VAVF over a wide power range.

C. Conversion Efficiency and Loss Breakdown

The conversion efficiency of VAVF and PS control is shown in Fig. 15. Compared with PS control, the efficiency is significantly improved under light power operation, but slightly reduced under heavy power operation. It is worth mentioned that the MV DCT are normally operating for a long time under light power

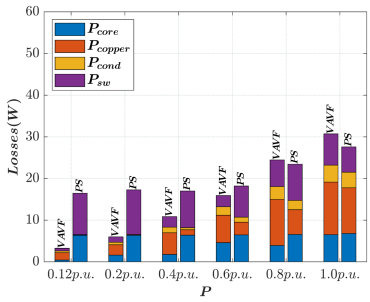


Fig. 16. Major loss breakdown.

conditions [31], [32]. Therefore, improving the efficiency under light power is necessary in practical MV applications.

To investigate the characteristics of the proposed VAVF control, major loss breakdown is given in Fig. 16, including the core loss of transformer and series connected inductor P_{core}, the copper losses of transformer, series connected inductor and arm inductors P_{copper}, as well as the conduction loss P_{cond} and switching loss P_{sw} of SMs. It should be noted that the core loss of arm inductors is relatively small due to coupling effects and can be neglected. As can be observed, the ac-link currents are increased to ensure wide power range ZVS implementation, thereby increasing conduction loss and copper loss. Consequently, the efficiency is reduced under heavy power. In addition, the efficiency of VAVF control can be further enhanced by adopting transformer and inductors with lower resistance. For switching loss, turn-ON loss can be eliminated owing to ZVS realization. Furthermore, for instance, at $P = 0.12$ p.u., only 2 out of 6 (8) SMs on the LVS (HVS) are bypassed or inserted within one switching cycle. This means that the equivalent switching frequency of SMs is reduced by 2/3 (3/4), and thus switching loss is reduced. Since the ac-link voltages decrease as the power decreases, the flux density ΔB is significantly reduced, and core loss of the transformer is reduced.

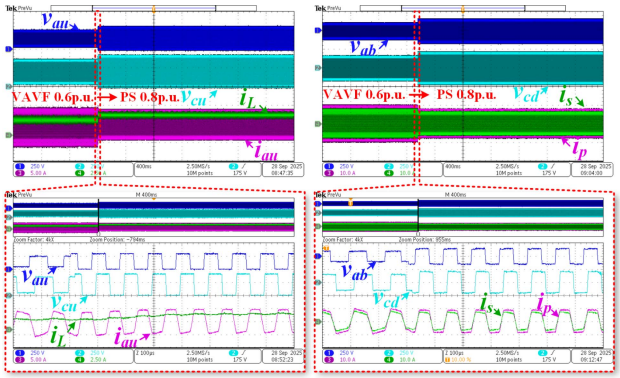


Fig. 17. Seamless transition from the VAVF control (0.6 p.u., $k_1 = 2/3$, $k_2 = 3/4$, and $f = 0.771$) to PS control (0.8 p.u., $k_1 = 1$, $k_2 = 1$, and $f = 1$).

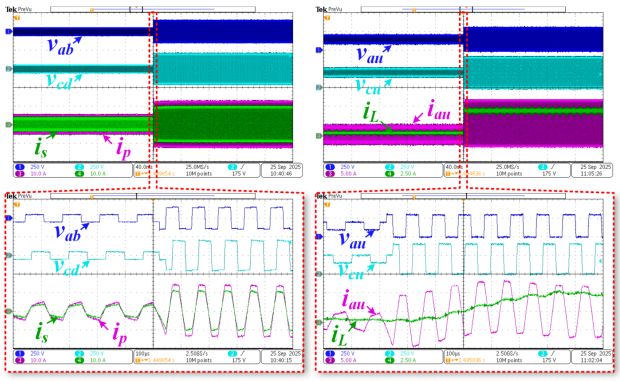


Fig. 18. Dynamic response from 0.12 to 1 p.u. power with VAVF control.

Besides, efficiency optimization over the entire power range can be achieved by combining VAVF control for light loads and PS control for heavy loads. The seamless transition between these two strategies only requires an update to the offline-generated LUT. For the PS control, where the control variables are set as $k_1 = 1$, $k_2 = 1$, and $f = 1$, only the PS angle φ_s needs to be predetermined based on Table I, as illustrated in Fig. 6. To validate the feasibility of this hybrid control strategy, the experimental results of transition from the VAVF to PS control are shown in Fig. 17. It can be observed that as the power increases from 0.6 to 0.8 p.u., the converter operates in the PS mode instead of the VAVF mode, with the transition occurring smoothly and without severe overshoot.

D. Dynamic Response

To suppress potential dc bias during transient processes, the dynamic control proposed in [33] is adopted. The experimental results of the dynamic response under VAVF control, with a power step change from 0.12 to 1 p.u., are shown in Fig. 18. As observed, k_1 and k_2 step from 1/3 and 1/4 to 1, respectively, while the frequency f increases from 0.75 to 1.071. Since the control variables are directly obtained from an LUT in the closed-loop implementation, which functions as a feedforward control and thus contributes to a fast dynamic response.

TABLE IV
COMPARISON OF DIFFERENT CONVERTER TOPOLOGIES AND STRATEGIES

	[18]	[29]	[26]	[31]	This paper
Topology	MMC-DAB	MMC-DAB	MMC-*LLC*	MMC-*LC*	MMC-DAB
Application	MVDC–MVDC/LVDC	MVDC/LVDC	MVDC/LVDC	MVDC/LVDC	MVDC/LVDC
Power range of ZVS operation	Narrow	Moderate	Moderate	Narrow	Wide
Bidirectional power flow	Yes	Yes	No	No	Yes
Control degrees of freedom	1	2	2	2	4

V. DISCUSSION AND COMPARISON

The comparison of different converter topologies and strategies is summarized in Table IV. In [18], the phase-shifted square wave modulation strategy is proposed for the DCT combining MMC and DAB (MMC-DAB), which increases the equivalent switching frequency to reduce the size of passive components. However, the ZVS range is narrow due to the frequent insertion and bypassing of SMs within half of the ac-link cycle, and only PS angle is used to control. To reduce the number of SMs, Jin et al. [29] proposed a shared-branch MMC-DAB structure where power is regulated via the PS angle. In [26], the MMC combined with the *LLC* resonant converter (MMC-*LLC*) is introduced, which uses switching frequency to regulate the output voltage while inheriting the soft-switching characteristics of the *LLC* converter. To mitigate loss caused by magnetizing current in the *LLC*, the MMC with the *LC* resonant converter (MMC-*LC*) is proposed [31]. This topology operates at a fixed switching frequency equal to the resonant frequency and employs PS angle θ among the SMs to adjust the output voltage. In [29], [26], and [31], due to the presence of dc component in the arm current, the power range of ZVS operation is limited. In contrast, these studies utilize the amplitude of the primary ac-link voltage as anther control degree of freedom to achieve a wide voltage gain range adaptation. Moreover, the capacitor voltage balancing requires reassigning SMs with new gate signals, which introduces extra switching actions and may lead to ZVS loss. Although the demand for real-time performance is increased employing the proposed voltage-balancing methods of this article, additional switching actions can be avoided, thereby preserving soft-switching performance. Furthermore, the MMC-DAB enables unified bidirectional power flow control, whereas the MMC-*LLC* and MMC-*LC* topologies employ an uncontrolled diode rectifier, which inherently limits bidirectional power flow capability. In this article, the proposed MMC-DAB is applied to interconnect different MVDC feeders. The control degrees of freedom include the PS angle, switching frequency, and amplitudes of both primary and secondary ac-link voltages. These four control variables are coordinately optimized to minimize conduction loss while maintaining ZVS across a wide power range. In addition, transformer core loss and switching loss are reduced, leading to improved light-power efficiency.

VI. CONCLUSION

In this article, a VAVF control strategy is proposed to extend ZVS range of MMC-DCT, which is achieved by adjusting the

number of constantly bypassed and inserted SMs as the transmitted power changes. With this strategy, ZVS is guaranteed within wide power range, and the conversion efficiency is enhanced at light power. In view of the impact of TRM, five operating modes are introduced first, and the expressions of the transferred power and transformer currents are given. According to it, ZVS range is analyzed in detail. Subsequently, a method for obtaining optimized control variables is given, where the transformer rms current is selected as the objective function to reduce conduction and copper loss. Then, a corresponding capacitor voltage-balancing algorithm is proposed, which can effectively balance the voltages of SM capacitors. Besides, by adding an offline optimized LUT, it is easy to achieve closed-loop control based on traditional PS control. Finally, the experimental results are provided to verify the performance of the proposed control strategy at different power.

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